

Programmable Synchronous PWM Buck Converter with Dual Adjustable Low Dropout Linear Regulator Controller

General Description

The RT9222 integrates a PWM controller and two low-dropout linear regulators into a single chip. The PWM controller provides the CPU core voltage controlled by a 5-bit DAC and the linear section regulates power for GTL bus, clock driver or other circuits on motherboards. The PWM controller provides an adjustable Intel-compatible 1.3V~3.5V output voltage. The synchronous N-MOSFET driver with 200 KHz switching frequency optimizes the efficiency, device size, and cost built-in over-voltage and current-limiting protection prevent the CPU from damage. Power-good signal is sent when the core voltage is within $\pm 10\%$ of the setting point.

The linear section is a low dropout regulator which drives low cost NPN transistors. The output level is user-adjustable and can be programmed by two external resistors and the internal 1.265V reference.

Ordering Information

RT9222□ □

Package type
S : SOP-24

Operating temperature range
C: Commercial standard

Features

- Provides 3 Regulated Voltages
- N-MOSFET Driver for High Efficiency Switching Section
- Power-good, Over-voltage, and Current-limiting Protection for Switching Section
- Adjustable Output Voltage for Linear Section
- Linear Section Uses Low Cost NPN Transistor as Power Device
- TTL-compatible 5-bit DAC Core Output Voltage

Applications

- Power Supply for Pentium, Pentium Pro™, Pentium II™, PowerPC™, K6™, 6x86™, and Alpha™ Microprocessors
- High-power 5V to 3.xV DC-DC Regulators
- Low-voltage Distributed Power Supplies
- Programmable Power Supplies

Pin Configurations

Part Number	Pin Configurations	
RT9222CS (Plastic SOP-24)	TOP VIEW	
	GND [1]	[24] GATE2
	GATE1 [2]	[23] LDOV
	LDOS1 [3]	[22] VID0
	LDOS2 [4]	[21] VID1
	VCC [5]	[20] VID2
	OVP [6]	[19] VID3
	PGOOD [7]	[18] VID4
	CSN [8]	[17] VSEN
	CSP [9]	[16] SHDN
	PGNDH [10]	[15] BSTH
	DH [11]	[14] BSTL
	PGNDL [12]	[13] DL

Absolute Maximum Ratings

• VCC to GND	-0.3 to +5.5V
• PGND to GND	± 0.3V
• BSTH and BSTL to GND	-0.3 to +14V
• Ambient Temperature Range	0 to +70°C
• Junction Temperature Range	0 to +125°C
• Storage Temperature Range	-65 to +150°C
• Lead Temperature (Soldering, 10 sec.)	300°C
• Package Thermal Resistance SOP-24, θ_{JA}	75°C/W

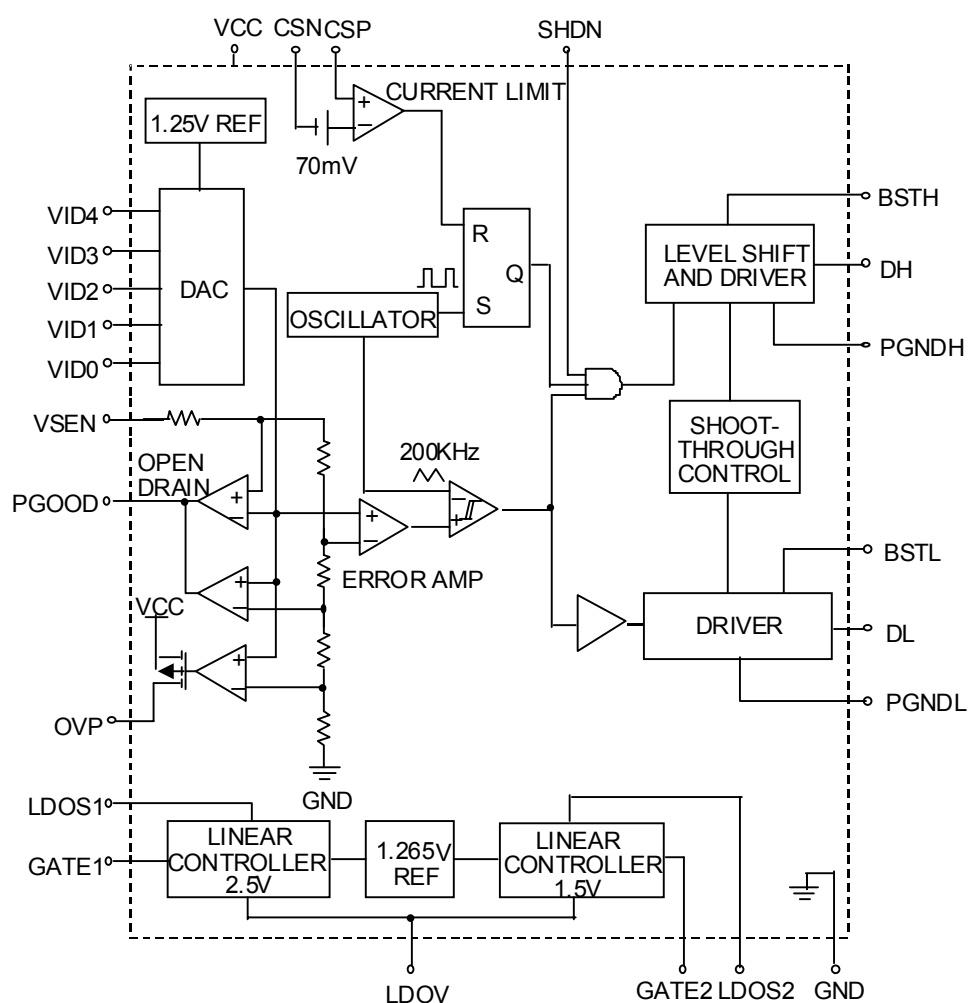
Electrical Characteristics

(VCC = 5V; GND = 0V; PGNDH = PGNDL = 0V; VSEN = VOUT; 0mV < (VCSP-VCSEN) < 60mV; TA = 25°C)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Switching Section						
Output Voltage	V _{OUT}	I _O = 2A	--	(1)	--	--
Supply Voltage	V _{CC}	VCC	4.5	--	5.5	V
Supply Current	I _{CC}		--	3	6	mA
Load Regulation	ΔV _{LOAD}	I _O = 0.8A to 15A	--	1	--	%
Line Regulation	ΔV _{LINE}	VCC = 4.75V to 5.25V	--	0.5	--	%
Power On Reset Trip Point		VCC Rising	--	4.2	--	V
Current Limit Voltage	V _{LIMIT}	VCSP - VCSEN	65	75	85	mV
Oscillator Frequency			170	200	230	KHz
Oscillator Max Duty Cycle	D _{MAX}		90	95	--	%
DH Source		V _{BSTH} - V _{DH} = 1V	--	3.5	--	Ω
DH Sink		V _{DH} - V _{PGNDH} = 1V	--	3.5	--	Ω
DL Source		V _{BSTL} - V _{DL} = 3V	--	2	--	Ω
DL Sink		V _{DL} - V _{PGNDL} = 1V	--	2	--	Ω
OVP Threshold Voltage			--	120	--	%
OVP Source Current	I _{OVP}	V _{OVP} = 3.0V	10	--	--	mA
Power Good Threshold Voltage		VSEN Rising	87	--	113	%
Linear Sections						
Quiescent Current	I _Q	LDOV = 12V	--	--	5	mA
Reference Voltage	V _{REF}		1.240	1.265	1.290	V
Gain (A _{OL})		LDOS1/2 to GATE1/2	--	65	--	dB
Load Regulation	ΔV _{LOAD}	I _O = 0 to 5A	--	1	--	%
Line Regulation	ΔV _{LINE}	LDOV = 11.4V to 12.6V	--	1	--	%

Note: (1) See output voltage table.

Function Block Diagram



Pin Description

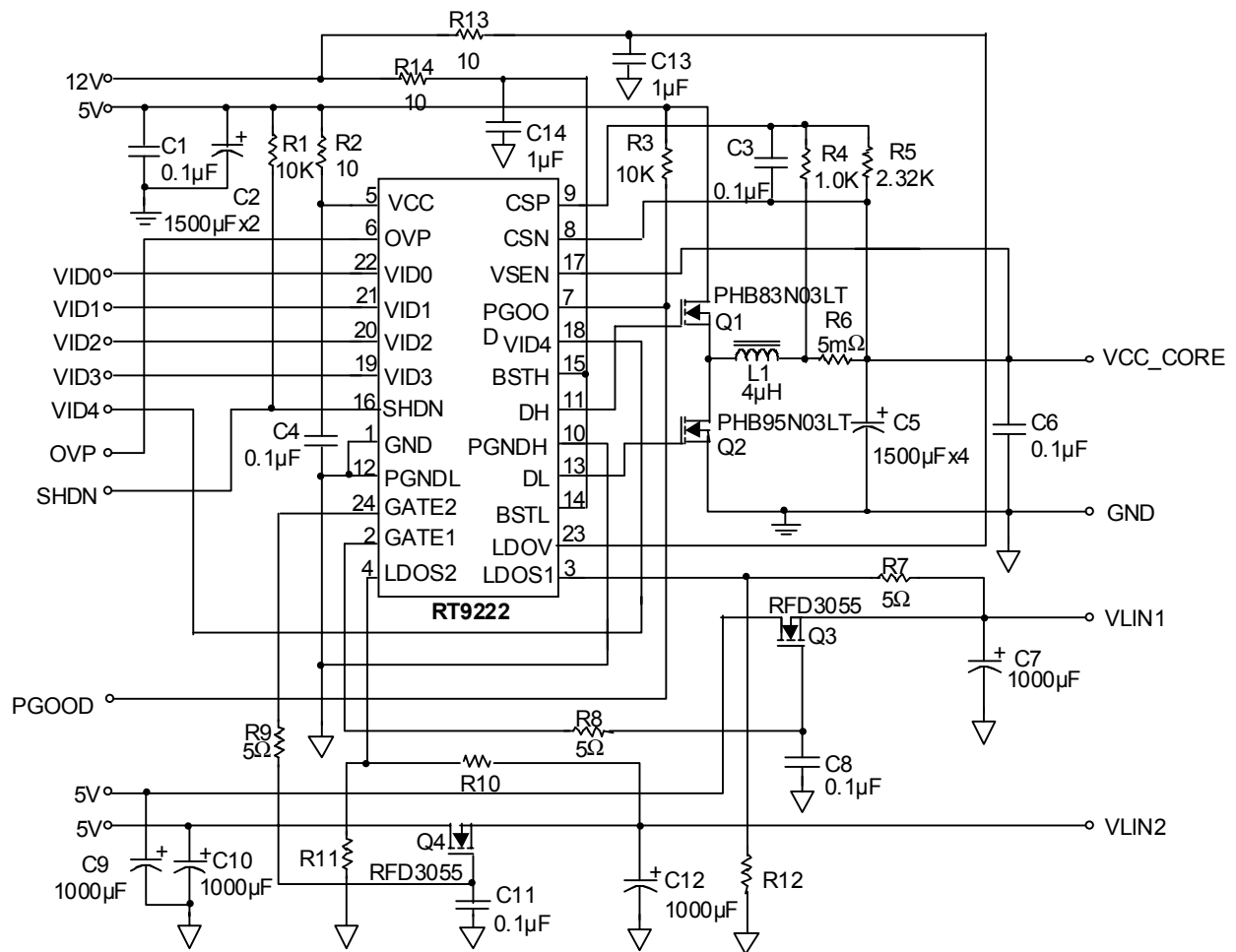
Pin No.	Pin Name	Pin Function
1	GND	Small signal analog and digital ground
2	GATE1	LDO1 gate drive output
3	LDOS1	LDO1 sense input
4	LDOS2	LDO2 sense input
5	VCC	Input voltage
6	OVP	High signal out if $V_O > \text{setting point} + 20\%$
7	PGOOD ⁽¹⁾	Open collector logic output, High if V_O within 10% of the setting point
8	CSN	Current sense input (Negative)
9	CSP	Current sense input (Positive)
10	PGNDH	High side drive GND
11	DH	High side driver output
12	PGNDL	Power ground for low side switch
13	DL	Low side driver output
14	BSTL	Supply for low side driver
15	BSTH	Supply for high side driver
16	SHDN ⁽¹⁾	Logic low shutdown the converter
17	VSEN	Top end of internal feedback chain
18	VID4 ⁽¹⁾	Programming input (MSB)
19	VID3 ⁽¹⁾	Programming input
20	VID2 ⁽¹⁾	Programming input
21	VID1 ⁽¹⁾	Programming input
22	VID0 ⁽¹⁾	Programming input (LSB)
23	LDOV	+12V for LDO section
24	GATE2	LDO2 gate drive output

Note: (1) All logic level inputs and outputs are TTL compatible.

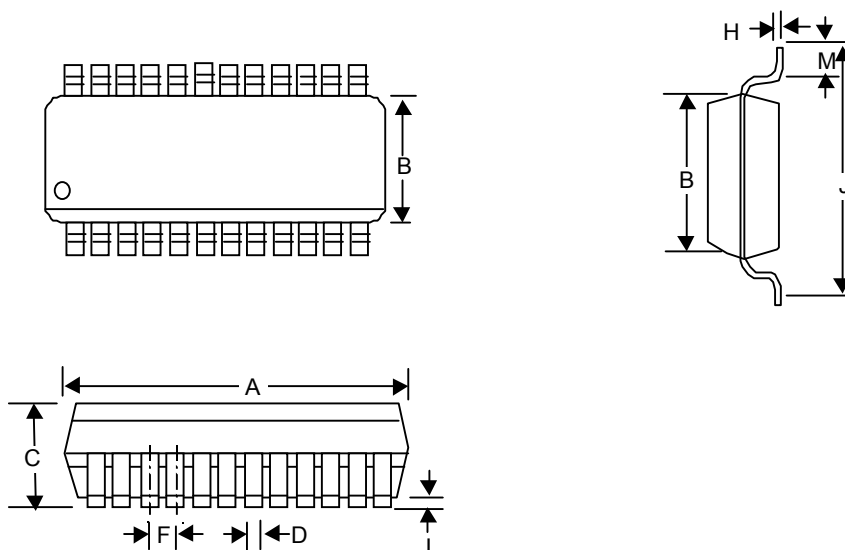
Table 1 Output Voltage Program

Test	Conditions	VID 43210	Min	Typ	Max	Units
Output Voltage	$I_O = 2A$ in application circuit	01111	1.281	1.300	1.320	V
		01110	1.330	1.350	1.370	
		01101	1.379	1.400	1.421	
		01100	1.428	1.450	1.472	
		01011	1.478	1.500	1.523	
		01010	1.527	1.550	1.573	
		01001	1.576	1.600	1.624	
		01000	1.625	1.650	1.675	
		00111	1.675	1.700	1.726	
		00110	1.724	1.750	1.776	
		00101	1.773	1.800	1.827	
		00100	1.822	1.850	1.878	
		00011	1.871	1.900	1.929	
		00010	1.921	1.950	1.979	
		00001	1.970	2.000	2.030	
		00000	2.019	2.050	2.081	
		11111	1.960	2.000	2.040	
		11110	2.058	2.100	2.142	
		11101	2.156	2.200	2.244	
		11100	2.254	2.300	2.346	
		11011	2.352	2.400	2.448	
		11010	2.450	2.500	2.550	
		11001	2.548	2.600	2.652	
		11000	2.646	2.700	2.754	
		10111	2.744	2.800	2.856	
		10110	2.842	2.900	2.958	
		10101	2.940	3.000	3.060	
		10100	3.038	3.100	3.162	
		10011	3.136	3.200	3.264	
		10010	3.234	3.300	3.366	
		10001	3.332	3.400	3.468	
		10000	3.430	3.500	3.570	

Typical Application Circuit



Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	15.189	15.596	0.598	0.614
B	7.391	7.595	0.291	0.299
C	2.362	2.642	0.093	0.104
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.229	0.330	0.009	0.013
I	0.102	0.305	0.004	0.012
J	10.008	10.643	0.394	0.419
M	0.381	1.270	0.015	0.050

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