Dual-Channel, Multi-Phase PWM Controller with I²C Interface for AMD SVI2 CPU Power Supply

General Description

The RT8881A is a multi-phases PWM controller. Moreover, it is compliant with AMD SVI2 Voltage Regulator Specification to support both CPU core (VDD) and Northbridge portion (VDDNB) of the CPU. The RT8881A adopts the G-NAVP™ (Green-Native AVP), which is a Richtek's proprietary topology. The G-NAVP makes it an easy setting controller to meet all AMD AVP (Adaptive Voltage Positioning) requirements. The droop is easily programmed by setting the DC gain of the error amplifier. With proper compensation, the load transient response can achieve optimized AVP performance. The RT8881A uses SVI2 interface to control 8-bit DAC to set output voltage and operation mode, and support a dynamic platform master. An I²C interface is available for advanced power configuration and monitoring. The RT8881A also features programmable power states with different sets of operating phase number, over clocking offset, switching frequency, load-line and protection setting. The platform master can optimize the performance and efficiency of the power according to different working scenarios via the I²C interface. The RT8881A also provides power good indication, over-current indication and dual OCP mechanism for AMD SVI2 CPU core and NB. It also features complete fault protection functions including over-voltage, under-voltage and negative-voltage protections.

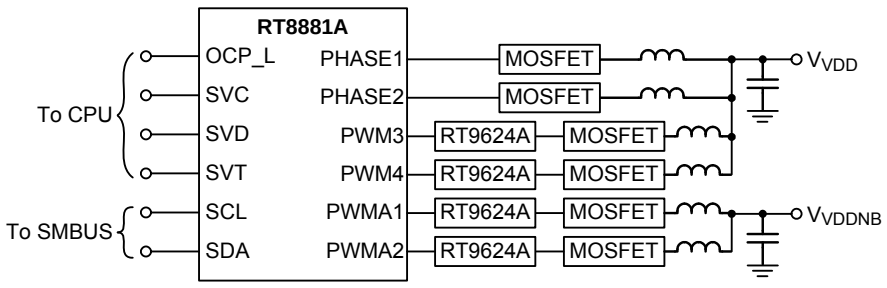
Features

- **Dual Outputs :**
  - **4/3/2/1-Phase for VDD**
  - **2/1/0-Phase for VDDNB**
- **G-NAVP™ Topology**
- **Support Dynamic Load-Line and Zero Load-Line**
- **Diode Emulation Mode at Light Load Condition**
- **SVI2 Interface to Comply with AMD Power Management Protocol**
- **I²C Interface for Platform Configuration**
- **Build-in ADC for V_{OUT} and I_{OUT} Reporting**
- **Immediate OV, UV and NV Protections and UVLO**
- **Programmable Dual OCP Mechanism**
- **Accurate Current Balance**
- **Fast Transient Response**
- **Dynamic Phase Up/Down Control**
- **Programmable Power State Control**
- **Power Good Indicator**
- **Over-Current Indicator**
- **Over Clocking Offset Capabilities**
- **52-Lead WQFN Package**
- **RoHS Compliant and Halogen Free**

Applications

- AMD SVI2 CPU
- Desktop Computer

Simplified Application Circuit



Ordering Information

RT8881A □□

- Package Type
  QW : WQFN-52L 6x6 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Marking Information

RT8881AGQW : Product Number

YMDNN : Date Code

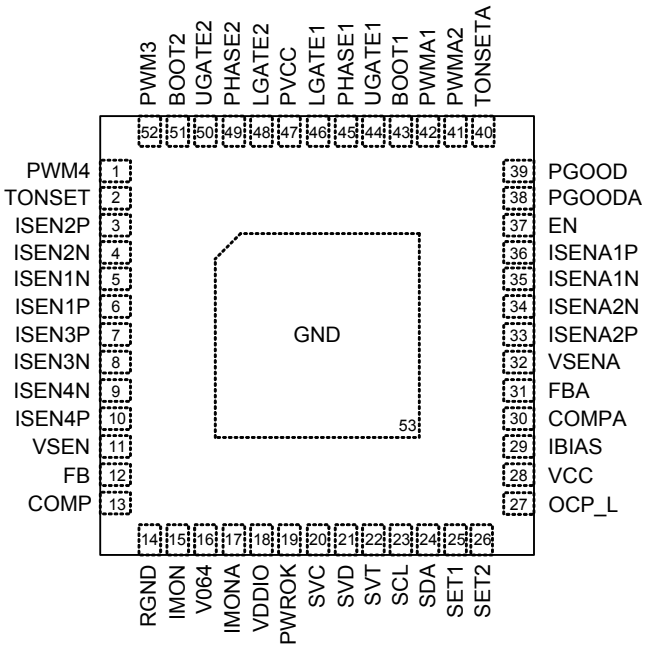
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Pin Configurations

(TOP VIEW)



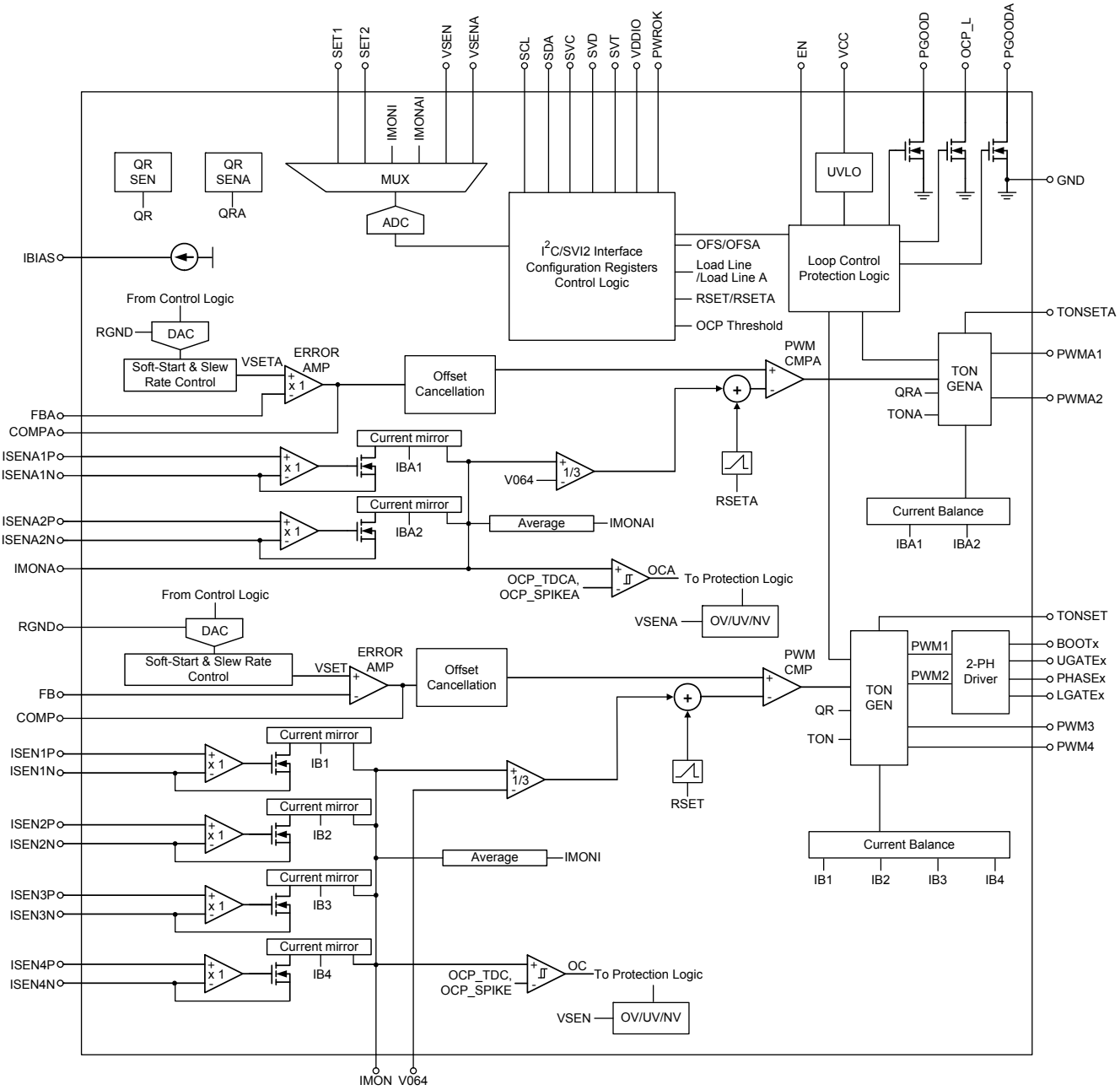
WQFN-52L 6x6

Functional Pin Description

Pin No.	Pin Name	Pin Function
1, 52	PWM4, PWM3	PWM Outputs for Channel 3 and 4 of VDD Controller.
2	TONSET	VDD Controller On-Time Setting. Connect this pin to the converter input voltage, Vin, through a resistor, RTON, to set the on-time of UGATE and also the output voltage ripple of VDD controller.
5, 4, 8, 9	ISEN1N to ISEN4N	Negative Current Sense Input of Channel 1, 2, 3 and 4 for VDD Controller.
6, 3, 7, 10	ISEN1P to ISEN4P	Positive Current Sense Input of Channel 1, 2, 3 and 4 for VDD Controller.
11	VSEN	VDD Controller Voltage Sense Input. This pin is connected to the terminal of VDD controller output voltage.
12	FB	Output Voltage Feedback Input of VDD Controller. This pin is the negative input of the error amplifier for the VDD controller.
13	COMP	Compensation Node of the VDD Controller.
14	RGND	Return Ground of VDD and VDDNB Controller. This pin is the common negative input of output voltage differential remote sense for VDD and VDDNB controllers.
15	IMON	Current Monitor Output for the VDD Controller. This pin outputs a voltage proportional to the output current.
16	V064	Fixed 0.64V Reference Voltage Output. This voltage is only used to offset the output voltage of IMON pin and IMONA pin. Connect a 0.47μF capacitor from this pin to GND.
17	IMONA	Current Monitor Output for the VDDNB Controller. This pin outputs a voltage proportional to the output current.
18	VDDIO	Processor memory interface power rail and serves as the reference for PWROK, SVD, SVC and SVT. This pin is used by the VR to reference the SVI pins.
19	PWROK	System Power Good Input. If PWROK is low, the SVI interface is disabled and VR returns to BOOT-VID state with initial load line slope and initial offset. If PWROK is high, the SVI interface is running and the DAC decodes the received serial VID codes to determine the output voltage.
20	SVC	Serial VID Clock Input from Processor.
21	SVD	Serial VID Data input from Processor. This pin is a serial data line.
22	SVT	Serial VID Telemetry Input from VR. This pin is a push-pull output.
23	SCL	I^2C Clock Signal from Platform Master.
24	SDA	I^2C Data Signal. Bi-directional Data Signal from / to the Platform Master.
25	SET1	OCP_TDC threshold setting individually for VDD and VDDNB controllers and also the internal ramp slew rate setting (RSET and RSETA) individually for VDD and VDDNB controllers.
26	SET2	Quick response threshold (QRTH and QRTHA) setting individually for VDD and VDDNB controllers and also the OCP_TDC trigger delay time setting for both controllers and over clocking offset enable setting.
27	OCP_L	Over Current Indicator for Dual OCP Mechanism. This pin is an open-drain output.
28	VCC	Controller Power Supply Input. Connect this pin to 5V with an 1μF or greater ceramic capacitor for decoupling.

Pin No.	Pin Name	Pin Function
29	IBIAS	Internal Bias Current Setting. Connect only a 100kΩ resistor from this pin to GND to generate bias current for internal circuit. Place this resistor as close to the IBIAS pin as possible.
30	COMPA	Compensation Node of the VDDNB Controller.
31	FBA	Output Voltage Feedback Input of VDDNB Controller. This pin is the negative input of the error amplifier for the VDDNB controller.
32	VSENA	VDDNB Controller Voltage Sense Input. This pin is connected to the terminal of VDDNB controller output voltage.
33, 36	ISENA2P, ISENA1P	Positive Current Sense Input of Channel 1 and 2 for VDDNB Controller.
34, 35	ISENA2N, ISENA1N	Negative Current Sense Input of Channel 1 and 2 for VDDNB Controller.
37	EN	Controller Enable Control Input. A logic high signal enables the controller.
38	PGOODA	Power Good Indicator for the VDDNB Controller. This pin is an open-drain output.
39	PGOOD	Power Good Indicator for the VDD Controller. This pin is an open-drain output.
40	TONSETA	VDDNB Controller On-Time Setting. Connect this pin to the converter input voltage, Vin, through a resistor, RTONNB, to set the on-time of UGATE_VDDNB and also the output voltage ripple of VDDNB controller.
41, 42	PWMA2, PWMA1	PWM Output for Channel 1 and 2 of VDDNB Controller.
43, 51	BOOT1, BOOT2	Bootstrap Supply for High-Side MOSFET Driver.
44, 50	UGATE1, UGATE2	High-Side Gate Driver Outputs. Connect this pin to Gate of high-side MOSFET.
45, 49	PHASE1, PHASE2	Switch nodes of High-Side Driver. Connect this pin to high-side MOSFET Source together with the low-side MOSFET Drain and the inductor.
46, 48	LGATE1, LGATE2	Low-Side Driver Outputs. This pin drives the Gate of low-side MOSFET.
47	PVCC	Driver Power. Connect this pin to GND by ceramic capacitor larger than 1μF.
53 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Function Block Diagram



Operation

QRSEN/QRSENA

The QRSEN/QRSENA detects VSEN/VSENA and generates QR/QRA signals.

MUX and ADC

The MUX switches ADC input to SET1, SET2, IMON or IMONA. ADC converts these analog signals to digital codes for reporting or performance adjustment. (In RT8881A, TSEN and TSENA are not connected to MUX)

I²C/SVI2 Interface

I²C/SVI2 interface uses the SVC, SVD, and SVT pins to communicate with CPU, and uses the SCL and SDA pins to communicate with platform. The RT8881A's performance and behavior can be adjusted by commands sent by CPU or platform.

UVLO

UVLO detects the VCC pin voltages to generate UVLO signal.

Loop Control Protection Logic

Loop control protection logic detects the EN pin voltage and UVLO signal to initiate soft-start, and generates open-drain PGOOD and PGOODA signals after soft-start is finished. When OCP_L event occurs, the OCP_L pin voltage will be pulled low.

DAC

The DAC receives VID codes to generate internal reference voltage (VSET/VSETA) for controller to regulate.

Soft-Start and Slew-Rate Control

This block controls the slew rate of internal reference change to control the slew rate when output voltage changes.

Error Amplifier

The Error amplifier generates COMP/COMPA signal by the difference between VSET/VSETA and FB/FBA.

Offset Cancellation

This block cancels the output offset voltage due to voltage and current ripples to achieve accurate output voltage.

PWM CMP

PWM comparator compares COMP signal and current feedback signal to initial PWM signal.

TONGEN/TONGENA

This block generates PWM signal's high interval based on on-time setting and current balance.

Current Balance

Per-phase current is sensed and adjusted by adjusting on-time of each phase to achieve current balance among each phase.

OC/OV/UV/NV

VSEN/VSENA and output current are sensed for over-current, over-voltage, under-voltage, negative-voltage protections.

RSET

Ramp generator to improve noise immunity and reduce jitter.

Table 1. Serial VID Codes

SVID [7:0]	Voltage (V)	SVID [7:0]	Voltage (V)	SVID [7:0]	Voltage (V)	SVID [7:0]	Voltage (V)
0000_0000	1.55000	0010_0111	1.30625	0100_1110	1.06250	0111_0101	0.81875
0000_0001	1.54375	0010_1000	1.30000	0100_1111	1.05625	0111_0110	0.81250
0000_0010	1.53750	0010_1001	1.29375	0101_0000	1.05000	0111_0111	0.80625
0000_0011	1.53125	0010_1010	1.28750	0101_0001	1.04375	0111_1000	0.80000
0000_0100	1.52500	0010_1011	1.28125	0101_0010	1.03750	0111_1001	0.79375
0000_0101	1.51875	0010_1100	1.27500	0101_0011	1.03125	0111_1010	0.78750
0000_0110	1.51250	0010_1101	1.26875	0101_0100	1.02500	0111_1011	0.78125
0000_0111	1.50625	0010_1110	1.26250	0101_0101	1.01875	0111_1100	0.77500
0000_1000	1.50000	0010_1111	1.25625	0101_0110	1.01250	0111_1101	0.76875
0000_1001	1.49375	0011_0000	1.25000	0101_0111	1.00625	0111_1110	0.76250
0000_1010	1.48750	0011_0001	1.24375	0101_1000	1.00000	0111_1111	0.75625
0000_1011	1.48125	0011_0010	1.23750	0101_1001	0.99375	1000_0000	0.75000
0000_1100	1.47500	0011_0011	1.23125	0101_1010	0.98750	1000_0001	0.74375
0000_1101	1.46875	0011_0100	1.22500	0101_1011	0.98125	1000_0010	0.73750
0000_1110	1.46250	0011_0101	1.21875	0101_1100	0.97500	1000_0011	0.73125
0000_1111	1.45625	0011_0110	1.21250	0101_1101	0.96875	1000_0100	0.72500
0001_0000	1.45000	0011_0111	1.20625	0101_1110	0.96250	1000_0101	0.71875
0001_0001	1.44375	0011_1000	1.20000	0101_1111	0.95625	1000_0110	0.71250
0001_0010	1.43750	0011_1001	1.19375	0110_0000	0.95000	1000_0111	0.70625
0001_0011	1.43125	0011_1010	1.18750	0110_0001	0.94375	1000_1000	0.70000
0001_0100	1.42500	0011_1011	1.18125	0110_0010	0.93750	1000_1001	0.69375
0001_0101	1.41875	0011_1100	1.17500	0110_0011	0.93125	1000_1010	0.68750
0001_0110	1.41250	0011_1101	1.16875	0110_0100	0.92500	1000_1011	0.68125
0001_0111	1.40625	0011_1110	1.16250	0110_0101	0.91875	1000_1100	0.67500
0001_1000	1.40000	0011_1111	1.15625	0110_0110	0.91250	1000_1101	0.66875
0001_1001	1.39375	0100_0000	1.15000	0110_0111	0.90625	1000_1110	0.66250
0001_1010	1.38750	0100_0001	1.14375	0110_1000	0.90000	1000_1111	0.65625
0001_1011	1.38125	0100_0010	1.13750	0110_1001	0.89375	1001_0000	0.65000
0001_1100	1.37500	0100_0011	1.13125	0110_1010	0.88750	1001_0001	0.64375
0001_1101	1.36875	0100_0100	1.12500	0110_1011	0.88125	1001_0010	0.63750
0001_1110	1.36250	0100_0101	1.11875	0110_1100	0.87500	1001_0011	0.63125
0001_1111	1.35625	0010_0110	1.11250	0110_1101	0.86875	1001_0100	0.62500
0010_0000	1.35000	0100_0111	1.10625	0110_1110	0.86250	1001_0101	0.61875
0010_0001	1.34375	0100_1000	1.10000	0110_1111	0.85625	1001_0110	0.61250
0010_0010	1.33750	0100_1001	1.09375	0111_0000	0.85000	1001_0111	0.60625
0010_0011	1.33125	0100_1010	1.08750	0111_0001	0.84375	1001_1000	0.60000
0010_0100	1.32500	0100_1011	1.08125	0111_0010	0.83750	1001_1001	0.59375
0010_0101	1.31875	0100_1100	1.07500	0111_0011	0.83125	1001_1010	0.58750
0010_0110	1.31250	0100_1101	1.06875	0111_0100	0.82500	1001_1011	0.58125

SVID [7:0]	Voltage (V)	SVID [7:0]	Voltage (V)	SVID [7:0]	Voltage (V)	SVID [7:0]	Voltage (V)
1001_1100	0.57500	1011_0101 *	0.41875	1100_1110 *	0.26250	1110_0111*	0.10625
1001_1101	0.56875	1011_0110 *	0.41250	1100_1111 *	0.25625	1110_1000*	0.10000
1001_1110	0.56250	1011_0111 *	0.40625	1101_0000 *	0.25000	1110_1001*	0.09375
1001_1111	0.55625	1011_1000 *	0.40000	1101_0001 *	0.24375	1110_1010*	0.08750
1010_0000	0.55000	1011_1001 *	0.39375	1101_0010 *	0.23750	1110_1011*	0.08125
1010_0001	0.54375	1011_1010 *	0.38750	1101_0011 *	0.23125	1110_1100*	0.07500
1010_0010	0.53750	1011_1011 *	0.38125	1101_0100 *	0.22500	1110_1101*	0.06875
1010_0011	0.53125	1011_1100 *	0.37500	1101_0101 *	0.21875	1110_1110*	0.06250
1010_0100	0.52500	1011_1101 *	0.36875	1101_0110 *	0.21250	1110_1111*	0.05625
1010_0101	0.51875	1011_1110 *	0.36250	1101_0111 *	0.20625	1111_0000*	0.05000
1010_0110	0.51250	1011_1111 *	0.35625	1101_1000 *	0.20000	1111_0001*	0.04375
1010_0111	0.50625	1100_0000 *	0.35000	1101_1001 *	0.19375	1111_0010*	0.03750
1010_1000 *	0.50000	1100_0001 *	0.34375	1101_1010 *	0.18750	1111_0011*	0.03125
1010_1001 *	0.49375	1100_0010 *	0.33750	1101_1011 *	0.18125	1111_0100*	0.02500
1010_1010 *	0.48750	1100_0011 *	0.33125	1101_1100 *	0.17500	1111_0101*	0.01875
1010_1011 *	0.48125	1100_0100 *	0.32500	1101_1101 *	0.16875	1111_0110*	0.01250
1010_1100 *	0.47500	1100_0101 *	0.31875	1101_1110 *	0.16250	1111_0111*	0.00625
1010_1101 *	0.46875	1100_0110 *	0.31250	1101_1111 *	0.15625	1111_1000*	0.00000
1010_1110 *	0.46250	1100_0111 *	0.30625	1110_0000*	0.15000	1111_1001*	OFF
1010_1111 *	0.45625	1100_1000 *	0.30000	1110_0001*	0.14375	1111_1010*	OFF
1011_0000 *	0.45000	1100_1001 *	0.29375	1110_0010*	0.13750	1111_1011*	OFF
1011_0001 *	0.44375	1100_1010 *	0.28750	1110_0011*	0.13125	1111_1100*	OFF
1011_0010 *	0.43750	1100_1011 *	0.28125	1110_0100*	0.12500	1111_1101*	OFF
1011_0011 *	0.43125	1100_1100 *	0.27500	1110_0101*	0.11875	1111_1110*	OFF
1011_0100 *	0.42500	1100_1101 *	0.26875	1110_0110*	0.11250	1111_1111*	OFF

* Indicates TOB is 80mV for this VID code; unconditional VR controller stability required at all VID codes

Table 2. SET1 Pin Setting for VDD Controller

SET1 Pin Voltage Before Current Injection V_{SET1} (mV)	OCP_TDC (Respect to OCP_SPIKE)	RSET	SET1 Pin Voltage Before Current Injection V_{SET1} (mV)	OCP_TDC (Respect to OCP_SPIKE)	RSET
34	70%	61%	836	90%	61%
59		74%	861		74%
85		87%	886		87%
110		100%	911		100%
135		113%	936		113%
160		126%	961		126%
235	75%	61%	1036	95%	61%
260		74%	1061		74%
285		87%	1086		87%
310		100%	1112		100%
335		113%	1137		113%
360		126%	1162		126%
435	80%	61%	1237	100%	61%
460		74%	1262		74%
485		87%	1287		87%
510		100%	1312		100%
535		113%	1337		113%
560		126%	1362		126%
636	85%	61%	1437	Disable OCPTDC	61%
661		74%	1462		74%
686		87%	1487		87%
711		100%	1512		100%
736		113%	1537		113%
761		126%	1562		126%

Table 3. SET1 Pin Setting for VDDNB Controller

SET1 Pin Voltage Difference ΔV_{SET1} (Before and After Current Injection) (mV)	OCP_TDCA (Respect to OCP_SPIKEA)	RSETA	SET1 Pin Voltage Difference ΔV_{SET1} (Before and After Current Injection) (mV)	OCP_TDCA (Respect to OCP_SPIKEA)	RSETA
34	70%	61%	836	90%	61%
59		74%	861		74%
85		87%	886		87%
110		100%	911		100%
135		113%	936		113%
160		126%	961		126%
235	75%	61%	1036	95%	61%
260		74%	1061		74%
285		87%	1086		87%
310		100%	1112		100%
335		113%	1137		113%
360		126%	1162		126%
435	80%	61%	1237	100%	61%
460		74%	1262		74%
485		87%	1287		87%
510		100%	1312		100%
535		113%	1337		113%
560		126%	1362		126%
636	85%	61%	1437	Disable OCPTDC	61%
661		74%	1462		74%
686		87%	1487		87%
711		100%	1512		100%
736		113%	1537		113%
761		126%	1562		126%

Table 4. SET2 Pin Setting

SET2 Pin Voltage Before Current Injection V_{SET2} (mV)	QRTH (for VDD)	OCPTRGDELAY (for VDD/VDDNB)
34 to 85	Disable	10ms
110 to 160		40ms
235 to 285	Disable	10ms
310 to 360		40ms
435 to 485	30mV	10ms
510 to 560		40ms
636 to 686	35mV	10ms
711 to 761		40ms
836 to 886	40mV	10ms
911 to 961		40ms
1036 to 1086	45mV	10ms
1112 to 1162		40ms
1237 to 1287	50mV	10ms
1312 to 1362		40ms
1437 to 1487	55mV	10ms
1512 to 1562		40ms

Table 5. Quick Response Threshold for VDDNB Controller

SET2 Pin Voltage Difference ΔV_{SET2} (Before and After Current Injection) (mV)	QRTHA (for VDDNB)
19	Disable
72	Disable
122	30mV
172	35mV
222	40mV
272	45mV
323	50mV
373	55mV

Absolute Maximum Ratings (Note 1)

- VCC to GND ---------- –0.3V to 6.5V
- PVCC to GND ---------- –0.3V to 15V
- RGND to GND ---------- –0.3V to 0.3V
- TONSET, TONSETA to GND ---------- –0.3V to 6.5V
- BOOTx to PHASEx ---------- –0.3V to 15V
- PHASEx to GND
  - DC ---------- –0.3V to 30V
  - < 20ns ---------- –10V to 35V
- LGATEx to GND
  - DC ---------- –0.3V to (PVCC + 0.3V)
  - < 20ns ---------- –2V to (PVCC + 0.3V)
- UGATEx to GND
  - DC ---------- (V_{PHASE} – 0.3V) to (V_{BOOT} + 0.3V)
  - < 20ns ---------- (V_{PHASE} – 2V) to (V_{BOOT} + 0.3V)
- VDDIO, PWROK, SVT, SVD and SVC ---------- –0.3V to 3.3V
- Other Pins ---------- –0.3V to (V_{CC} + 0.3V)
- Power Dissipation, P_D @ T_A = 25°C
  - WQFN-52L 6x6 ---------- 3.77W
- Package Thermal Resistance (Note 2)
  - WQFN-52L 6x6, θ_{JA} ---------- 26.5°C/W
  - WQFN-52L 6x6, θ_{JC} ---------- 6.5°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Voltage, VCC ---------- 4.5V to 5.5V
- Driver Supply Voltage, PVCC ---------- 4.5V to 13.2V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C
- Input Voltage + Driver Supply Voltage, VIN + PVCC ---------- <35V

Electrical Characteristics

(V_{CC} = 5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Power Supply						
Supply Current	I_{VCC}	EN = 3V, Not Switching	--	--	15	mA
Shutdown Current	I_{SHDN}	EN = 0V	--	--	5	μA
Reference and DAC						
DC Accuracy	V_{FB}	V_{FB} = 1.0000 – 1.5500 (No Load, CCM Mode)	–0.5	0	0.5	%SVID
		V_{FB} = 0.8000 – 1.0000	–5	0	5	mV
		V_{FB} = 0.3000 – 0.8000	–8	0	8	
		V_{FB} = 0.2500 – 0.3000	–80	0	80	
RGND Current						
RGND Current	I_{RGND}	EN = 3V, Not Switching	--	--	400	μA
Slew Rate						
Dynamic VID Slew Rate	SR	SetVID Fast	7.5	12	--	mV/μs
Error Amplifier						
Input Offset	V_{EAOFS}		–2	--	2	mV
DC Gain	ADC	R_L = 47kΩ	70	80	--	dB
Gain-Bandwidth Product	GBW	C_{LOAD} = 5pF	--	10	--	MHz
Output Voltage Range	V_{COMP}		0.3	--	3.6	V
Maximum Source Current	I_{EAsr}		1	--	--	mA
Maximum Sink Current	I_{EAsk}		1	--	--	mA
Current Sense Amplifier						
Input Offset Voltage	V_{OSCS}		–0.8	--	0.8	mV
Current Mirror Gain for CORE	$A_{MIRROR, VDD}$		97	--	103	%
Current Mirror Gain for NB	$A_{MIRROR, VDDNB}$		97	--	103	%
Impedance at Negative Input	R_{ISENxN}		1	--	--	MΩ
Impedance at Positive Input	R_{ISENxP}		1	--	--	MΩ
Internal Sum Current Sense DC Gain for CORE	Ai, VDD	GBD	0.32	0.33	0.34	V/V
Internal Sum Current Sense DC Gain for NB	Ai, VDDNB	GBD	0.32	0.33	0.34	V/V
Maximum Source Current	I_{CSsr}	0 < V_{FB} < 2.35	100	--	--	μA
Maximum Sink Current	I_{CSsk}	0 < V_{FB} < 2.35	10	--	--	μA
Zero Current Detection						
Zero Current Detection Threshold	V_{ZCD_TH}	V_{ZCD_TH} = GND – V_{PHASEx}	--	10	--	mV

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Ton Setting							
TONSETx Pin Minimum Voltage		$V_{TON(MIN)}$		--	0.5	--	V
TONSETx TON		T_{ON}	I_{RTON} = 80μA, V_{FB} = 1.1V	270	305	340	ns
TONSETx Input Current Range		I_{RTON}	V_{FB} = 1.1V	25	--	280	μA
Minimum TOFF		T_{OFF}		--	250	--	ns
IBIAS							
IBIAS Pin Voltage		V_{IBIAS}	R_{IBIAS} = 100k	1.95	2	2.05	V
V064							
Reference Voltage Output		V_{064}		--	0.64	--	V
Sink Current Capability		I_{V064sk}	V064 = 0.64V	800	--	--	μA
Source Current Capability		I_{V064sr}		--	--	100	μA
Logic Inputs							
EN Input Voltage	Logic-High	V_{IH_EN}		2	--	--	V
	Logic-Low	V_{IL_EN}		--	--	0.8	
Leakage Current of EN, SCL SDA		I_{LEK_IN}		–1	--	1	μA
SVC, SVD, SVT, PWROK Input Voltage	Logic-High	V_{IH_SVI}	Respect to VDDIO	70	--	100	%
	Logic-Low	V_{IL_SVI}	Respect to VDDIO	0	--	35	
Hysteresis of SVC, SVD, SVT, PWROK		V_{HYS_SVI}	Respect to VDDIO	10	--	--	%
SCL, SDA Input Voltage	Logic-High	V_{IH_I2C}		2.4	--	--	V
	Logic-Low	V_{IL_I2C}		--	--	0.8	
Protection							
Under-Voltage Lockout Threshold		V_{UVLO}	VCC Falling edge	3.9	4.1	4.3	V
Under-Voltage Lockout Hysteresis		ΔV_{UVLO}		--	200	--	mV
Under-Voltage Lockout Delay		T_{UVLO}	V_{CC} Rising above UVLO Threshold	--	3	--	μs
Over-Voltage Protection Threshold		V_{OVP}	I^2C Default Setting	275	325	375	mV
Over-Voltage Protection Delay		T_{OVP}	VSENx Rising above Threshold	--	1	--	μs
Under-Voltage Protection Threshold		V_{UVP}	I^2C Default Setting	–350	–425	–500	mV
Under-Voltage Protection Delay		T_{UVP}	VSENx Falling below Threshold	--	3	--	μs
Negative-Voltage Protection Threshold		V_{NV}		--	0	--	mV

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Per-Phase OCP Threshold	$I_{OCP\_Per\text{-}Phase}$	I_{ISENxN} Per-Phase OCP Threshold, R_{SENSE} = 680Ω	80	130	180	μA
Delay of Per-Phase OCP	T_{PHOCP}		--	1	--	μs
OCP_SPIKE Threshold	I_{OCP_SPIKE}	DCR = 0.57mΩ, R_{SENSE} = 680Ω, R_{IMON} = 17.19kΩ	162	180	198	A
OCP_SPIKE Action Delay	$T_{OCP\_SPIKE\_Action\_Dly}$		6	--	12	μs
OCP_TDC Action Delay	$T_{OCP\_TDC\_Action\_Dly}$		12	--	24	μs
PGOOD, PGOODA and OCP_L						
Output Low Voltage at OCP_L	V_{OCP_L}	I_{OCP_L} = 4mA	0	--	0.2	V
OCP_L Assertion Time	T_{OCP_L}		2	--	--	μs
Output Low Voltage at PGOOD, PGOODA	V_{PGOOD}, V_{PGOODA}	I_{PGOOD} = 4mA, I_{PGOODA} = 4mA	0	--	0.2	V
PGOOD and PGOODA Threshold Voltage	V_{TH_PGOOD} V_{TH_PGOODA}	Respect to V_{BOOT}	--	–300	--	mV
PGOOD and PGOODA Delay Time	T_{PGOOD} T_{PGOODA}	VSENx = V_{BOOTx} to PGOOD/PGOODA High	70	100	130	μs
Current Report						
Maximum Reported Current (FFh = OCP)			--	100	--	%SPIKE_OCP
Minimum Reported Current (00h)			--	0	--	%SPIKE_OCP
IDDSpike Current Accuracy			--	--	3	%
Voltage Report						
Maximum Reported Voltage (0_00h)			--	3.15	--	V
Minimum Reported Voltage (1_F8h)			--	0	--	V
Voltage Accuracy		800mV ≤ VID ≤ 1.2V	–1	--	1	LSB
		VID < 800 mV, VID > 1.2V	–2	--	2	
QR Setting of VDD and VDDNB						
Quick Response Threshold Voltage Setting Range Minimum Value		Refer to Table 4 and Table 5	--	35	--	mV
Quick Response Threshold Voltage Setting Range Maximum Value	$V_{QRTH(MAXx)}$	Refer to Table 4 and Table 5	--	60	--	mV
PWM Driving Capability						
PWMx Source Resistance	R_{PWMsr}		--	20	--	Ω
PWMx Sink Resistance	R_{PWMsk}		--	10	--	Ω

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Timing						
UGATEx Rise Time	t_{UGATEr}	3nF Load	--	25	--	ns
UGATEx Fall Time	t_{UGATEf}	3nF Load	--	12	--	ns
LGATEx Rise Time	t_{LGATEr}	3nF Load	--	24	--	ns
LGATEx Fall Time	t_{LGATEf}	3nF Load	--	10	--	ns
Propagation Delay	$t_{UGATEpdh}$	$V_{BOOTx} - V_{PHASEx}$ = 12V See Timing Diagram	--	60	--	ns
	$t_{UGATEpdl}$		--	22	--	
	$t_{LGATEpdh}$	See Timing Diagram	--	30	--	ns
	$t_{LGATEpdl}$		--	8	--	
Output						
UGATEx Drive Source	I_{UGATE_sr}	$V_{BOOTx} - V_{PHASEx}$ = 12V, I_{Source} = 100mA	--	1.7	--	Ω
UGATEx Drive Sink	R_{UGATE_sk}	$V_{BOOTx} - V_{PHASEx}$ = 12V, I_{Sink} = 100mA	--	1.4	--	Ω
LGATEx Drive Source	I_{LGATE_sr}	I_{Source} = 100mA	--	1.6	--	Ω
LGATEx Drive Sink	R_{LGATE_sk}	I_{Sink} = 100mA	--	1.1	--	Ω

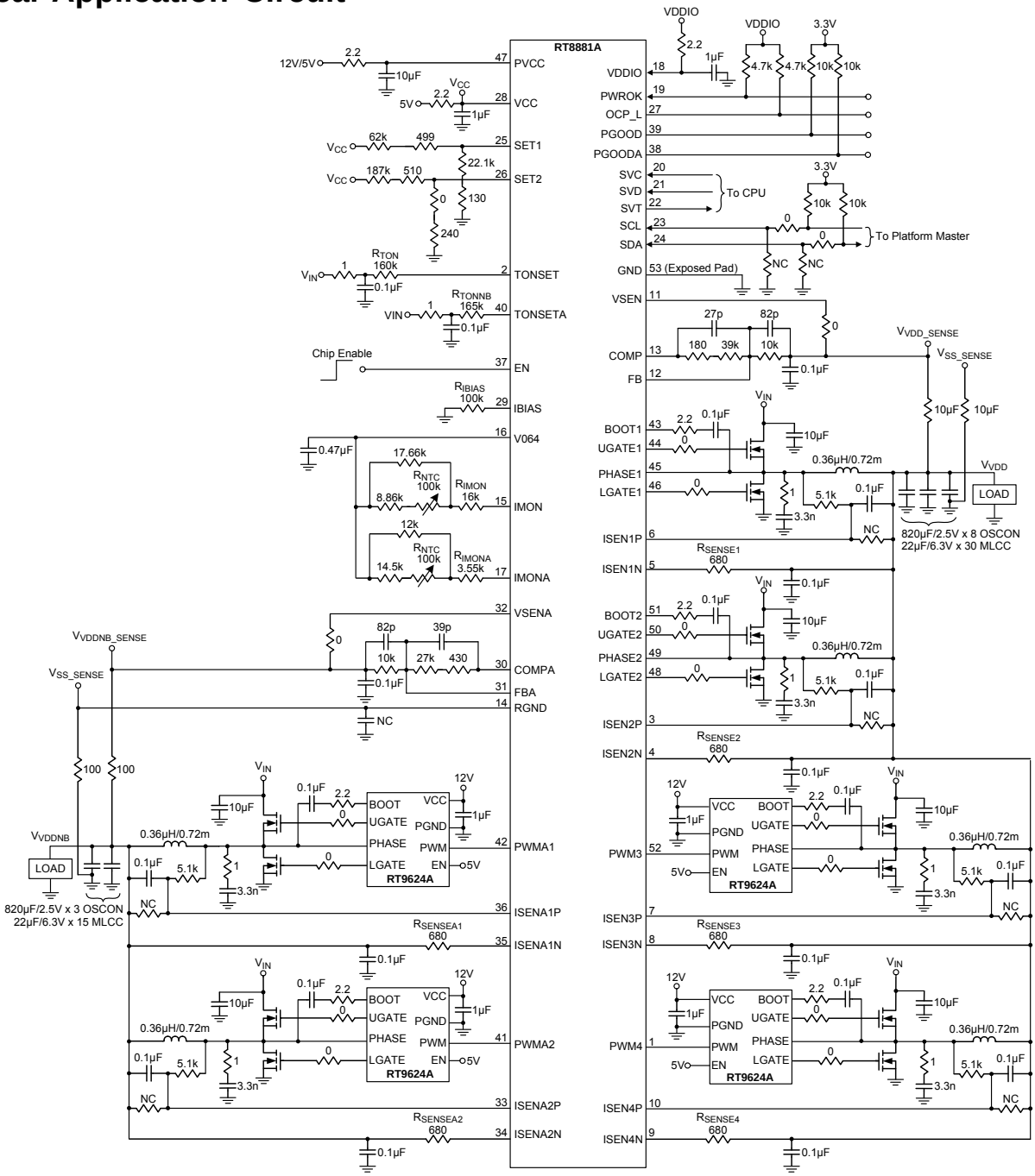
Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

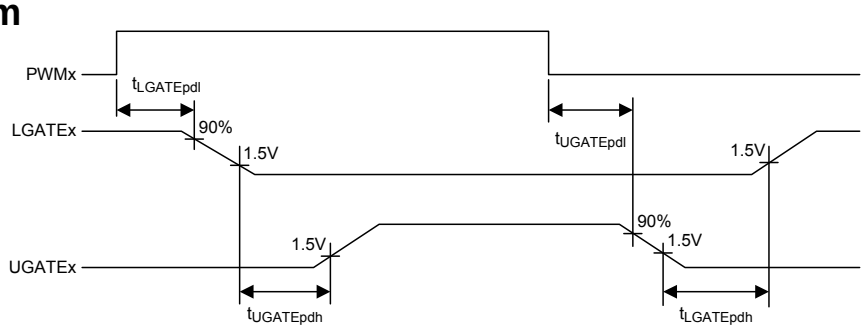
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit

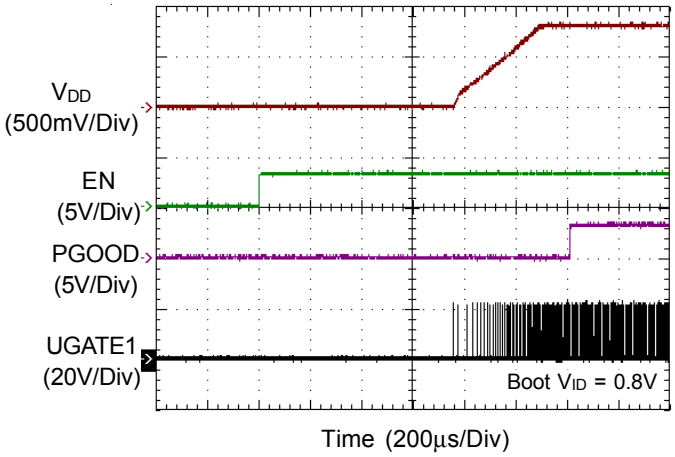


Timing Diagram

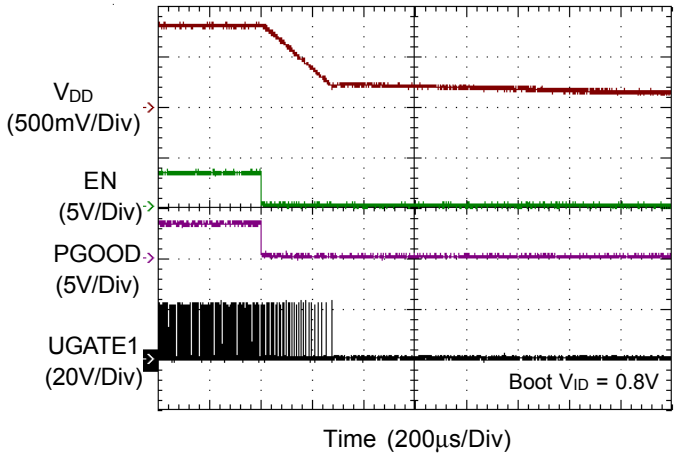


Typical Operating Characteristics

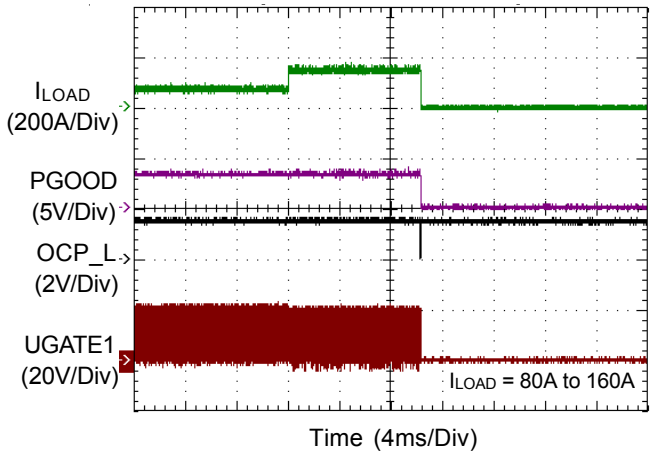
CORE VR Power On from EN



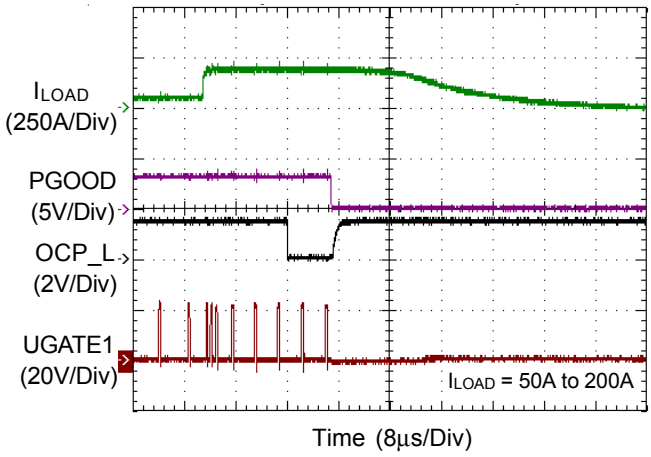
CORE VR Power Off from EN



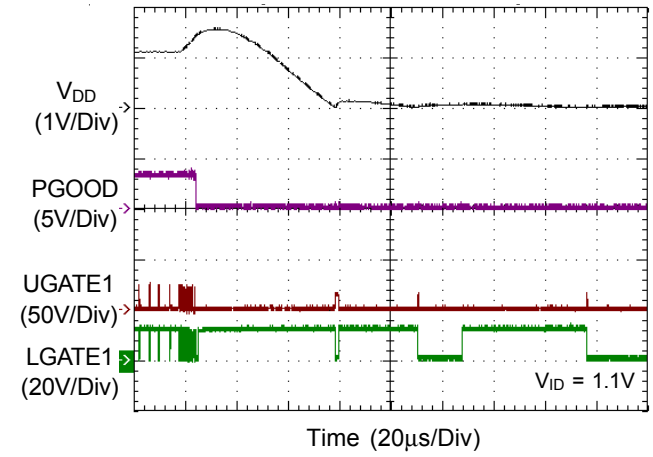
CORE VR OCP_TDC



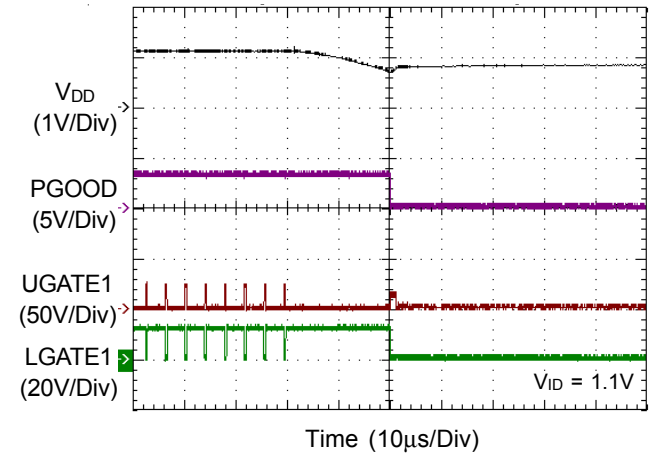
CORE VR OCP_SPIKE



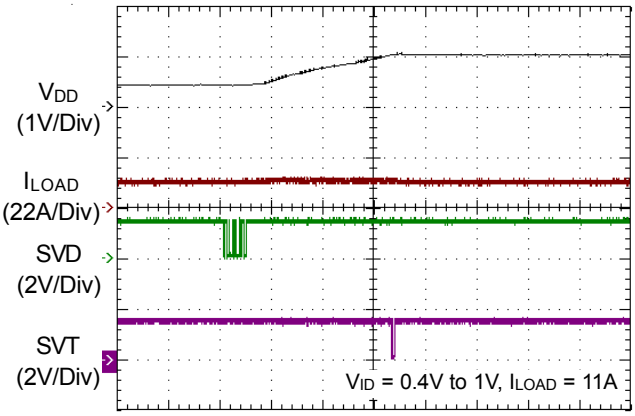
CORE VR OVP and NVP



CORE VR UVP



CORE VR Dynamic VID Up



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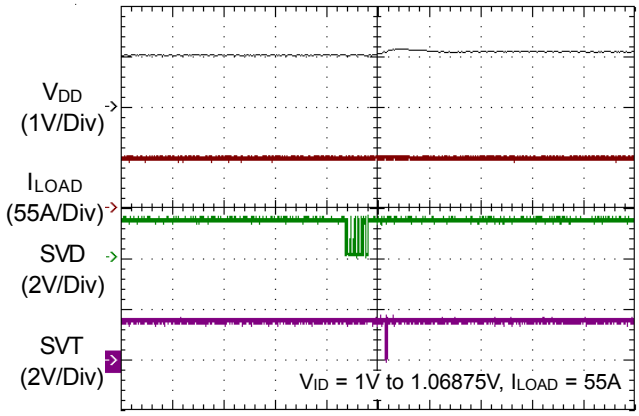

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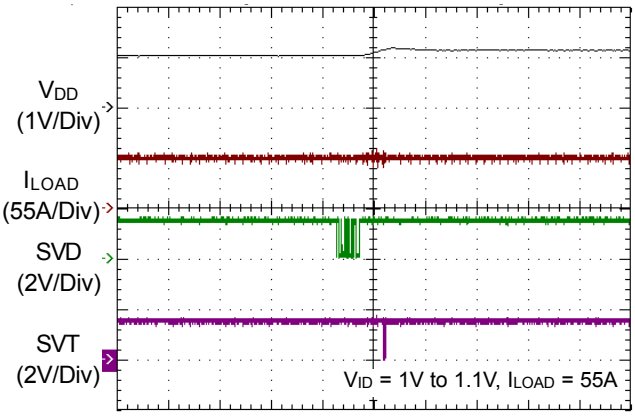

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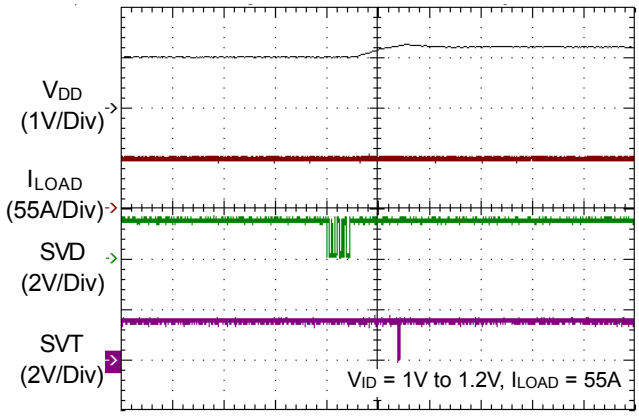
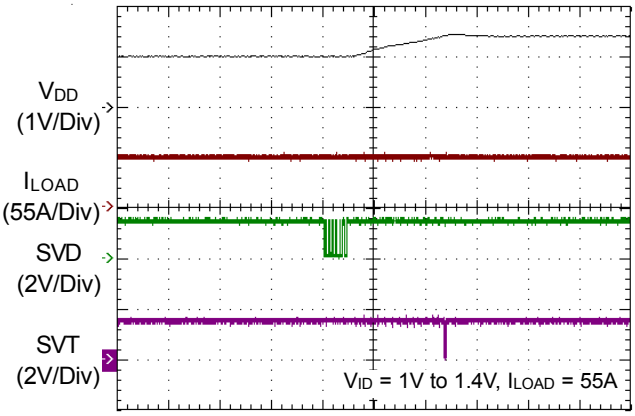
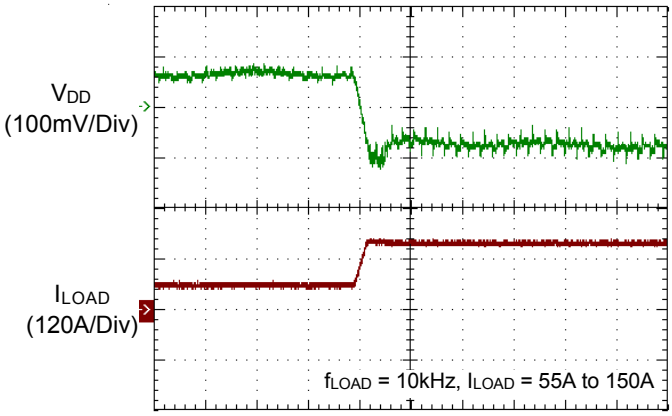


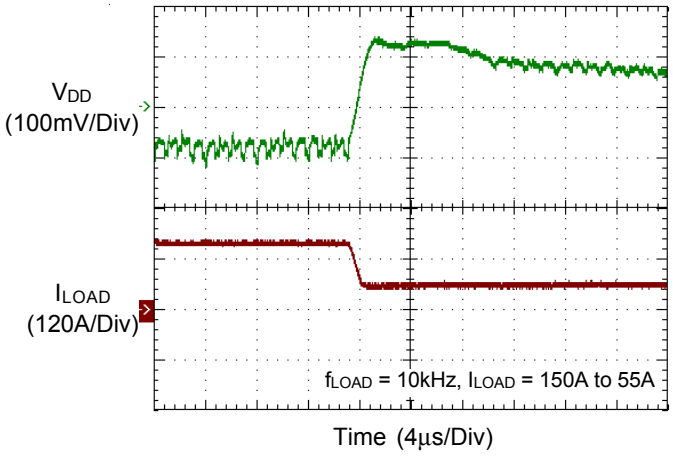
CORE VR Dynamic VID Up



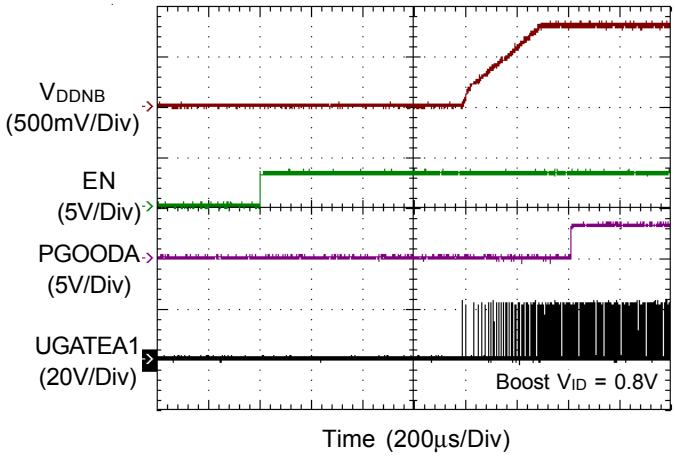
CORE VR Load Transient



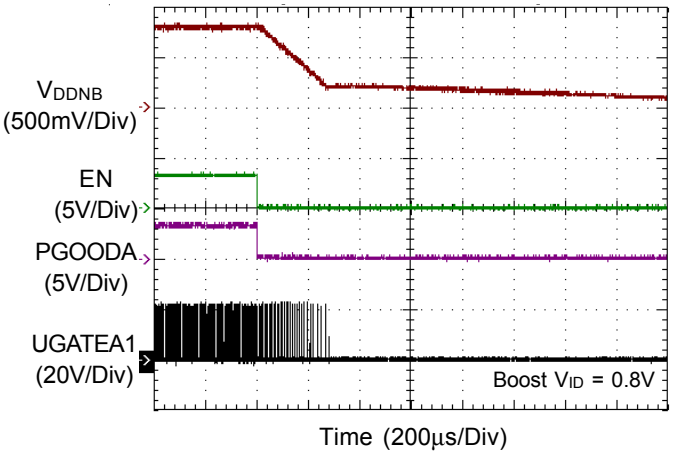
CORE VR Load Transient



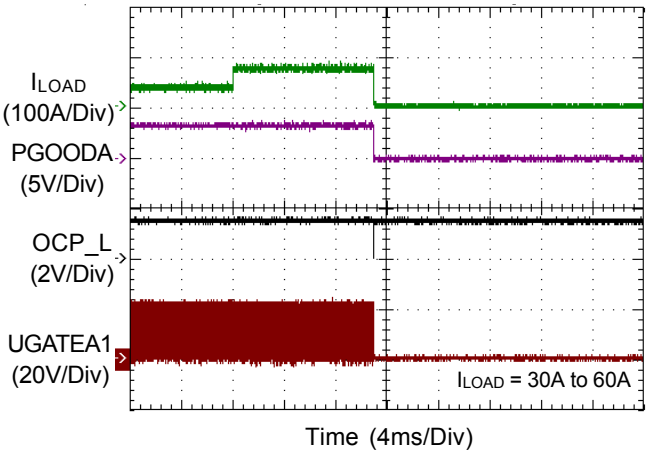
NB VR Power On from EN



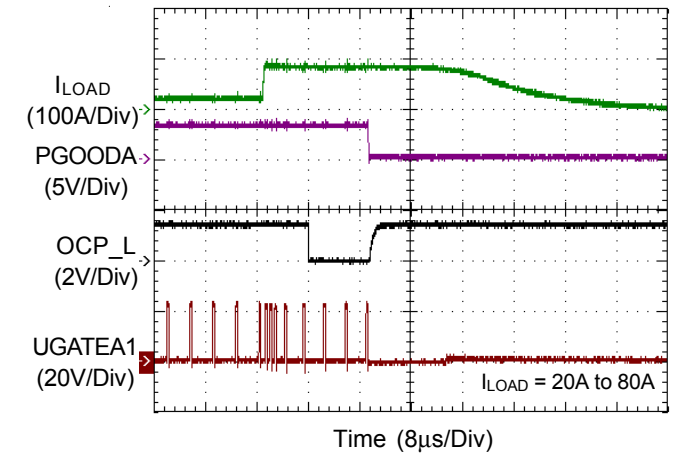
NB VR Power Off from EN



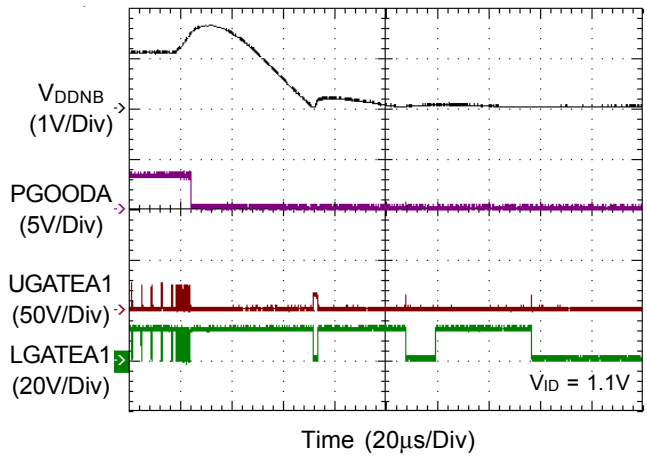
NB VR OCP_TDC



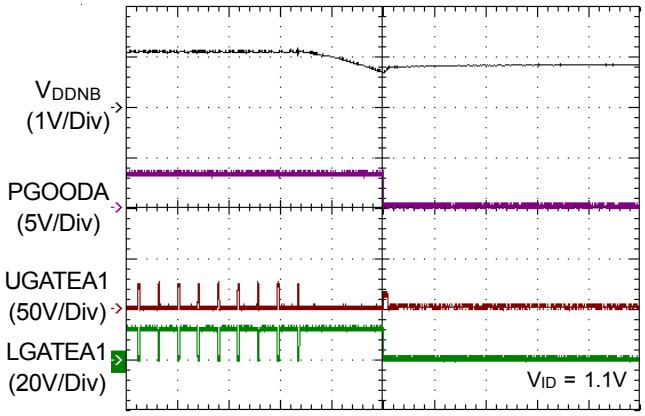
NB VR OCP_SPIKE



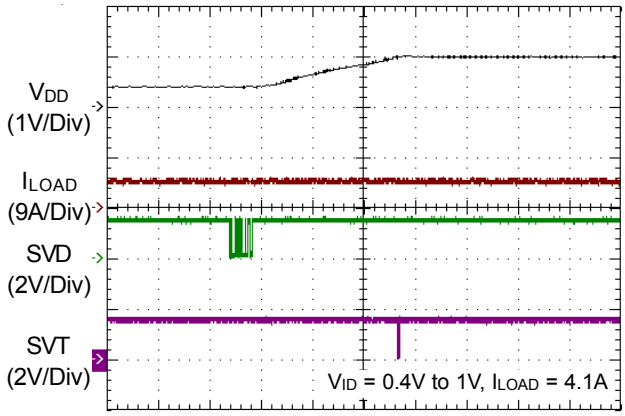
NB VR OVP and NVP



NB VR UVP



NB VR Dynamic VID Up



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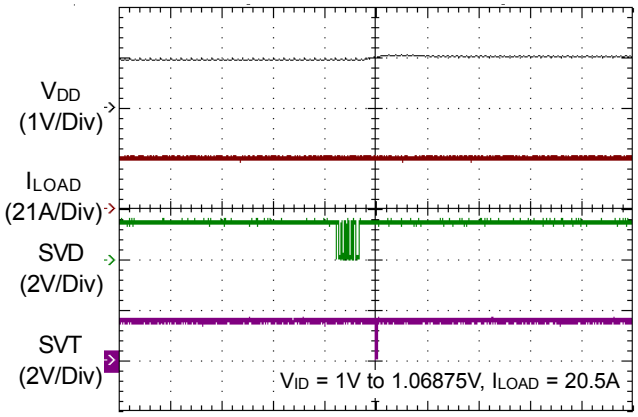

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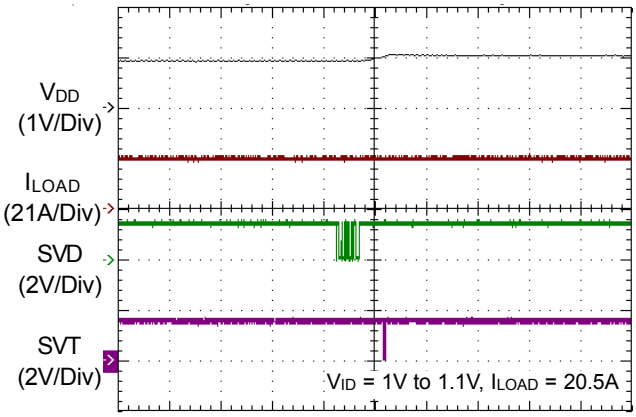
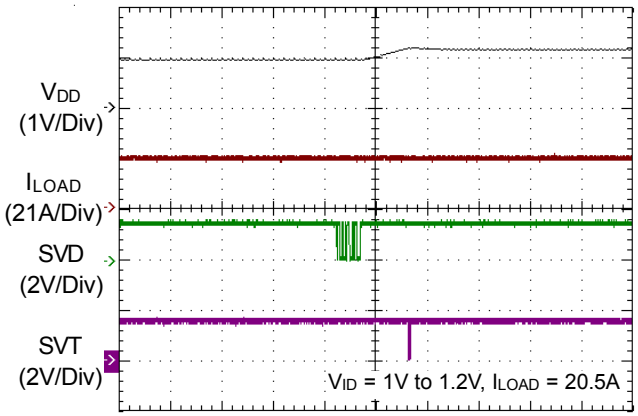


NB VR Dynamic VID Up



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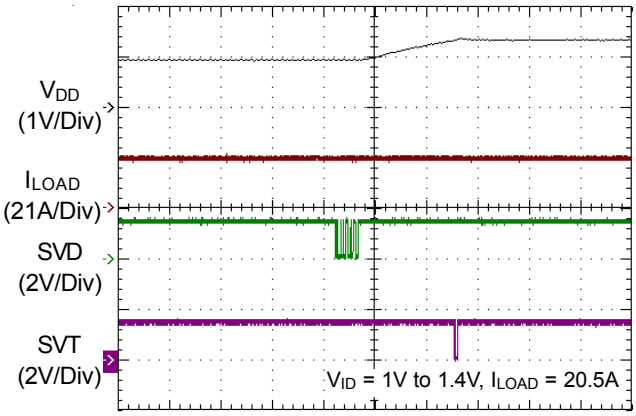
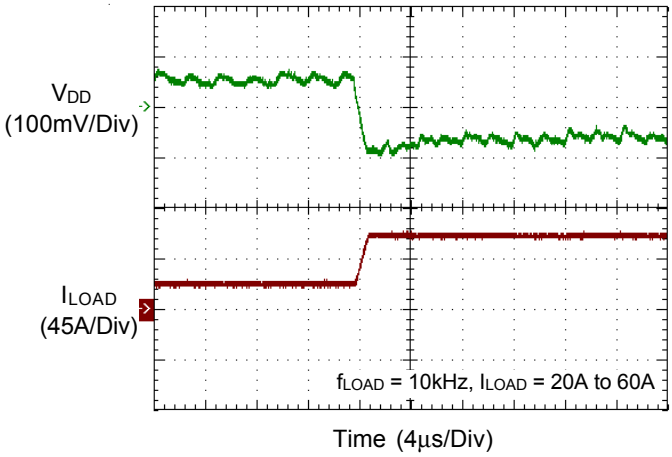
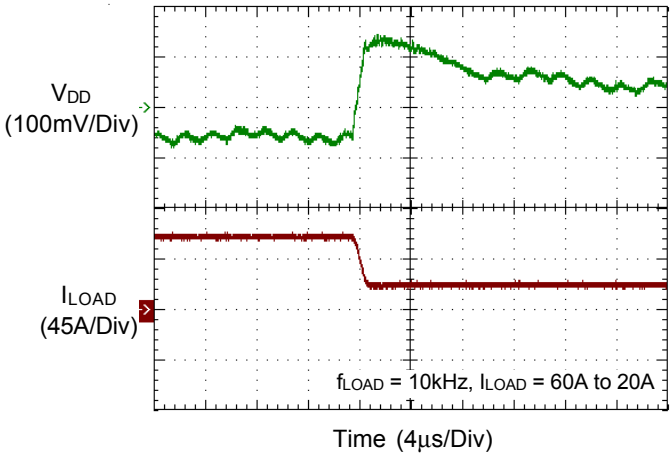


NB VR Load Transient



NB VR Load Transient



Application Information

The RT8881A is a multi-phase PWM controller supporting two outputs. It is compliant with AMD SVI2 Voltage Regulator Specification and to support both core (VDD) and Northbridge (VDDNB) portion of the CPU. Unless otherwise described, the following functions are performed on the RT8881A on each rail independently.

G-NAVP™

The RT8881A adopts the G-NAVP™ controller, which is a current-mode constant on-time control with DC offset cancellation. The approach can not only improve DC offset problem for increasing system accuracy but also provide fast transient response. The control loop consists of PWM modulators with power stages, current sense amplifiers and an error amplifier as shown in Figure 1.

In the RT8881A, when current feedback signal reaches comp signal to generate an on-time width to achieve PWM modulation. Figure 2 shows the basic G-NAVP™ behavior waveforms in Continuous Conduction Mode (CCM).

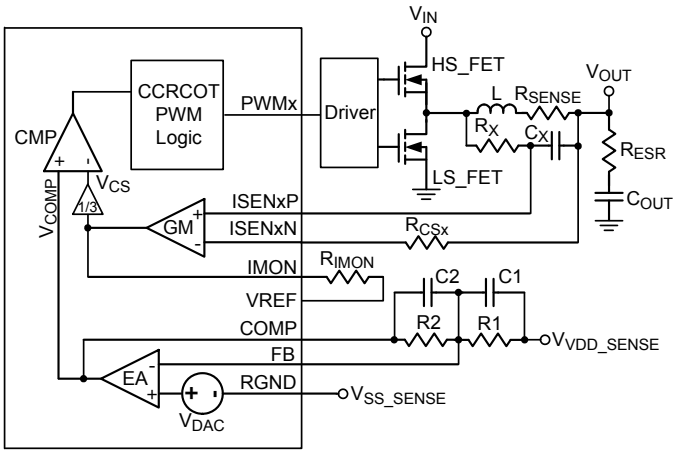
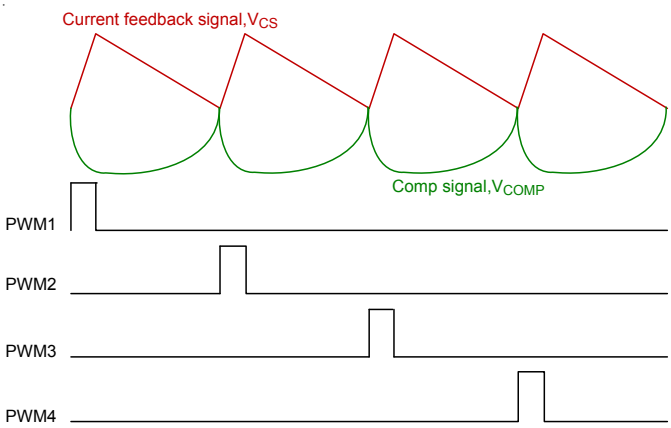
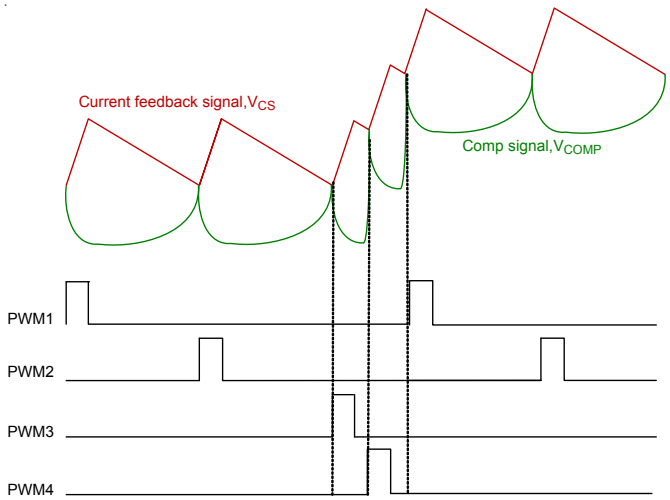


Figure 1. Simplified Schematic for Droop and Remote Sense in CCM



(a). G-NAVP™ Behavior Waveforms in CCM in Steady State



(b). G-NAVP™ Behavior Waveforms in CCM in Load Transient

Figure 2

Diode Emulation Mode (DEM)

As well-known, the dominate power loss is switching related loss during light load, hence VR needs to be operated in asynchronous mode (or called discontinuous conduction mode, DCM) to reduce switching related loss due to switching frequency is dependent on loading in the asynchronous mode. The RT8881A can operate in Diode Emulation Mode (DEM) in order to improve light load efficiency. In DEM operation, the behavior of the low-side MOSFET(s) needs to work like a diode, that is, the low-side MOSFET(s) will be turned on when the phase voltage is a negative value, i.e. the inductor current follows

from Source to Drain of low-side MOSFET(s). The low-side MOSFET(s) will be turned off when phase voltage is a positive value, i.e. reversed current is not allowed. Figure 3 shows the control behavior in DEM. Figure 4 shows the G-NAVP™ operation in DEM to illustrate the control behaviors. When the load decreases, the discharge time of output capacitors increases during UGATE and LGATE are turned off. Hence, the switching frequency and switching loss will be reduced to improve efficiency in light load condition.

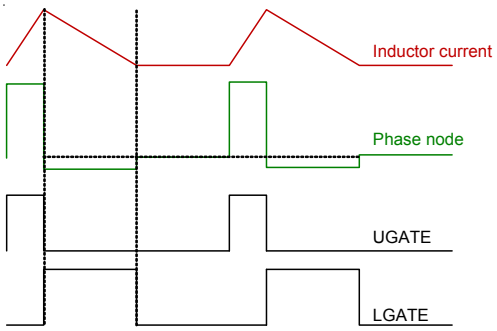
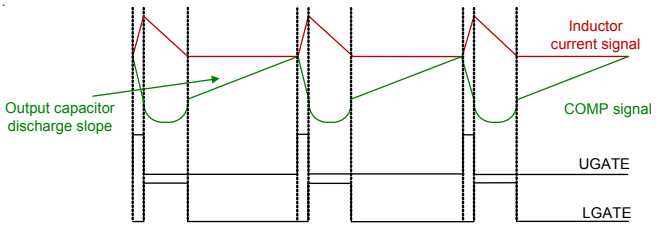
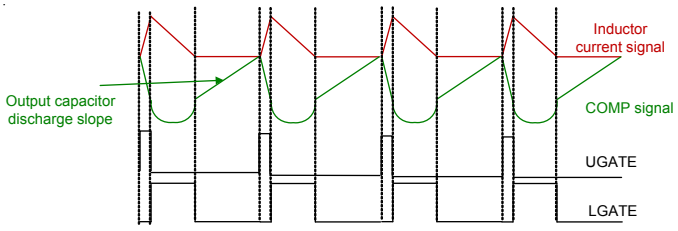


Figure 3. Diode Emulation Mode (DEM) in Steady State



(a). Lighter Load Condition

Capacitor discharge slope is lower than Figure 4 (b)



(b). Load Increased Condition

Capacitor discharge slope is higher than Figure 4 (a)

Figure 4. G-NAVP™ Operation in DEM

Phase Interleaving Function

The RT8881A is a multiphase controller, which has a phase interleaving function in VDD and VDDNB rails, 90 degree phase shift for 4-phase operation, 120 degree phase shift for 3-phase operation and 180 degree phase shift for 2-phase operation, which can help reduce output voltage ripple and EMI problem.

Current Balance

The RT8881A implements internal current balance mechanism in the current loop. The RT8881A senses and compares per-phase current signal with average current. If the sensed current of any particular phase is larger than average current, the on-time of this phase will be adjusted to be shorter.

Active Phase Determination : Before POR

The number of active phases is determined by the internal circuitry that monitors the ISENxN voltages during start-up. Pull ISEN (N + 1) N + 1 pin to VCC to configure for N phase operation. For example, setting the controller in a 3 + 1 configuration, pulling ISEN4N to VCC programs a 3-phase operation of the VDD VR and pulling ISENA2N to VCC programs a 1-phase operation of the VDDNB VR.

Before POR, the controller detects whether the voltages of ISENxN are higher than "VCC – 1V" respectively to decide how many phases should be active. When POR = high, the number of active phases of each rail are determined and latched. The unused ISENxP pins are recommended to be connected to VCC and unused PWM pins can be left floating.

Differential Remote Sense Setting

The RT8881A includes differential, remote-sense inputs to eliminate the effects of voltage drops along the PC board traces, CPU internal power routes and socket contacts. Figure 5 shows the CORE VR differential remote voltage sense connection. The CPU contains on-die sense pins, V_{DD_SENSE} and V_{SS_SENSE}. Connect RGND to V_{SS_SENSE}. Connect FB to V_{DD_SENSE} with a resistor to build the negative input path of the error amplifier. The V_{DAC} and the precision voltage reference are referred to RGND for accurate remote sensing.

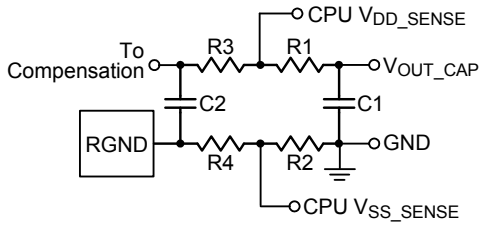


Figure 5. Differential Remote Voltage Sense Connection

Switching Frequency (TON) Setting

High frequency operation optimizes the application for the smaller component size, trading off efficiency due to higher switching losses. This may be acceptable in ultra portable devices where the load currents are lower and the controller is powered from a lower voltage supply. Low frequency operation offers the best overall efficiency at the expense of component size and board space. Figure 6 shows the on-time setting circuit. Connect a resistor (R_{TON}) between V_{IN} and TONSET to set the on-time of UGATE :

$$t_{ON}\ (0.5V < V_{DAC} < 1.8V) = \frac{24.4 \times 10^{-12} \times R_{TON}}{V_{IN} - V_{DAC}} \quad (1)$$

where t_{ON} is the UGATE turn on period, V_{IN} is input voltage of the VR, and V_{DAC} is the DAC voltage.

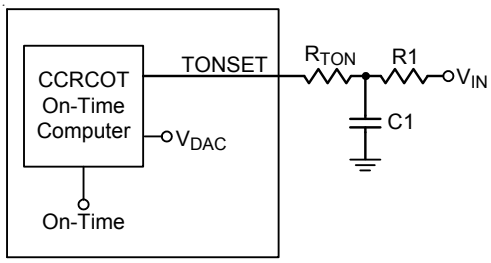


Figure 6. CORE VR : On-Time Setting with RC Filter

When V_{DAC} is larger than 1.8V, the equivalent switching frequency may be over 500kHz, and this fast switching frequency is unacceptable. Therefore, the CORE VR implements a pseudo constant frequency technology to avoid this disadvantage of CCRCOT topology. When V_{DAC} is larger than 1.8V, the on-time equation will be modified to :

$$t_{ON}\ (V_{DAC} \geq 1.8V) = \frac{13.55 \times 10^{-12} \times R_{TON} \times V_{DAC}}{V_{IN} - V_{DAC}} \quad (2)$$

For better efficiency of the given load range, the maximum switching frequency is suggested to be :

$$f_{SW(MAX)} \cong \frac{V_{DAC\_PS0} + \frac{IDDTDC}{N}}{(t_{ON} - 60ns) + \left(\frac{IDDTDC}{N} \times R_{ON\_HS\text{-}FET(MAX)}\right) \times 50ns} \times \frac{(DCR + R_{ON\_LS\text{-}FET(MAX)} - N \times R_{LL})}{\left[V_{IN(MAX)} + \frac{IDDTDC}{N} \times (R_{ON\_LS\text{-}FET(MAX)} - R_{ON\_HS\text{-}FET(MAX)})\right]} \quad (3)$$

where $f_{SW(MAX)}$ is the maximum switching frequency, V_{DAC_PS0} is the test VID of application at normal full phase operation, $V_{IN(MAX)}$ is the maximum application input voltage, IDDTDC is the thermal design current of application, N is the phase number, $R_{ON\_HS\text{-}FET(MAX)}$ is the maximum equivalent high-side FET $R_{DS(ON)}$, $R_{ON\_LS\text{-}FET(MAX)}$ is the maximum equivalent low-side FET $R_{DS(ON)}$, DCR is the inductor DCR, and R_{LL} is the load-line setting.

Current Sense Setting

The current sense topology of the VR is continuous inductor current sensing. Therefore, the controller has less noise sensitive. Low offset amplifiers are used for current balance, loop control and over current detection. The ISENxP and ISENxN pins denote the positive and negative input of the current sense amplifier of each phase.

Users can either use a current-sense resistor or the inductor DCR for current sensing. Using the inductor's DCR allows higher efficiency as shown in Figure 7.

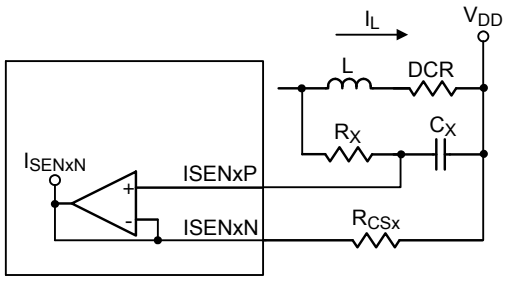


Figure 7. Lossless Inductor Sensing

In order to optimum transient performance, R_X and C_X must be set according to the equation below :

$$\frac{L}{DCR} = R_X \times C_X \quad (4)$$

Then the proportion between the phase current I_L and the sensed current I_{SENxN} can be described as below :

$$I_{SENxN} = I_L \times \frac{DCR}{R_{CSx}} \quad (5)$$

where R_{CSx} is sense resistor and it only with a exact 680Ω resistor. The resistance accuracy of R_{CSx} is recommended to be 1% or higher.

In addition to consider the inductance tolerance, the resistor R_X has to be tuned on board by examining the transient voltage. If the output voltage transient has an initial dip below the minimum load-line requirement and the recovery is too fast causing a ring back. Vice versa, with a resistance too large the output voltage transient has only a small initial dip with a slow recovery.

Using current sense resistor in series with the inductor can have better accuracy, but the efficiency is a trade-off. Considering the equivalent inductance (L_{ESL}) of the current sense resistor, an RC filter is recommended. The RC filter calculation method is similar to the inductor DCR sensing method mentioned above.

OCPSpike Current Setting and Current Reporting

The RT8881A provides the current monitor function for VR. In VDD VR, IMON pin reports VDD VR inductor sum current. The IMON pin outputs a high-speed analog current source that is 1 times of the summed current. Thus I_{IMON} can be described as below :

$$I_{IMON} = \sum I_{SENxN} \quad (6)$$

The RT8881A monitors the IMON pin voltage and considers that VDD VR has reached the OCPSpike current when the IMON pin voltage is 3.19375V.

As show in Figure 1, a resistor R_{IMON} is connected between the IMON and V064 pins. Through the R_{IMON} to convert the IMON pin current to voltage. The voltage of the IMON pin is expressed in Equation 7 :

$$V_{IMON} = I_{IMON} \times R_{IMON} + 0.64 \quad (7)$$

Rewriting Equations 5 and 6 gives Equation 8 :

$$I_{IMON} = \frac{DCR}{R_{CSx}} \times I_{LOAD} \quad (8)$$

Substitution of Equation 8 in to Equation 7 gives Equation 9 :

$$V_{IMON} = \frac{DCR}{R_{CSx}} \times I_{LOAD} \times R_{IMON} + 0.64 \quad (9)$$

Rewriting Equation 9 and application of full load condition gives Equation 10 :

$$R_{IMON} = \frac{R_{CSx}}{DCR} \times \frac{(V_{IMON} - 0.64)}{OCPSpike} \quad (10)$$

For example, given R_{CSx} = 680Ω, DCR = 0.82mΩ, V_{IMON} = 3.19375V at OCPSpike = 200A, Equation 10 gives R_{IMON} = 10.588kΩ.

In addition, Richtek provides a Microsoft Excel-based spreadsheet to help design the IMON resistor network with temperature compensation for VDD VR.

Load-Line (Droop) Setting

It's very easy to achieve Active Voltage Positioning (AVP) by properly setting the error amplifier gain due to the native droop characteristics. This target is to have

$$V_{OUT} = V_{DAC} - I_{LOAD} \times R_{LL} \quad (11)$$

Then solving the switching condition $V_{COMP} = V_{CS}$ in Figure 1 yields the desired error amplifier gain as

$$A_V = \frac{R2}{R1} = \frac{A_I}{R_{LL}} \quad (12)$$

where R_{LL} is the equivalent load line resistance as well as the desired static output impedance.

The summed current sense gain A_I is

$$A_I = \frac{DCR}{R_{CSx}} \times R_{IMON} \times \frac{1}{3} \quad (13)$$

The load line equation is

$$R_{LL} = \frac{A_I}{A_V} = \frac{1}{3} \times \frac{R1}{R2} \times \frac{DCR}{R_{CSx}} \times R_{IMON}\ (m\Omega) \quad (14)$$

For example, given R_{LL} = 1.3mΩ, R_{CSx} = 680Ω, DCR = 0.82mΩ, R_{IMON} = 10.588kΩ and R1 = 10kΩ, Equation 14 gives R2 = 32.738kΩ.

Loop Compensation

Optimized compensation of the VR allows for best possible load step response of the regulator's output. A type-I compensator with one pole and one zero is adequate for proper compensation. Figure 1 shows the compensation circuit. Prior design procedure shows how to select the resistive feedback components for the error amplifier gain. Next, C1 and C2 must be calculated for

the compensation. The target is to achieve constant resistive output impedance over the widest possible frequency range.

The pole frequency of the compensator must be set to compensate the output capacitor ESR zero, where C_{OUT} is the capacitance of output capacitor, and R_{ESR} is the ESR of output capacitor.

$$f_p = \frac{1}{2\pi \times C_{OUT} \times R_{ESR}} \quad (15)$$

C2 can be calculated as follows :

$$C2 = \frac{C_{OUT} \times R_{ESR}}{R2} \quad (16)$$

The zero of compensator has to be placed at half of the switching frequency to filter the switching related noise. Such that,

$$C1 = \frac{1}{R1 \times \pi \times f_{SW}} \quad (17)$$

Quick Response (QR) Mechanism

When the transient load step-up becomes quite large, it is difficult loop response to meet the energy transfer. Hence, the output voltage generates undershoot to fail specification.The RT8881A has Quick Response (QR) mechanism which is able to improve this issue. It adopts a nonlinear control mechanism which can disable interleaving function and simultaneously turn on all UGATE one pulse at instantaneous step-up transient load to restrain the output voltage drooping, Figure 8 shows the QR behavior.

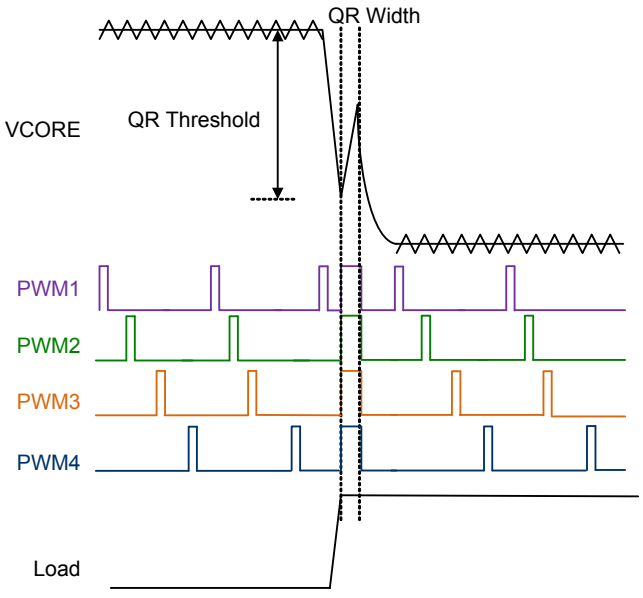


Figure 8. Quick Response Mechanism

The output voltage signal behavior needs to be detected so that QR mechanism can be trigged. The output voltage signal is via a remote sense line to connect at the VSEN pin that is shown in Figure 9. The QR mechanism needs to set QR width and QR threshold (In SVI mode, only QR threshold can be set in SET2 pin, QR width is 1.1 x T_{ON}). Both definitions are shown in Figure 8.The QR threshold setting for VDD controller refers to Table 4 and Table 5.

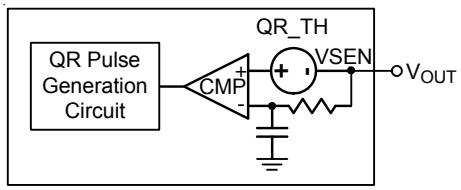


Figure 9. Quick Response Triggering Circuit

Ramp Compensation

The G-NAVP™ topology is one type of ripple based control that has fast transient response, no beat frequency issue in high repetitive load frequency operation and low BOM cost. However, ripple based control usually don't have good noise immunity. The RT8881A provides a ramp compensation to increase noise immunity and reduce jitter at the switching node. Figure 10 shows the ramp compensation.

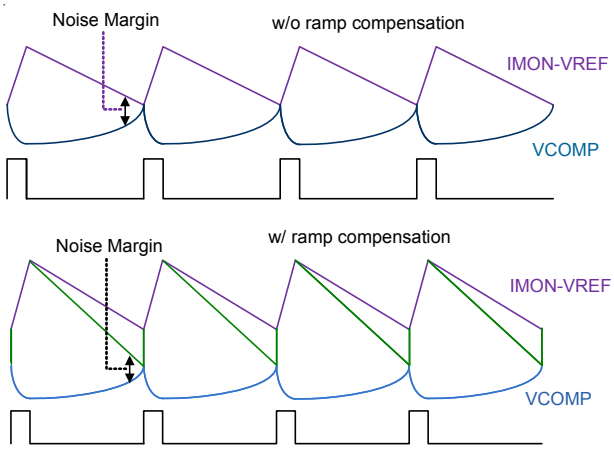


Figure 10. Ramp Compensation

Multi-Function Pin Setting

The RT8881A provides the SET1 pin for platform users to set the VDD and VDDNB VR OCP_TDC threshold and internal ramp compensation amplitude (RSET & RSETA), and the SET2 pin to set VDD and VDDNB VR OCP trigger delay (OCPTRGDELAY) and quick response threshold (QRTH & QRTHA). For more description for OCP_TDC threshold and OCP trigger delay settings, please refer to over-current protection section.

To set these pins, platform designers should use resistive voltage divider on these pins, refer to Figure 11 and Figure 12. The voltage at the SET1 and SET2 pins are

$$V_{SET1} = V_{CC} \times \frac{R_{OCPTDC,D}}{R_{OCPTDC,U} + R_{OCPTDC,D}} \quad (18)$$

$$V_{SET2} = V_{CC} \times \frac{R_{QRTH,D}}{R_{QRTH,U} + R_{QRTH,D}} \quad (19)$$

The ADC monitors and decodes the voltage at this pin only after power up. After ADC decoding (only once), a 80μA current will be generated at the SET1 and SET2 pins for internal use. The voltage at the SET1 and SET2 pins are

$$\Delta V_{SET1} = 80\mu A \times \frac{R_{OCPTDC,U} \times R_{OCPTDC,D}}{R_{OCPTDC,U} + R_{OCPTDC,D}} \quad (20)$$

$$\Delta V_{SET2} = 80\mu A \times \frac{R_{QRTH,U} \times R_{QRTH,D}}{R_{QRTH,U} + R_{QRTH,D}} \quad (21)$$

From equation (18) to equation (21) and Table 2 to Table 5, platform users can set the OCP_TDC threshold, OCP trigger delay, internal ramp amplitude and quick response threshold for VDD and VDDNB VR.

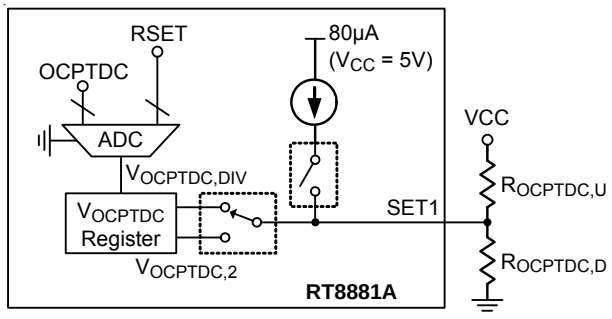


Figure 11. OCP_TDC/RSET Setting

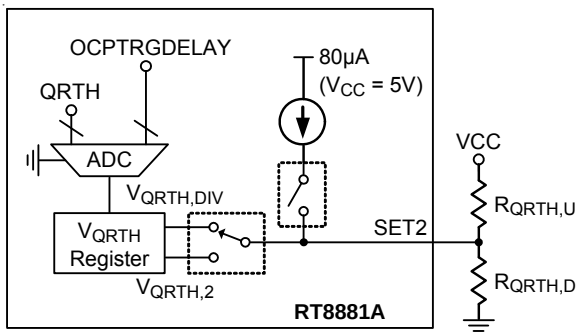


Figure 12. QRTH/OCPTRGDELAY Setting

Power Ready (POR) Detection

During start-up, the RT8881A will detect the voltage at the voltage input pins : VCC, EN and PVCC. When V_{CC} > 4.3V and PVCC > 4V, the IC will recognize the power state of system to be ready (IC POR = high). After 50μs delay, enable signal can be asserted at the EN pin. After POR = high and V_{EN} > 2V, the IC will enter start-up sequence for both VDD VR and VDDNB VR. If the voltage at any voltage input pin drops below low threshold (POR = low), the IC will enter power down sequence and all the functions will be disabled. Normally, connecting system enable signal to the EN pin is recommended. The SVID will be ready in 2ms (MAX) after the chip has been enabled. All the protection latches (OVP, OCP, UVP) will be cleared only after POR = low. The condition of V_{EN} = low will not clear these latches.

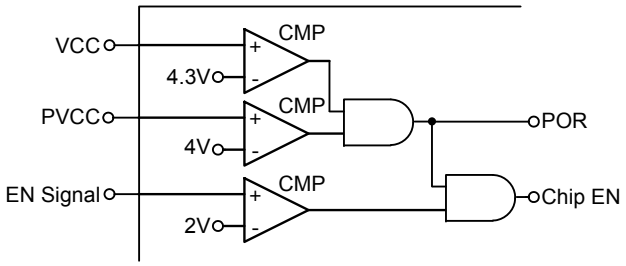


Figure 13. Power Ready (POR) Detection

Start-Up Sequence

The start-up sequence is initiated when all the following conditions are satisfied. Figure 14 shows the simplified sequence timing diagram of the RT8881A.

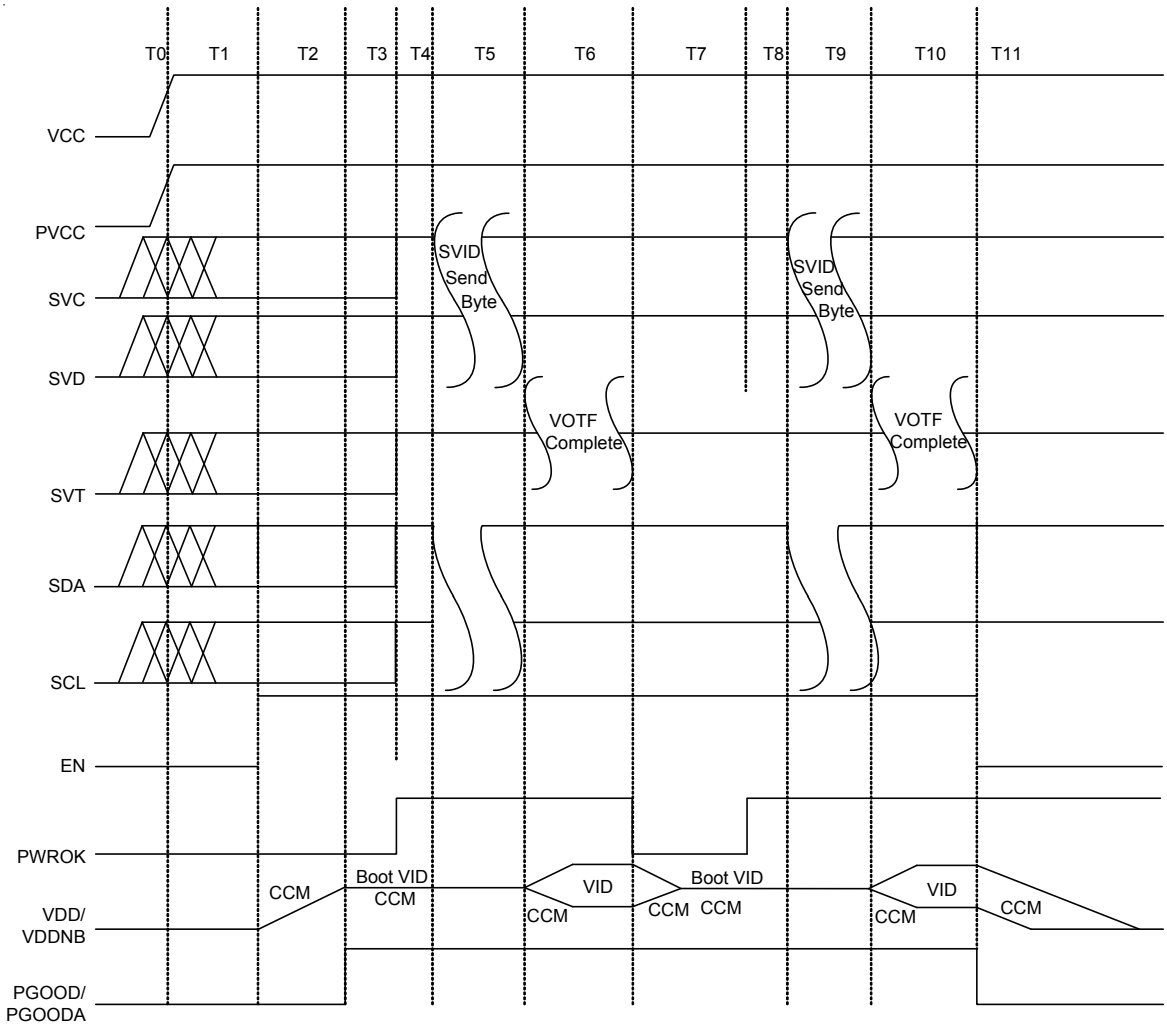


Figure 14. Simplified Sequence Timing Diagram

The detailed operation is described in the following.

T0 : The RT8881A waits for VCC and PVCC POR. The number of active phases is determined and latched when POR = high.

T1 : The SVC and SVD pins set the Boot VID. The SCL and SDA pins set the operating mode. Boot VID and operating mode are latched at EN rising edge.

T2 : The enable signal goes high and all output voltages ramp up to the boot VID in CCM. The soft start slew rate is 3mV/μs.

T3 : All output voltages are within the regulation limits and the PGOOD and PGOODA signal goes high.

T4 : The PWROK pin goes high and the SVI2 interface and I^2C interface start running. The RT8881A waits for SVID command from processor and the operating parameters that can be adjusted through the I^2C interface. If RT8881A operates in SVI mode, the I^2C interface is disabled.

T5 : A valid SVID command transaction occurs between the processor and the RT8881A.

T6 : The RT8881A starts VID-on-the-fly transition according to the received SVID command and send a VOTF Complete if the VID reaches target VID.

T7 : The PWROK pin goes low and the SVI2 interface and I^2C interface stop running. All output voltages go back to the boot VID in CCM operating but the operating parameters are not affected.

T8 : The PWROK pin goes high and the SVI2 interface and I^2C interface start running. The RT8881A waits for SVI command from processor and the operating parameters that can be adjusted through the I^2C interface.

Power-Down Sequence

If the voltage at the EN pin falls below the enable falling threshold, the controller is disabled. The voltage at the PGOOD and PGOODA pins will immediately go low when the EN pin voltage is pulled low and the controller will execute soft-shutdown operation. The internal digital circuit ramps down the reference voltage at the same slew rate in soft-start, making VDD and VDDNB output voltages gradually decrease in CCM. Each channel stops switching when the voltage at the VSEN/VSENA pin reaches about 0.2V. The Boot VID information stored in the internal register is cleared at POR. This event forces the RT8881A to check the SVC and SVD inputs for a new boot VID when the EN voltage goes high again.

PWROK Operation

The PWROK pin is an input pin, which is connected to the global power good signal from the platform. In SVI mode, logic high at this pin enables the SVI2 interface, allowing data transaction between processor and the RT8881A. If the PWROK input goes low during normal operation, the SVI2 protocol stops running. The RT8881A immediately drives SVT high and modifies all output voltages back to the boot VID, which is stored in the internal register right after the controller is enabled. The controller does not read SVD and SVC inputs after the loss of PWROK. If the PWROK input goes high again, the SVI2 protocol resumes running. The RT8881A then waits for decoding the SVID command from processor for a new VID and acts as previously described. The SVI2 protocol runs only when the PWROK input goes high after the voltage at the EN pin goes high; otherwise, the RT8881A will not soft-start due to incorrect signal sequence.

Also, this pin enables the I^2C interface in I^2C mode, allowing data transaction between SMBUS and the RT8881A. If the PWROK input goes low during normal operation, the I^2C protocol stops running and the I^2C register do not affected by SDA and SCL. If the PWROK input goes high again, the I^2C protocol resumes running.

PGOOD and PGOODA

The PGOOD and PGOODA are open-drain logic outputs. The PGOOD and PGOODA pins provide the power good signal when VDD and VDDNB output voltage are within the regulation limits and no protection is triggered. The PGOOD and PGOODA pins are typically tied to 3.3V or 5V power source through a pull-high resistor. During shutdown state (EN = low) and the soft-start period, the PGOOD and PGOODA voltage are pulled low. After a successful soft-start and VDD and VDDNB output voltages are within the regulation limits, the PGOOD and PGOODA are released high individually.

The voltage at the PGOOD and PGOODA pins are pulled low individually during normal operation when any of the following events occurs : over-voltage protection, under-voltage protection, over-current protection, and logic-low EN voltage. If one rail triggers protection, another rail's PGOOD will be pull low after 5μs delay.

VID on-the-Fly Transition

After the RT8881A has received a valid SVID code, it enters CCM mode and executes the VID on-the-fly transition by stepping up/down the reference voltage of the required controller channel(s) in a controlled slew rate, hence allowing the output voltage(s) to ramp up/down to the target VID. The output voltage slew rate during the VID on-the-fly transition is faster than that in a soft-start/soft-shutdown operation. If the new VID level is higher than the current VID level, the controller begins stepping up the reference voltage with a typical slew rate of 12mV/μs upward to the target VID level. If the new level is lower than the current VID level, the controller begins stepping down the reference voltage with a typical slew rate of –12mV/μs downward to the target VID level.

During the VID on-the-fly transition, the RT8881A will force the controller channel to operate in CCM mode. If the controller channel operates in the power-saving mode prior to the VID on-the-fly transition, it will be in CCM mode during the transition and then back to the power saving mode at the end of the transition. The voltage at the PGOOD and PGOODA pins will keep high during the VID on-the-fly transition. The RT8881A checks the output voltage for voltage related protections and send a VOTF Complete at the end of VID on-the-fly transition. In the event of receiving a VID off code, the RT8881A steps the reference voltage of required controller channel down to zero, hence making the required output voltage decreases

to zero. The voltage at the PGOOD and PGOODA pins will remain high since the VID code is valid.

Precise Reference Current Generation

The RT8881A includes complicated analog circuits inside the controller. These analog circuits need very precise reference voltage/current to drive these analog devices. The RT8881A will auto generate a 2V voltage source at IBIAS pin, and a 100kΩ resistor is required to be connected between IBAIS and analog ground, as shown in Figure 15. Through this connection, the RT8881A will generate a 20μA current from the IBIAS pin to analog ground, and this 20μA current will be mirrored inside the RT8881A for internal use. Note that other type of connection or other values of resistance applied at the IBIAS pin may cause failure of the RT8881A's functions, such as slew rate control, OFS accuracy, etc. In other words, the IBIAS pin can only be connected with a 100kΩ resistor to GND. The resistance accuracy of this resistor is recommended to be 1% or higher.

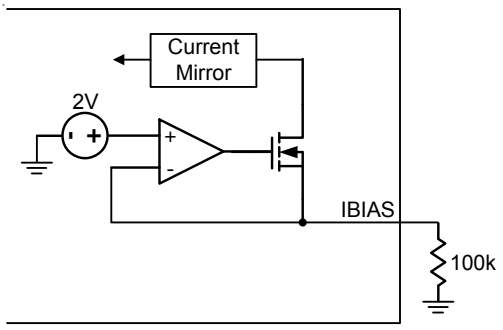


Figure 15. IBAIS Setting

Power State Transition

In SVI mode, the RT8881A supports power state transition function in VDD and VDDNB VR for the PSI[x]_L and command from AMD processor. The PSI[x]_L bit in the SVI2 protocol controls the operating mode of the RT8881A controller channels. The default operation mode of VDD and VDDNB VR is CCM.

When the VDD VR is in full-phase configuration and receives PSI0_L = 0 and PSI1_L = 1, the VDD VR will keep full-phase operation. When the VDD VR receives PSI0_L = 0 and PSI1_L = 0, the VDD VR takes phase shedding operation and enters diode emulation mode. In reverse, the VDD VR goes back to full-phase operation in CCM upon receiving PSI0_L = 1 and PSI1_L = 0 or 1, or PSI0_L = 0 and PSI1_L = 1, see Table 6. When the VDDNB VR receives PSI0_L = 0 and PSI1_L = 1, it enters single-phase CCM, when the VDDNB VR receives PSI0_L = 0 and PSI1_L = 0, it enters single-phase diode emulation mode. When the VDDNB VR goes back to full-phase CCM operation after receiving PSI0_L = 1 and PSI1_L = 0 or 1, see Table 7.

Table 6. VDD VR Power State

Full Phase Number	PSI0_L : PSI1_L	Mode
4	11	4 phase CCM
	01	4 phase CCM
	00	1 phase DEM
3	11	3 phase CCM
	01	3 phase CCM
	00	1 phase DEM
2	11	2 phase CCM
	01	2 phase CCM
	00	1 phase DEM
1	11	1 phase CCM
	01	1 phase CCM
	00	1 phase DEM

Table 7. VDDNB VR Power State

Full Phase Number	PSI0_L : PSI1_L	Mode
2	11	2 phase CCM
	01	1 phase CCM
	00	1 phase DEM
1	11	1 phase CCM
	01	1 phase CCM
	00	1 phase DEM

Dynamic Phase Control Capability (only in I²C mode)

In I²C mode, the RT8881A has the ability to automatically shed its operating phase number according to the total load current to improve medium to light load range. This function can be enabled or disabled through a register setting in I²C mode, and the power state change command from AMD processor by SVI interface is ignored.

Because the IMON pin voltage (V_{IMON}) represents the total current, and maximum V_{IMON} corresponds to OCPSpike current, the controller compares V_{IMON} with threshold1 (V_{TH1}) and threshold2 (V_{TH2}) to decide the number of operating phase. The RT8881A hops to higher phase number operation when V_{IMON} higher than V_{TH1} or V_{TH2}. No hysteresis and extra delay exists during an up phase decision. However, hysteresis (V_{HYS}) and delay time (<100μs) exist during a down phase decision. The RT8881A triggers a timer when V_{IMON} is lower than (V_{TH1} – V_{HYS1}) or (V_{TH2} –V_{HYS2}). If V_{IMON} is always lower than (V_{TH1} – V_{HYS2}) or (V_{TH2} – V_{HYS2}) during a certain amount of time (<100μs), the controller goes to lower phase number operation. For example, the default threshold2 is 4% of OCPSpike and the hysteresis is 2% of OCPSpike. If OCPSpike is designed as 200A, the down phase operation can only take place when load current is continuously lower than 4A for 100μs and increases phase number when load current higher then 8A. When RT8881A detected the inductor current is down to zero in PS2 state by phase pins, the RT8881A enters diode emulation mode. Furthermore, when a DVID up or a QR event is triggered, the RT8881A jumps back to maximum-phase operation immediately. See Figure 16 for the dynamic phase control mechanism.

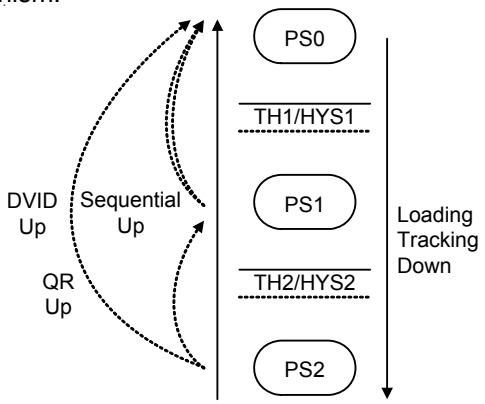


Figure 16. Dynamic Phase Control Mechanism

Operation Mode Decision (SVI mode or I²C mode)

The RT8881A supports three modes for operating, allowing one chip to be used for multiple applications. This greatly enhances the freedom of design for users. The designer should use pin-strapped method with SCL and SDA pins to decide which mode to operate before EN rising. After those pins are configured, the EN signal is used to force the RT8881A into either pure SIV mode or I²C mode. Table 8 shows the Mode Decision setting.

Table 8. Mode Decision Setting

SCL	SDA	Function
0	0	SVI Mode
1	1	I²C Mode

SVI Mode

In SVI mode, the RT8881A configures its function to be fully compliant with AMD SVI2 Specification. All the setting of RT8881A is configured by the SET1 and SET2 pins.

I²C Mode

In I²C mode, control and communication with RT8881A may occur either through the SVI interface where an AMD SVI command is present or alternatively through the I²C interface for any other performance registers setting.

Boot VID

When EN goes high, both VDD and VDDNB output begin to soft-start to the boot VID in CCM. Table 9 shows the boot VID setting. The boot VID is determined by the SVC and SVD input states at EN rising edge and it is stored in the internal register. The digital soft-start circuit ramps up the reference voltage at a controlled slew rates to reduce inrush current during start up. When all the output voltage are above power good threshold (300mV below boot VID) at the end of soft-start, the controller asserts power good after a time delay.

Table 9. 2-Bit Boot VID Code

Initial Startup VID Code		
SVC	SVD	VDD/VDDNB Output Voltage (V)
0	0	1.1
0	1	1
1	0	0.9
1	1	0.8

Protection Function

Over-Current Protection

The RT8881A has dual OCP and per phase OCP mechanisms. The dual OCP mechanism has two types of thresholds. The first type, referred to as OCPTDC, is a time and current based threshold. OCPTDC should trip when the average output current exceeds TDC by some percentage and for a period of time. This period of time is referred to as the trigger delay. The second type, referred to as OCPSpike, is a current based threshold. OCPSpike should trip when the cycle-by-cycle output current exceeds spike current by some percentage. If either mechanism trips, then the controller asserts OCP_L and delays any further action. This delay is called an action delay. Refer to action delay time. After the action delay has expired and the controller has allowed its current sense filter to settle out and the current has not decreased below the threshold, then the controller will turn off both high-side MOSFETs and low-side MOSFETs of all channels.

The controller determines OCP by comparing the I_{IMON} with OCPTDC threshold and OCPSpike threshold, which setting refer to the I_{MON} pin setting section. Users can set OCPSpike threshold, $I_{L(Spike)}$, by the current monitor resistor R_{IMON} of the following equation :

$$I_{L,SUM}\ (SPIKE) = \frac{3.19375 - 0.64}{DCR} \times \frac{R_{CSx}}{R_{IMON}} \quad (24)$$

And set the OCPTDC threshold, $I_{L(TDC)}$, refer to some percentage of OCPSpike through Table 2.

For per phase OCP mechanism, the controller provides over-current protection in each phase. For controller in four-phase configuration, each phase can trigger Per-Phase Over-Current Protection (PHOCP). The controller senses each phase inductor current I_L, and PHOCP comparator compares sensed current with PHOCP threshold current, as shown in Figure 17.

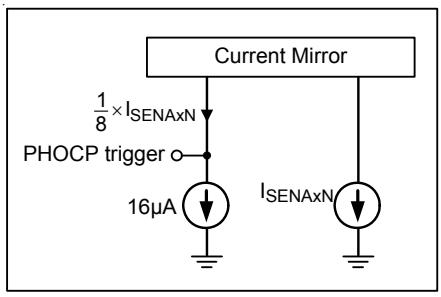


Figure 17. Per-Phase OCP Setting

The PHOCP threshold is determined as equation 25 :

$$I_{L,PERPHASE(MAX)} = \frac{680\Omega}{DCR} \times 8 \times 16\mu A \quad (25)$$

The controller will turn off all high-side/low-side MOSFETs to protect CPU if the per-phase over-current protection is triggered.

Over-Voltage Protection (OVP)

The over-voltage protection circuit of the controller monitors the output voltage via the VSENx pin after POR. When VID is lower than 0.9V, once VSENx exceeds "0.9V + 325mV", OVP is triggered and latched. When VID is larger than 0.9V, once VSENx exceeds the internal reference by 325mV, OVP is triggered and latched. The controller will try to turn on low-side MOSFETs and turn off high-side MOSFETs of all active phases of the controller to protect the CPU. When OVP is triggered by one rail, the other rail will also enter soft shut down sequence. A 1μs delay is used in OVP detection circuit to prevent false trigger.

Negative-Voltage Protection (NVP)

During OVP latch state, the controller also monitors the VSENx pin for negative-voltage protection. Since the OVP latch continuously turns on all low-side MOSFETs of the controller, the controller may suffer negative output voltage. As a consequence, when the VSENx voltage drops below 0V after triggering OVP, the controller will trigger NVP to turn off all low-side MOSFETs of the controller while the high-side MOSFETs remains off. After triggering NVP, if the output voltage rises above 0V, the OVP latch will restart to turn on all low-side MOSFETs. The NVP function will be active only after OVP is triggered.

Under-Voltage Protection (UVP)

The controller implements under-voltage protection of V_{OUT}. If VSENx is less than the internal reference by –425mV, the controller will trigger UVP latch. The UVP latch will turn off both high-side and low-side MOSFETs. When UVP is triggered by one rail, the other rail will also enter soft shutdown sequence. A 3μs delay is used in UVP detection circuit to prevent false trigger.

Under-Voltage Lock Out (UVLO)

During normal operation, if the voltage at the VCC pin drops below 4.1V or the voltage at PVCC pin drops below 3.5V, the VR will trigger UVLO. The UVLO protection forces all high-side MOSFETs and low-side MOSFETs off by shutting down internal PWM logic drivers. A 3μs delay is used in UVLO detection circuit to prevent false trigger.

SVI2 Wire Protocol

The RT8881A complies with AMD's Voltage Regulator Specification, which defines the Serial VID Interface 2 (SVI2) protocol. With SVI2 protocol, the processor directly controls the reference voltage level of each individual controller channel and determines which controller operates in power saving mode.

The SVI2 interface is a three wire bus that connects a single master to one or above slaves. The master initiates and terminates SVI2 transactions and drives the clock, SVC, and the data, SVD, during a transaction. The slave drives the telemetry, SVT during a transaction. The AMD processor is always the master. The RT8881A always is the slave and do not driver the SVD during the ACK bit. The RT8881A receives the SVID code and acts accordingly. The SVI protocol of the RT8881A supports 20MHz high speed mode I^2C, which is based on SVD data packet and is listed in Figure 18. Table 10 shows the SVD data packet of the RT8881A. An SVD packet consists of a Start signal, three data bytes after each byte, and a Stop signal. The 8-bit serial VID codes are listed in Table 1.

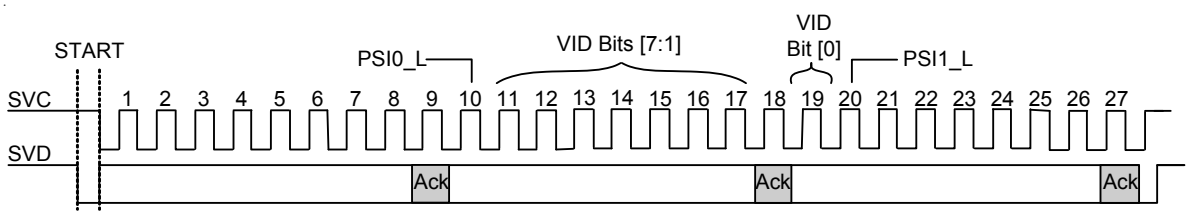


Figure 18. SVD Bit Definition

Table 10. SVD Data Packet

Bit Time	Description
1 : 5	Always 11000b
6	VDD domain selector bit, if set then the following two data bytes contains the VID for VDD, the PSI state for VDD, and the load-line slope trim and offset trim state for VDD
7	VDDNB domain selector bit, if set then the following two data bytes contains the VID for VDDNB, the PSI state for VDDNB, and the load-line slope trim and offset trim state for VDDNB.
8	Always 0b
9	ACK bit
10	PSI0_L
11 : 17	VID Code bits [7:1]
19	VID Code bit [0]
20	PSI1_L
21	TFN (Telemetry Functionality)
22 : 24	Load Line Slope Trim [2:0]
25 : 26	Offset Trim [1:0]
27	ACK bit

PSI[x]_L and TFN

SVI2 defines two PSI levels, showed as Table 10. It is possible for the processor to assert or deassert PSI0_L and PSI1_L out of order. PSI0_L takes priority over PSI1_L. If PSI0_L is deasserted but PSI1_L is still asserted, the VR must be ready to deliver full infrastructure current, meaning IDDSpike current.

Table 11. PSI0_L, PSI1_L and TFN Definition

Bit	Define	Description
10	PSI0_L	Power State Indicate level 0. When this signal is asserted (active-low) the processor is in a low enough power state for the VR to take some action to boost efficiency, such as drop phases.
20	PSI1_L	Power State Indicate level 1. When this signal is asserted (active-low) the processor is in a low enough power state for the VR to take some action, in additional to what it is doing with PSI0_L asserted, to boost efficiency, such as pulse skip or diode emulation.
21	TFN	Telemetry Functionality. This is an active high signal that allows the processor to control the telemetry functionality of the VR.

The TFN along with the VDD and VDDNB domain selector bits are used by the processor to change the functionality of telemetry, see Table 12 for more information.

Table 12. TFN Truth Table

VDD, VDDNB and TFN Bits [6, 7, 21]	Description
001	Telemetry is in voltage only mode. Only the voltage of VDD and VDDNB domains are sent. (Default)
011	Telemetry is in voltage and current mode. V & I are sent for VDD and VDDNB domains.
101	Telemetry is disabled.
111	Reserved

Dynamic Load-Line Slope Trim

The RT8881A have the ability for the processor to manipulate the load-line slope of VDD and VDDNB independently via the serial VID interface. The slope manipulation applies to the initial load-line slope. A load-line slop trim will typically coincide with a VOTF change. Refer to Table 13 for more information about the load-line capabilities of the RT8881A.

Table 13. Load Line Slope Trim Definition

LL Slope Trim [22 : 24]	Description
000	Remove all LL droop from output
001	Initial LL Slope –40%
010	Initial LL Slope –20%
011	Initial LL Slope (Default)
100	Initial LL Slope +20%
101	Initial LL Slope +40%
110	Initial LL Slope +60%
111	Initial LL Slope +80%

Dynamic Offset Trim

The RT8881A have ability for the processor to manipulate the offset of VDD and VDDNB independently via the serial VID interface. Refer to Table 14 for more information about the offset capabilities of the RT8881A. For RT8881A, the initial offset always be set to zero.

Table 14. Offset Trim Definition

Offset Trim [25:26]	Description
00	Remove all Offset from output
01	Initial Offset –25mV
10	Use Initial Offset (Default)
11	Initial Offset +25mV

Telemetry Format

After the RT8881A has received the stop sequence, it decodes the received serial VID code and executes the command. SVI2 VR Controller has the ability to sample and report voltage and current for the VDD and VDDNB domains. The Controller reports this telemetry serially over the SVT wire which is clocked by the processor driven SVC. A bit TFN at SVD packet along with the VDD and VDDNB domain selector bits are used by the processor to change the functionality of telemetry. The telemetry bit definition is listed in Figure 19. The detailed SVI2 specification is outlined in the AMD Voltage Regulator and Voltage Regulator Module (VRM) and Serial VID Interface 2 (SVI2) Specification.

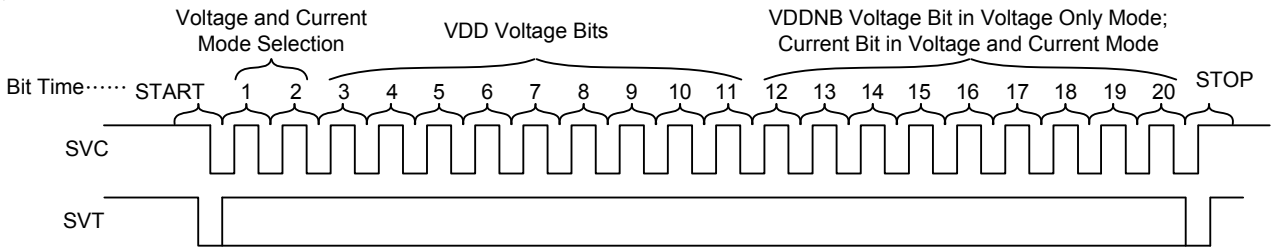


Figure 19. Telemetry Bit Definition

I²C Interface

An I²C interface is used to communicate with the RT8881A and the address for RT8881A is 0x40. Figure 20 shows the I²C format employed by the RT8881A.

The bus provides read and write access to the internal performance registers for setting and reading of operating parameters and operates at 400kHz. The Operating parameters that can be adjusted through the I²C interface.

It is important to note that the I²C interface of the RT8881A should write register I2C_LOCK_IND to 0x5A before any online register update and write back to 0xff after update done.

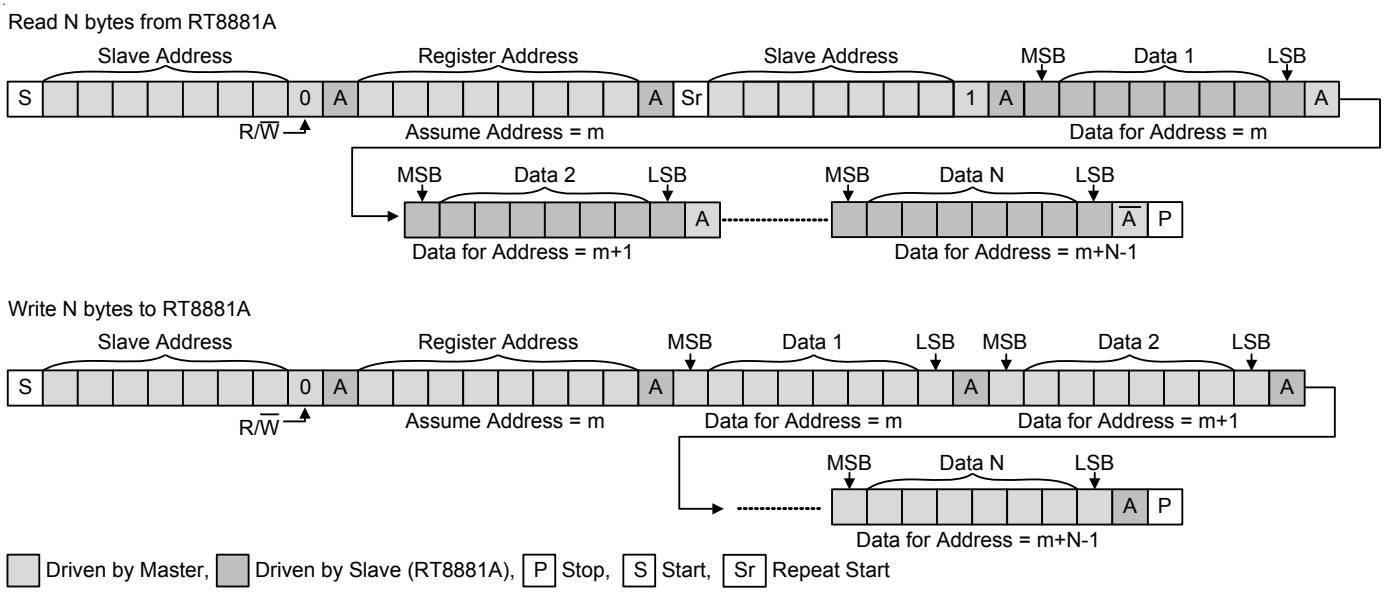


Figure 20. I²C format

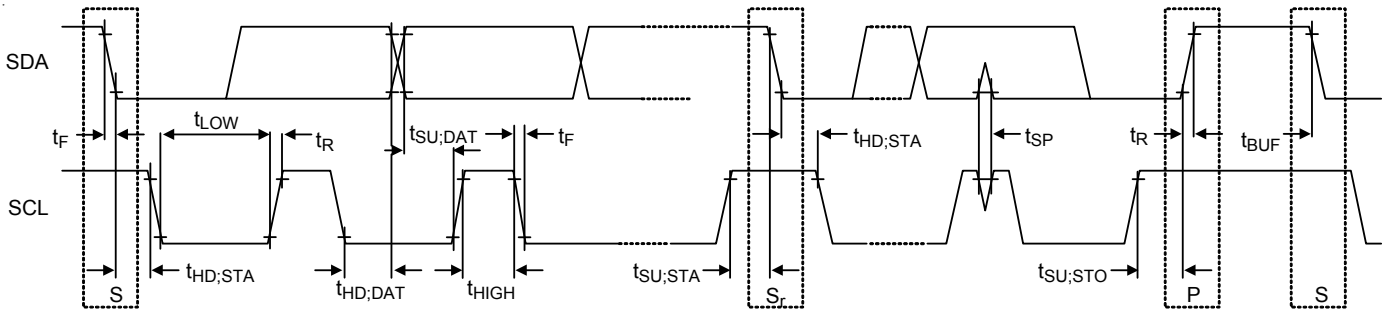


Figure 21. I²C Waveform Information

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WQFN-52L 6x6 package, the thermal resistance, θ_{JA}, is 26.5°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (26.5°C/W) = 3.77W for WQFN-52L 6x6 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 22 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

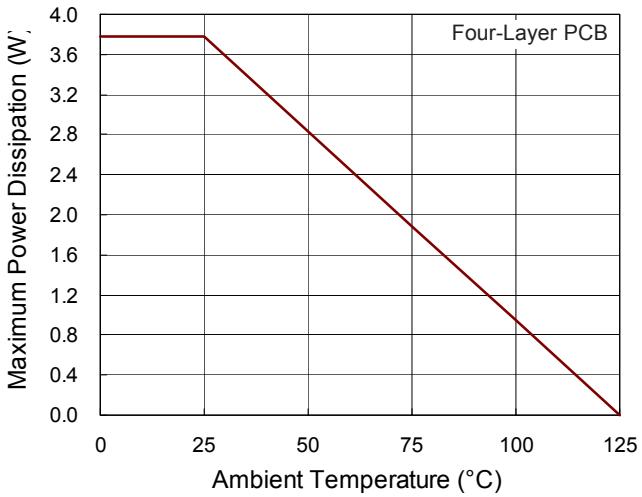
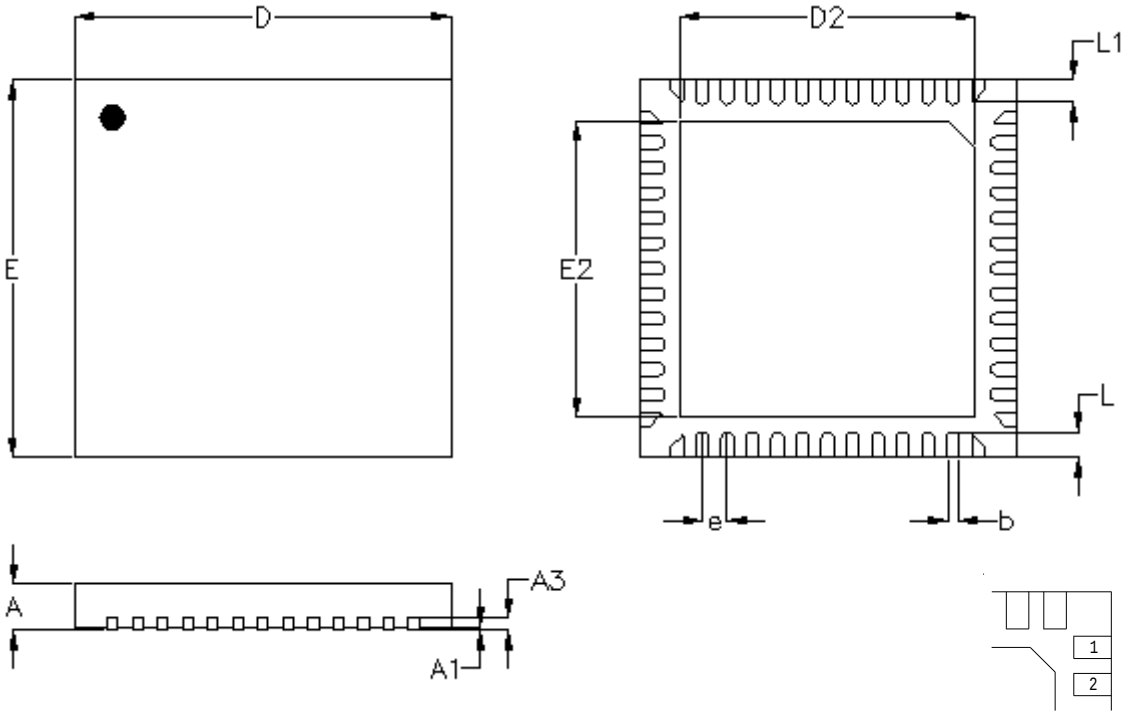


Figure 22. Derating Curve of Maximum Power Dissipation

Outline Dimension



DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	5.950	6.050	0.234	0.238
D2	4.650	4.750	0.183	0.187
E	5.950	6.050	0.234	0.238
E2	4.650	4.750	0.183	0.187
e	0.400		0.016	
L	0.350	0.450	0.014	0.018
L1	0.300	0.400	0.012	0.016

W-Type 52L QFN 6x6 Package

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