Dual-Output Synchronous DC/DC Converter

General Description

The RT8553A is a dual-output DC/DC converter which is designed to provide the power for consumer products. It integrates a Boost converter and an inverting-Boost converter for enhancing the overall system efficiency of battery powered products. The RT8553A operates in Forced CCM mode for light load and heavy load condition. The high frequency allows for reduction of external components. In shutdown mode, the RT8553A consumes less than 1 μ A current. The RT8553A provides soft-start, OCP, OTP, OVP and UVLO function. The RT8553A is available in the tiny UDFN-12L 3x3 package to achieve best solution for saving PCB space and total BOM cost saving considerations.

Ordering Information

RT8553A Package Type QU : UDFN-12L 3x3 (U-Type) Lead Plating System G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

- Boost Converter to Supply Positive Voltage from 4.6V to 5.4V Through External Feedback Resistors
- Buck-Boost Converter to Supply Negative Voltage from -4.6V to -5.4V Through External Feedback Resistors
- Maximum Output Current up to 200mA
- Typical Efficiency : 85%
- PWM Mode @ 1.5MHz Switching Frequency
- High Output Voltage Accuracy
- Excellent Line and Load Transient
- Excellent Line and Load Regulation
- Soft-Start to Limit Inrush Current
- Over-Temperature Protection (OTP)
- Over-Current Protection (OCP)
- Over-Voltage Protection (OVP)
- Low Quiescent Current < 1µA in Shutdown Mode
- RoHS Compliant and Halogen Free

Applications

- Cellular Phones
- Digital Cameras
- PDAs and Smart Phones
- Probable Instruments

Simplified Application Circuit







Marking Information

3S=YM DNN 3S= : Product Code YMDNN : Date Code

Pin Configurations



UDFN-12L 3x3

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	LX1	Switch Node of Boost Converter.
2	VOUT1	Boost Converter Output.
3	PGND	Power Ground.
4	FB1	Feedback Voltage Input of Boost Converter.
5	AGND	Analog Ground.
6	EN	Enable Control Input. (Active High)
7	VINA	Analog Supply Voltage Input.
8	VREF	Reference Voltage.
9	FB2	Feedback Voltage Input of Inverting Boost Converter.
10	VOUT2	Buck-Boost Converter Output.
11	LX2	Switch Node of Buck-Boost Converter.
12	VINP	Power Supply Voltage Input.
13 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to AGND for maximum power dissipation.

Function Block Diagram



Operation

The RT8553A is a dual-output synchronous DC/DC converter for consumer product applications that it can support input voltage range from 2.5V to 4.5V and the output current up to 200mA. The RT8553A uses current mode architecture for the purpose of high efficiency and high transient response. The VOUT1 positive output voltage is produced from the DC/DC Boost converter, and output voltage can be adjusted by external feedback resistors. The VOUT2 negative output voltage is produced from the DC/DC Buck-Boost converter, and the negative output voltage can be adjusted by external feedback resistors. When the EN goes high, the positive output voltage will be enabled with an internal soft-start process.

The RT8553A provides protection functions, such as Over-Current Protection (OCP), Over-Temperature Protection (OTP) and Over-Voltage Protection (OVP) to protect application products and itself. The RT8553A employs an internal soft-start feature to avoid high inrush currents during start-up. Both the Boost and the Buck-Boost converters can operate in Force Continuous Conduction Mode (FCCM) for better stability and minimum output ripple.



Absolute Maximum Ratings (Note 1)

Supply Input Voltage, VINA, VINP	–0.3 to 6V
Boost Output Voltage, VOUT1	–0.3 to 6V
Boost Switching Voltage, LX1	–0.3 to 6V
Boost Feedback Voltage, FB1	–0.3 to 6V
Reference Voltage, VREF	–0.3 to 6V
Inverting Output Voltage, VOUT2	–6.5 to 0.3V
Inverting Boost Switching Voltage, LX2	6.5 to (VINP + 0.3V)
Inverting Boost Feedback Voltage, FB2	–0.3 to 6V
Enable Input Voltage, EN	–0.3 to 6V
• Power Dissipation, $P_D @ T_A = 25^{\circ}C$	
UDFN-12L 3x3	3.09W
Package Thermal Resistance (Note 2)	
UDFN-12L 3x3, θ _{JA}	32.3°C/W
UDFN-12L 3x3, θ _{JC}	6.6°C/W
Lead Temperature (Soldering, 10 sec.)	260°C
Junction Temperature	150°C
Storage Temperature Range	–65°C to 150°C
ESD Susceptibility (Note 3)	
HBM (Human Body Model)	2kV
MM (Machine Model)	200V

Recommended Operating Conditions (Note 4)

Supply Voltage, VIN	2.5V to 4.5V
Junction Temperature Range	40°C to 125°C
Ambient Temperature Range	–40°C to 85°C

Electrical Characteristics

 $(V_{\text{INA}} = V_{\text{INP}} = V_{\text{EN}} = 3.7V, C_{\text{IN}} = C_{\text{OUT1}} = C_{\text{OUT2}} = 10 \mu\text{F}, \text{ L1} = \text{L2} = 4.7 \mu\text{H}, \text{ T}_{\text{A}} = 25^{\circ}\text{C}, \text{ unless otherwise specified})$

Parameter		Symbol	Test Conditions		Тур	Мах	Unit
General Specification							
Input Voltage	Range	V _{IN}	$V_{OUT1} = 5V$	2.5	3.7	4.5	V
Under-Voltage Lockout High Voltage		V _{UVLOH}	V _{INA} Rising		2.22	2.4	V
Under-Voltage Lockout Low Voltage		Vuvlol	V _{INA} Falling	1.9	2.18		V
VIN Quiescent Current		IQ	No Load Condition, No Switching $V_{OUT1} = 5V$, $V_{OUT2} = -5V$		2		mA
VIN Shutdown Current		I _{SHDN}	V _{EN} = GND			1	μA
EN Input	Logic-High	V _{IH}	$V_{INA} = 2.5V$ to $4.5V$	1.2			V
Voltage	Logic-Low	VIL	V _{INA} = 2.5V to 4.5V			0.6	V
EN Pull Down Resistor		I _{EN}	$V_{INA} = V_{EN} = 4.5V$		150		kΩ

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Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit
Switching Frequency	f _{SWPWM}	FCCM Mode	1.35	1.5	1.65	MHz
Reference Voltage	V _{REF}	VREF		1		V
Boost Maximum Duty	D1 _{MAX}	Open Loop Condition		85		%
Inverting-Boost Maximum Duty	D2 _{MAX}	Open Loop Condition		85		%
Suctom Efficiency	E _{SYS}	$I_{OUT1} = I_{OUT2} = 10$ mA to 30mA, $V_{OUT1} = 5$ V, $V_{OUT2} = -5$ V		80		0/
System Enciency		$I_{OUT1} = I_{OUT2} = 30$ mA to 200mA, $V_{OUT1} = 5$ V, $V_{OUT2} = -5$ V		85		70
Over-Temperature Protection	ОТР			140		°C
Over-Temperature Protection Hysteresis	OTP _{HYST}			15		°C
Boost Converter		-				
Positive Output Voltage Range	V _{OUT1}		4.6	5.0	5.4	V
Positive Output Voltage Total Variation		$V_{INA} = V_{INP} = 2.9V \text{ to } 4.5V$ $I_{OUT1} = 5\text{mA} \text{ to } 200\text{mA}$ $I_{OUT2} = \text{No Load}$	-2		2	%
Maximum Output Current	I _{OUT1MAX}	$V_{INA} = V_{INP} = 2.9V \text{ to } 4.5V$	200			mA
Feedback Voltage of Boost Converter	V _{FB1}	$V_{INA} = V_{INP} = 2.9V \text{ to } 4.5V$		1		V
Over Voltage of Boost Converter	V _{OVP1}			6		V
Load Transient	Vout1load_lt	$I_{OUT1} = 3mA$ to 30mA and $I_{OUT1} = 30mA$ to 3mA, $T_R = T_F = 150\mu s$, Output Variation respect to VOUT1		±20		mV
		$I_{OUT1} = 10$ mA to 100mA and $I_{OUT1} = 100$ mA to 10mA, $T_R = T_F = 150$ µs, Output Variation respect to V _{OUT1}		±25		mV
Static Line Regulation	V _{OUT1LINE_SL}	$V_{INA} = V_{INP} = 2.9V \text{ to } 4.5V,$ $I_{OUT1} = 5\text{mA}, I_{OUT2} = \text{No Load}$		0.5		0/
		$V_{INA} = V_{INP} = 2.9V \text{ to } 4.5V,$ $I_{OUT1} = 100\text{mA}, I_{OUT2} = \text{No Load}$	0.5			70
Statia Load Degulation	VOUT1LOAD_SL	$I_{OUT1} = 5$ to 100mA, $I_{OUT2} = No$ Load, $V_{INA} = V_{INP} = 2.9V$		0.5		
Static Load Regulation		$I_{OUT1} = 5$ to 100mA, $I_{OUT2} = No$ Load, $V_{INA} = V_{INP} = 4.5V$		0.5		/0
Boost Switching Current Limit	I _{LX1}	$V_{INA} = V_{INP} = 2.9V \text{ to } 4.35V$		1		А
N1 N-MOSFET On-Resistance	Brownia	$V_{INA} = V_{INP} = 3.7V, I_{LX1} = 100mA$		0.2		Ω
P1 P-MOSFET On-Resistance	US(UN)1	$V_{INA} = V_{INP} = 3.7V, I_{LX1} = 100mA$		0.3		Ω

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Parameter	Symbol	Test Conditions		Тур	Max	Unit
Inverting-Boost Converter						
Negative Output Voltage Range	V _{OUT2}		-4.6	-5	-5.4	V
Negative Output Voltage Total Variation		$V_{INA} = V_{INP} = 2.9V \text{ to } 4.5V$ $I_{OUT2} = 5\text{mA to } 300\text{mA}$ $I_{OUT1} = \text{No Load}$	-2		2	%
Maximum Output Current	IOUT2MAX	$V_{INA} = V_{INP} = 2.9V$ to $4.5V$	200			mA
Feedback Voltage of Inverting Converter	V _{FB2}	$V_{INA} = V_{INP} = 2.9V$ to $4.5V$		0		V
Over-Voltage of Inverting-Boost Converter	V _{OVP2}			-6		V
Load Transient	Vout2load_lt	I_{OUT2} = 3mA to 30mA and I_{OUT2} = 30mA to 3mA, T_R = T_F = 150µs, Output Variation respect to V _{OUT2}	and ct to V _{OUT2}			mV
		$I_{OUT2} = 10mA$ to 100mA and $I_{OUT2} = 100mA$ to 10mA, $T_R = T_F = 150\mu s$, Output Variation respect to V _{OUT2}		±50		mV
	Vout2line_sl	$V_{INA} = V_{INP} = 2.9V$ to 4.5V, I _{OUT2} = 5mA, I _{OUT1} = No Load		0.5		%
Static Line Regulation		$V_{INA} = V_{INP} = 2.9V$ to 4.5V, $I_{OUT2} = 100$ mA, $I_{OUT1} = $ No Load		0.5		%
Static Load Regulation	V _{OUT2LOAD_SL}	$I_{OUT2} = 5mA$ to 100mA, $I_{OUT1} = No$ Load, $V_{INA} = V_{INP} = 2.9V$		0.5		%
		$I_{OUT2} = 5mA$ to 100mA, $I_{OUT1} = No$ Load, $V_{INA} = V_{INP} = 4.5V$		0.5		%
Inverting-Boost Switching Current Limit	I _{LX2}	$V_{INA} = V_{INP} = 2.9V$ to $4.5V$		1.2		А
N2 N-MOSFET On-Resistance	Backet	$V_{INA} = V_{INP} = 3.7V, I_{LX2} = 100mA$		0.2		Ω
P2 P-MOSFET On-Resistance	TUS(ON)2	$V_{INA} = V_{INP} = 3.7V, I_{LX2} = 100 \text{mA}$		0.3		Ω

- **Note 1.** Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.
- Note 2. θ_{JA} is measured at $T_A = 25^{\circ}C$ on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.
- Note 3. Devices are ESD sensitive. Handling precaution is recommended.
- Note 4. The device is not guaranteed to function outside its operating conditions.



Typical Application Circuit



Timing Diagram

Power Sequence





Typical Operating Characteristics















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Vout1 (10mV/Div) I_{LOAD} (50mA/Div) VIN = 3.7V, VOUT1 = 5V, $T_R = T_F = 150 \mu s$, $I_{OUT1} = 10 mA$ to 100 mA

VOUT1 Load Transient

Time (100µs/Div)







VOUT1 Line Transient









Application Information

The RT8553A is a dual channel DC/DC converter capable of generating both positive and negative outputs by external feedback voltage-divider resistors from an input voltage range of 2.5V to 4.5V. Each converter works independently of one another and both outputs are separately controlled by a fixed frequency Pulse-Width-Modulated (PWM) regulator.

Soft-Start

The RT8553A employs a soft-start feature for both converters to limit the inrush current and prevent input voltage droop. When each converter is enabled, the implemented switch current limit ramps up slowly to its nominal programmed value in about 2ms for the Boost converter and Buck-Boost converter.

Over-Voltage Protection (OVP)

The RT8553A has over-voltage circuit protection mechanism which prevents feedback pin floating when the IC is enabled. When output voltage exceeds OVP threshold voltage, the IC would be clamped at fixed voltage with minimum duty.

Over-Current Protection (OCP)

The RT8553A includes a current sensing circuitry which monitors the inductor current during each charging cycle. If the current value becomes greater than the current limit, the converter will be shutdown and can only re-start normal operation after triggering EN pin or re-power on again.

Over-Temperature Protection (OTP)

The RT8553A includes an Over-Temperature Protection (OTP) feature to prevent the device from overheat due to excessive power dissipation. The OTP function shuts down all device operations when the junction temperature exceeds 140°C. Once the junction temperature cools down by approximately 15°C, the converter resumes operation. To maintain continuous operation, prevent the maximum junction temperature form rising above 125°C.

Under-Voltage Lockout (UVLO)

The Under-Voltage Lockout (UVLO) circuitry compares the input voltage with the UVLO threshold to ensure that the input voltage is high enough for reliable operation. Once the input voltage exceeds the UVLO rising threshold at 2.22V (typ.), start-up begins. A 40mV (typ.) hysteresis is included to prevent supply transients from causing a shutdown.

Positive Output Voltage Setting

The output voltage setting can be calculated according to the following equation :

 $V_{OUT1} = V_{FB1} \times \left(1 + \frac{R1}{R2}\right)$

where V_{FB1} is the reference voltage with a typical value of 1V.

Input Capacitor Selection

Input ceramic capacitors with 10μ F capacitance are suggested for the RT8553A applications. However, to achieve best performance with the RT8553A, larger capacitance can be used. For better voltage filtering, select ceramic capacitors with low ESR, X5R and X7R types are suitable because of their wider voltage and temperature ranges.

Boost Inductor Selection

The inductance depends on the maximum input current. As a general rule, the inductor ripple current range is 20% to 40% of the maximum input current. If 40% is selected as an example, the inductor ripple current can be calculated according to the following equations :

$$I_{IN(MAX)} = \frac{V_{OUT} \times I_{OUT(MAX)}}{\eta \times V_{IN}}$$
$$\Delta I_{L} = 0.4 \times I_{IN(MAX)}$$

where η is the efficiency of the converter, $I_{IN(MAX)}$ is the maximum input current, and ΔI_L is the inductor ripple current. The input peak current can then be obtained by adding the maximum input current with half of the inductor ripple current as shown in the following equation :

$$I_{\text{peak}} = 1.2 \text{ x } I_{\text{IN(MAX)}}$$

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Note that the saturated current of the inductor must be greater than $I_{\mbox{\scriptsize peak}}.$

The inductance can eventually be determined according to the following equation :

$$L = \frac{\eta \times (V_{IN})^{2} \times (V_{OUT} - V_{IN})}{0.4 \times (V_{OUT})^{2} \times I_{OUT(MAX)} \times f_{OSC}}$$

where f_{OSC} is the switching frequency. For better system performance, a shielded inductor is preferred to avoid EMI problems.

Boost Output Capacitor Selection

The output ripple voltage is an important index for estimating chip performance. This portion consists of two parts. One is the product of the inductor peak current with the ESR of the output capacitor, while the other part is formed by the charging and discharging process of the output capacitor. As shown in Figure 1, ΔV_{OUT1} can be evaluated based on the ideal energy equalization. According to the definition of Q, the Q value can be calculated as the following equation :

$$\begin{split} \mathsf{Q} &= \frac{1}{2} \times \left[\left(\mathsf{I}_{\mathsf{IN}} + \frac{1}{2} \Delta \mathsf{I}_{\mathsf{L}} - \mathsf{I}_{\mathsf{OUT}} \right) + \left(\mathsf{I}_{\mathsf{IN}} - \frac{1}{2} \Delta \mathsf{I}_{\mathsf{L}} - \mathsf{I}_{\mathsf{OUT}} \right) \right] \\ &\times \frac{\mathsf{V}_{\mathsf{IN}}}{\mathsf{V}_{\mathsf{OUT}}} \times \frac{1}{\mathsf{f}_{\mathsf{OSC}}} = \mathsf{C}_{\mathsf{OUT}} \times \Delta \mathsf{V}_{\mathsf{OUT1}} \end{split}$$

where f_{OSC} is the switching frequency and ΔI_L is the inductor ripple current. Bring C_{OUT} to the left side to estimate the value of ΔV_{OUT1} according to the following equation :

$$\Delta V_{OUT1} = \frac{D \times I_{OUT}}{\eta \times C_{OUT} \times f_{OSC}}$$

where D is the duty cycle and η is the Boost converter efficiency. Finally, taking ESR into consideration, the overall output ripple voltage can be determined by the following equation :

$$\begin{split} \Delta V_{OUT1} = \Delta V_{ESR} \ + \ \frac{D \times I_{OUT}}{\eta \times C_{OUT} \times f_{OSC}} \\ \text{where} \ \Delta V_{ESR} = \Delta I_C \times R_{C_ESR} \ = I_{peak} \times R_{C_ESR} \end{split}$$

The output capacitor, C_{OUT}, should be selected accordingly.



Figure 1. The Output Ripple Voltage without the Contribution of ESR

Negative Output Voltage Setting

The output voltage setting can be calculated according to the following equation :

 $V_{OUT2} = V_{FB2} - (V_{REF} - V_{FB2}) \times \frac{R3}{R4}$

where V_{REF} is the reference voltage with a typical value of 1V and $V_{FB2} = 0V$.

Buck-Boost Converter Inductor Selection

The first step in the design procedure is to verify whether the maximum possible output current of the Buck-Boost converter supports the specific application requirements. To simplify the calculation, the fastest approach is to estimate converter efficiency by taking the efficiency numbers from provided efficiency curves or to use a worst case assumption for the expected efficiency, e.g., 80%. The calculation must be performed for the minimum assumed input voltage where the peak switch current is the highest. The inductor and internal switch have to be able to handle this current.

Converter Duty Cycle :

$$\mathsf{D} = \frac{\left|\mathsf{V}_{\mathsf{OUT}}\right|}{\mathsf{V}_{\mathsf{IN}} \times \eta + \left|\mathsf{V}_{\mathsf{OUT}}\right|}$$

Maximum output current :

$$\mathsf{IOUT}(\mathsf{MAX}) = \left(\mathsf{I}_{\mathsf{LX2}} - \frac{\mathsf{V}_{\mathsf{IN}(\mathsf{MIN})} \times \mathsf{D}}{2 \times \mathsf{f}_{\mathsf{OSC}}(\mathsf{MAX}) \times \mathsf{L}}\right) \times \left(1 - \mathsf{D}\right)$$

Inductor peak current :

 $I_{\text{peak}} = \frac{I_{\text{OUT}}}{1 - D} + \frac{V_{\text{IN}} \times D}{2 \times f_{\text{OSC}} \times L}$

where, I_{LX2} is switching current limit.

As for inductance, we are going to derive the transition point, where the converter toggles from CCM to DCM. We need to define the point at which the inductor current ripple touches zero, and as the power switch LX is immediately reactivated, the current ramps up again. Figure 2 portrays the input current activity of the Buck-Boost converter.



Figure 2. The Buck-Boost input signature in BCM

The inductance can eventually be determined according to the following equation :

 $\Delta V = \frac{D \times |V_{OUT}|}{f_{OSC} \times R_{LOAD} \times C_{OUT}} + \Delta V_{ESR}$ where $\Delta V_{ESR} = \Delta I_C \times R_{C_ESR} = I_{peak} \times R_{C_ESR}$

 ΔV_{ESR} can be neglected in many cases since ceramic capacitors provide very low ESR.

Thermal Considerations

For continuous operation, do not exceed the maximum operation junction temperature 125°C. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature differential between junction to ambient. The maximum power dissipation can be calculated by following formula :

 $\mathsf{P}_{\mathsf{D}(\mathsf{MAX})} = (\mathsf{T}_{\mathsf{J}(\mathsf{MAX})} - \mathsf{T}_{\mathsf{A}}) / \theta_{\mathsf{J}\mathsf{A}}$

where $T_{J(MAX)}$ is the maximum operation junction temperature 125°C, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA} , is layout dependent. For UDFN-12L 3x3 package, the thermal resistance θ_{JA} is 32.3°C/W on the standard JEDEC 51-7 four-layers thermal test board. The maximum power dissipation at $T_A = 25$ °C can be calculated by following formula :

 $\mathsf{P}_{\mathsf{D}(\mathsf{MAX})}$ = ($125^\circ C$ – $25^\circ C)$ / $32.3^\circ C/W$ = 3.09W for UDFN-12L 3x3 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA} . The derating curve in Figure 3 allow the designer to see the effect of rising ambient temperature on the maximum power dissipation.



Figure 3. Derating Curve of Maximum Power Dissipation

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Layout Consideration

For the best performance of RT8553A the following PCB layout guidelines should be strictly followed.

- For good regulation, place the power components as close to the IC as possible. The traces should be wide and short especially for the high current output loop.
- The input and output bypass capacitor should be placed as close to the IC as possible and connected to the ground plane of the PCB.
- Minimize the size of the LX1, LX2 nodes and keep the traces wide and short. Care should be taken to avoid running traces that carry any noise-sensitive signals near LX or high-current traces.

- The feedback voltage-divider resistors must be placed near the Feedback pin. The divider center trace must be shorter and avoid the trace near any switching nodes.
- Separate power ground (PGND) and analog ground (AGND). Connect the AGND and the PGND islands at a single end.
- Connect the exposed pad to a strong ground plane for maximum thermal dissipation.



Figure 4. PCB Layout Guide

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Outline Dimension



Symbol	Dimensions I	n Millimeters	Dimensions In Inches		
	Min.	Max.	Min.	Max.	
А	0.500	0.600	0.020	0.024	
A1	0.000	0.050	0.000	0.002	
A3	0.100	0.175	0.004	0.007	
b	0.150	0.250	0.006	0.010	
D	2.950	3.050	0.116	0.120	
D2	2.300	2.650	0.091	0.104	
E	2.950	3.050	0.116	0.120	
E2	1.400	1.750	0.055	0.069	
е	0.450		0.0	18	
L	0.350	0.450	0.014	0.018	

U-Type 12L DFN 3x3 Package

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