Single Synchronous Buck with LDO Controller

General Description

The RT8204A PWM controller provides the high efficiency, excellent transient response, and high DC output accuracy needed for stepping down high voltage batteries to generate low voltage CPU core, I/O, and chipset RAM supplies in notebook computers.

The constant-on-time PWM control scheme handles wide input/output voltage ratios with ease and provides 100ns "instant-on" response to load transients while maintaining a relatively constant switching frequency.

The RT8204A achieves high efficiency at a reduced cost by eliminating the current sense resistor found in traditional current mode PWMs. Efficiency is further enhanced by its ability to drive very large synchronous rectifier MOSFETs. The buck conversion allows this device to directly step down high voltage batteries for the highest possible efficiency. The RT8204A is intended for CPU core, chipset, DRAM, or other low voltage supplies as low as 0.75V.

A built-in LDO controller can drive an external N-MOSFET to provide a second output voltage from PWM output or other power source. The RT8204A can provide adjustable voltage down to 0.75V and maximum output voltage is depended on the selected MOSFET. The internal 0.75V reference voltage with ±1.5% accuracy provides tight regulation for the output voltage. The independent enable control, open drain power good indicator, under-voltage protection and soft start make RT8204A to power the system friendly. The RT8204A is available in WQFN-16L 3x3 package.

Applications

- Notebook Computers
- CPU Core Supply
- Chipset/RAM Supply as Low as 0.75V

Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

Features

- **PWM Controller**
  - **Ultra-High Efficiency**
  - **Resistor Programmable Current Limit by Low Side $R_{DS(ON)}$ Sense (Lossless Limit) or Sense Resistor (High Accuracy)**
  - **Quick Load Step Response within 100ns**
  - **1% V_{OUT} Accuracy Over Line and Load**
  - **Adjustable 0.75V to 3.3V Output Range**
  - **3V to 26V Battery Input Range**
  - **Resistor Programmable Frequency**
  - **Over/Under Voltage Protection**
  - **2 Steps Current Limit During Soft-Start**
  - **Drives Large Synchronous-Rectifier FETs**
  - **Power Good Indicator**
- **LDO Controller**
  - **1.5% Accuracy Over Line and Load**
  - **Adjustabe Output Voltage down to 0.75V**
  - **Independent Enable and Power Good Indicator**
  - **Drive N-MOSFETs within Rail to Rail Controller Voltage**
  - **MLCC and POSCAP Stable**
- **RoHS Compliant and 100% Lead (Pb)-Free**

Ordering Information

RT8204A□□

Package Type
QW : WQFN-16L 3x3 (W-Type)

Lead Plating System
P : Pb Free
G : Green (Halogen Free and Pb Free)

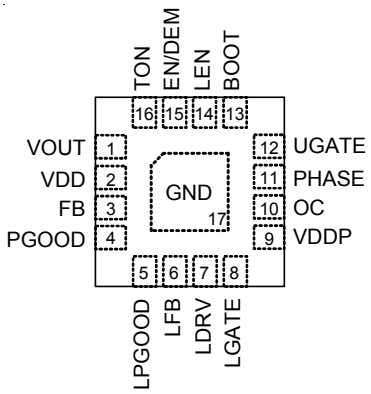
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

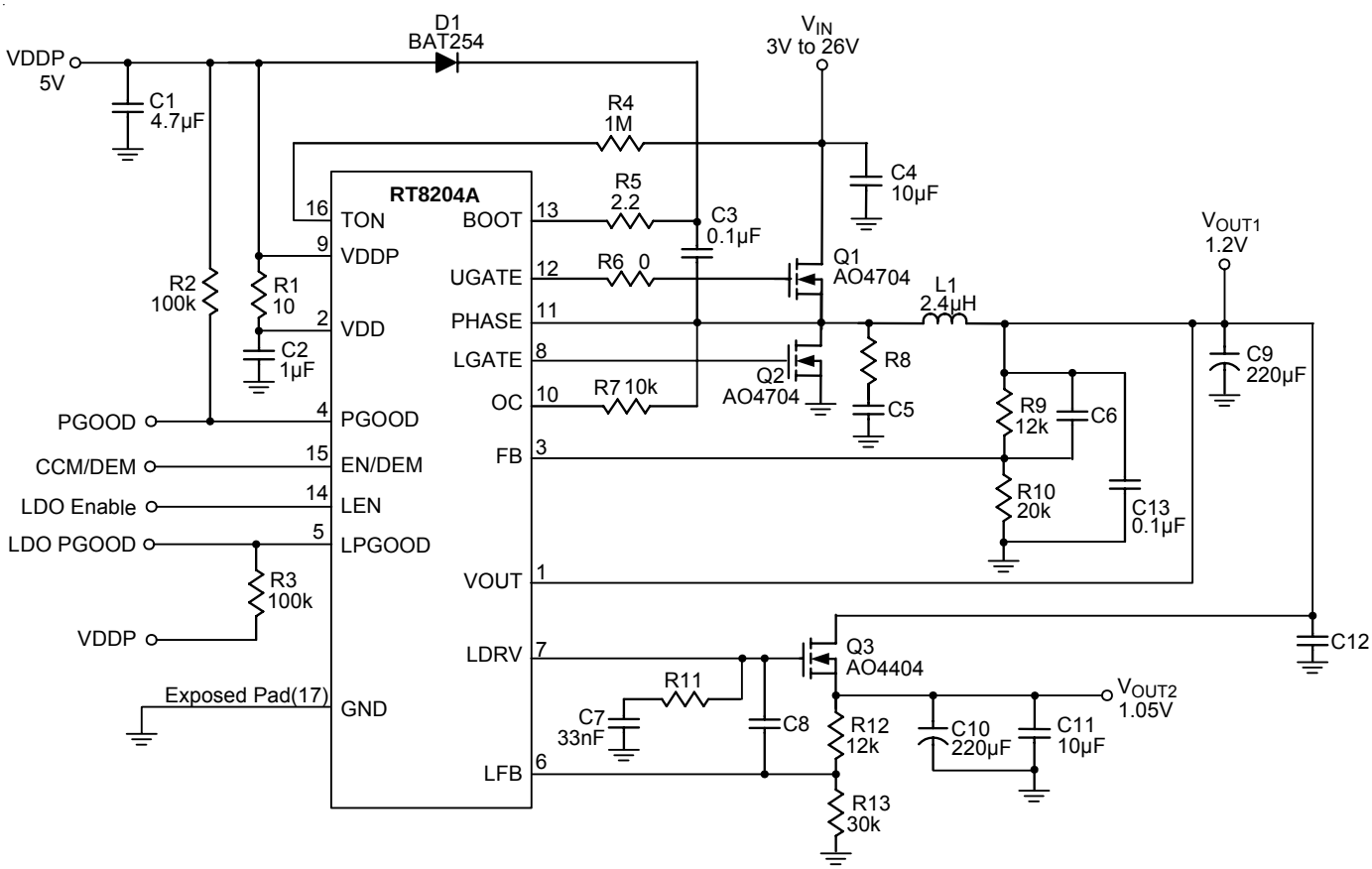
Pin Configurations

(TOP VIEW)



WQFN-16L 3x3

Typical Application Circuit

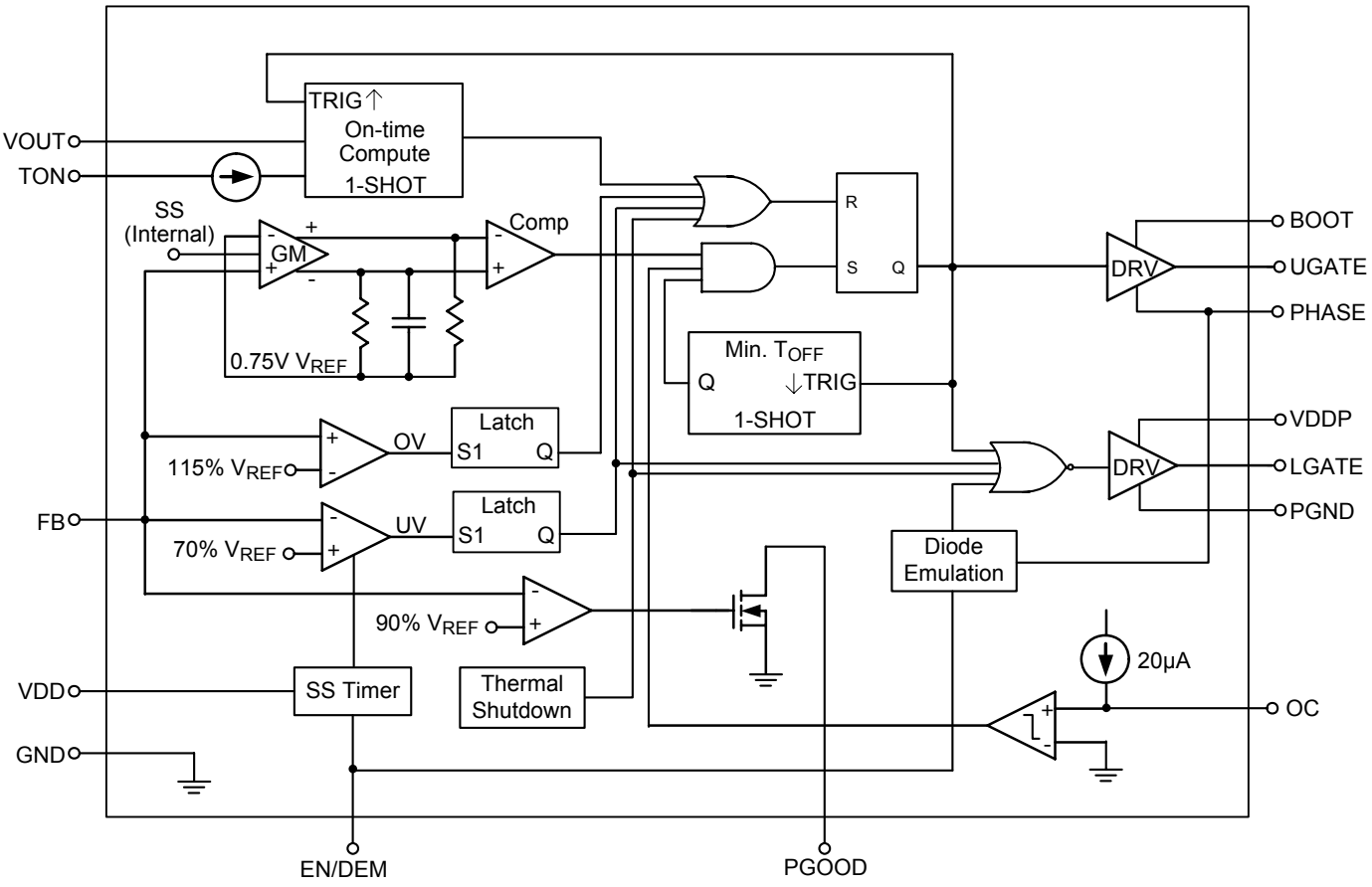


Functional Pin Description

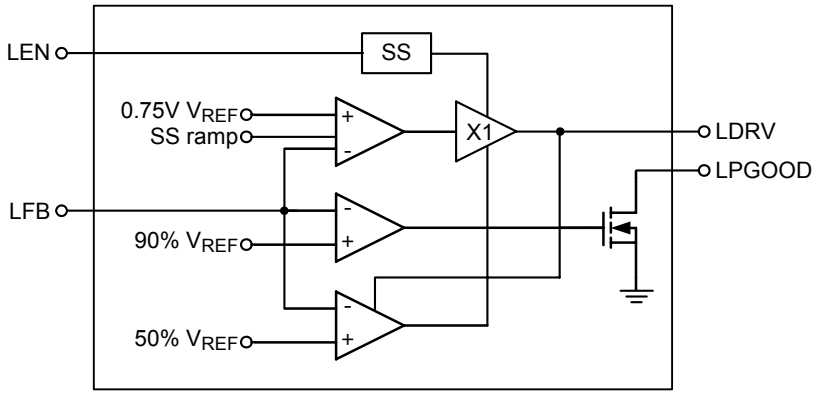
Pin No.	Pin Name	Pin Function
1	VOUT	VOUT Sense Input. Connect to the output of PWM converter. VOUT is an input of the PWM controller.
2	VDD	Analog Supply Voltage Input for the internal analog integrated circuit. Bypass to GND with a 1μF ceramic capacitor.
3	FB	VOUT Feedback Input. Connect FB to a resistor voltage divider from VOUT to GND to adjust the output from 0.75V to 3.3V.
4	PGOOD	Power Good Signal Open-Drain Output of PWM Converter. This pin will be pulled high when the output voltage is within the target range.
5	LPGOOD	Power Good signal Open-Drain Output of LDO Regulator. This pin will be pulled high when the output voltage is within the target range.
6	LFB	LDO Feedback Input. Connect LFB to a resistor voltage divider from VOUT to GND to adjust the output greater than 0.75V.
7	LDRV	Drive Signal for the LDO's path MOSFET.
8	LGATE	Low side N-MOSFET Gate-Drive Output for PWM. This pin swings between GND and VDDP.
9	VDDP	VDDP is the gate driver supply for the external MOSFETs. Bypass to GND with a 1μF ceramic capacitor.
10	OC	PWM Current Limit Setting and sense. Connect a resistor between OC to PHASE for current limit setting.
11	PHASE	Inductor Connection. This pin is not only the zero-current-sense input for the PWM converter, but also the UGATE high side gate driver return.
12	UGATE	High Side N-MOSFET Floating Gate-Driver Output for the PWM converter. This pin swings between PHASE and BOOT.
13	BOOT	Boost Capacitor Connection for PWM Converter. Connect an external ceramic capacitor to PHASE and an external diode to VDDP.
14	LEN	LDO Enable Input with internal pull low resistor. LDO is enabled if LEN is greater than the on level and disabled if LEN is less than the off level.
15	EN/DEM	PWM Enable and Operation Mode Selection Input. Connect to VDD for diode emulation mode, connect to GND for shutdown mode and floating the pin for CCM mode.
16	TON	VIN Sense Input. Connect to VIN through a resistor. TON is an input of the PWM controller.
17 (Exposed Pad)	GND	Analog Ground and Power Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Function Block Diagram

PWM Controller



LDO Controller



Absolute Maximum Ratings (Note 1)

- Input Voltage, TON to GND ---------- –0.3V to 32V
- BOOT to GND ---------- –0.3V to 38V
- PHASE to BOOT ---------- –6V to 0.3V
- PHASE to GND
  - DC ---------- –0.3V to 32V
  - <20ns ---------- –8V to 38V
- VDD, VDDP, VOUT, EN/DEM, LEN, LFB, FB, PGOOD, LPGOOD, LDRV to GND ---------- –0.3V to 6V
- UGATE to PHASE
  - DC ---------- –0.3V to 6V
  - <20ns ---------- –5V to 7.5V
- OC to GND ---------- –0.3V to 28V
- LGATE to GND
  - DC ---------- –0.3V to 6V
  - <20ns ---------- –2.5V to 7.5V
- Power Dissipation, P_D @ T_A = 25°C
  - WQFN-16L 3x3 ---------- 1.471W
- Package Thermal Resistance (Note 2)
  - WQFN-16L 3x3, θ_{JA} ---------- 68°C/W
  - WQFN-16L 3x3, θ_{JC} ---------- 7.5C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Mode) ---------- 2kV
  - MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Input Voltage, V_{IN} ---------- 3V to 26V
- Supply Voltage, V_{DD}, V_{DDP} ---------- 4.5V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{DD} = V_{DDP} = 5V, V_{IN} = 15V, V_{OUT} = 1.25V, EN/DEM = V_{DD}, R_{TON} = 1MΩ, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
PWM Controller						
Quiescent Supply Current		VDD + VDDP, FB = 0.8V, forced above the regulation point	--	--	1250	μA
TON Operating Current		R_{TON} = 1MΩ	--	15	--	μA
Shutdown Current	I_{SHDN}	VDD + VDDP	--	1	10	μA
		TON	--	1	--	
		EN/DEM = 0V	–10	–1	--	

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
FB Reference Voltage	V_{FB}	V_{DD} = 4.5 to 5.5V	0.742	0.75	0.758	V
FB Input Bias Current		FB = 0.75V	−1	0.1	1	μA
Output Voltage Range			0.75	–	3.3	V
On-Time		V_{IN} = 15V, V_{OUT} = 1.25V, R_{TON} = 1MΩ	267	334	401	ns
Minimum Off-Time			250	400	550	ns
V_{OUT} Shutdown Discharge Resistance		EN/DEM = GND	--	20	--	Ω
Current Sensing						
I_{LIM} Source Current		LGATE = High	18	20	22	μA
Current Comparator Offset		GND to OC	−10	–	10	mV
Zero Crossing Threshold		PHASE to GND, EN/DEM = 5V	−10	–	5	mV
Fault Protection						
Current Limit Sense Voltage	V_{RILIM}	GND to PHASE, R_{ILIM} = 2.5kΩ	35	50	65	mV
		GND to PHASE, R_{ILIM} = 10kΩ	170	200	230	
Output UV Threshold			60	70	80	%
OVP Threshold		With respect to error comparator threshold	10	15	20	%
OV Fault Delay		FB forced above OV threshold	--	20	--	μs
VDD UVLO Threshold		Rising edge, Hysteresis = 20mV, PWM disabled below this level	4.1	4.3	4.5	V
Soft-Start Ramp Time		From EN high to internal V_{REF} reach 0.71V (0→95%)	--	1.35	--	ms
UV Blank Time		From EN signal going high	--	3.1	--	ms
Thermal Shutdown			--	155	--	°C
Thermal Shutdown Hysteresis			--	10	--	°C
Driver On-Resistance						
UGATE Driver Pull Up		BOOT to PHASE forced to 5V	--	1.5	5	Ω
UGATE Driver Sink	$R_{UGATEsk}$	BOOT to PHASE forced to 5V	--	1.5	5	Ω
LGATE Driver Pull Up		LGATE, High State (Source)	--	1.5	5	Ω
LGATE Driver Pull Down		LGATE, Low State (Sink)	--	0.6	2.5	Ω
UGATE Driver Source/Sink Current		UGATE forced to 2.5V, BOOT to PHASE forced to 5V	--	1	--	A
LGATE Driver Source Current		LGATE forced to 2.5V	--	1	--	A
LGATE Driver Sink Current		LGATE forced to 2.5V	--	3	--	A
Dead Time		LGATE Rising (PHASE = 1.5V)	--	30	--	ns
		UGATE Rising	--	30	--	
Logic I/O						
Logic Input Low Voltage		EN/DEM Low	--	–	0.8	V
Logic Input High Voltage		EN/DEM High	2.9	–	--	V
		EN/DEM Float	--	2	--	
Logic Input Current		EN/DEM = V_{DD}	--	1	5	μA
		EN/DEM = 0	−5	−1	--	

To be continued

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
PGOOD (upper side threshold decide by OV threshold)							
Trip Threshold (Falling)			Measured at FB with respect to reference, no load. Hysteresis = 3%	−13	−10	−7	%
Fault Propagation Delay			Falling edge, FB forced below PGOOD trip threshold	--	2.5	--	μs
Output Low Voltage			I_{SINK} = 1mA	--	--	0.4	V
Leakage Current			High state, forced to 5V	--	--	1	μA
LDO Controller							
Quiescent Current		I_Q	PWM off, LDO on, I_{OUT} = 0mA	--	--	400	μA
Shut-down Current		I_{SHDN}		--	--	5	μA
Input Voltage UVLO				4.1	--	4.5	V
LEN Logic High Voltage		V_{LEN_H}		2	--	--	V
LEN Logic Low Voltage		V_{LEN_L}		--	--	0.8	V
LEN Input Current		I_{LEN}	LEN = 5V (Internal pull low)	--	--	10	μA
LFB Reference Voltage		V_{LFB}		0.739	0.75	0.761	V
LFB Input Current		I_{LFB}		−1	--	1	μA
LDRV Output Current	Sourcing	I_{LDRV_sr}	V_{LFB} = 0.72V	1.4	2	--	mA
	Sinking	I_{LDRV_sk}	V_{LFB} = 0.78V	1.4	2	--	
Output UVP Threshold			Measured at LFB pin	40	50	60	%
UVP Propagation Delay				--	2.5	--	μs
PGOOD Threshold (Falling)			Measured at LFB pin	87	90	93	%
PGOOD Propagation Delay			Falling edge, FB forced below PGOOD trip threshold	--	2.5	--	μs
PGOOD Low Voltage			I_{SINK} = 1mA	--	--	0.4	V
PGOOD Leakage Current			High state, forced to 5V	--	--	1	μA
Thermal Shutdown				--	155	--	°C
Thermal Shutdown Hysteresis				--	10	--	°C

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

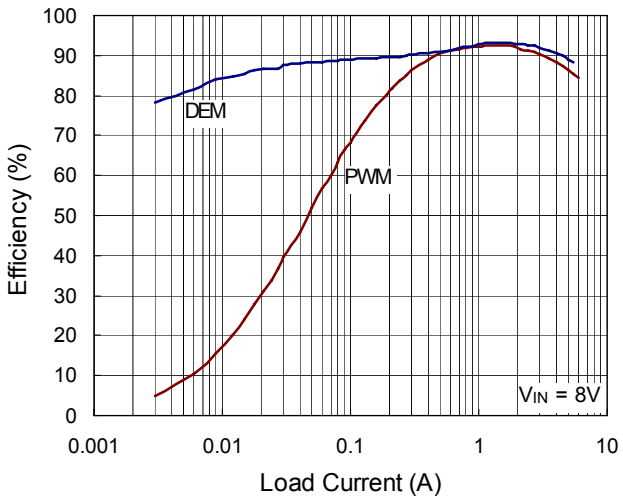
Note 2. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard. The case point of θ_{JC} is on the expose pad for the WQFN package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

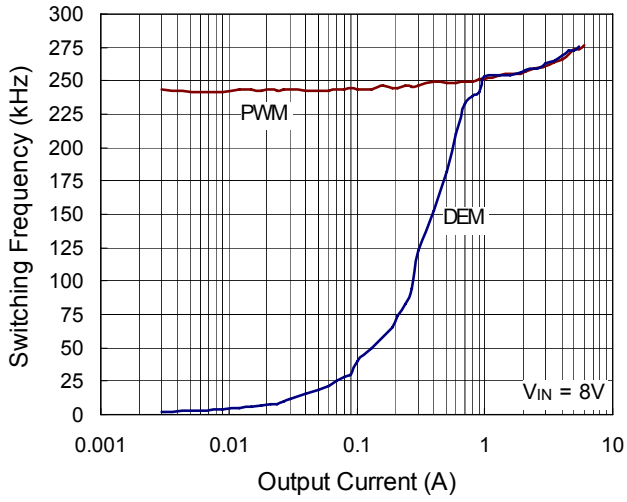
Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Operating Characteristics

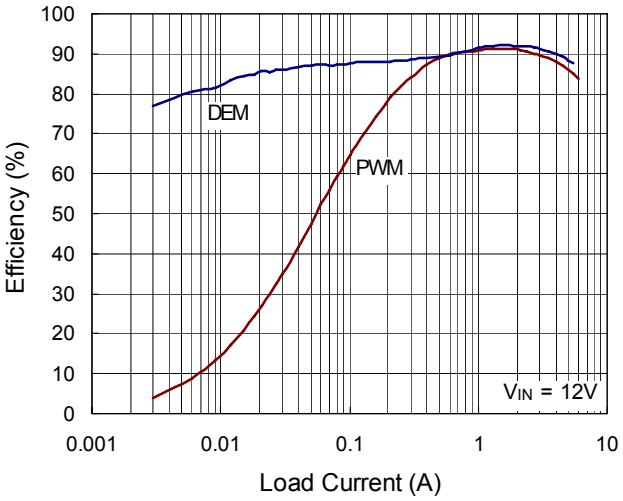
VOUT1 Efficiency vs. Load Current



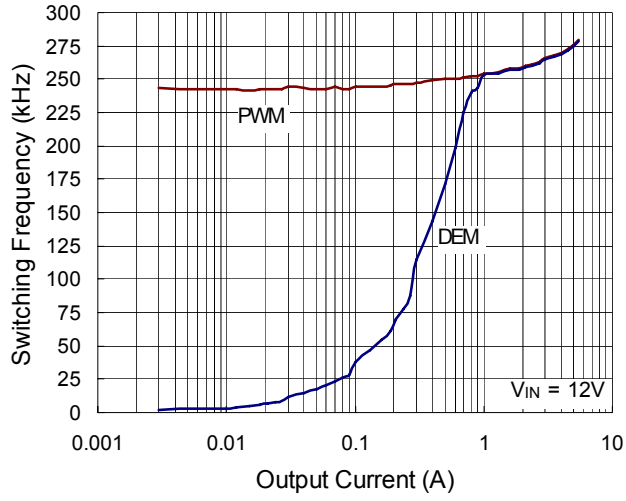
Switching Frequency vs. Output Current



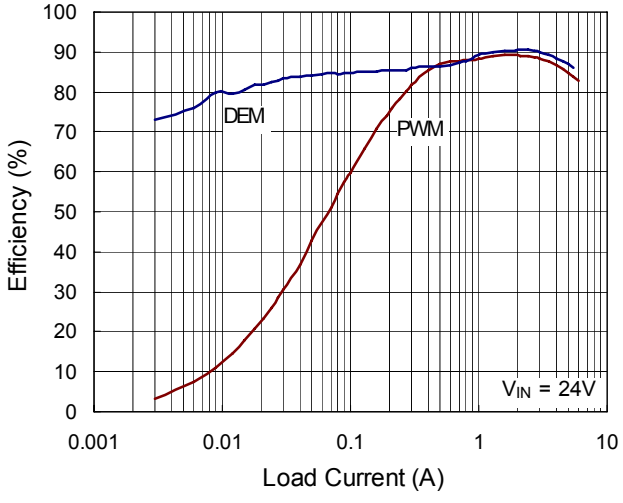
VOUT1 Efficiency vs. Load Current



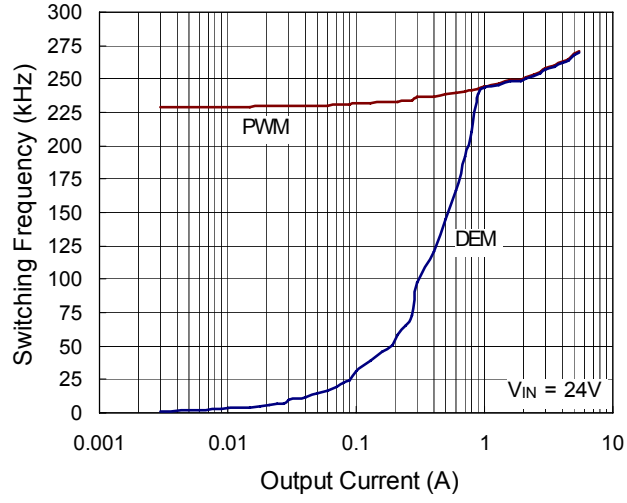
Switching Frequency vs. Output Current



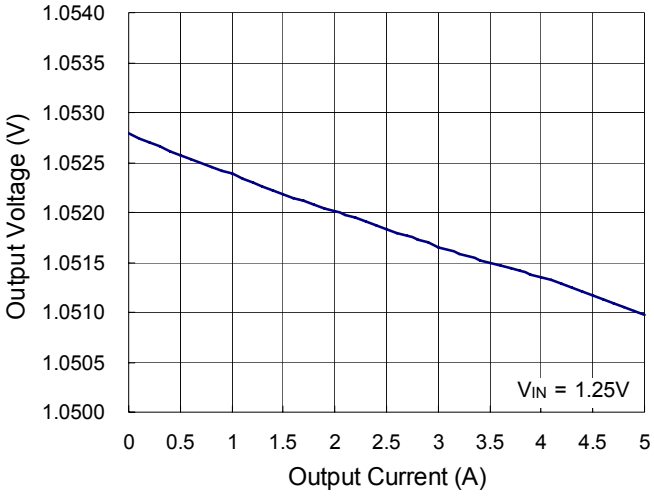
VOUT1 Efficiency vs. Load Current



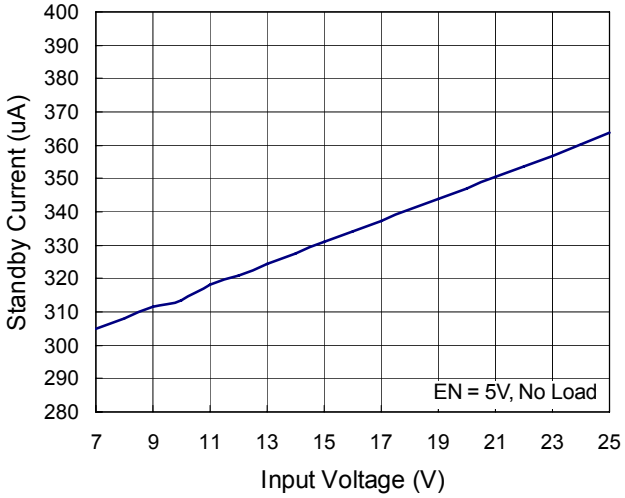
Switching Frequency vs. Output Current



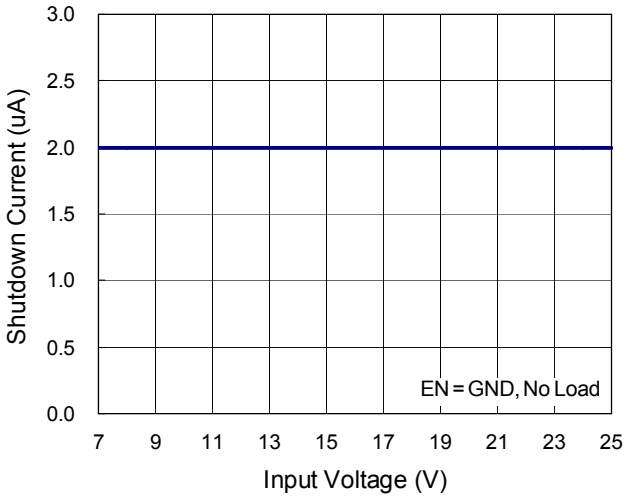
LDO Output Voltage vs. Output Current



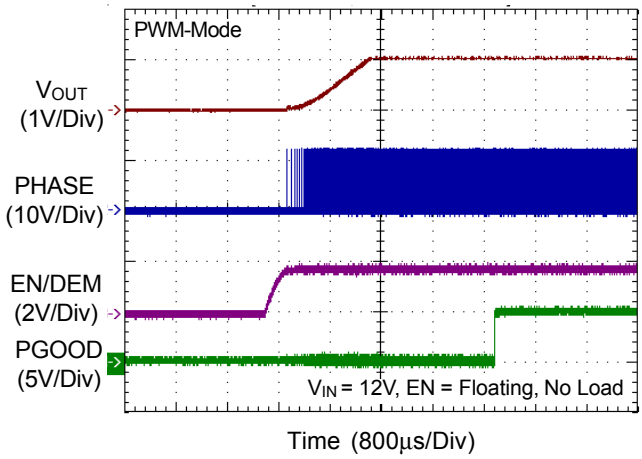
Standby Current vs. Input Voltage



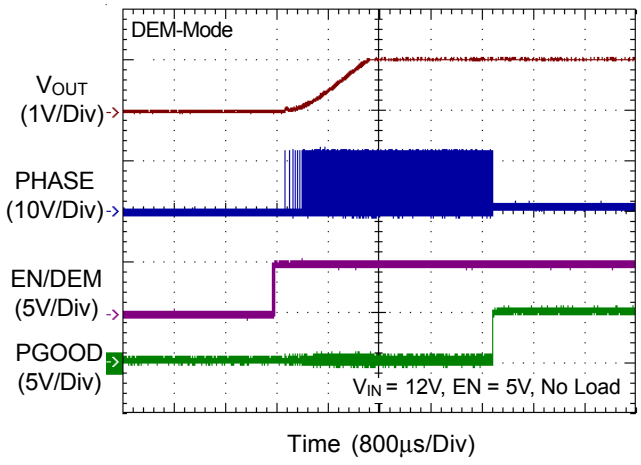
Shutdown Current vs. Input Voltage



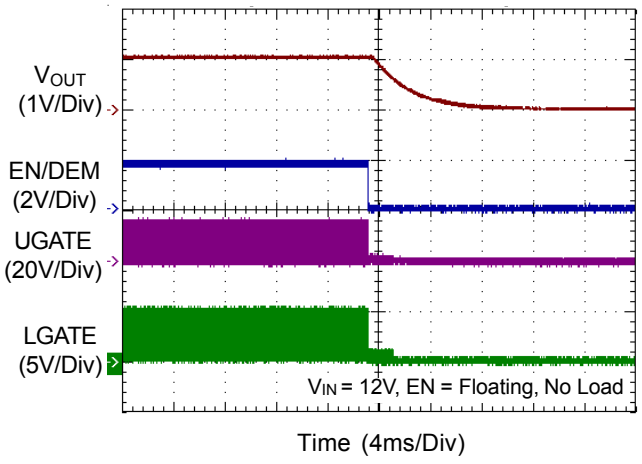
Power On from EN



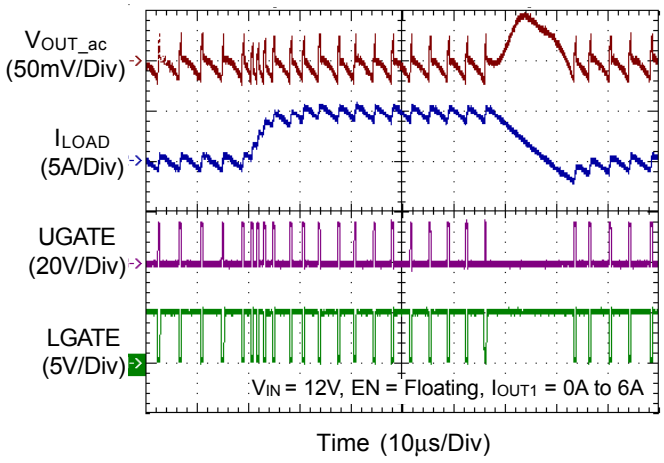
Power On from EN



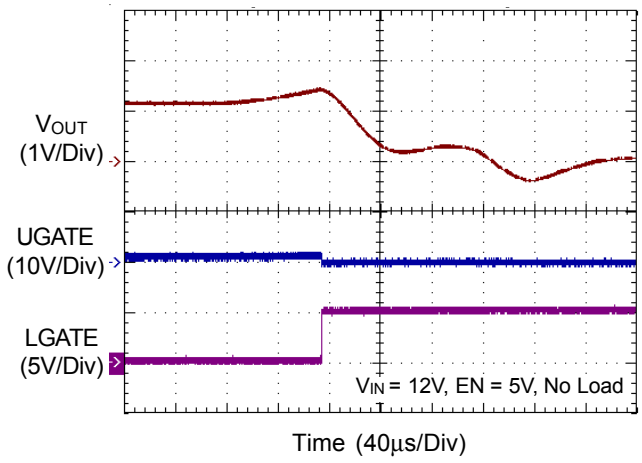
Power Off from EN



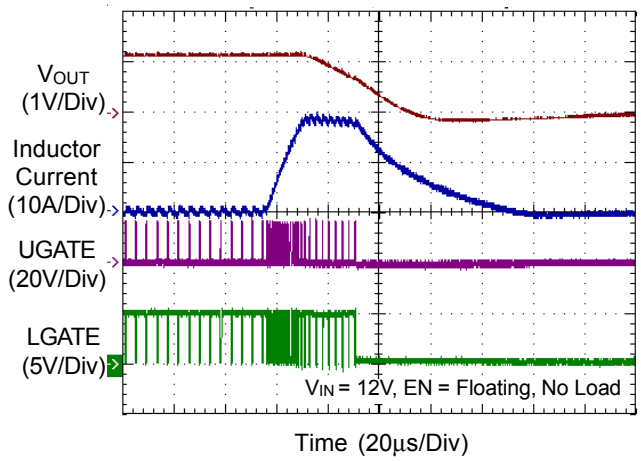
VOUT1 Load Transient Response



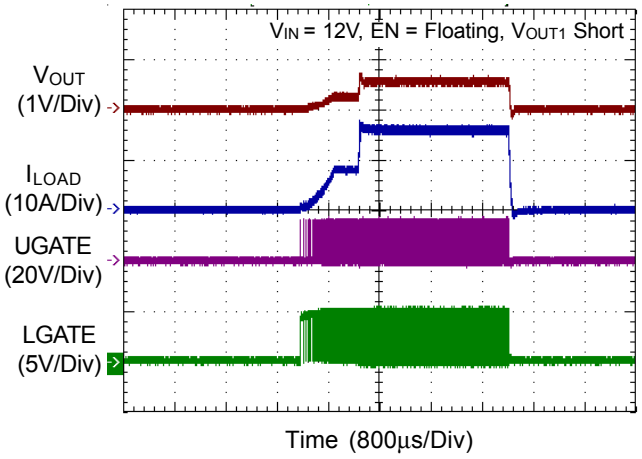
OVP



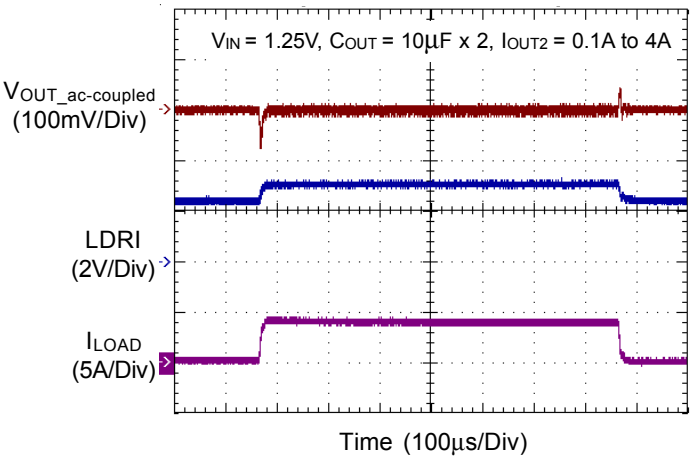
UVP



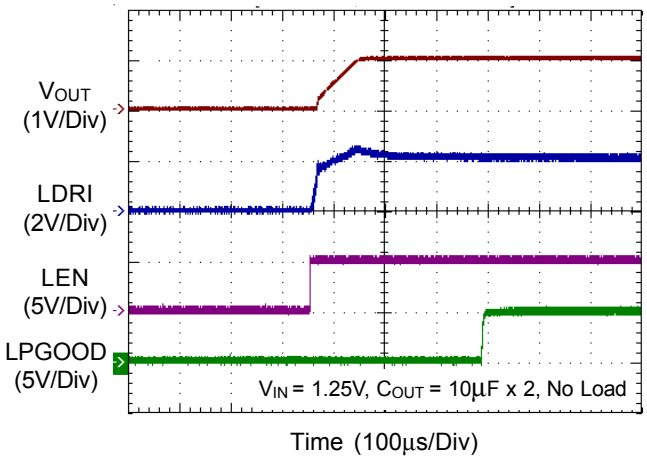
Power On in Short Condition



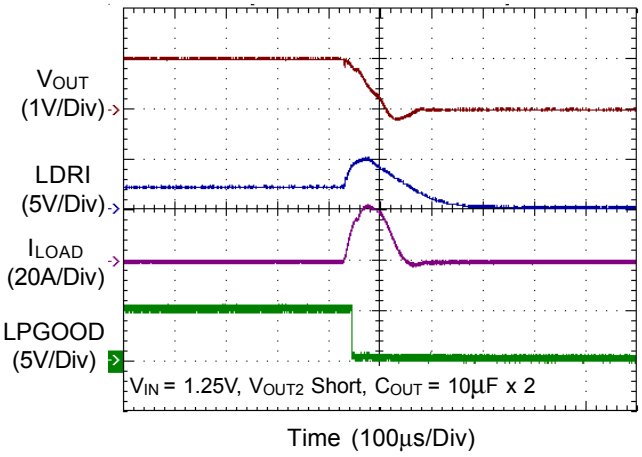
LDO Load Transient Response



LDO Power On from LEN



LDO Short-Circuit Protection



Application Information

The RT8204A PWM controller provides the high efficiency, excellent transient response, and high DC output accuracy needed for stepping down high voltage batteries to generate low voltage CPU core, I/O, and chipset RAM supplies in notebook computers. Richtek's Mach Response™ technology is specifically designed for providing 100ns "instant-on" response to load steps while maintaining a relatively constant operating frequency and inductor operating point over a wide range of input voltages. The topology circumvents the poor load transient timing problems of fixed-frequency current mode PWMs while avoiding the problems caused by widely varying switching frequencies in conventional constant-on-time and constant-off-time PWM schemes. The DRV™ mode PWM modulator is specifically designed to have better noise immunity for such a single output application.

PWM Operation

The Mach Response™, DRV™ mode controller relies on the output filter capacitor's effective series resistance (ESR) to act as a current-sense resistor, so the output ripple voltage provides the PWM ramp signal. Refer to the function diagrams of RT8204A, the synchronous high side MOSFET is turned on at the beginning of each cycle. After the internal one-shot timer expires, the MOSFET is turned off. The pulse width of this one shot is determined by the converter's input and output voltages to keep the frequency fairly constant over the input voltage range. Another one-shot sets a minimum off-time (400ns typ.).

On-Time Control (TON)

The on-time one-shot comparator has two inputs. One input looks at the output voltage, while the other input samples the input voltage and converts it to a current. This input voltage proportional current is used to charge an internal on-time capacitor. The on-time is the time required for the voltage on this capacitor to charge from zero volts to V_{OUT}, thereby making the on-time of the high side switch directly proportional to output voltage and inversely proportional to input voltage. The implementation results in a nearly constant switching frequency without the need of a clock generator.

$T_{ON} = 3.85p \times R_{TON} \times V_{OUT} / (V_{IN} - 0.5)$

And then the switching frequency is :

Frequency = $V_{OUT} / (V_{IN} \times T_{ON})$

R_{TON} is a resistor connected from the input supply (V_{IN}) to the TON pin.

Mode Selection (EN/DEM) Operation

The EN/DEM pin enables the supply. When EN/DEM is tied to VDD, the controller is enabled and operates in diode-emulation mode. When the EN/DEM pin is floating, the RT8204A will operate in forced-CCM mode.

Diode-Emulation Mode (EN/DEM = High)

In diode-emulation mode, RT8204A automatically reduces switching frequency at light load conditions to maintain high efficiency. This reduction of frequency is achieved smoothly without increasing the V_{OUT} ripple or load regulation. As the output current decreases from heavy load condition, the inductor current is also reduced, and eventually comes to the point that its valley touches zero current, which is the boundary between continuous conduction and discontinuous conduction modes. By emulating the behavior of diodes, the low side MOSFET allows only partial of negative current when the inductor freewheeling current reach negative. As the load current is further decreased, it takes longer and longer to discharge the output capacitor to the level than requires the next "ON" cycle. The on-time is kept the same as that in the heavy-load condition. In reverse, when the output current increases from light load to heavy load, the switching frequency increases to the preset value as the inductor current reaches the continuous condition. The transition load point to the light-load operation can be calculated as follows (Figure 1) :

$$I_{LOAD} \approx \frac{(V_{IN} - V_{OUT})}{2L} \times T_{ON}$$

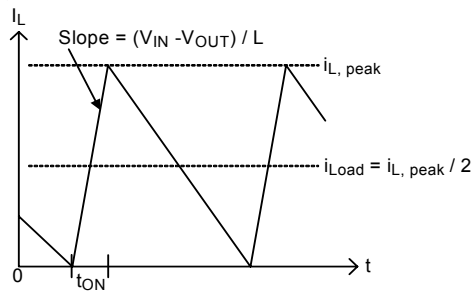


Figure 1. Boundary Condition of CCM/DEM

The switching waveforms may appear noisy and asynchronous when light loading causes diode-emulation operation, but this is a normal operating condition that results in high light-load efficiency. Trade-off in DEM noise vs. light-load efficiency is made by varying the inductor value. Generally, low inductor values produce a broader efficiency vs. load curve, while higher values result in higher full-load efficiency (assuming that the coil resistance remains fixed) and less output voltage ripple. The disadvantages for using higher inductor values include larger physical size and degrades load-transient response (especially at low input-voltage levels).

Forced-CCM Mode (EN/DEM = floating)

The low noise, forced-CCM mode (EN/DEM = floating) disables the zero-crossing comparator, which controls the low-side switch on-time. This causes the low side gate-drive waveform to become the complement of the high-side gate-drive waveform. This in turn causes the inductor current to reverse at light loads as the PWM loop to maintain a duty ratio V_{OUT}/V_{IN}. The benefit of forced-CCM mode is to keep the switching frequency fairly constant, but it comes at a cost: The no-load battery current can be up to 10mA to 40mA, depending on the external MOSFETs.

Current Limit Setting (OCP)

The RT8204A has cycle-by-cycle current limiting control. The current limit circuit employs a unique "valley" current sensing algorithm. If the magnitude of the current-sense signal at OC is above the current limit threshold, the PWM is not allowed to initiate a new cycle (Figure 2).

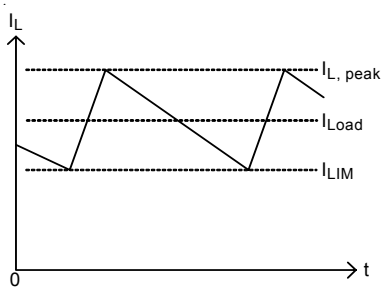


Figure 2. Valley Current-Limit

Current sensing of the RT8204A can be accomplished in two ways. Users can either use a current sense resistor or the on-state of the low-side MOSFET ($R_{DS(ON)}$). For resistor sensing, a sense resistor is placed between the source of low-side MOSFET and PGND (Figure 3(a)). $R_{DS(ON)}$ sensing is more efficient and less expensive (Figure 3(b)). There is a compromise between current limit accuracy and sense resistor power dissipation.

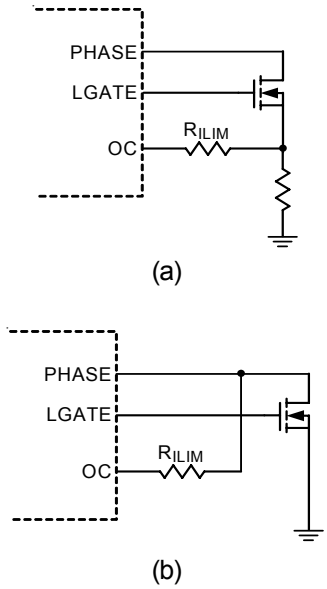


Figure 3. Current-Sense Methods

In both cases, the R_{ILIM} resistor between the OC pin and PHASE pin sets the over current threshold. This resistor R_{ILIM} is connected to a 20µA current source within the RT8204A which is turned on when the low side MOSFET turns on. When the voltage drop across the sense resistor or low-side MOSFET equals the voltage across the R_{ILIM} resistor, positive current limit will be activated. The high side MOSFET will not be turned on until the voltage drop across the sense element (resistor or MOSFET) falls below the voltage across the R_{ILIM} resistor.

Choose a current limit resistor by following equation :

$R_{ILIM} = I_{LIMIT} \times R_{SENSE} / 20\mu A$

Carefully observe the PC board layout guidelines to ensure that noise and DC errors do not corrupt the current-sense signal seen by OC and PGND. Mount the IC close to the low-side MOSFET and sense resistor with short, direct traces, making a Kelvin sense connection to the sense resistor.

MOSFET Gate Driver (UGATE, LGATE)

The high side driver is designed to drive high current, low $R_{DS(ON)}$ N-MOSFETs. When configured as a floating driver, 5V bias voltage is delivered from VDDP supply. The average drive current is proportional to the gate charge at V_{GS} = 5V times switching frequency. The instantaneous drive current is supplied by the flying capacitor between BOOT and PHASE pins.

A dead time to prevent shoot through is internally generated between high side MOSFET off to low side MOSFET on, and low side MOSFET off to high side MOSFET on.

The low side driver is designed to drive high current, low $R_{DS(ON)}$ N-MOSFETs. The internal pull-down transistor that drives LGATE low is robust, with a 0.6Ω typical on-resistance. A 5V bias voltage is delivered form VDDP supply. The instantaneous drive current is supplied by the flying capacitor between VDDP and PGND.

For high current applications, some combinations of high and low side MOSFETs might be encountered that will cause excessive gate-drain coupling, which can lead to efficiency-killing, EMI-producing shoot-through currents. This is often remedied by adding a resistor in series with BOOT, which increases the turn-on time of the high-side MOSFET without degrading the turn-off time (Figure 4).

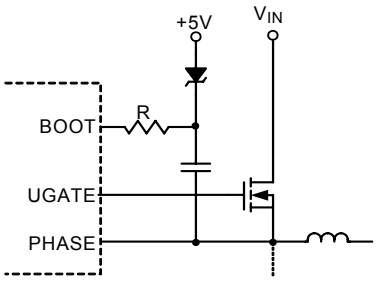


Figure 4. The UGATE Rise Time Reduction

Power-Good Output (PGOOD)

The power good output is an open-drain output and requires a pull-up resistor. When the output voltage is 15% above or 10% below its set voltage, the PGOOD gets pulled low. It is held low until the output voltage returns to within these tolerances once more. In soft start, the PGOOD is actively held low and is allowed to be pulled high until soft start is over and the output reaches 93% of its set voltage. There is a 2.5μs delay built into the PGOOD circuitry to prevent false transition.

POR, UVLO and Soft-Start

Power-on reset (POR) occurs when VDD rises above to approximately 4.3V, the RT8204A will reset the fault latch and prepare the PWM for operation. If the VDD is below 4.1V $_{(MIN)}$, the VDD undervoltage-lockout (UVLO) circuitry inhibits switching by keeping UGATE and LGATE low.

A built-in soft-start is used to prevent the surge current from power supply input after EN/DEM is enabled. It clamps the ramping of internal reference voltage which is compared with the FB signal. The typical soft-start duration is 1.35ms.

Furthermore, the maximum allowed current limit is segment in 2 steps during 1.35ms period.

Output Over Voltage Protection (OVP)

The output voltage can be continuously monitored for over voltage protection. When the output voltage exceeds 15% of the its setting voltage threshold, the over voltage protection is triggered and the low side MOSFET is latched on. This activates the low side MOSFET to discharge the output capacitor.

The RT8204A is latched once OVP is triggered and can only be released by VDD or EN/DEM power on reset. There is a 20μs delay built into the over voltage protection circuit to prevent false transitions.

Output Under Voltage Protection (UVP)

The output voltage can be continuously monitored for under voltage protection. When the output voltage is less than 70% of its set voltage threshold, the under voltage protection is triggered and then both UGATE and LGATE gate drivers are forced low. In order to remove the residual charge on the output capacitor during the under voltage period, if the PHASE is greater than 1V, the LGATE is forced high until PHASE is lower than 1V. There is 2.5μs delay built into the under voltage protection circuit to prevent false transitions. During the soft-start, the UVP will be blanked around 3.1ms.

Output Voltage Setting (FB)

The output voltage can be adjusted from 0.75V to 3.3V by setting the feedback resistor R1 and R2 (Figure 5). Choose R2 to be approximately 10kΩ, and solve for R1 using the equation :

$$V_{OUT} = V_{FB} \times \left[1 + \left(\frac{R1}{R2}\right)\right]$$

where V_{FB} is 0.75V.

Note that in order for the device to regulate in a controlled manner, the ripple content at the feedback pin, V_{FB}, should be approximately 15mV at minimum V_{BAT}, and worst case no smaller than 10mV. If V_{ripple} at minimum V_{BAT} is less than 15mV, the above component values should be revisited in order to improve this. Quite often a small capacitor, C1, is required in parallel with the top feedback resistor, R1, in order to ensure that V_{FB} is large enough. The value of C1 can be calculated as follows, where R2 is the bottom feedback resistor.

Firstly calculating the value of Z1 required :

$$Z1 = \frac{R2}{0.015} \times \left(V_{ripple\_VBAT(MIN)} - 0.015\right) \quad \Omega$$

Secondly calculating the value of C1 required to achieve this :

$$C1 = \frac{\left(\frac{1}{Z1} - \frac{1}{R1}\right)}{2 \times \pi \times f_{SW\_VBAT(MIN)}} \quad F$$

Finally using the equation as follows to verify the value of V_{FB} :

$$V_{FB\_VBAT(MIN)} = V_{ripple\_VBAT(MIN)} \times \left[\frac{R2}{R2 + \frac{1}{\frac{1}{R1} + 2 \times \pi \times f_{SW\_VBAT(MIN)} \times C1}}\right] \quad V$$

where $V_{ripple\_VBAT(MIN)}$ is the output ripple voltage in minimum V_{BAT} ;

$f_{sw\_VBAT(MIN)}$ is the switching frequency in minimum V_{BAT};

$V_{FB\_VBAT(MIN)}$ is the ripple voltage into FB pin in minimum V_{BAT}.

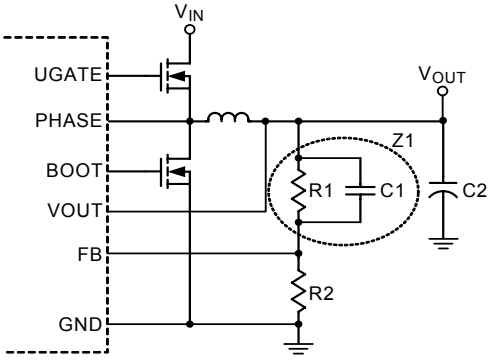


Figure 5. Setting The Output Voltage

For application that output voltage is higher than 3.3V, user can also use a voltage divider to keep VOUT pin voltage within 0.75V to 2.8V as shown in Figure 6. For this case, T_{ON} can be determined as below :

$$\text{If } R_{TON} < 2M\Omega \text{ then } T_{ON} = 3.85p \times \frac{R_{TON} \times V_{OUT\_FB}}{V_{IN} - 0.5}$$

$$\text{If } R_{TON} \geq 2M\Omega \text{ then } T_{ON} = 3.55p \times \frac{R_{TON} \times V_{OUT\_FB}}{V_{IN} - 0.4}$$

Where R_{TON} is T_{ON} set resistor and the V_{OUT_FB} is the output signal of resistor divider. Since the switching frequency is

$$F_S = \frac{V_{OUT}}{V_{IN} \times T_{ON}}$$

For a given switching frequency, we can obtain the R_{TON} as below

If $R_{TON} < 2M\Omega$ then

$$R_{TON} = \frac{V_{OUT} - 0.5}{V_{IN}} \times \frac{V_{OUT}}{V_{OUT\_FB}} \times \frac{1}{F_S \times 3.85p}$$

If $R_{TON} \geq 2M\Omega$ then

$$R_{TON} = \frac{V_{OUT} - 0.4}{V_{IN}} \times \frac{V_{OUT}}{V_{OUT\_FB}} \times \frac{1}{F_S \times 3.55p}$$

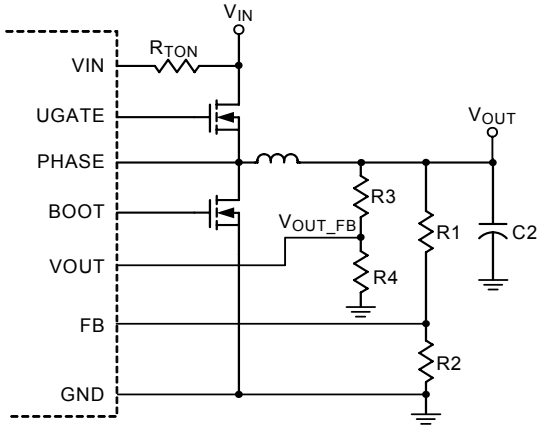


Figure 6. Output Voltage Setting for V_{OUT} > 3.3V Application

Output Inductor Selection

The switching frequency (on-time) and operating point (% ripple or L_{IR}) determine the inductor value as follows :

$$L = \frac{T_{ON} \times (V_{IN} - V_{OUT})}{L_{IR} \times I_{LOAD(MAX)}}$$

Find a low pass inductor having the lowest possible DC resistance that fits in the allowed dimensions. Ferrite cores are often the best choice, although powdered iron is inexpensive and can work well at 200kHz. The core must be large enough and not to saturate at the peak inductor current (I_{PEAK}) :

$I_{PEAK} = I_{LOAD(MAX)} + [(L_{IR} / 2) \times I_{LOAD(MAX)}]$

Output Capacitor Selection

The output filter capacitor must have ESR low enough to meet output ripple and load transient requirement, yet have high enough ESR to satisfy stability requirements. Also, the capacitance value must be high enough to absorb the inductor energy going from a full-load to no-load condition without tripping the OVP circuit.

For CPU core voltage converters and other applications where the output is subject to violent load transient, the output capacitor's size depends on how much ESR is needed to prevent the output from dipping too low under a load transient. Ignoring the sag due to finite capacitance :

$$ESR \leq \frac{V_{P-P}}{I_{LOAD(MAX)}}$$

In non-CPU applications, the output capacitor's size depends on how much ESR is needed to maintain at an acceptable level of output voltage ripple :

$$ESR \leq \frac{V_{P-P}}{L_{IR} \times I_{LOAD(MAX)}}$$

Organic semiconductor capacitors or specially polymer capacitors are recommended.

Output Capacitor Stability

Stability is determined by the value of the ESR zero relative to the switching frequency. The point of instability is given by the following equation :

$$f_{ESR} = \frac{1}{2 \times \pi \times ESR \times C_{OUT}} \leq \frac{f_{SW}}{4}$$

Do not put high-value ceramic capacitors directly across the outputs without taking precautions to ensure stability. Large ceramic capacitors can have a high ESR zero frequency and cause erratic and unstable operation. However, it is easy to add sufficient series resistance by placing the capacitors a couple of inches downstream from the inductor and connecting V_{OUT} or FB divider close to the inductor.

There are two related but distinct ways including double-pulsing and feedback loop instability to identify the unstable operation.

Double-pulsing occurs due to noise on the output or because the ESR is too low that there is not enough voltage ramp in the output voltage signal. The "fools" the error comparator into triggering a new cycle immediately after 400ns minimum off-time period has expired. Double-pulsing is more annoying than harmful, resulting in nothing worse than increased output ripple. However, it may indicate the possible presence of loop instability, which is caused by insufficient ESR.

Loop instability can result in oscillation at the output after line or load perturbations that can trip the over voltage protection latch or cause the output voltage to fall below the tolerance limit.

The easiest method for stability checking is to apply a very zero-to-max load transient and carefully observe the output-voltage-ripple envelope for overshoot and ringing. It helps to simultaneously monitor the inductor current with AC probe. Do not allow more than one ringing cycle after the initial step-response under- or over-shoot.

LDO Normal Operation

The RT8204A LDO controls an N-MOSFET to produce a tightly regulated output voltage from higher supply voltage. It takes 5V power supply for controller and draws maximally 400μA while operating.

The feedback voltage is regulated to compare with the internal 0.75V reference voltage. To set the output voltage, feedback the conjunction of a resistor voltage divider from output node to ground for the LFB pin.

Depending upon the input voltage used for the device, the LDRV pin can be pulled up near to VDD. Thus the device can be used to regulate a large range of output voltage by careful selection of the external MOSFETs.

A built-in active high enable control (LEN pin) is used to turn the RT8204A LDO on. If this pin is pulled low, the LDRV pin is pulled low, turning off the N-MOSFET. If this pin is pulled higher than 2V, the LDRV pin is enabled.

The RT8204A LDO contains a power good output pin (LPGOOD pin) which is an open drain output that will be pulled low if the output is below the power good threshold (typically 90% of the programmed output voltage, or 93% at the start up). The power good detection is active if the RT8204A LDO is enabled.

The RT8204A LDO also includes a under voltage protection circuit that monitors the output voltage. If the output voltage drops below 50% (typical) of the nominal value, as would occur during over current or short condition, the RT8204A LDO will pull the LDRV pin low and latch off. The RT8204A LDO is latched once the UVP is triggered and can only be relieved by the VDD or LEN power-on reset.

LDO Driver and Stability Design

The drive output (LDRV pin) is sink/source capable. The sink current is typically 2mA while the source current is typically 2mA in normal operation.

The drive output is also used for stabilizing the loop of the system using different type of the output capacitor. The components listed in the table below should be used.

Table 1. LDO Configuration and Compensation

LDO Configuration		Compensator		
Input Voltage	Output Voltage	C7	C8	R11
1.25V	1.05V	33nF	39pF	82Ω
1.5V	1.05V	33nF	47pF	43Ω
1.5V	1.25V	33nF	47pF	30Ω
1.8V	1.5V	33nF	39pF	100Ω

Note: test condition is output capacitor 220μF(ESR : 9 to 25mΩ) or 100μF(ESR : 9 to 15mΩ) + MLCC 10μFoutput current is from 0.1A to 5A

LDO Output Under Voltage Protection(UVP)

The RT8204A LDO has output under voltage protection that looks at the output to see if it is :

(a) The LDO output voltage is less than 50% (typical) of its nominal value and

(b) The V_{DRV} is within 900mV (typical) of its maximum.

This provides inherent immunity to under voltage shut down at start up since V_{DRV} has a slow rate of rising at this moment. If both of these criteria are met, the output will be shut down by means of the V_{DRV} pulled to ground immediately.

If the VDDP input is coming prior to the LDO_VIN, it could accidentally meet the UVP fault protection. To avoid entering UVP latch off, using enable control (LEN pin) to turn the system on whenever all power supplies are ready. Please see the power sequencing example as below (Figure 7).

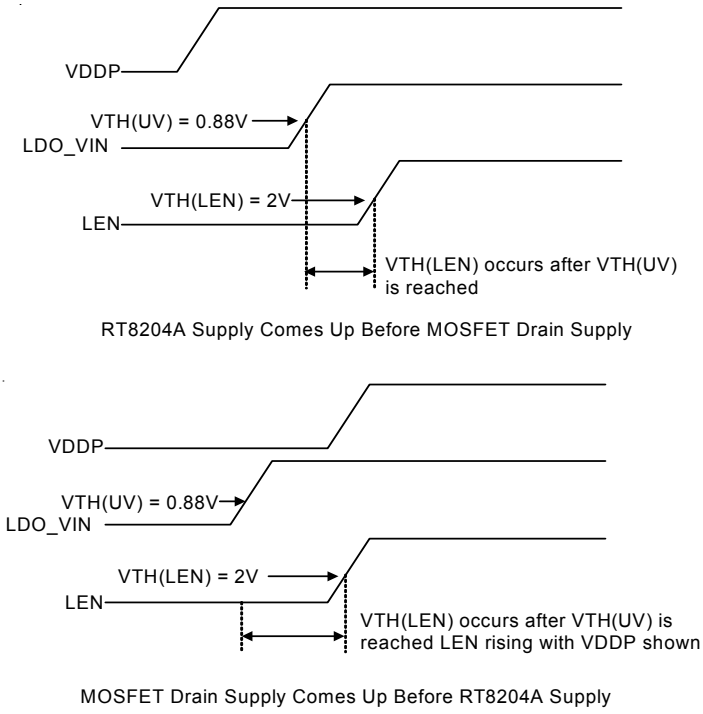


Figure 7. Power Supply Sequencing

LDO Output Voltage Setting

The LFB pin connects directly to the inverting input of the error amplifier, and the output voltage is set using external resistor R3 and R4 (Figure 8). The following equation is for adjusting the output voltage.

$$V_{OUT} = V_{LFB} \times \left[1 + \left(\frac{R3}{R4}\right)\right]$$

where V_{LFB} is 0.75V (typ.).

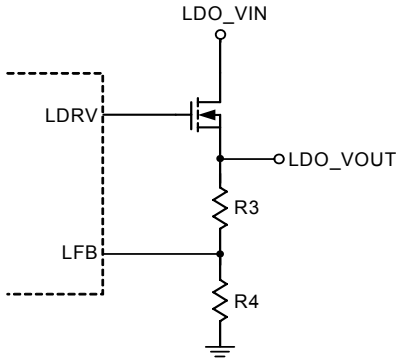


Figure 8. LDO Output Voltage Setting

LDO Output Capacitor Selection

Low ESR capacitors such as Sanyo POSCAPs or Panasonic SP-caps are recommended for bulk capacitance, and ceramic bypass capacitors are recommended for decoupling high frequency transients.

LDO Input Capacitor Selection

Low ESR capacitors such as Sanyo POSCAPs or Panasonic SP-caps are recommended for the input capacitors to provide better load transient response. If the LDO input is connected from the output of buck converter (V_{OUT1}), a 0.1μF ceramic capacitor will sufficient.

LDO MOSFET Selection

Low threshold N-MOSFETs are required. For the device to work under all operating conditions, a maximum $R_{DS(ON)}$ must be met to ensure that the output will not go into dropout :

$$R_{DS(ON)(MAX)} = \frac{V_{IN(MIN)} - V_{OUT(MAX)}}{I_{OUT(PEAK)}} \quad \Omega$$

Note that $R_{DS(ON)}$ must be met for operating temperature range at the minimum V_{GS} condition.

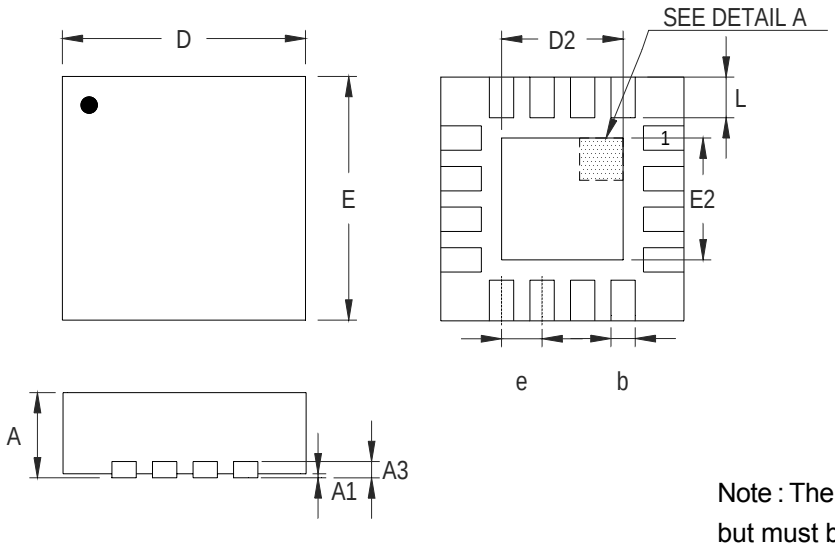
Power consumptions of the N-MOSFETs should be taken into consideration for the selection of various package types.

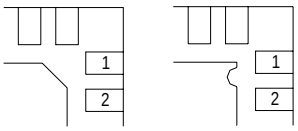
Layout Considerations

Layout is very important in high frequency switching converter design. If the Layout is designed improperly, the PCB could radiate excessive noise and contribute to the converter instability. Certain points must be considered before starting a layout for the RT8204A.

- Connect an RC low pass filter from VDDP to VDD, 1μF and 10Ω are recommended. Place the filter capacitor close to the IC.
- Keep current limit setting network as close as possible to the IC. Routing of the network should avoid coupling to high voltage switching node.
- Connections from the drivers to the respective gate of the high side or the low side MOSFET should be as short as possible to reduce stray inductance.
- All sensitive analog traces and components such as VOUT, FB, GND, EN/DEM, PGOOD, OC, VDD, and TON should be placed away from high voltage switching nodes such as PHASE, LGATE, UGATE, or BOOT nodes to avoid coupling. Use internal layers as ground planes and shield the feedback trace from power traces and components.
- Current sense connections must always be made using Kelvin connections to ensure an accurate signal, with the current limit resistor located at the device.
- Power sections should connect directly to ground planes using multiple vias as required for current handling (including the chip power ground connections). Power components should be placed to minimize loops and reduce losses.

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	1.300	1.750	0.051	0.069
E	2.950	3.050	0.116	0.120
E2	1.300	1.750	0.051	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 16L QFN 3x3 Package

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