# 2A, 4MHz, Synchronous Step-Down Regulator

## General Description

The RT8015 is a high efficiency synchronous, step-down DC/DC converter. Its input voltage range is from 2.6V to 5.5V and provides an adjustable regulated output voltage from 0.8V to 5V while delivering up to 2A of output current.

The internal synchronous low on-resistance power switches increase efficiency and eliminate the need for an external Schottky diode. Switching frequency is set by an external resistor or can be synchronized to an external clock. 100% duty cycle provides low dropout operation extending battery life in portable systems. Current mode operation with external compensation allows the transient response to be optimized over a wide range of loads and output capacitors.

RT8015 operation in forced continuous PWM Mode which minimizes ripple voltage and reduces the noise and RF interference. 100% duty cycle in Low Dropout Operation further maximize battery life.

## Ordering Information

RT8015 □ □

- Package Type
  SP : SOP-8 (Exposed Pad)
- Operating Temperature Range
  P : Pb Free with Commercial Standard
  G : Green (Halogen Free with Commercial Standard)

Note :

RichTek Pb-free and Green products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.
- 100% matte tin (Sn) plating.

## Features

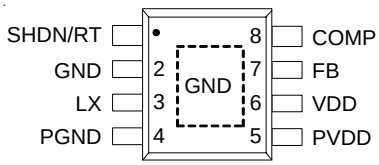
- **High Efficiency : Up to 95%**
- **Low $R_{DS(ON)}$ Internal Switches : 110mΩ**
- **Programmable Frequency : 300kHz to 4MHz**
- **No Schottky Diode Required**
- **0.8V Reference Allows Low Output Voltage**
- **Forced Continuous Mode Operation**
- **Low Dropout Operation : 100% Duty Cycle**
- **RoHS Compliant and 100% Lead (Pb)-Free**

## Applications

- Portable Instruments
- Battery-Powered Equipment
- Notebook Computers
- Distributed Power Systems
- IP Phones
- Digital Cameras

## Pin Configurations

(TOP VIEW)

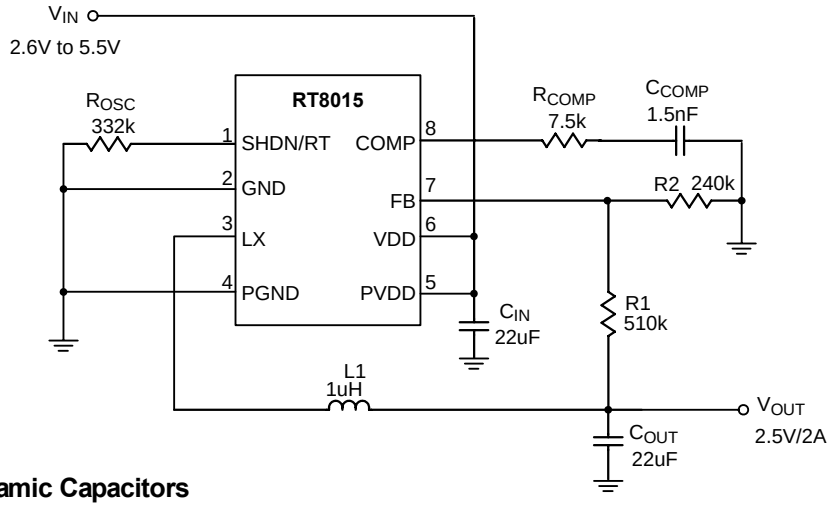



SOP-8 (Exposed Pad)

## Marking Information

For marking information, contact our sales representative directly or through a RichTek distributor located in your area, otherwise visit our website for detail.

## Typical Application Circuit




**Note : Using all Ceramic Capacitors**

### Layout Guide

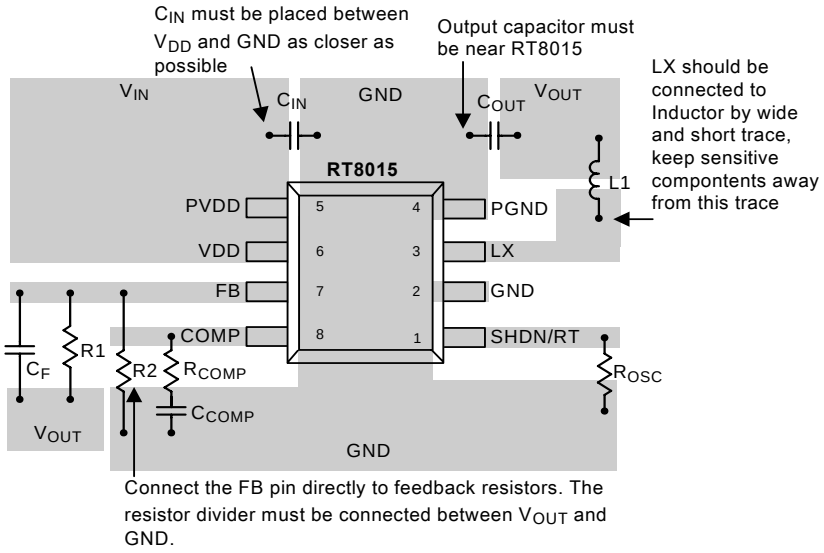



**Table 1**

| Component Supplier | Series | Inductance (uH) | DCR (mΩ) | Current Rating (mA) | Dimensions (mm) |
|---|---|---|---|---|---|
| **TAIYO YUDEN** | NR 4018 | 2.2 | 60 | 2700 | 4x4x1.8 |
| **Sumida** | CDRH4D28 | 2.2 | 31.3 | 2040 | 4.5x4.5x3 |
| **GOTREND** | GTSD53 | 2.2 | 29 | 2410 | 5x5x2.8 |
| **ABC** | SR0403 | 2.2 | 47 | 2600 | 4.5x4x3.2 |

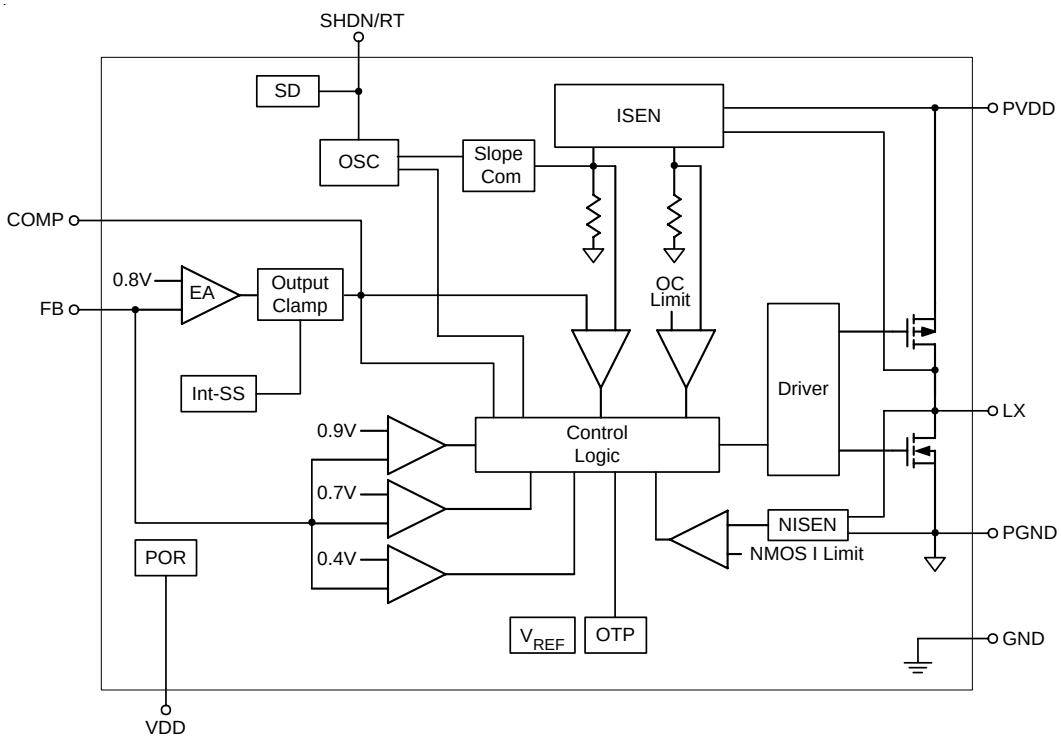
**Table 2**

| Component Supplier | Part No. | Capacitance (uF) | Case Size |
|---|---|---|---|
| **TDK** | C3225X5R0J226M | 22 | 1210 |
| **TDK** | C2012X5R0J106M | 10 | 0805 |
| **Panasonic** | ECJ4YB0J226M | 22 | 1210 |
| **Panasonic** | ECJ4YB1A226M | 22 | 1210 |
| **Panasonic** | ECJ4YB1A106M | 10 | 1210 |
| **TAIYO YUDEN** | LMK325BJ226ML | 22 | 1210 |
| **TAIYO YUDEN** | JMK316BJ226ML | 22 | 1206 |
| **TAIYO YUDEN** | JMK212BJ106ML | 10 | 0805 |

## Functional Pin Description

| Pin Number | Pin Name | Pin Function |
|---|---|---|
| 1 | SHDN/RT | Oscillator Resistor Input. Connecting a resistor to ground from this pin sets the switching frequency. Forcing this pin to $V_{DD}$ causes the device to be shut down. |
| 2 | GND, Exposed Pad | Signal Ground. All small-signal components and compensation components should connect to this ground, which in turn connects to PGND at one point. Exposed pad should be soldered to PCB board and connected to GND. |
| 3 | LX | Internal Power MOSFET Switches Output. Connect this pin to the inductor. |
| 4 | PGND | Power Ground. Connect this pin close to the (–) terminal of $C_{IN}$ and $C_{OUT}$. |
| 5 | PVDD | Power Input Supply. Decouple this pin to PGND with a capacitor. |
| 6 | VDD | Signal Input Supply. Decouple this pin to GND with a capacitor. Normally $V_{DD}$ is equal to PVDD. |
| 7 | FB | Feedback Pin. Receives the feedback voltage from a resistive divider connected across the output. |
| 8 | COMP | Error Amplifier Compensation Point. The current comparator threshold increases with this control voltage. Connect external compensation elements to this pin to stabilize the control loop. |

## Function Block Diagram



## Operation

### Main Control Loop

The RT8015 is a monolithic, constant-frequency, current mode step-down DC/DC converter. During normal operation, the internal top power switch (P-Channel MOSFET) is turned on at the beginning of each clock cycle. Current in the inductor increases until the peak inductor current reach the value defined by the voltage on the COMP pin. The error amplifier adjusts the voltage on the COMP pin by comparing the feedback signal from a resistor divider on the FB pin with an internal 0.8V reference. When the load current increases, it causes a reduction in the feedback voltage relative to the reference. The error amplifier raises the COMP voltage until the average inductor current matches the new load current. When the top power MOSFET shuts off, the synchronous power switch (N-Channel MOSFET) turns on until either the bottom current limit is reached or the beginning of the next clock cycle.

The operating frequency is set by an external resistor connected between the RT pin and ground. The practical switching frequency can range from 300kHz to 4MHz. Power Good comparators will pull the PGOOD output low if the output voltage comes out of regulation by 12.5%. In an over-voltage condition, the top power MOSFET is turned off and the bottom power MOSFET is switched on until either the over-voltage condition clears or the bottom MOSFET's current limit is reached.

### Frequency Synchronization

The internal oscillator of the RT8011 can be synchronized to an external clock connected to the SYNC pin. The frequency of the external clock can be in the range of 300kHz to 4MHz. For this application, the oscillator timing resistor should be chosen to correspond to a frequency that is about 20% lower than the synchronization frequency.

### Dropout Operation

When the input supply voltage decreases toward the output voltage, the duty cycle increases toward the maximum on-time. Further reduction of the supply voltage forces the main switch to remain on for more than one cycle eventually reaching 100% duty cycle.

The output voltage will then be determined by the input voltage minus the voltage drop across the internal P-Channel MOSFET and the inductor.

### Low Supply Operation

The RT8015 is designed to operate down to an input supply voltage of 2.6V. One important consideration at low input supply voltages is that the $R_{DS(ON)}$ of the P-Channel and N-Channel power switches increases. The user should calculate the power dissipation when the RT8015 is used at 100% duty cycle with low input voltages to ensure that thermal limits are not exceeded.

### Slope Compensation and Inductor Peak Current

Slope compensation provides stability in constant frequency architectures by preventing sub-harmonic oscillations at duty cycles greater than 50%. It is accomplished internally by adding a compensating ramp to the inductor current signal. Normally, the maximum inductor peak current is reduced when slope compensation is added. In the RT8015, however, separated inductor current signals are used to monitor over current condition. This keeps the maximum output current relatively constant regardless of duty cycle.

### Short-Circuit Protection

When the output is shorted to ground, the inductor current decays very slowly during a single switching cycle. A current runaway detector is used to monitor inductor current. As current increasing beyond the control of current loop, switching cycles will be skipped to prevent current runaway from occurring.

## Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, VDD, PVDD ---------- –0.3V to 6V
- LX Pin Switch Voltage ---------- –0.3V to (PVDD + 0.3V)
- Other I/O Pin Voltages ---------- –0.3V to (VDD + 0.3V)
- LX Pin Switch Current ---------- 4A
- Power Dissipation, $P_D$ @ $T_A$ = 25°C
  SOP-8 (Exposed Pad) ---------- 1.33W
- Package Thermal Resistance (Note 4)
  SOP-8 (Exposed Pad), $\theta_{JA}$ ---------- 75°C/W
  SOP-8 (Exposed Pad), $\theta_{JC}$ ---------- 15°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 2)
  HBM (Human Body Mode) ---------- 2kV
  MM (Machine Mode) ---------- 200V

## Recommended Operating Conditions (Note 3)

- Supply Input Voltage ---------- 2.6V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

## Electrical Characteristics

($V_{DD}$ = 3.3V, $T_A$ = 25°C, unless otherwise specified)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Input Voltage Range | $V_{DD}$ | | 2.6 | -- | 5.5 | V |
| Feedback Voltage | $V_{FB}$ | | 0.784 | 0.8 | 0.816 | V |
| DC Bias Current | | Active , $V_{FB}$ = 0.78V, Not Switching | -- | 460 | -- | μA |
| | | Shutdown | -- | -- | 1 | μA |
| Output Voltage Line Regulation | | $V_{IN}$ = 2.7V to 5.5V | -- | 0.04 | -- | %/V |
| Output Voltage Load Regulation | | 0A < $I_{LOAD}$ < 2A | -- | 0.25 | -- | % |
| Error Amplifier Transconductance | $g_m$ | | -- | 800 | -- | μs |
| Current Sense Transresistance | $R_T$ | | -- | 0.4 | -- | Ω |
| Power Good Range | | | -- | ±12.5 | ±15 | % |
| Power Good Pull-Down Resistance | | | -- | -- | 120 | Ω |
| Switching Frequency | | $R_{OSC}$ = 332k | 0.8 | 1 | 1.2 | MHz |
| | | Switching Frequency | 0.3 | -- | 4 | MHz |
| Sync Frequency Range | | | 0.3 | -- | 4 | MHz |

*To be continued*

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Switch On Resistance, High | $R_{PMOS}$ | $I_{SW}$ = 0.5A | -- | 110 | 160 | mΩ |
| Switch On Resistance, Low | $R_{NMOS}$ | $I_{SW}$ = 0.5A | -- | 110 | 170 | mΩ |
| Peak Current Limit | $I_{LIM}$ | | 2.2 | 3.2 | -- | A |
| Under Voltage Lockout Threshold | | $V_{DD}$ Rising | -- | 2.4 | -- | V |
| | | $V_{DD}$ Falling | -- | 2.3 | -- | V |
| Shutdown Threshold | | | -- | $V_{IN}$ – 0.7 | $V_{IN}$ – 0.4 | V |

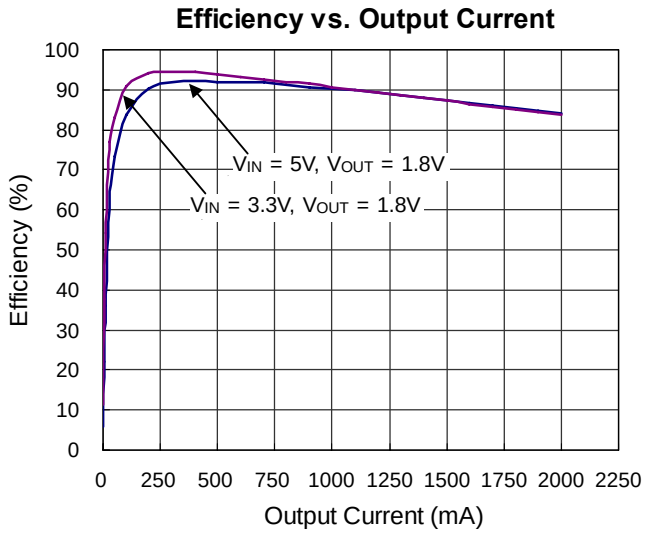
**Note 1.** Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

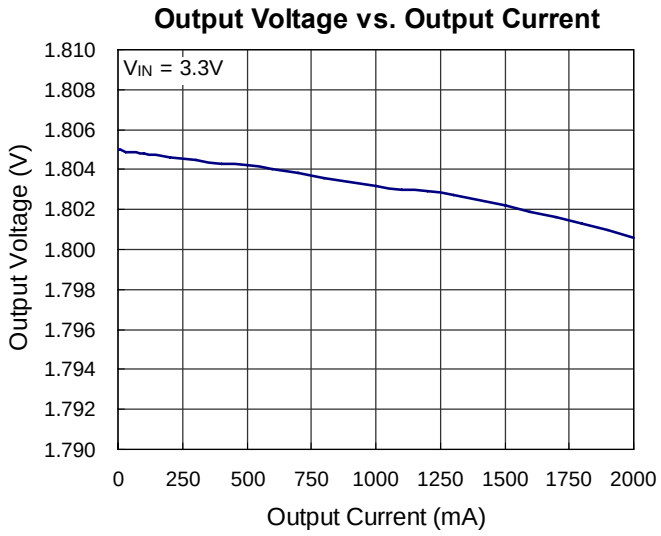
**Note 2.** Devices are ESD sensitive. Handling precaution recommended.

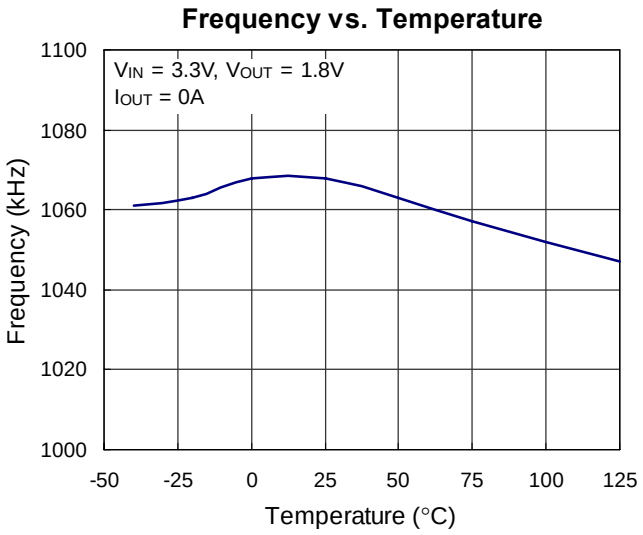
**Note 3.** The device is not guaranteed to function outside its operating conditions.

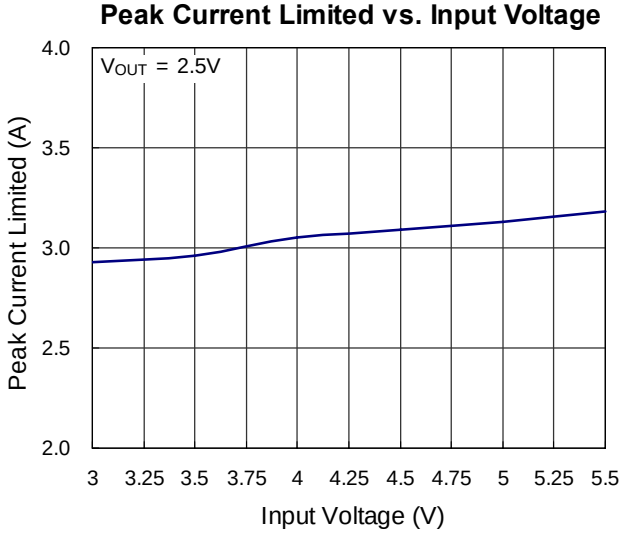
**Note 4.** $\theta_{JA}$ is measured in the natural convection at $T_A$ = 25°C on 4-layers high effective thermal conductivity test board of JEDEC 51-7 thermal measurement standard. The case point of $\theta_{JC}$ is on the expose pad for SOP-8 (Exposed Pad) package.

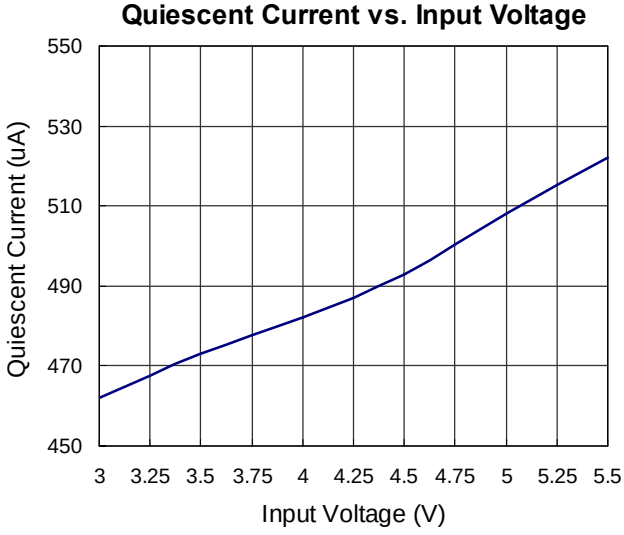
## Typical Operating Characteristics

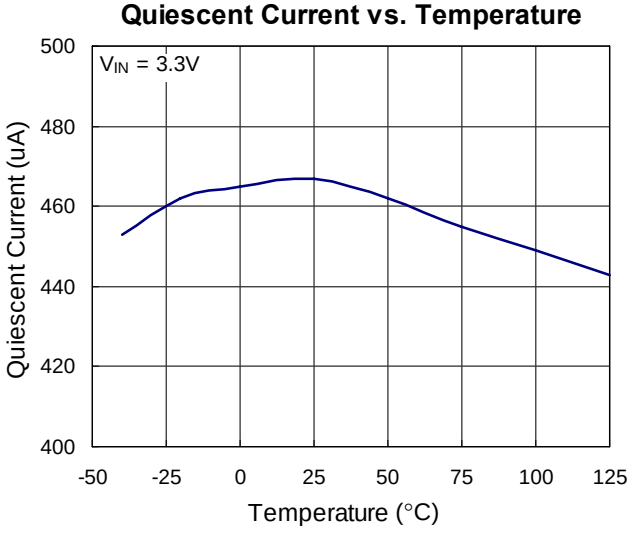


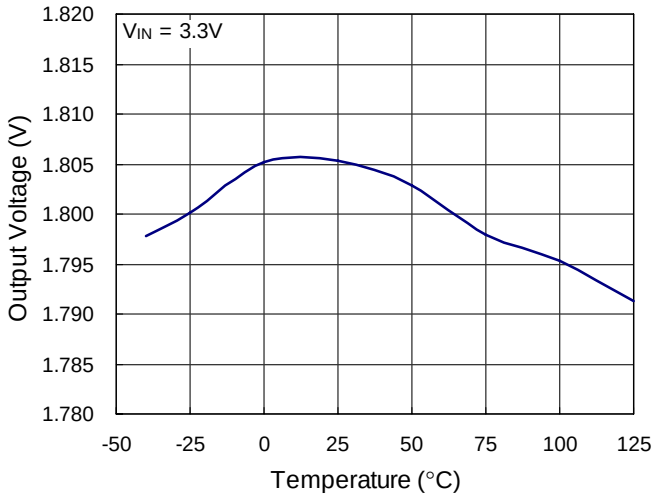



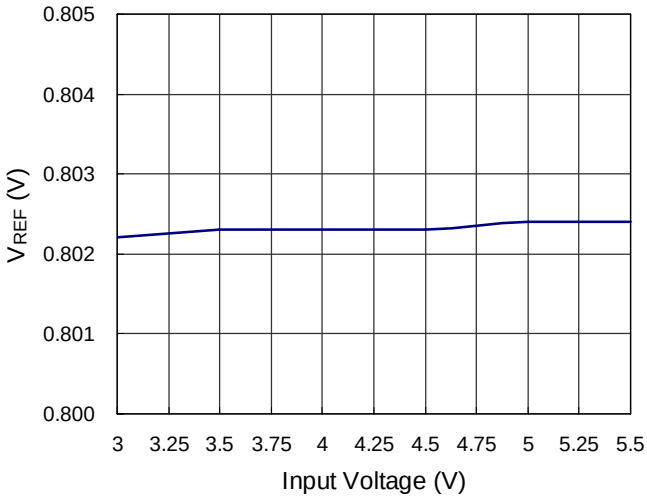



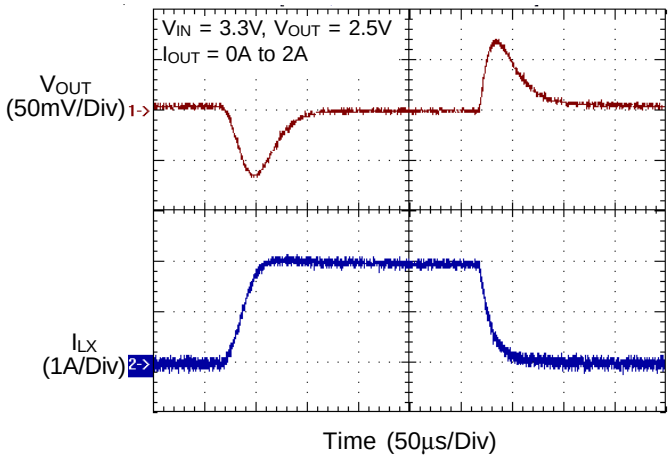
**Output Voltage vs. Temperature**




**$V_{REF}$ vs. Input Voltage**




**Load Transient Response**

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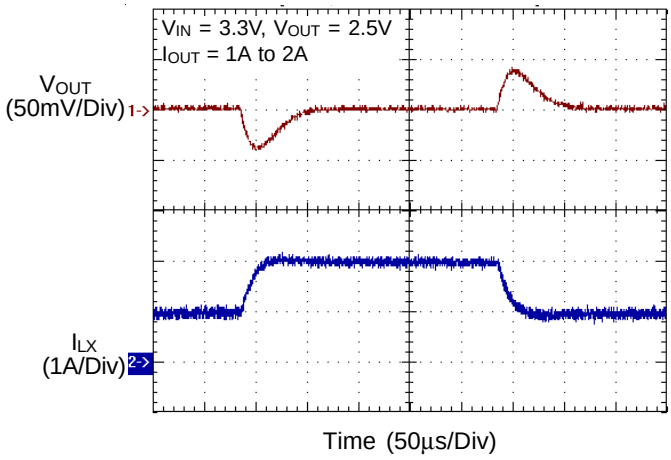
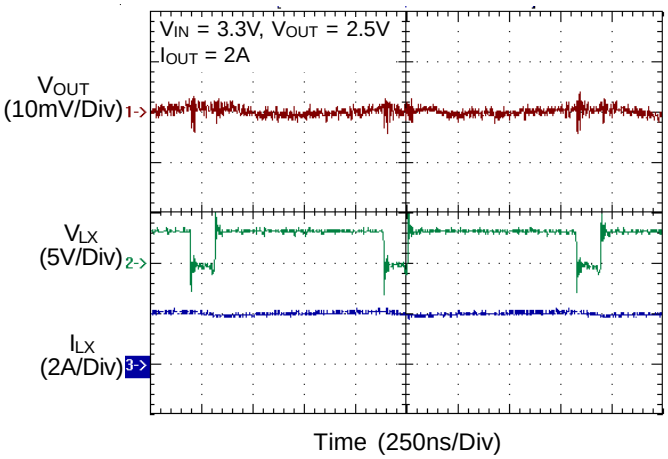
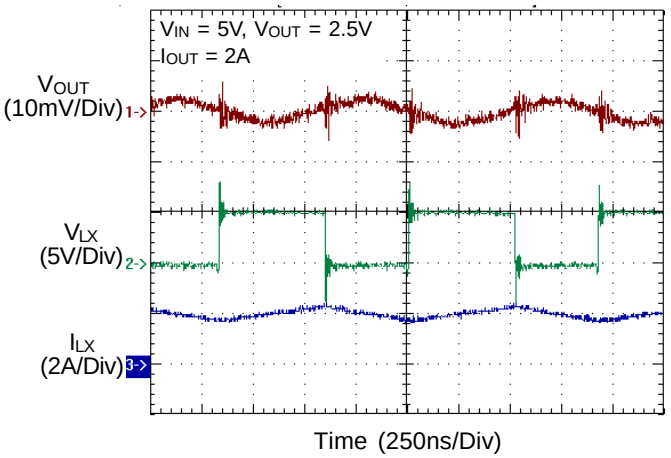


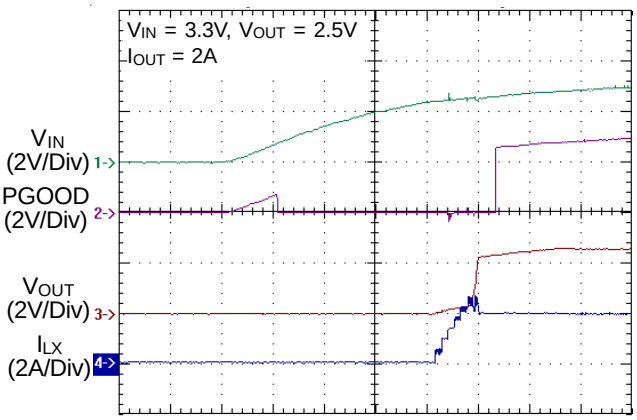

**Output Ripple**



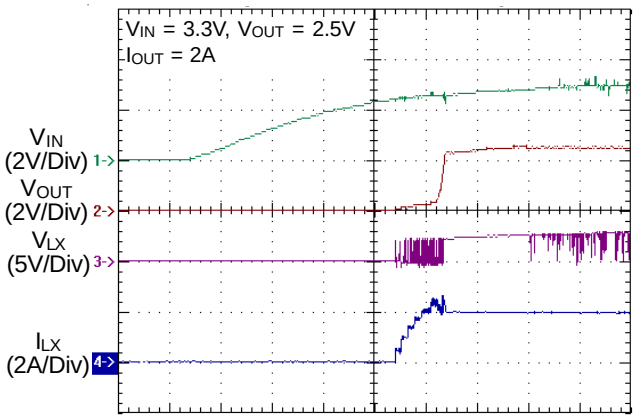

**Output Ripple**



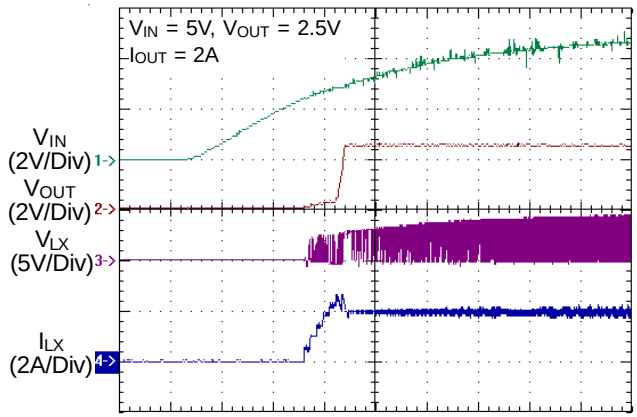
### Power Good



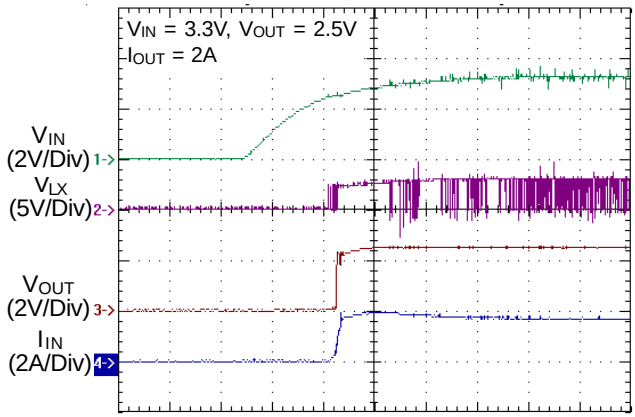

### Power On & Inductor Current




### Power On & Inductor Current




### Soft Start and Inrush Current

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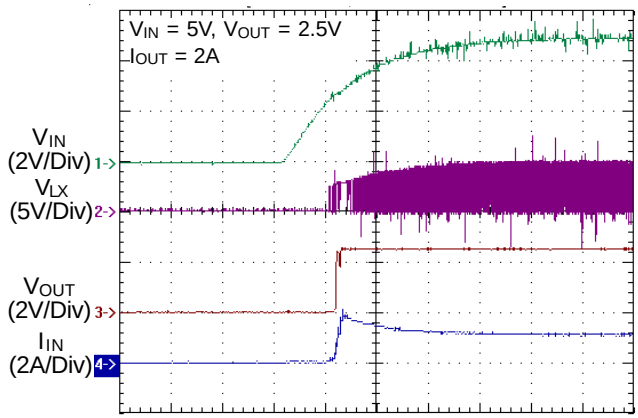


## Application Information

The basic RT8015 application circuit is shown in Typical Application Circuit. External component selection is determined by the maximum load current and begins with the selection of the inductor value and operating frequency followed by $C_{IN}$ and $C_{OUT}$.

### Operating Frequency

Selection of the operating frequency is a tradeoff between efficiency and component size. High frequency operation allows the use of smaller inductor and capacitor values. Operation at lower frequency improves efficiency by reducing internal gate charge and switching losses but requires larger inductance and/or capacitance to maintain low output ripple voltage.

The operating frequency of the RT8015 is determined by an external resistor that is connected between the RT pin and ground. The value of the resistor sets the ramp current that is used to charge and discharge an internal timing capacitor within the oscillator. The RT resistor value can be determined by examining the frequency vs. RT curve. Although frequencies as high as 4MHz are possible, the minimum on-time of the RT8015 imposes a minimum limit on the operating duty cycle. The minimum on-time is typically 110ns. Therefore, the minimum duty cycle is equal to 100 x 110ns x f(Hz).

### Inductor Selection

For a given input and output voltage, the inductor value and operating frequency determine the ripple current. The ripple current $\Delta I_L$ increases with higher $V_{IN}$ and decreases with higher inductance.

$$\Delta I_L = \left[\frac{V_{OUT}}{f \times L}\right]\left[1 - \frac{V_{OUT}}{V_{IN}}\right]$$

Having a lower ripple current reduces the ESR losses in the output capacitors and the output voltage ripple. Highest efficiency operation is achieved at low frequency with small ripple current. This, however, requires a large inductor. A reasonable starting point for selecting the ripple current is $\Delta I = 0.4(I_{MAX})$. The largest ripple current occurs at the highest $V_{IN}$. To guarantee that the ripple current stays below a specified maximum, the inductor value should be chosen according to the following equation :

$$L = \left[\frac{V_{OUT}}{f \times \Delta I_{L(MAX)}}\right]\left[1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right]$$

The transition from low current operation begins when the peak inductor current falls below the minimum peak current. Lower inductor values result in higher ripple current which causes this to occur at lower load currents. This causes a dip in efficiency in the upper range of low current operation.

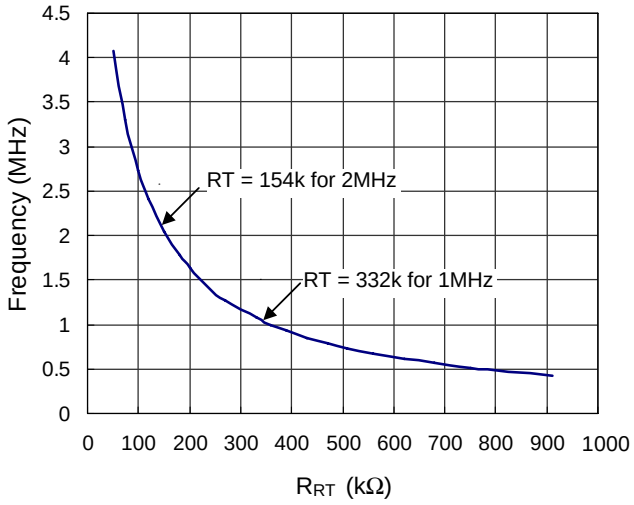



Figure 1

### Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite or mollypermalloy cores. Actual core loss is independent of core size for a fixed inductor value but it is very dependent on the inductance selected. As the inductance increases, core losses decrease. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates “hard”, which means that inductance collapses abruptly when the peak design current is exceeded.

This result in an abrupt increase in inductor ripple current and consequent output voltage ripple.

Do not allow the core to saturate!

Different core materials and shapes will change the size/ current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate energy but generally cost more than powdered iron core inductors with similar characteristics. The choice of which style inductor to use mainly depends on the price vs. size requirements and any radiated field/EMI requirements.

### $C_{IN}$ and $C_{OUT}$ Selection

The input capacitance, $C_{IN}$, is needed to filter the trapezoidal current at the source of the top MOSFET. To prevent large ripple voltage, a low ESR input capacitor sized for the maximum RMS current should be used. RMS current is given by :

$$I_{RMS} = I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required.

Several capacitors may also be paralleled to meet size or height requirements in the design.

The selection of $C_{OUT}$ is determined by the effective series resistance (ESR) that is required to minimize voltage ripple and load step transients, as well as the amount of bulk capacitance that is necessary to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response as described in a later section. The output ripple, $\Delta V_{OUT}$, is determined by :

$$\Delta V_{OUT} \leq \Delta I_L \left[ ESR + \frac{1}{8fC_{OUT}} \right]$$

The output ripple is highest at maximum input voltage since $\Delta I_L$ increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR but have lower capacitance density than other types. Tantalum capacitors have the highest capacitance density but it is important to only use types that have been surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR but can be used in cost-sensitive applications provided that consideration is given to ripple current ratings and long term reliability. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can also lead to significant ringing.

### Using Ceramic Input and Output Capacitors

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, $V_{IN}$. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at $V_{IN}$ large enough to damage the part.

### Output Voltage Programming

The output voltage is set by an external resistive divider according to the following equation :

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right)$$

where $V_{REF}$ equals to 0.8V typical.

The resistive divider allows the FB pin to sense a fraction of the output voltage as shown in Figure 2.

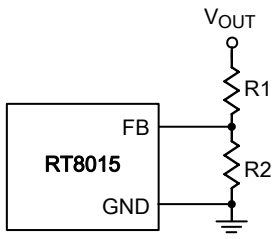



Figure 2. Setting the Output Voltage

### Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Efficiency can be expressed as :

Efficiency = 100% – (L1+ L2+ L3+ ...) where L1, L2, etc. are the individual losses as a percentage of input power. Although all dissipative elements in the circuit produce losses, two main sources usually account for most of the losses: $V_{DD}$ quiescent current and $I^2R$ losses.

The $V_{DD}$ quiescent current loss dominates the efficiency loss at very low load currents whereas the $I^2R$ loss dominates the efficiency loss at medium to high load currents. In a typical efficiency plot, the efficiency curve at very low load currents can be misleading since the actual power lost is of no consequence.

1. The $V_{DD}$ quiescent current is due to two components : the DC bias current as given in the electrical characteristics and the internal main switch and synchronous switch gate charge currents. The gate charge current results from switching the gate capacitance of the internal power MOSFET switches. Each time the gate is switched from high to low to high again, a packet of charge $\Delta Q$ moves from $V_{DD}$ to ground. The resulting $\Delta Q/\Delta t$ is the current out of $V_{DD}$ that is typically larger than the DC bias current. In continuous mode, $I_{GATECHG} = f(QT+QB)$ where QT and QB are the gate charges of the internal top and bottom switches.

Both the DC bias and gate charge losses are proportional to $V_{DD}$ and thus their effects will be more pronounced at higher supply voltages.

2. $I^2R$ losses are calculated from the resistances of the internal switches, RSW and external inductor RL. In continuous mode the average output current flowing through inductor L is "chopped" between the main switch and the synchronous switch. Thus, the series resistance looking into the LX pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (D) as follows :

RSW = $R_{DS(ON)}$TOP x D + $R_{DS(ON)}$BOT x (1"D) The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus, to obtain $I^2R$ losses, simply add RSW to RL and multiply the result by the square of the average output current. Other losses including $C_{IN}$ and $C_{OUT}$ ESR dissipative losses and inductor core losses generally account for less than 2% of the total loss.

### Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, $V_{OUT}$ immediately shifts by an amount equal to $\Delta I_{LOAD(ESR)}$, where ESR is the effective series resistance of $C_{OUT}$. $\Delta I_{LOAD}$ also begins to charge or discharge $C_{OUT}$ generating a feedback error signal used by the regulator to return $V_{OUT}$ to its steady-state value. During this recovery time, $V_{OUT}$ can be monitored for overshoot or ringing that would indicate a stability problem. The COMP pin external components and output capacitor shown in Typical Application Circuit will provide adequate compensation for most applications.

### Thermal Considerations

For continuous operation, do not exceed absolute maximum operation junction temperature 125°C.

The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junctions to ambient. The maximum power dissipation can be calculated by following formula:

$P_{D(MAX)} = ( T_{J(MAX)} – T_A ) / \theta_{JA}$

Where $T_{J(MAX)}$ is the maximum operation junction temperature 125°C, $T_A$ is the ambient temperature and the $\theta_{JA}$ is the junction to ambient thermal resistance.

For recommended operating conditions specification of RT8015, where $T_{J(MAX)}$ is the maximum junction temperature of the die (125°C) and $T_A$ is the maximum ambient temperature. The junction to ambient thermal resistance for SOP-8 (Exposed Pad) package is 75°C/W on the standard JEDEC 51-7 (4 layers, 2S2P) thermal test board. The copper thickness is 2oz. The maximum power dissipation at $T_A$ = 25°C can be calculated by following formula:

$P_{D\ (MAX)}$ = (125°C – 25°C) / (75°C/W) = 1.33W (SOP-8 Exposed Pad on the minimum layout)

### Layout Considerations

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance $\theta_{JA}$. For RT8015 package, the Figure 3 of de-rating curves allows the designer to see the effect of rising ambient temperature on the maximum power allowed.

The thermal resistance $\theta_{JA}$ of SOP-8 (Exposed Pad) is determined by the package design and the PCB design. However, the package design had been designed. If possible, it' s useful to increase thermal performance by the PCB design. The thermal resistance $\theta_{JA}$ can be decreased by adding a copper under the exposed pad of SOP-8 (Exposed Pad) package.

As shown in Figure 4, the amount of copper area to which the SOP-8 (Exposed Pad) is mounted affects thermal performance. When mounted to the standard SOP-8 (Exposed Pad) pad (Figure 4.a), $\theta_{JA}$ is 75°C/W. Adding copper area of pad under the SOP-8 (Exposed Pad) (Figure 4.b) reduces the $\theta_{JA}$ to 64°C/W. Even further, increasing the copper area of pad to 70mm$^2$ (Figure 4.e) reduces the $\theta_{JA}$ to 49°C/W.

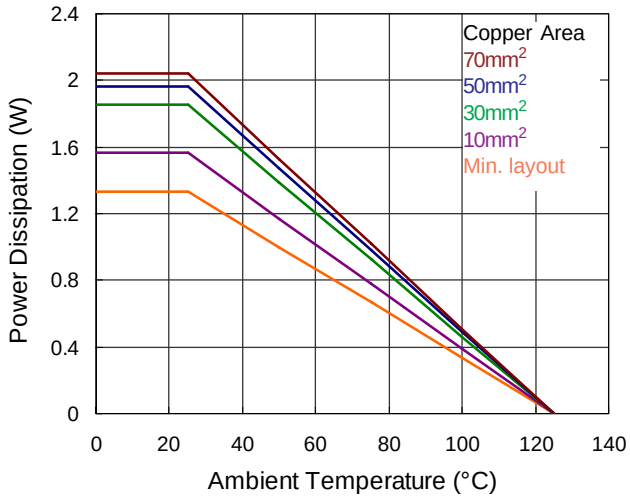
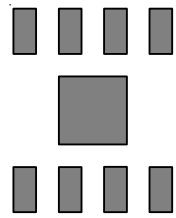
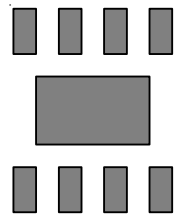


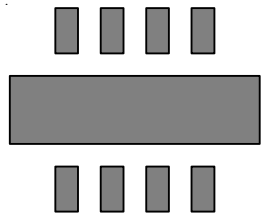

Figure 3. Derating Curve for Package



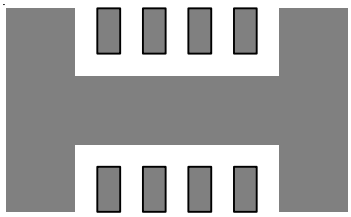
(a) Copper Area = (2.3 x 2.3) mm$^2$, $\theta_{JA}$ = 75°C/W



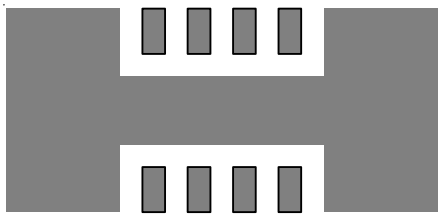
(b) Copper Area = 10mm$^2$, $\theta_{JA}$ = 64°C/W



(c) Copper Area = 30mm$^2$, $\theta_{JA}$ = 54°C/W



(d) Copper Area = 50mm$^2$, $\theta_{JA}$ = 51°C/W



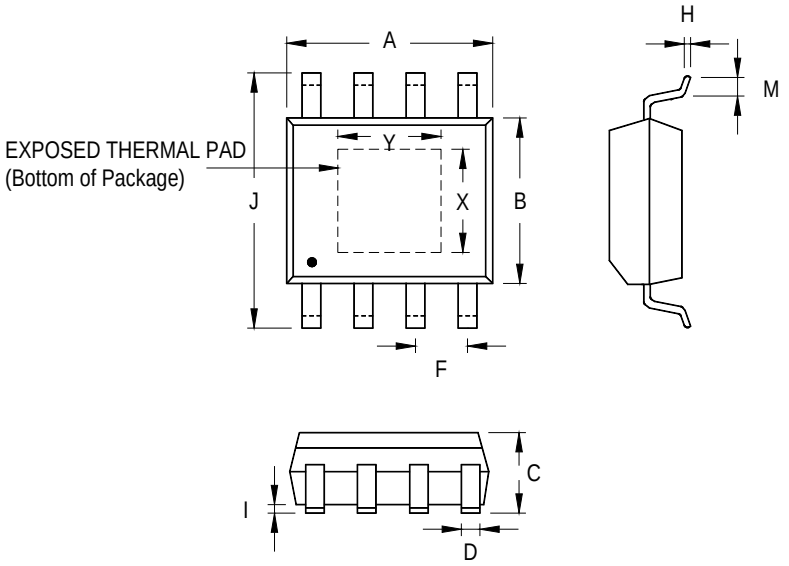
(e) Copper Area = 70mm$^2$, $\theta_{JA}$ = 49°C/W

Figure 4. Thermal Resistance vs. Copper Area Layout Thermal Design

## Datasheet Revision History

| Version | Data | Page No. | Item | Description |
|---|---|---|---|---|
| 00C | | | | first edition |
| 01C | 2006/9/11 | | Layout Guide<br>Functional Pin Description<br>Application Information | Modify |
| 02C | 2006/10/12 | | Outline Information | Modify |
| 03C | 2007/2/8 | | | Modify Logo |

## Outline Information




| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 4.801 | 5.004 | 0.189 | 0.197 |
| B | 3.810 | 4.000 | 0.150 | 0.157 |
| C | 1.346 | 1.753 | 0.053 | 0.069 |
| D | 0.330 | 0.510 | 0.013 | 0.020 |
| F | 1.194 | 1.346 | 0.047 | 0.053 |
| H | 0.170 | 0.254 | 0.007 | 0.010 |
| I | 0.000 | 0.152 | 0.000 | 0.006 |
| J | 5.791 | 6.200 | 0.228 | 0.244 |
| M | 0.406 | 1.270 | 0.016 | 0.050 |
| X | 1.900 | 2.700 | 0.075 | 0.106 |
| Y | 1.900 | 3.600 | 0.075 | 0.142 |

**8-Lead SOP (Exposed Pad) Plastic Package**

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