SmartJitter™ Multi-Mode Flyback Controller

General Description

The RT7740 series is an enhanced high-efficiency multi-mode PWM flyback controller, incorporating Richtek's proprietary SmartJitter™ technology. The innovative SmartJitter™ technology can reduce EMI emissions of a switch-mode power supply in green mode as well as eliminate output ripple due to frequency jittering. Also, the RT7740 series features a multi-mode control scheme, operating from continuous-conduction mode (CCM) to discontinuous-conduction mode (DCM) with valley switching, to achieve high efficiency and optimal performance.

The RT7740 is a current-mode PWM controller for flyback converters. It integrates comprehensive and programmable protection features, which include propagation delay compensation, output over-voltage protection (OVP), external over-temperature protection (OTP), and bulk-capacitor brown-in/brown-out protection. With the above features, the RT7740 enables a cost-effective and compact design for a wide range of AC-DC conversion applications. It is available in a SOT-23-6 package.

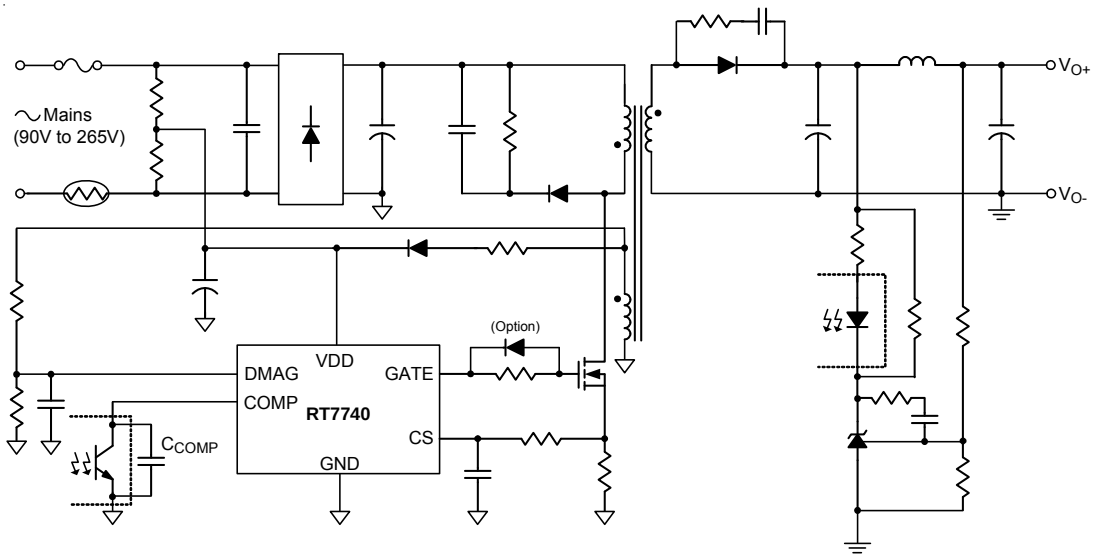
Features

- **Proprietary SmartJitter™ Technology**
  - **Reducing EMI Emissions of SMPS**
  - **Eliminating Frequency-Jittering-Induced Output Ripple**
- **Operating in Continuous-Conduction Mode (CCM), Discontinuous-Conduction Mode (DCM), DCM with Valley-Switching**
- **Ultra-low Start-Up Current (< 3μA)**
- **Accurate Over-Current Protection (OCP)**
- **Programmable Line Compensation**
- **Programmable Output Over-Voltage Protection**
- **Programmable External Over-Temperature Protection**
- **Programmable Bulk-Capacitor Brown-In/Brown-Out Protection**
- **Driver Capability : 250mA/–400mA**
- **High Noise Immunity**

Applications

- Switching AC-DC Adapter
- NB Adapter
- TV/Monitor Standby Power
- PC Peripherals

Simplified Application Circuit



Ordering Information

RT7740□□□□

- Package Type
  E : SOT-23-6
- Lead Plating System
  G : Green (Halogen Free and Pb Free)
- RT7740 Version
  (Refer to Version Table)

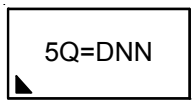
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

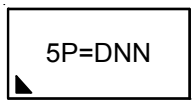
Marking Information

RT7740GAGE



5Q= : Product Code
DNN : Date Code

RT7740GHGE



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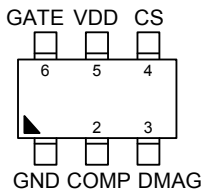
Pin Configuration

(TOP VIEW)



SOT-23-6

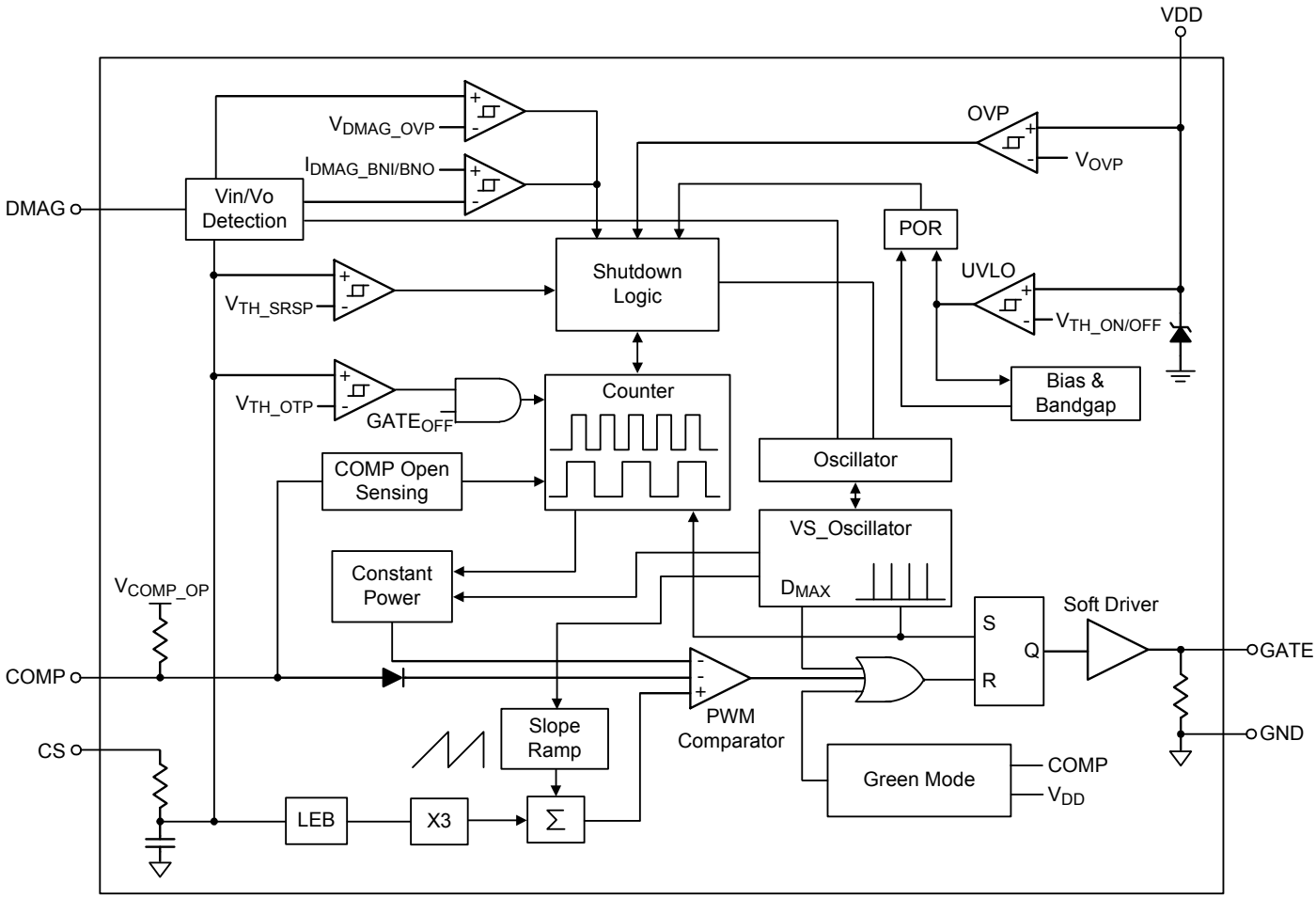
RT7740 Version Table

Version	RT7740GA	RT7740GH
Normal-Mode Frequency (f_{NOR})	65kHz	100kHz
OCP Delay Time @ f_{NOR}	63ms	41ms
DMAG UVP Delay Time @ 0.5 x f_{NOR}	31.5ms	20.5ms
Brown-Out Delay Time @ f_{NOR}	63ms	41ms
VDD OVP	Auto-Recovery	Auto-Recovery
DMAG OVP	Auto-Recovery	Auto-Recovery
DMAG UVP	Auto-Recovery	Auto-Recovery
Over-Current Protection	Auto-Recovery	Auto-Recovery
CS Pin Open-Circuit Protection	Auto-Recovery	Auto-Recovery
CS Pin Short-Circuit Protection	Auto-Recovery	Auto-Recovery
External OTP	Auto-Recovery	Auto-Recovery

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	GND	Ground.
2	COMP	Feedback input. Connect an opto-coupler from the COMP pin to GND to close the control loop to achieve output voltage regulation.
3	DMAG	Demagnetization input. Input and output voltages are sensed from the auxiliary winding.
4	CS	Current sense input. The current sense resistor, connected from the CS pin to GND, is used to set current limit for the power system.
5	VDD	Supply input voltage. The controller is enabled when the VDD voltage exceeds V_{TH_ON} and is disabled when the VDD voltage drops below V_{TH_OFF}.
6	GATE	Gate driver output.

Functional Block Diagram



Operation

Multi-Mode PWM

The RT7740 is a multi-mode PWM controller and features an internal oscillator to provide a PWM frequency for the system to operate in CCM/DCM. As the load decreases, the system will enter DCM with valley switching. In light load or no load condition, the controller will enter green mode. The RT7740 provides a multi-mode control to optimize performance under different load conditions.

SmartJitter™ Technology

In general PWM controllers, frequency jittering scheme is usually adopted to spread frequency spectrum in order to alleviate EMI problems. However, due to inherent operating characteristics of valley switching mode and green mode, the frequency spectrum in high line conditions or in deeper extended valley switching conditions cannot be spread wide enough as expected so that the targeted frequency jittering range cannot be achieved, which therefore degrades suppression of the EMI emissions.

The RT7740 incorporates RICHTEK's proprietary SmartJitter™ technology to optimize the frequency jittering range. The innovative SmartJitter™ technology can reduce EMI emissions of a switch-mode power supply in all operation conditions as well as output ripple as a consequence of frequency jittering.

Oscillator

During normal-mode operation, the built-in oscillator runs at a frequency, 65 kHz, with a feature of frequency jittering. Its frequency jittering range Δf is in percentage of the oscillator frequency; that is, Δf is proportional to the oscillator frequency. t_{JIT} is the frequency jittering repetition period.

Leading-Edge Blanking (LEB)

Each time when the MOSFET is turned on, an initial spike, induced by the parasitic capacitances, inevitably appears on the current-sense signal. This spike may falsely trigger the PWM comparator. In the RT7740, a leading-edge blanking time t_{LEB} is provided to prevent the MOSFET from being prematurely turned off by the spike.

Gate Driver

A totem-pole gate driver is designed to meet the requirements for both EMI and efficiency in low-power applications. An internal pull-down circuit is included to prevent the external MOSFET from being falsely turned on when V_{DD} is too low and an under-voltage lockout (UVLO) event is triggered.

Demagnetization Sensing

Through a resistive divider, the DMAG pin senses input voltage at the bulk capacitor, and output voltage of the power stage, which are coupled to the auxiliary winding during the MOSFET on-time and off-time alternatively. By programming the resistors at the DMAG pin, the RT7740 implements programmable output over-voltage protection and bulk-capacitor brown-in and brown-out protection.

CS Pin Open-Circuit Protection

If the CS pin is open-circuited or unconnected, a fault condition is assumed and the controller will stop operating within a few cycles.

VDD Over-Voltage Protection

Output voltage of the power system, coupled to the auxiliary winding, can be sensed via the VDD pin. If the sensed VDD voltage exceeds VDD OVP threshold voltage V_{OVP}, the controller will be shut down after a deglitch delay.

Feedback Loop Open-Circuit and Opto-Coupler Short-Circuit Protection

If the feedback loop of the converter output becomes open or the opto-coupler emitter diode shorts out, no feedback signal will be fed to the controller. To prevent this potential failure condition, VDD over-voltage protection, DMAG over-voltage protection, or over-current protection functions will be triggered, depending on whichever occurs first.

Output Short-Circuit Protection

The RT7740 uses the DMAG pin to sense the output voltage of the power stage to implement output short-circuit protection. When an output short-circuit condition occurs, especially at high line input voltages, this protection can minimize power loss and thermal stress.

Secondary Rectifier Short-Circuit Protection (SRSP)

When secondary rectifier short-circuit condition occurs during the MOSFET on-time, the main transformer becomes saturated and the primary-side current rate of rise is then limited only by the leakage inductance of the transformer, which is about a few percentage of the primary magnetizing inductance. Therefore, the current slope will be much higher than in normal operation. In high line condition, peak current through the MOSFET will become extremely high after over-current protection delay time elapses. To provide safer and better protection, the RT7740 will be shut down in a few cycles, as secondary rectifier short-circuit condition is detected.

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, VDD to GND ---------- –0.3V to 35V
- GATE to GND ---------- –0.3V to 16V
- DMAG, COMP, CS to GND ---------- –0.3V to 6.5V
- Power Dissipation, P_D @ T_A = 25°C
  SOT-23-6 ---------- 0.38W
- Package Thermal Resistance (Note 2)
  SOT-23-6, θ_{JA} ---------- 260.7°C/W
  SOT-23-6, θ_{JC} ---------- 135°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, VDD ---------- 12V to 25V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{DD} = 15V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VDD Section						
VDD Over-Voltage Protection Threshold Voltage	V_{OVP}		--	28	--	V
Turn-On Threshold Voltage	V_{TH_ON}			16.5	--	V
Turn-Off Threshold Voltage	V_{TH_OFF}		--	7	--	V
V_{DD} Holdup Mode Entry Voltage	V_{DD_ET}	V_{COMP} < 0.85V	--	8	--	V
V_{DD} Holdup Mode Exit Voltage	V_{DD_ED}	V_{COMP} < 0.85V	--	8.5	--	V
Start-Up Current	I_{DD_ST}	V_{DD} < V_{TH_ON} – 0.1V, T_A = –40°C to 85°C	--	--	3	μA
Operating Supply Current	I_{DD_OP1}	GATE pin open-circuit, V_{COMP} = 2V, I_{DMAG} = 200μA	--	850	--	μA
	I_{DD_OP2}	GATE pin open-circuit, V_{COMP} = 1.4V, I_{DMAG} = 200μA	--	800	--	
IDD Sinking Current for Auto-Recovery Mode	I_{DD_ARP}	During entering auto-recovery mode, T_A = –40°C to 85°C	--	550	--	μA

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Oscillator Section							
Normal-Mode PWM Frequency	f_{NOR}	V_{COMP} > V_{GM_ET}	RT7740GA	--	65	--	kHz
			RT7740GH	--	100	--	
Maximum Duty Cycle	D_{MAX}	f_{OSC} = 65kHz, RT7740GA		--	75	--	%
		f_{OSC} = 100kHz, RT7740GH		--	70	--	
Minimum Green-Mode Frequency	f_{GM_MIN}	V_{COMP} < V_{GM_ED}		21	25	29	kHz
PWM Frequency Jittering Range	Δf			--	±6	--	%
PWM Frequency Jittering Repetition Period	t_{JIT}	f_{OSC} = 65kHz, RT7740GA		--	15.8	--	ms
		f_{OSC} = 100kHz, RT7740GH		--	10.2	--	
Frequency Variation with VDD	Δf_{VDD}	V_{DD} = 10V to 23V		--	--	2	%
Frequency Variation with Temperature	Δf_T	T_A = −30°C to 105°C (Note 5)		--	5	--	%
COMP Input Section							
Open-Loop Voltage	V_{COMP_OP}	COMP pin open-circuit		--	3	--	V
COMP Pin Short Circuit Current	I_{ZERO}	V_{COMP} = 0V		--	150	--	μA
Over-Current Protection Delay Time	t_{D_OCP}	f_{OSC} = 65kHz, RT7740GA		--	63	--	ms
		f_{OSC} = 100kHz, RT7740GH		--	41	--	
Green-Mode Entry Voltage	V_{GM_ET}	I_{DMAG} < I_{DMAG_GMSW}		--	1.75	--	V
		I_{DMAG} > I_{DMAG_GMSW}		--	1.85	--	
Green-Mode Exit Voltage	V_{GM_ED}	I_{DMAG} < I_{DMAG_GMSW}	RT7740GA	--	1.6	--	V
			RT7740GH	--	1.55	--	
		I_{DMAG} > I_{DMAG_GMSW}	RT7740GA	--	1.7	--	
			RT7740GH	--	1.65	--	
Valley-Switching Turn-Off Threshold Voltage	V_{DIS_VS}	RT7740GA		--	1.7	--	V
		RT7740GH		--	1.65	--	
Current Sense Section							
Over-Current Protection Threshold Voltage	V_{CS_OCP}			--	0.4	--	V
Leading-Edge Blanking Time	t_{LEB}	(Minimum on-time)		--	475	--	ns
Internal Propagation Delay	t_{PD}	(Note 5)		--	50	--	ns
Secondary Rectifier Short-Circuit Protection Threshold Voltage	V_{TH_SRSP}	(Note 5)		--	1.1	--	V
External Over-Temperature Protection Threshold Voltage	V_{TH_OTP}			--	0.7	--	V

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
External Over-Temperature Protection Delay Time	t_{D_OTP}	f_{OSC} = 65kHz, RT7740GA		--	63	--	ms
		f_{OSC} = 100kHz, RT7740GH		--	41	--	
GATE Section							
Rising Time	t_R	C_L = 1nF		--	270	--	ns
Falling Time	t_F	C_L = 1nF		--	45	--	ns
Gate Output Clamp Voltage	V_{CLAMP}	V_{DD} = 23V		--	12	--	V
DMAG Section							
Over-Voltage Protection Threshold Voltage	V_{DMAG_OVP}			--	3.6	--	V
Over-Voltage Protection Blanking Time	t_{BLK_OVP}	V_{CS} = 0.36V; V_{COMP} < V_{DIS_VS}		--	2.9	--	μs
Under-Voltage Protection Threshold Voltage	V_{DMAG_UVP}	After $t_{D\_DMAGUVP}$, COMP pin open-circuit		--	0.6	--	V
Under-Voltage Protection Delay Time	$t_{D\_DMAGUVP}$	At start-up, 0.5 x f_{NOR}	RT7740GA	--	31.5	--	ms
			RT7740GH	--	20.5	--	
Brown-In Protection Threshold Current	I_{DMAG_BNI}			--	160	--	μA
Brown-Out Protection Threshold Current	I_{DMAG_BNO}			--	145	--	μA
Maximum Sourcing Current	I_{DMAG_MAX}	(Note5)		1.5	--	--	mA
Green Mode Switching Current	I_{DMAG_GMSW}			--	330	--	μA
Green Mode Switching Current Hysteresis	I_{GMSW_HYS}			--	7	--	μA
Brown-Out Protection Delay Time	t_{D_BNO}	f_{OSC} = 65kHz, RT7740GA		--	63	--	ms
		f_{OSC} = 100kHz, RT7740GH		--	41	--	

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

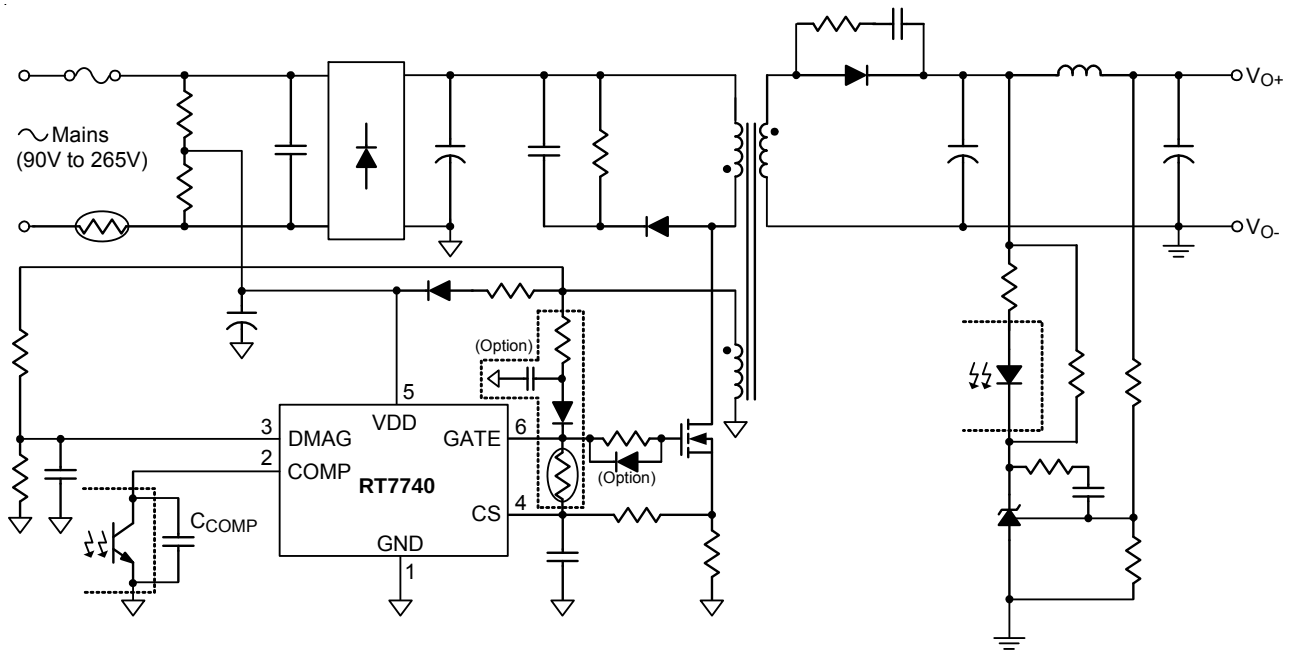
Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a low effective-thermal-conductivity single-layer test board on a JEDEC 51-3 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Guaranteed by design.

Typical Application Circuit



Application Information

The RT7740 is a multi-mode PWM flyback controller, which can automatically switch from CCM/DCM to DCM with valley-switching, depending on load conditions. As load decreases, the controller may enter into different modes, such as green mode, burst mode, and VDD holdup mode. The RT7740 can automatically switch among several control modes to optimize efficiency of power system when operating under various load conditions.

Line Compensation

The RT7740 provides line compensation to ensure constant output current limit I_{O_MAX} over a wide range of AC line input voltages, as shown in Figure 1.

For different power stage designs, the propagation delay may vary with the transformer inductances, parasitic capacitances of the MOSFET, or series resistances at the gate of the MOSFET. With the same design, however, the current overshoot caused by the propagation delay may become significant at high line, where the inductor current di/dt is higher. There is a significant difference between the overshoot at high input voltage and that at low input voltage, to the actual peak current.

To compensate such difference to achieve accurate over-current protection under different input line voltages, the RT7740 outputs a line compensation current on the CS pin to add an offset voltage proportional to the input voltage by adding a propagation delay resistor (R_{PDC}). The propagation delay differences due to different input line voltages can be compensated by adjusting the propagation delay resistor (R_{PDC}) or the propagation delay capacitor (C_{RC}) to keep output current limit as a constant across different line voltages.

To start with, R_{PDC} = 470Ω and C_{RC} = 100pF can be used as reasonable initial setting for line compensation. In Figure 2, curve (1) is an ideal output current limit curve for over-current protection, which remains constant from low line to high line input voltages. If the output current limit curve is like curve (2), the resistance R_{PDC} should be increased. However, if the output current limit curve is like curve (3), the capacitance C_{RC} should be increased. The output current limit I_{O_MAX} under different line voltages can be optimized by adjusting the propagation delay resistor (R_{PDC}) or the propagation delay capacitor (C_{RC}) to achieve accurate over-current protection.

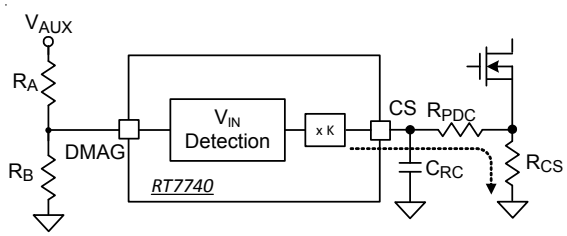


Figure 1. Functional Block Diagram of Line Compensation

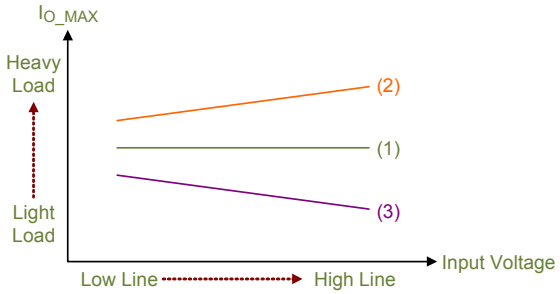


Figure 2. Output Current Limits for Over-Current Protection

External Over-Temperature Protection (External OTP)

The RT7740 includes programmable external over-temperature protection (External OTP), implemented with a fast diode and a resistive voltage divider, which consists of an external NTC resistor (R_{NTC}) to sense the power system temperature, as shown in Figure 3. During the MOSFET off-time, the auxiliary winding voltage V_{AUX} is constant, and the CS voltage is sampled as a fraction of the clamped voltage V_{AUX_CLAMP} and compared with the internal reference voltage to set the over-temperature protection threshold voltage. When the system temperature gets higher, the resistance of the NTC resistor will become smaller. By adjusting the value of the setting resistor (R_{SET}), the threshold temperature for over-temperature protection can be programmed. During the off-time, if the sampled CS voltage exceeds the External OTP threshold voltage V_{TH_OTP} and sustains for the External OTP delay time t_{D_OTP}, the controller will be shut down and the switching will be stopped. If the OTP condition is removed, the controller with auto-recovery option will

automatically resume operation. The design equation for the External OTP threshold voltage is expressed as below :

$$V_{TH\_OTP} = \left[(V_O + V_F) \times \frac{N_A}{N_S} - V_{F\_OTP} \right] \times \frac{R_{PDC} + R_{CS}}{R_{NTC\_OTP} + R_{SET} + R_{PDC} + R_{CS}},$$

where R_{NTC_OTP} is the NTC resistance at the threshold temperature for External OTP.

It is highly recommended to use a fast diode (diode capacitance (C_D) ≤ 5pF and reverse recovery time (t_{rr}) ≤ 50ns), ex.1N4148 or BAV21 series, for external OTP application to prevent the CS pin from wrong regulation or being damaged by the negative voltage spikes.

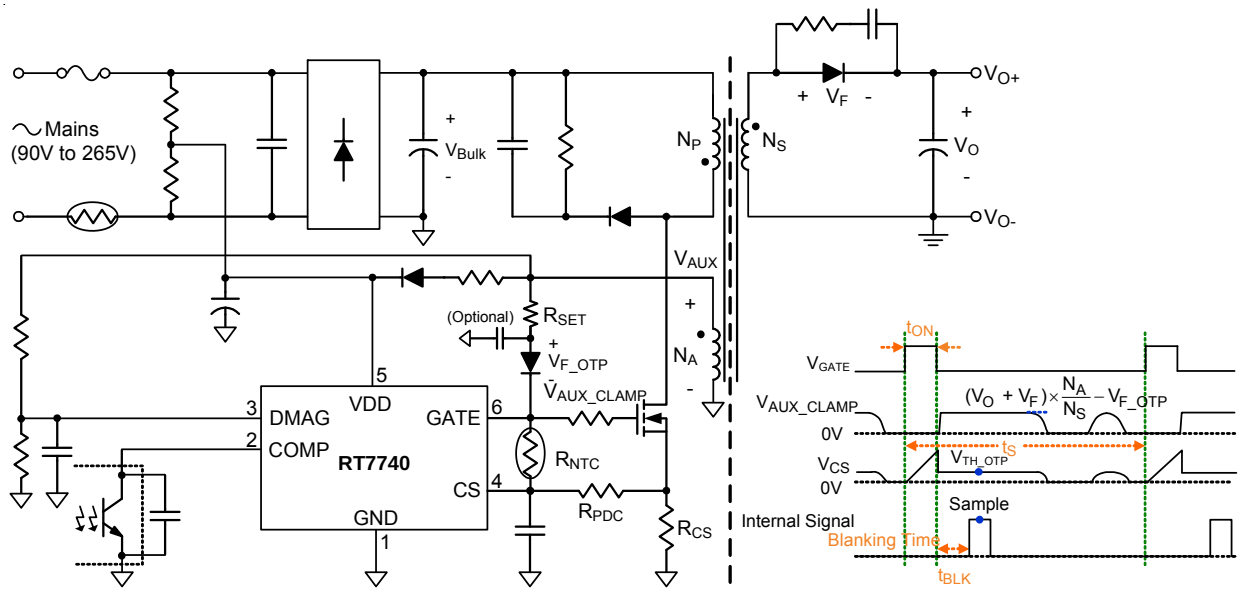


Figure 3. Application Circuit for External Over-Temperature Protection

Resistors at the DMAG Pin

During the MOSFET on-time, the auxiliary winding voltage is negative, and the RT7740 outputs a clamp current, proportional to the input line voltage, to clamp the DMAG voltage at 0.1V. The RT7740 has built-in characteristics, DMAG brown-in protection threshold current I_{DMAG_BNI} and a DMAG brown-out protection threshold current I_{DMAG_BNO}, for the DMAG pin. The bulk-capacitor brown-in and brown-out threshold voltages, V_{Bulk_BNI} and V_{Bulk_BNO}, can be programmed by adjusting R_A and R_B at the DMAG pin, as shown in Figure 4.

Once the brown-in/brown-out threshold voltage is set, the other one will be determined accordingly.

The bulk-capacitor brown-out threshold voltage V_{Bulk_BNO} can be obtained according to the following equation :

$$V_{Bulk\_BNO} = \frac{V_{Bulk\_BNI} \times I_{DMAG\_BNO}}{I_{DMAG\_BNI}}$$

When the MOSFET turns off, the DMAG pin senses the output voltage of the power stage across the auxiliary winding, with a ratio equal to the turns ratio of the auxiliary and secondary windings, and then scaled with the resistive divider R_A / R_B, as shown in Figure 4. The RT7740 can implement output over-voltage protection with the threshold of V_{O_OVP} by means of DMAG over-voltage protection with the threshold of V_{DMAG_OVP} :

$$\begin{cases} \dfrac{V_{Bulk\_BNI} \times N_A}{N_P} + 0.1 \over R_A + \dfrac{0.1}{R_B} = I_{DMAG\_BNI} \\ \dfrac{(V_{O\_OVP} + V_F) \times N_A}{N_S} \times \dfrac{R_B}{R_A + R_B} = V_{DMAG\_OVP} \end{cases}$$

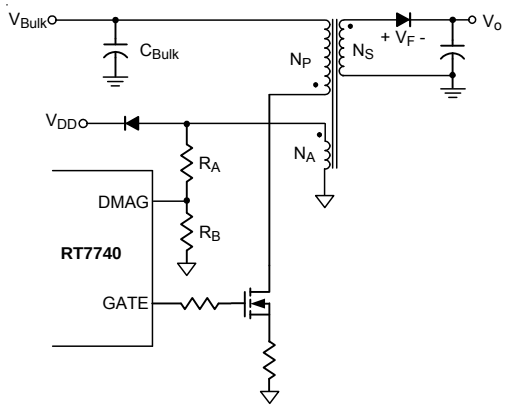


Figure 4. Design Resistors at the DMAG Pin

Adaptive Blanking Time

When the MOSFET just turns off, leakage inductance of the transformer and parasitic capacitance (C_{OSS}) of the MOSFET induces resonant oscillations on the DMAG pin, as shown in Figure 5. The resonant oscillations may cause the controller to falsely trigger DMAG over-voltage protection ($V_{DMAG} > V_{DMAG\_OVP}$), which thus fails to reflect actual output over-voltage fault condition ($V_O > V_{O\_OVP}$) so that the controller may not function properly. As load increases, the duration of the resonant oscillation may also increase. A small bypass capacitor, sized from 10pF to 47pF and placed as close to the DMAG pin as possible, is recommended to be added to suppress such noises on the DMAG pin. A larger bypass capacitor may cause the DMAG voltage to be phase-shifted too much for the MOSFET to be switched on at exact valley points.

Correspondingly, the RT7740 provides adaptive blanking time to prevent DMAG over-voltage protection from being falsely triggered. The built-in blanking time for over-voltage protection (t_{BLK_OVP}) varies with the system peak current limit (as V_{CS_PK}).The blanking time can be calculated with the following formula :

$$t_{BLK\_OVP} = 2\mu s + V_{CS\_PK} \times 2.5(\mu s/V),$$
if $f_{OSC} < 65kHz$

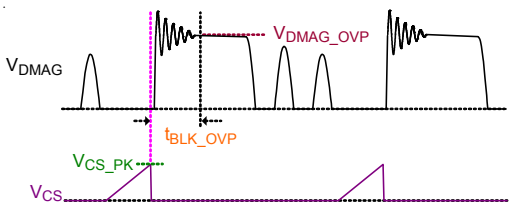


Figure 5. Resonant Oscillations On the DMAG Pin

Start-Up Circuit

To optimize power efficiency, bleeder resistors can be added to the start-up circuit, which not only can reduce power loss but can reset latched-mode protections faster. Figure 6 shows the curve for I_{DD} average current I_{DD_Avg} vs. bleeder resistance ($R_{Bleeder}$). The curve can be used to design bleeder resistance values.

During hiccup mode, the off-time duration is extended to minimize power loss and heat dissipation. During auto-recovery protection mode, the controller will sink a very small sinking current, I_{DD_ARP}. The start-up current at maximum AC line input voltage must be smaller than I_{DD_ARP} (Min). Otherwise, when the controller enters an auto-recovery protection mode, the VDD capacitor cannot be discharged to V_{TH_OFF} by the sinking current I_{DD_ARP} to restart the controller. The controller will then behave as in a latched-protection mode or even trigger the SCR of VDD.

CS Pin Short-Circuit Protection

The RT7740 provides CS pin short-circuit protection to protect a power supply unit (PSU). When the CS pin is shorted to GND or no CS signal is sensed, the gate driver will remain turned-on for a couple of cycles and then the system will be shut down. CS pin short-circuit protection can limit power consumption to protect the PSU during safety test. Since CS pin short-circuit protection is implemented by sensing the slope of the CS signal, the ratio of the current sense resistor and the transformer is therefore recommended to follow the following equation :

$$\frac{R_{CS}}{L_P} > \frac{2x10^4}{V_{Bulk\_BNO}} \left(\frac{\Omega}{H}\right)$$

where R_{CS} is the current sense resistance, L_P is primary magnetizing inductance of the transformer, and V_{Bulk_BNO} is the brown-out threshold voltage at the input bulk capacitor.

Over-Current Protection

The RT7740 implements a debounce time of 5 ms (f_{OSC} = 65kHz) for over-current protection to prevent false triggering. Once the rising CS voltage reaches V_{CS_OCP}, the controller starts counting an over-current protection

counter for an over-current protection delay time, t_{D_OCP}. During this period of time, if the CS voltage suddenly goes back below V_{CS_OCP} for a period of time longer than the debounce time 5 ms (f_{OSC} = 65kHz), the counter will be stopped and then reset. Otherwise, the counter will continue counting. When the system over-current condition occurs, the counter will count for the delay time t_{D_OCP} continuously to trigger over-current protection and then the RT7740 will cease switching.

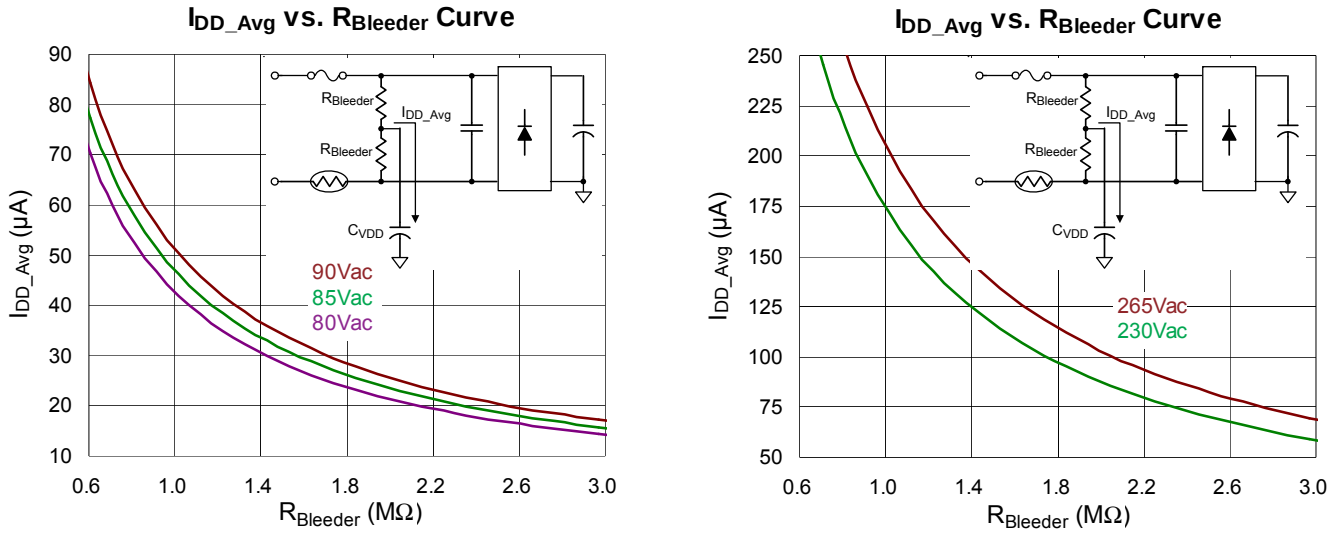


Figure 6. I_{DD_Avg} vs. $R_{Bleeder}$ Curve

VDD Discharge Time in Auto-Recovery Mode

Figure 7 shows the waveforms of the VDD voltage V_{DD} and the GATE voltage V_{GATE} during any auto-recovery protection mode (e.g., OCP). In this mode, the start-up resistors, VDD sinking current I_{DD_ARP} and VDD decoupling capacitance will affect the restart time. The VDD voltage discharge time t_{D_DISCHG} can be calculated by the following equation :

$$t_{D\_DISCHG} = \frac{C_{VDD} \times (V_{DD\_DISCHG} - V_{TH\_OFF})}{I_{DD\_ARP} - I_{START}}$$

where C_{VDD} is the VDD decoupling capacitor, V_{DD_DISCHG} is the initial VDD voltage after entering the auto-recovery mode, V_{TH_OFF} is the turn-off threshold voltage of the controller, I_{DD_ARP} is the sinking current of the VDD pin during auto-recovery protection mode, and I_{START} is the start-up current of the power system.

Please note that the start-up current at the maximum input voltage must be smaller than I_{DD_ARP} (Min). Otherwise, the VDD voltage can never reach V_{TH_OFF} to activate the next start-up sequence after entering the auto-recovery protection mode, and the system will operate as in latched-protection mode.

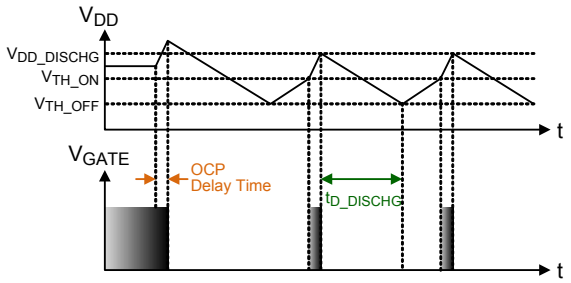


Figure 7. Auto Recovery Mode (e.g., OCP)

VDD Holdup Mode

VDD holdup mode is implemented to prevent VDD from dropping below the turn-off threshold voltage V_{TH_OFF} when the system operates under light load, no load, or fast load transient conditions. VDD holdup mode can help reduce the power loss caused by the start-up resistor, and can meet the requirement for the start time. However, compared to burst mode, VDD holdup mode consumes more

switching power loss. Hence, it is highly recommended that the system will not be designed to operate in this mode under light load or no load condition.

Output Short-Circuit Protection

The RT7740 uses the DMAG pin to sense the output voltage signal of the power stage to implement output short-circuit protection. If the signal goes outside of a certain range for regulation, the controller will react to the fault after a delay time ($t_{D\_DMAGUVP}$). When an output short-circuit condition occurs, especially at high line input voltages, this protection can minimize power loss and thermal stress.

Resistors at the GATE Pin

As the typical application circuit shown in Figure 8, a resistor R_G can be applied to mitigate ringing spikes induced by the gate drive loop. Therefore, the value of the resistor R_G should be chosen carefully to meet the requirements for both EMI and efficiency for applications.

The RT7740 has a built-in discharge resistor R_{ID}, internally connected from the GATE pin to GND, to prevent the MOSFET suffering from any uncertain condition. However, if the GATE pin is open-circuited, not connecting to the gate of the MOSFET, the MOSFET may be falsely triggered by the stored charge on the gate-to-drain parasitic capacitor C_{GD} of the MOSFET and then be damaged. Therefore, it is recommended to add an external discharge resistor R_{ED} between the gate of MOSFET and GND so that the charge stored on the parasitic capacitor C_{GD} can be discharged by the external discharge resistor and the MOSFET can be protected from being falsely triggered even if the RT7740 is not in place or GATE pin is open-circuited.

Feedback Resistor

To enhance efficiency at light load, the power loss caused by the feedback resistor, in parallel with the opto-coupler as shown in Figure 9, must be reduced. Since the current through the feedback resistor is very small, a shunt regulator (e.g. TL431), especially with its minimum regulated current, should be carefully chosen to ensure that the shunt regulator can still regulate the output voltage at such a small cathode current.

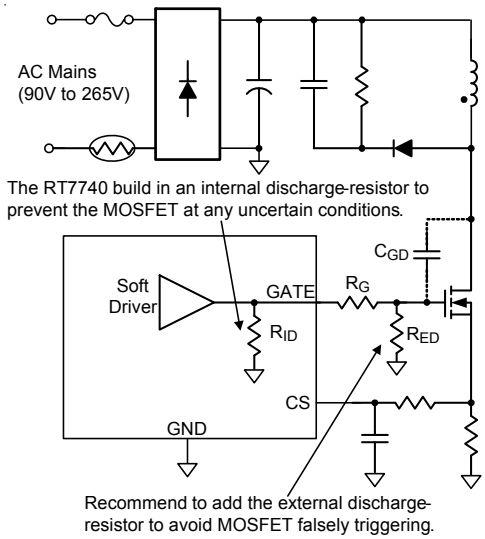


Figure 8. Resistors at the Gate Pin

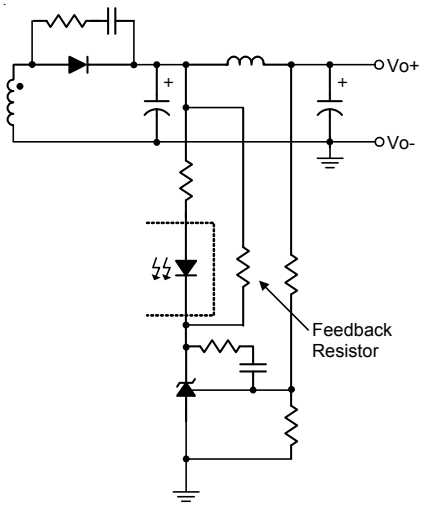


Figure 9. Feedback Resistor

Negative Voltage Spike on Each Pin

Any negative voltage which is less than –0.3V on each controller pin may cause a large injection current into the substrate to damage the controller or to falsely trigger the circuit. For example, the negative voltage spikes on the CS pin may result from poor PCB layout or the inductance of the current sense resistor, and therefore an R-C filter, as shown in Figure 10, is recommended to be added to prevent the CS pin from being damaged by the negative voltage spikes. During circuit design stage, proper PCB layout and component selection must be carefully devised and considered.

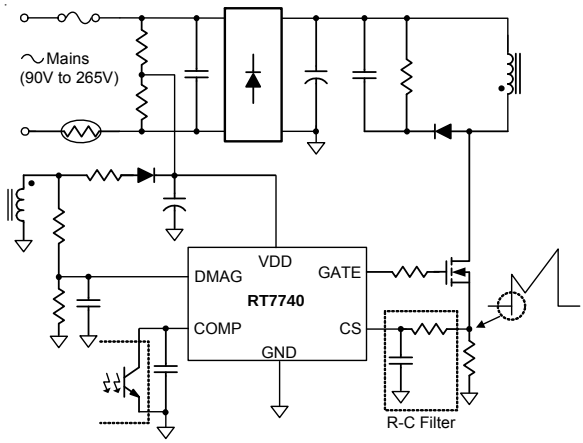


Figure 10. R-C Filter at the CS Pin

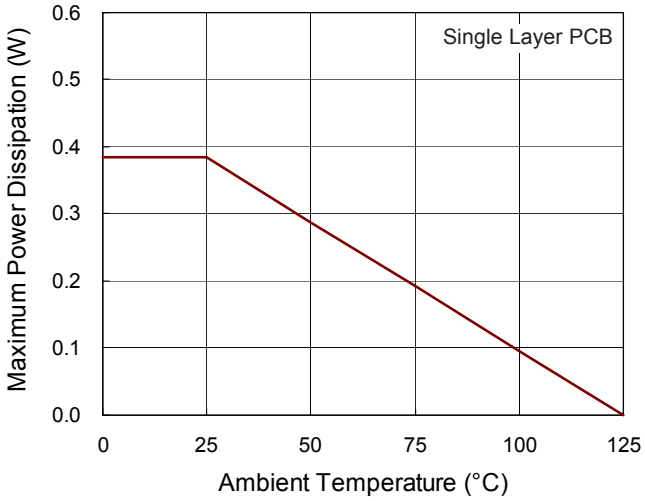


Figure 11. Derating Curve of Maximum Power Dissipation

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a SOT-23-6 package, the thermal resistance, θ_{JA}, is 260.7°C/W on a standard JEDEC 51-3 low effective-thermal-conductivity single-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C – 25°C) / (260.7°C/W) = 0.38W for a SOT-23-6 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 11 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

Layout Considerations

A proper PCB layout can alleviate unknown noise interference and EMI emission in a switch-mode power supply (SMPS). It is recommended to follow the following PCB layout guidelines when a switch-mode power supply is to be designed :

- The current path (1), starting from the bulk capacitor, the transformer, the MOSFET, the resistor R_{CS}, and back to the bulk capacitor, is a high-frequency and high-current loop. The loop should be as small as possible to decrease noise coupling, and should be kept away from other low-voltage traces, especially away from the control circuit paths of the controller.
- The current path (2), formed by the RCD snubber circuit, is also a high-frequency loop and should be kept as small as possible.
- The ground traces of the bulk capacitor (a), the MOSFET (b), the auxiliary winding (c), and the controller IC (d) should be separated to reduce noise, output ripple, and EMI emissions. Connect the ground traces of the MOSFET (b), the auxiliary winding (c), and the controller IC (d) together at the bulk capacitor ground (a). The areas of these ground traces should be large enough.
- The bypass capacitor should be placed as close to the IC as possible.

- In order to reduce the reflected trace inductance and EMI emissions, the trace length connecting the secondary winding, the output diode, and the output filter capacitor should be as short as possible. In addition, the copper areas at the anode and cathode of the diode must be large enough to ease sinking heat from the diode.

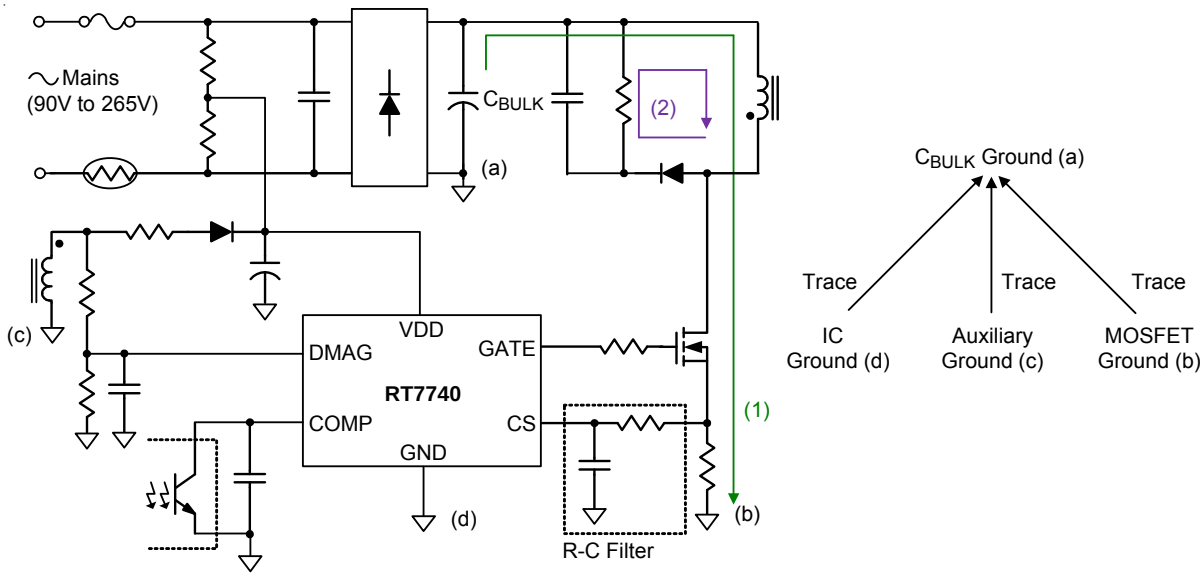
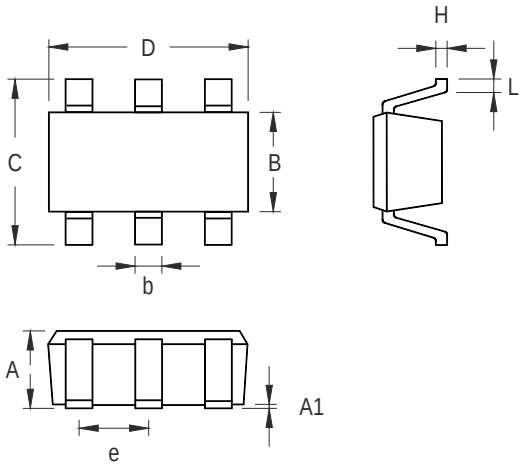


Figure 12. PCB Layout Guide

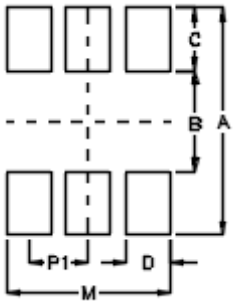
Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.889	1.295	0.031	0.051
A1	0.000	0.152	0.000	0.006
B	1.397	1.803	0.055	0.071
b	0.250	0.560	0.010	0.022
C	2.591	2.997	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

SOT-23-6 Surface Mount Package

Footprint Information



Package	Number of Pin	Footprint Dimension (mm)						Tolerance
		P1	A	B	C	D	M	
TSOT-26/TSOT-26(FC)/SOT-26	6	0.95	3.60	1.60	1.00	0.70	2.60	±0.10

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Datasheet Revision History

Version	Date	Item	Description
P00	2018/7/4		First Edition