RICHTEK®

RT5128A

General PMIC for Intel and AMD Platforms

1 General Description

The RT5128A is a multi-output integrated circuit (MOIC) designed for use with Intel MTL-UPH and AMD SVI3 mobile CPU platforms. The RT5128A integrates two buck controllers, four buck converters, and one load switch. Furthermore, the RT5128A supports both DDR5 and LPDDR5 applications.

To prevent abnormal operation or electrical overstress, the RT5128A features UVLO, OVP, UVP, OTP, and overcurrent-limit protections for each rail. The RT5128A is available in a UQFN-42L 5x5 (FC) package.

2 Ordering Information

RT5128A □□

- Package Type
  QUF: UQFN-42L 5x5 (FC) (U-Type)
- Lead Plating System
  G: Richtek Green Policy Compliant

Note:

Richtek products are Richtek Green Policy compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.

3 Features

- **High Integration**
  - **Two Controllers, Four Converters, and One Switch**
- **Input Voltage Range**
  - **Controller: 4.5V to 23V**
  - **Converter: 2.7V to 5.5V**
- **Internal Soft-Start to Reduce Inrush Current**
- **Stable with POSCAP and MLCC**
- **Output Load Discharge Function**
- **DDR Type Selection: DDR5 or LPDDR5**
- **Cycle-by-Cycle Current Limit**
- **Output Overvoltage and Undervoltage Protection (OVP and UVP)**
- **Input Undervoltage Lockout (UVLO)**
- **Over-Temperature Protection (OTP)**
- **Support I^2C Interface for Programming**
  - **Adjustable Current Limit**
  - **Selectable Switching Frequency**
  - **Selectable Output Discharge Resistance**
  - **Provide Four Power Good Indicators**

4 Applications

- Intel MTL-UPH Mobile CPU
- AMD SVI3 FP7/FP8 Mobile CPU

5 Marking Information

RT5128AGQUF: Product Code
YMDAN: Date Code

6 Simplified Application Circuit

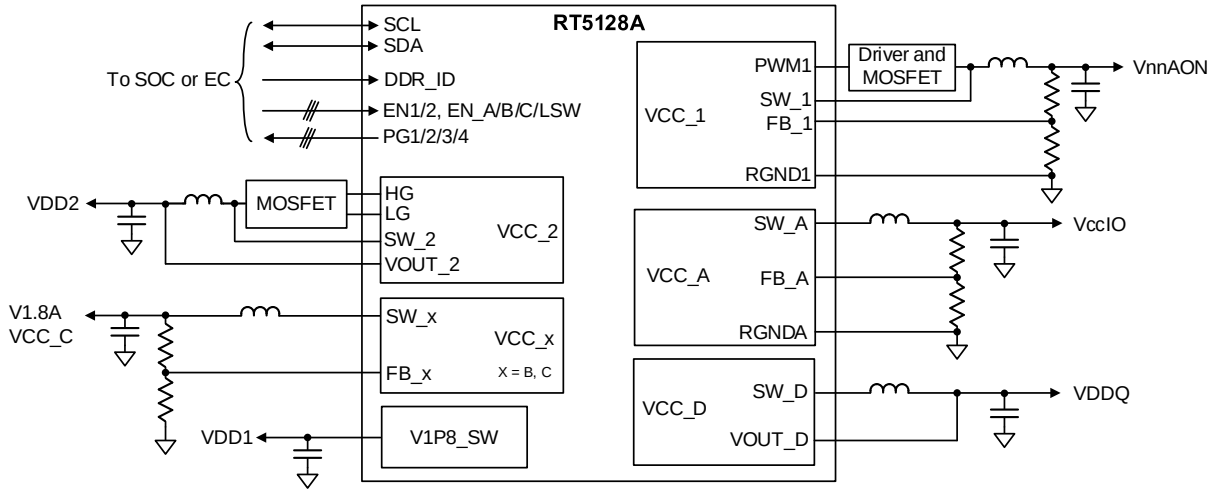

Figure 1. Simplified Application Circuit for Intel MTL-UPH

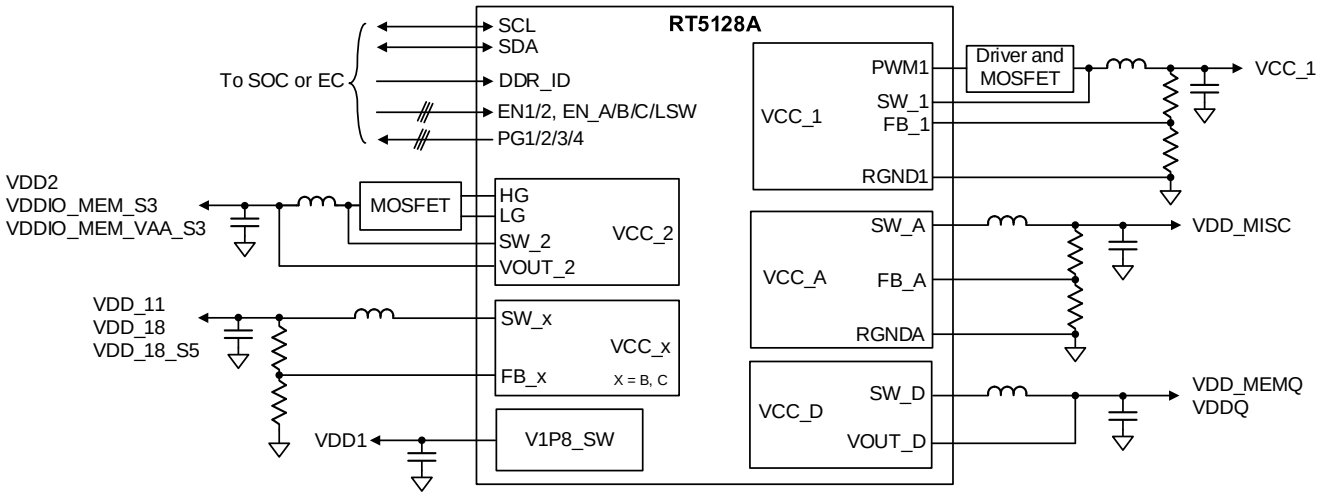

Figure 2. Simplified Application Circuit for AMD SVI3

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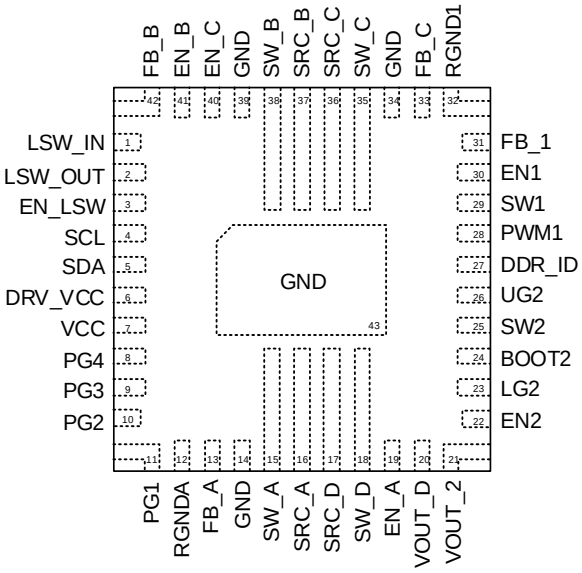
7 Pin Configuration

(TOP VIEW)



UQFN-42L 5x5 (FC)

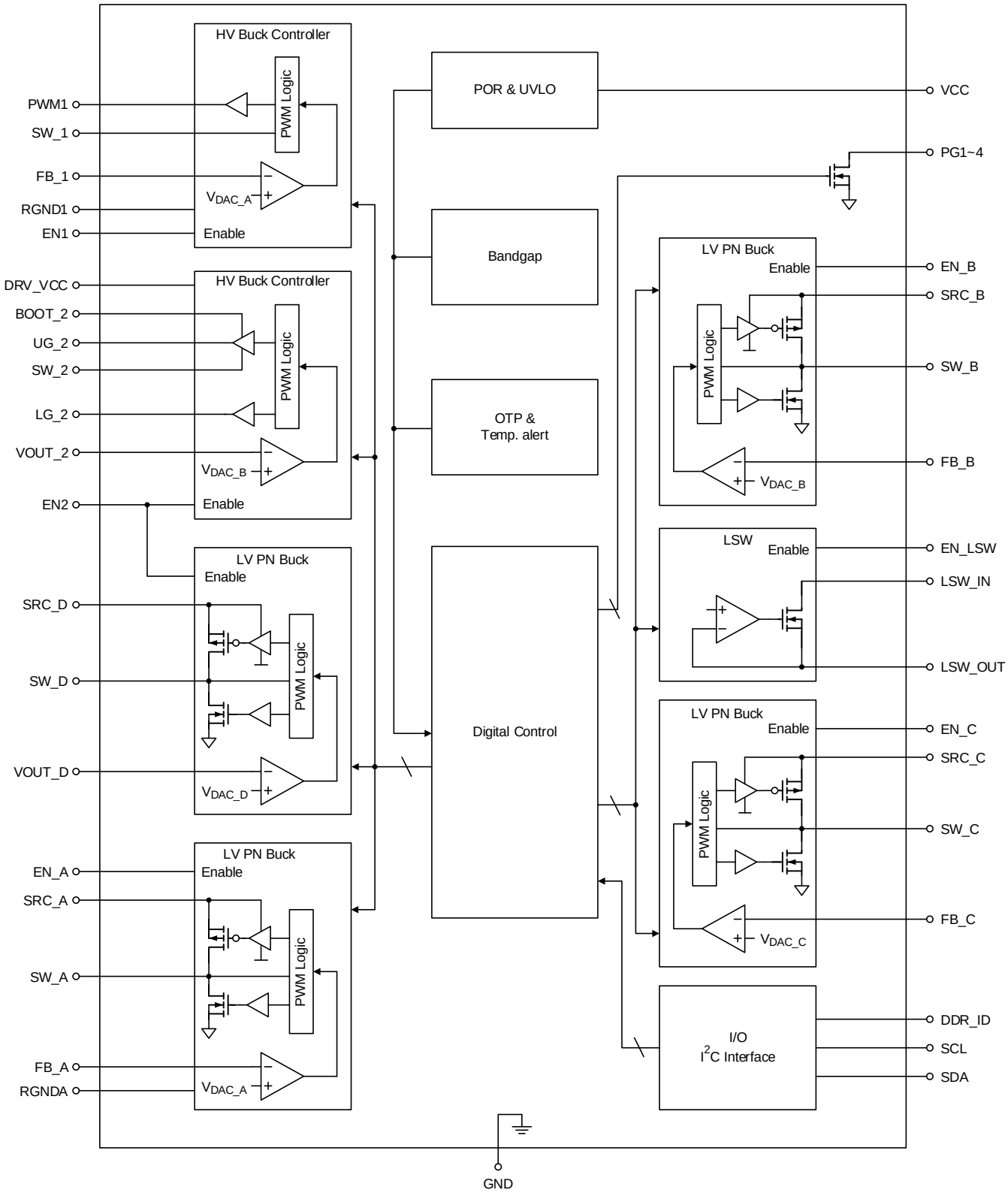
8 Functional Pin Description

Pin No.	Pin Name	Pin Function
1	LSW_IN	Input voltage pin for the load switch.
2	LSW_OUT	Output voltage pin for the load switch.
3	EN_LSW	Enable control input. DO NOT leave this pin floating. As EN_LSW voltage is lower than 0.4V, the load switch is turned off and enters shutdown mode. As EN_LSW is higher than 1V, the load switch wakes up.
4	SCL	I^2C clock pin. This pin is the input of the serial bus clock signal.
5	SDA	I^2C data pin. This pin is the input and output of the serial bus data signal.
6	DRV_VCC	Bias voltage for the internal gate driver. The typical required bias voltage for DRV_VCC is 5V. To avoid noise disturbance, the supplied bias voltage must remain stable. Besides, a RC filter (R = 2.2Ω/0603 and C = 1μF/0603) from the bias voltage to the DRV_VCC pin is necessary and should be placed as close as physically possible to the DRV_VCC pin. Both DRV_VCC and VCC should be connected to the same power supply.
7	VCC	Bias voltage for control logic. The required bias voltage for VCC is typically 5V. To avoid noise disturbance, the supplied bias voltage must be stable. Besides, an RC filter (R = 2.2Ω/0603 and C = 1μF/0603) from bias voltage to the VCC pin is necessary and should be placed as close as physically possible to the VCC pin. Both DRV_VCC and VCC should be connected to the same power supply.
8	PG4	PG4 is a power good indicator that can be assigned for any rail using I^2C (default is VCC_C). PG4 is an open-drain output, pulled low when UVP/OVP/OTP/EN is low or when the output voltage is not regulated (such as before soft-start). A pull-up resistor of 10kΩ to 100kΩ is necessary if this function is used.

Pin No.	Pin Name	Pin Function
9	PG3	PG3 is a power good indicator that can be assigned for any rail using I^2C (default is VCC_A). PG3 is an open-drain output, pulled low when UVP/OVP/OTP/EN is low or when the output voltage is not regulated (such as before soft-start). A pull-up resistor of 10kΩ to 100kΩ is necessary if this function is used.
10	PG2	PG2 is a power good indicator that can be assigned for any rail using I^2C (default is VCC_2). PG2 is an open-drain output, pulled low as UVP/OVP/OTP/EN is low or when the output voltage is not regulated (such as before soft-start). A pull-up resistor of 10kΩ to 100kΩ is necessary if this function is used.
11	PG1	PG1 is a power good indicator that can be assigned for any rail using I^2C (default is VCC_1). PG1 is an open-drain output, pulled low as UVP/OVP/OTP/EN is low or when the output voltage is not regulated (such as before soft-start). A pull-up resistor of 10kΩ to 100kΩ is necessary if this function is used.
12	RGNDA	Remote sense ground of VCC_1. Connect RGNDA to the negative terminal of the output capacitor.
13	FB_A	VCC_A feedback pin. Connect a pair of voltage dividers to set the target output voltage. The FB_A pin is well regulated at the reference voltage (0.6V) by the internal control loop.
14, 34, 39, 43 (Exposed Pad)	GND	Ground pin and exposed pad of package. This pin is electrically isolated. It is recommended to directly solder to the large GND plane and add enough thermal vias to enhance heat dissipation and achieve better thermal performance.
15	SW_A	Switch node of VCC_A. Connect it to the power inductor. Since this pin is noisy, keep the sensitive trace or signal away from the SW_A net.
16	SRC_A	Input voltage for VCC_A.
17	SRC_D	Input voltage for VCC_D.
18	SW_D	Switch node of VCC_D. Connect it to the power inductor. Since this pin is noisy, keep the sensitive trace or signal away from the SW_D net.
19	EN_A	Enable control input. DO NOT leave this pin floating. If the EN_A voltage is lower than 0.4V, VCC_A is turned off and enters shutdown mode. If EN_A is higher than 1V, VCC_A wakes up.
20	VOUT_D	VCC_D unity feedback pin. Connect this pin to the positive terminal of the output capacitors for voltage regulation.
21	VOUT_2	VCC_2 unity feedback pin. Connect this pin to the positive terminal of the output capacitors for voltage regulation.
22	EN2	Enable control input. DO NOT leave this pin floating. If the EN2 voltage is lower than 0.4V, both VCC_2 and VCC_D are turned off and enter shutdown mode. If the EN2 voltage is higher than 1V and less than 1.5V, VCC_2 is active and suitable to operate with pure MLCC type output capacitors. If the EN2 voltage is higher than 1.7V, VCC_2 is active and suitable to operate with POSCAP type output capacitors. Furthermore, EN2 is also used to control the VCC_D rail status. VCC_D is powered on if the EN2 voltage is higher than 1V.
23	LG2	VCC_2 low-side gate driver output pin. Connect this pin to the gate of the low-side MOSFET. Note that the trace impedance between the LG2 pin and gate terminal of the low-side MOSFET should be as small as possible. DO NOT connect a resistor between LG2 and gate terminal of the low-side MOSFET; otherwise, it might cause undesired shoot-through since the LG2 voltage is monitored for shoot-through protection.

Pin No.	Pin Name	Pin Function
24	BOOT2	VCC_2 bootstrap supply for high-side gate driver. Connect a high-quality and low-ESR ceramic capacitor (minimum 0.1μF, X7R) from BOOT2 to the SW2 pin. The bootstrap capacitor supplies current to the high-side gate driver and should be placed as close to the BOOT2 pin as possible.
25	SW2	Switch node of VCC_2. This pin is the return node of the high-side MOSFET driver. Connect this pin to the source of the high-side MOSFET together with the drain of the low-side MOSFET and the inductor.
26	UG2	VCC_2 upper gate driver with sink and source output. Connect to the gate of the high-side MOSFET through a short and low-inductance path.
27	DDR_ID	DDR type selection. The RT5128A operates in LPDDR5 mode if the DDR_ID voltage is higher than 1V, on the other hand, the RT5128A operates in DDR5 mode if the DDR_ID voltage is lower than 0.4V.
28	PWM1	PWM control output for the VCC_1 driver circuit. When the PWM output is high, the high-side MOSFET is turned on. When the PWM output is in the tri-state level, both MOSFETs are turned off. When the PWM input is low, the low-side MOSFET is turned on.
29	SW1	Switch node of VCC_1. Connect this pin to the source of the high-side MOSFET, along with the drain of low-side MOSFET and the inductor.
30	EN1	Enable control input. DO NOT leave this pin floating. When the EN1 voltage is lower than 0.4V, VCC_1 is turned off and enters shutdown mode. When the EN1 voltage is higher than 1V but less than 1.5V, VCC_1 is active and suitable for operation with pure MLCC type output capacitors. When EN1 is higher than 1.7V, VCC_1 is active and suitable for operation with POSCAP type output capacitors.
31	FB_1	VCC_1 feedback input. A resistor divider from VOUT to FB sets the desired VOUT level. VOUT is regulated by FB tracking internal reference voltage of 0.6V.
32	RGND1	Remote sense ground of VCC_1. RGND1 is for remote negative sense feedback.
33	FB_C	VCC_C feedback input. Connect a pair of voltage dividers to set the target output voltage. The FB_C is well regulated at the reference voltage (0.6V) by the internal control loop.
35	SW_C	Switch node of VCC_C. Connect it to the power inductor. This pin is noisy, so keep the sensitive trace or signal away from the SW_C net.
36	SRC_C	Input voltage for VCC_C.
37	SRC_B	Input voltage for VCC_B.
38	SW_B	Switch node of VCC_B. Connect to the power inductor. This pin is noisy, so keep the sensitive trace or signal away from the SW_B net.
40	EN_C	Enable control input. DO NOT leave this pin floating. When the EN_C voltage is lower than 0.4V, VCC_C is turned off and enters shutdown mode. When the EN_C voltage is higher than 1V, VCC_C wakes up.
41	EN_B	Enable control input. DO NOT leave this pin floating. When the EN_B voltage is lower than 0.4V, VCC_B is turned off and enters shutdown mode. When the EN_B voltage is higher than 1V, VCC_B wakes up.
42	FB_B	VCC_B feedback input. Connect a pair of voltage dividers to set the target output voltage. The FB_B is well regulated at the reference voltage (0.6V) by the internal control loop.

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 1)

- Supply Input Voltage, V_{IN} ---------- –0.3V to 30V
- Supply Input Voltage, V_{DRV_VCC}, V_{CC}, V_{SRC} ---------- –0.3V to 6V
- BOOT2 to GND
  - DC ---------- –0.3V to 36V
  - <100ns ---------- –5V to 42V
- BOOT2, UG2, LG2 to SW2
  - DC ---------- –0.3V to 6V
  - <100ns ---------- –5V to 7.5V
- SW1 to GND
  - DC ---------- –0.3V to 30V
  - <100ns ---------- –10V to 42V
- SW2 to GND
  - DC ---------- –5V to 30V
  - <100ns ---------- –10V to 42V
- UG2 to GND
  - DC ---------- –5V to 36V
  - <100ns ---------- –10V to 42V
- Other I/O Pins ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  - UQFN-42L 5x5 (FC) ---------- 5.12W
- Package Thermal Resistance (Note 2)
  - UQFN-42L 5x5 (FC), θ_{JA} ---------- 19.52°C/W
  - UQFN-42L 5x5 (FC), θ_{JC} ---------- 2.62°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 300°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Model) ---------- 2kV

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precautions are recommended.

11 Recommended Operating Conditions

(Note 4)

- Supply Input Voltage, V_{DRV_VCC}, V_{CC} ---------- 4.5V to 5.5V
- Supply Input Voltage, V_{IN} ---------- 4.5V to 23V
- Supply Input Voltage, V_{SRC} ---------- 2.7V to 5.5V
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 125°C

Note 4. The device is not guaranteed to function outside its operating conditions.

12 Electrical Characteristics

(V_{IN} = 12V, V_{CC} = 5V. The typical values are referenced to T_A = T_J = 25°C. Both the minimum and maximum values are referenced to T_A = T_J from –10°C to 105°C. Unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage						
VCC Supply Input Voltage	V_{CC}		4.5	--	5.5	V
VCC Shutdown Current	I_{VCC_SHDN}	All ENx = 0V	--	60	--	μA
UVLO						
VSRC Undervoltage Lockout Falling Threshold	$V_{SRC\_A\_UVLO\_F}$ $V_{SRC\_B\_UVLO\_F}$ $V_{SRC\_C\_UVLO\_F}$ $V_{SRC\_D\_UVLO\_F}$	Falling edge	--	2.4	--	V
VSRC Undervoltage Lockout Hysteresis	$V_{SRC\_A\_UVLO\_HYS}$ $V_{SRC\_B\_UVLO\_HYS}$ $V_{SRC\_C\_UVLO\_HYS}$ $V_{SRC\_D\_UVLO\_HYS}$	Hysteresis	--	200	--	mV
VCC Undervoltage Lockout Falling Threshold	$V_{CC\_UVLO\_F}$	Falling edge	--	3.8	--	V
VCC Undervoltage Lockout Hysteresis	$V_{CC\_UVLO\_HYS}$	Hysteresis	--	200	--	mV
Logic Threshold						
EN1 and EN2 Threshold Voltage	V_{EN1} V_{EN2}	VCC_1 or 2 is operating in POSCAP mode	1.7	--	--	V
		Enable corresponding rail, VCC_1 or 2 is operating in MLCC mode	1	--	1.5	
		Shutdown	--	--	0.4	
EN_A, EN_B, EN_C, and EN_LSW Threshold Voltage	V_{EN_A} V_{EN_B} V_{EN_C} V_{EN_LSW}	ENx > 1V, enable corresponding rail, VCC_1 & 2 is operating in MLCC mode	1	--	--	V
		Shutdown	--	--	0.4	
DDR_ID Input Voltage Logic High	$V_{DDR\_ID\_IH}$	Rising edge	1	--	--	V
DDR_ID Input Voltage Logic Low	$V_{DDR\_ID\_IL}$	Falling edge	--	--	0.4	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Thermal Alert						
Thermal Alert Assert Threshold	T_{ALERT_H}	GBD, default setting, PROCHOT_SET[1:0] = 01	100	110	120	°C
Thermal Alert De-Assert Threshold	T_{ALERT_L}		--	90	--	°C
Over-Temperature Protection Threshold	T_{OTP}	GBD	140	150	160	°C
Over-Temperature Protection Hysteresis	T_{OTP_HYS}		--	25	--	°C
VCC_1 (HV Buck Controller)						
Quiescent Current	I_{Q_NSW}	Enable, No switching	--	110	--	μA
Reference Voltage and Soft-Start						
Reference Voltage	V_{REF}	T_A = 25°C	0.597	0.6	0.603	V
Soft-Start Time	t_{SS}	V_{REF} 10% to 90%	--	1	--	ms
Current Limit						
Current-Limit Threshold	V_{CL}	OC_CTRL1[1:0] = 00	60	75	90	mV
		OC_CTRL1[1:0] = 01 (default)	110	125	140	
		OC_CTRL1[1:0] = 10	160	200	240	
		OC_CTRL1[1:0] = 11	184	230	276	
Switching Frequency and Minimum Off Timer						
Switching Frequency	f_{SW}	FSW_CTRL2[1:0] = 00	320	400	480	kHz
		FSW_CTRL2[1:0] = 01 (default)	480	600	720	
		FSW_CTRL2[1:0] = 10	640	800	960	
		FSW_CTRL2[1:0] = 11	800	1000	1200	
Minimum On-Time	t_{ON_MIN}		--	50	--	ns
Minimum Off-Time	t_{OFF_MIN}		150	400	500	ns
Protection						
Output Overvoltage Protection Threshold	V_{OVP}	OVP Detect	115	120	125	%
Output Overvoltage Protection Delay Time	t_{OVP_DLY}		--	5	--	μs
Output Undervoltage Protection Threshold	V_{UVP}		55	60	65	%
Output Undervoltage Protection Delay	t_{UVP_DLY}		--	5	--	μs
Zero Current Crossing Threshold	V_{PHASE_ZC}	GND-SW1	--	1	--	mV

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Discharge Resistance						
Discharge Resistor	R_{DISCHG}	DISCH_CTRL2[1:0] = 00	--	Hi-Z	--	Ω
		DISCH_CTRL2[1:0] = 01 (default)	--	100	--	
		DISCH_CTRL2[1:0] = 10	--	200	--	
		DISCH_CTRL2[1:0] = 11	--	500	--	
Power Good Indicator						
Power-Good Voltage Rising Threshold	V_{PGOOD_R}	PGOOD detect, rising edge	86	90	94	%
Power-Good Voltage Hysteresis	V_{PGOOD_HYS}	Hysteresis	--	6	--	%
PGOOD Available Time	$t_{PGOOD\_Available}$	EN rising to PGOOD rising	--	2	3	ms
PWM Driving Capability						
PWM Source	R_{PWM_SR}	VCC to PWM	--	--	35	Ω
PWM Sink	R_{PWM_SK}	PWM to GND	--	--	15	Ω
VCC_2 (HV Buck Controller w/ Driver)						
Quiescent Current	I_{Q_NSW}	Enable, no switching	--	110	--	μA
Output Voltage and Soft-Start						
Output Voltage	V_{OUT}	DDR_ID = H, T_A = 25°C	1.044	1.05	1.056	V
		DDR_ID = L, T_A = 25°C	1.094	1.1	1.106	
Soft-Start Time	t_{SS}	VCC_2 10% to 90%	--	1	--	ms
Current Limit						
Current-Limit Threshold	V_{CL}	OC_CTRL1[3:2] = 00	60	75	90	mV
		OC_CTRL1[3:2] = 01	100	125	150	
		OC_CTRL1[3:2] = 10 (default)	160	200	240	
		OC_CTRL1[3:2] = 11	184	230	276	
Switching Frequency and Minimum-Off Timer						
Switching Frequency	f_{SW}	FSW_CTRL2[3:2] = 00	320	400	480	kHz
		FSW_CTRL2[3:2] = 01 (default)	480	600	720	
		FSW_CTRL2[3:2] = 10	640	800	960	
		FSW_CTRL2[3:2] = 11	800	1000	1200	
Minimum On-Time	t_{ON_MIN}		--	50	--	ns
Minimum Off-Time	t_{OFF_MIN}		150	400	500	ns
Protection						
Output Overvoltage Protection Threshold	V_{OVP}	OVP Detect	115	120	125	%
Output Overvoltage Protection Delay Time	t_{OVP_DLY}		--	5	--	μs

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Undervoltage Protection Threshold	V_{UVP}		55	60	65	%
Output Undervoltage Protection Delay	V_{UVP_DLY}		--	5	--	μs
Zero Current Crossing Threshold	V_{PHASE_ZC}	GND-SW2	--	1	--	mV
Discharge Resistance						
Discharge Resistor	R_{DISCHG}	DISCH_CTRL2[3:2] = 00	--	Hi-Z	--	Ω
		DISCH_CTRL2[3:2] = 01 (default)	--	100	--	
		DISCH_CTRL2[3:2] = 10	--	200	--	
		DISCH_CTRL2[3:2] = 11	--	500	--	
Power Good Indicator						
Power-Good Voltage Rising Threshold	V_{PGOOD_R}	PGOOD detect, rising edge	86	90	94	%
Power-Good Voltage Hysteresis	V_{PGOOD_HYS}	Hysteresis	--	6	--	%
PGOOD Available Time	$t_{PGOOD\_Available}$	EN rising to PGOOD rising	--	2	3	ms
Driver On-Resistance						
UGATE Drive Source Impedance	R_{SRC_UGATE}	BOOT2 – SW2 forced to 5V	--	2	4	Ω
UGATE Drive Sink Impedance	R_{SNK_UGATE}	BOOT2 – SW2 forced to 5V	--	1	2	Ω
LGATE Drive Source Impedance	R_{SRC_LGATE}	LG2, high state	--	1.5	3	Ω
LGATE Drive Sink Impedance	R_{SNK_LGATE}	LG2, low state	--	0.7	1.5	Ω
UGATE Propagation Delay Time	t_{DLY_UG}	From LG2 falling to UG2 rising	--	30	--	ns
LGATE Propagation Delay Time	t_{DLY_LG}	From UG2 falling to LG2 rising	--	20	--	
Internal Boost Diode Resistor	R_{BOOT}	VCC to BOOT2, I_{BOOT} = 10mA	--	40	80	Ω
VCC_A (LV Buck Converter, 6A)						
SRC_A Supply Input Voltage	V_{SRC_A}		2.7	--	5.5	V
Quiescent Current	I_{Q_NSW}	Enable, no switching	--	35	--	μA
Reference Voltage and Soft-Start						
Reference Voltage	V_{REF}	T_A = 25°C	0.597	0.6	0.603	V
Soft-Start Time	t_{SS}	V_{REF} 10% to 90%	--	1	--	ms
Internal Switch On-Resistance						
On-Resistance of High-Side MOSFET	R_{DSON_H}		--	31	--	mΩ

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
On-Resistance of Low-Side MOSFET	R_{DSON_L}		--	15	--	mΩ
Current Limit						
Low-Side Switch (Valley) Current Limit	I_{LIM_L}	Valley current OC_CTRL1[1:0] = 00 (default)	8	9	10	A
		Valley current OC_CTRL1[1:0] = 01	6.3	7.8	9.3	
		Valley current OC_CTRL1[1:0] = 10	4.6	6.6	8.6	
		Valley current OC_CTRL1[1:0] = 11	3.3	5.3	7.3	
Switching Frequency and Minimum-Off Timer						
Switching Frequency	f_{SW}	FSW_CTRL1[1:0] = 00	480	600	720	kHz
		FSW_CTRL1[1:0] = 01 (default)	640	800	960	
		FSW_CTRL1[1:0] = 10	800	1000	1200	
		FSW_CTRL1[1:0] = 11	960	1200	1440	
Minimum Off-Time	t_{OFF_MIN}		--	100	--	ns
Protection						
Output Overvoltage Protection Threshold	V_{OVP}	OVP Detect	--	120	--	%
Output Overvoltage Protection Delay Time	t_{OVP_DLY}		--	5	--	µs
Output Undervoltage Protection Threshold	V_{UVP}	UVP Detect	55	60	65	%
Output Undervoltage Protection Delay	V_{UVP_DLY}		--	3	--	µs
Power Good Indicator						
Power-Good Voltage Rising Threshold	V_{PGOOD_R}	PGOOD detect, rising edge	86	90	94	%
Power-Good Voltage Hysteresis	V_{PGOOD_HYS}	Hysteresis	--	6	--	%
PGOOD Available Time	$t_{PGOOD\_Available}$	From EN Rising, VOUT > PGOOD Threshold	--	2	3	ms
Discharge Resistance						
Discharge Resistor	R_{DISCHG}	DISCH_CTRL1[1:0] = 00	--	Hi-Z	--	Ω
		DISCH_CTRL1[1:0] = 01 (Default)	--	100	--	
		DISCH_CTRL1[1:0] = 10	--	200	--	
		DISCH_CTRL1[1:0] = 11	--	500	--	
VCC_B (LV Buck Converter, 6A)						
SRC_B Supply Input Voltage	V_{SRC_B}		2.7		5.5	V
Quiescent Current	I_{Q_NSW}	Enable, no switching	--	35	--	µA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Reference Voltage and Soft-Start						
Reference Voltage	V_{REF}	T_A = 25°C	0.597	0.6	0.603	V
Soft-Start Time	t_{SS}	V_{REF} 10% to 90%	--	1	--	ms
Internal Switch On-Resistance						
On-Resistance of High-Side MOSFET	R_{DSON_H}		--	31	--	mΩ
On-Resistance of Low-Side MOSFET	R_{DSON_L}		--	15	--	mΩ
Current Limit						
Low-Side Switch (Valley) Current Limit	I_{LIM_L}	Valley current OC_CTRL1[3:2] = 00 (default)	8	9	10	A
		Valley current OC_CTRL1[3:2] = 01	6.3	7.8	9.3	
		Valley current OC_CTRL1[3:2] = 10	4.6	6.6	8.6	
		Valley current OC_CTRL1[3:2] = 11	3.3	5.3	7.3	
Switching Frequency and Minimum-Off Timer						
Switching Frequency	f_{SW}	FSW_CTRL1[3:2] = 00 (default)	960	1200	1440	kHz
		FSW_CTRL1[3:2] = 01	1120	1400	1680	
		FSW_CTRL1[3:2] = 10	1280	1600	1920	
		FSW_CTRL1[3:2] = 11	1440	1800	2160	
Minimum Off-Time	t_{OFF_MIN}		--	100	--	ns
Protection						
Output Overvoltage Protection Threshold	V_{OVP}	OVP Detect	115	120	125	%
Output Overvoltage Protection Delay Time	t_{OVP_DLY}		--	5	--	µs
Output Undervoltage Protection Threshold	V_{UVP}	UVP Detect	55	60	65	%
Output Undervoltage Protection Delay	V_{UVP_DLY}		--	3	--	µs
Power Good Indicator						
Power-Good Voltage Rising Threshold	V_{PGOOD_R}	PGOOD detect, rising edge	86	90	94	%
Power-Good Voltage Hysteresis	V_{PGOOD_HYS}	Hysteresis	--	6	--	%
PGOOD Available Time	$t_{PGOOD\_Available}$	From EN rising, VOUT > PGOOD threshold	--	2	3	ms
Discharge Resistance						
Discharge Resistor	R_{DISCHG}	DISCH_CTRL1[3:2] = 00	--	Hi-Z	--	Ω
		DISCH_CTRL1[3:2] = 01 (Default)	--	100	--	
		DISCH_CTRL1[3:2] = 10	--	200	--	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
		DISCH_CTRL1[3:2] = 11	--	500	--	
VCC_C (LV Buck Converter, 4A)						
SRC_C Supply Input Voltage	V_{SRC_C}		2.7	--	5.5	V
Quiescent Current	I_{Q_NSW}	Enable, No switching	--	35	--	μA
Reference Voltage and Soft-Start						
Reference Voltage	V_{REF}	T_A = 25°C	0.597	0.6	0.603	V
Soft-Start Time	t_{SS}	V_{REF} 10% to 90%	--	1	--	ms
Internal Switch On-Resistance						
On-Resistance of High-side MOSFET	R_{DSON_H}		--	42	--	mΩ
On-Resistance of Low-side MOSFET	R_{DSON_L}		--	21	--	mΩ
Current Limit						
Low-Side Switch (Valley) Current Limit	I_{LIM_L}	Valley current, OC_CTRL1[5:4] = 00	4.8	6	7.8	A
		Valley current OC_CTRL1[5:4] = 01	4	5	6.5	
		Valley current OC_CTRL1[5:4] = 10	3.2	4	4.8	
		Valley current OC_CTRL1[5:4] = 11 (default)	2.4	3	3.9	
Switching Frequency and Minimum-Off Timer						
Switching Frequency	f_{SW}	FSW_CTRL1[5:4] = 00 (default)	960	1200	1440	kHz
		FSW_CTRL1[5:4] = 01	1120	1400	1680	
		FSW_CTRL1[5:4] = 10	1280	1600	1920	
		FSW_CTRL1[5:4] = 11	1440	1800	2160	
Minimum Off-Time	t_{OFF_MIN}		--	100	--	ns
Protection						
Output Overvoltage Protection Threshold	V_{OVP}	OVP Detect	115	120	125	%
Output Overvoltage Protection Delay Time	t_{OVP_DLY}		--	5	--	μs
Output Undervoltage Protection Threshold	V_{UVP}	UVP Detect	55	60	65	%
Output Undervoltage Protection Delay	V_{UVP_DLY}		--	3	--	μs
Power Good Indicator						
Power-Good Voltage Rising Threshold	V_{PGOOD_R}	PGOOD detect, rising edge	86	90	94	%
Power-Good Voltage Hysteresis	V_{PGOOD_HYS}	Hysteresis	--	6	--	%
PGOOD Available Time	$t_{PGOOD\_Available}$	From EN rising, VOUT > PGOOD threshold	--	2	3	ms

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Discharge Resistance						
Discharge Resistor	R_{DISCHG}	DISCH_CTRL1[5:4] = 00	--	Hi-Z	--	Ω
		DISCH_CTRL1[5:4] = 01 (default)	--	100	--	
		DISCH_CTRL1[5:4] = 10	--	200	--	
		DISCH_CTRL1[5:4] = 11	--	500	--	
VCC_D (LV Buck Converter, 3A)						
SRC_D Supply Input Voltage	V_{SRC_D}		2.7	--	5.5	V
Quiescent Current	I_{Q_NSW}	Enable, no switching	--	35	--	μA
Output Voltage and Soft-Start						
Output Voltage	V_{OUT}	DDR_ID = H, T_A = 25°C	0.497	0.5	0.503	V
		DDR_ID = L, T_A = 25°C	1.094	1.1	1.106	
Soft-Start Time	t_{SS}	VOUT 10% to 90%	--	1	--	ms
Internal Switch On-Resistance						
On-Resistance of High-Side MOSFET	R_{DSON_H}		--	42	--	mΩ
On-Resistance of Low-Side MOSFET	R_{DSON_L}		--	21	--	mΩ
Current Limit						
Low-Side Switch (Valley) Current Limit	I_{LIM_L}	Valley current OC_CTRL1[7:6] = 00	4.8	6	7.8	A
		Valley current OC_CTRL1[7:6] = 01	4	5	6.5	
		Valley current OC_CTRL1[7:6] = 10	3.2	4	5.1	
		Valley current OC_CTRL1[7:6] = 11 (default)	2.4	3	3.8	
Switching Frequency and Minimum-Off Timer						
Switching Frequency	f_{SW}	FSW_CTRL1[7:6] = 00 (default)	960	1200	1440	kHz
		FSW_CTRL1[7:6] = 01	1120	1400	1680	
		FSW_CTRL1[7:6] = 10	1280	1600	1920	
		FSW_CTRL1[7:6] = 11	1440	1800	2160	
Minimum Off-Time	t_{OFF_MIN}		--	100	--	ns
Protection						
Output Overvoltage Protection Threshold	V_{OVP}	OVP Detect	115	120	125	%
Output Overvoltage Protection Delay Time	t_{OVP_DLY}		--	5	--	μs
Output Undervoltage Protection Threshold	V_{UVP}	UVP Detect	55	60	65	%
Output Undervoltage Protection Delay	V_{UVP_DLY}		--	3	--	μs

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Good Indicator						
Power-Good Voltage Rising Threshold	V_{PGOOD_R}	PGOOD detect, rising edge	86	90	94	%
Power-Good Voltage Hysteresis	V_{PGOOD_HYS}	Hysteresis	--	6	--	%
PGOOD Available Time	$t_{PGOOD\_Available}$	From EN rising, VOUT > PGOOD threshold	--	2	3	ms
Discharge Resistance						
Discharge Resistor	R_{DISCHG}	DISCH_CTRL1[7:6] = 00	--	Hi-Z	--	Ω
		DISCH_CTRL1[7:6] = 01 (default)	--	100	--	
		DISCH_CTRL1[7:6] = 10	--	200	--	
		DISCH_CTRL1[7:6] = 11	--	500	--	
Load Switch (LSW)						
Quiescent Current	I_Q	EN_LSW is enable	--	2	--	μA
Soft-Start						
Soft-Start Time	t_{SS}	LSW_IN=1.8V, from EN = H to 90% LSW_IN, load = 0A, C = 0.1μF	800	--	3300	μs
Rising Time	t_{Rising}	LSW_IN = 1.8V, 10% to 90% LSW_IN, load = 0A, C = 0.1μF	500	--	1600	μs
On-Resistance						
Load Switch On-Resistor	R_{ON_LSW}	VCC = 5V, LSW_IN = 1.8V, load = 0.1A	--	24	--	mΩ
Discharge Resistance						
Discharge Resistor	R_{DISCHG}	LSW_RDIS[1:0] = 00	--	Hi-Z	--	Ω
		LSW_RDIS[1:0] = 00	--	100	--	
		LSW_RDIS[1:0] = 00 (default)	--	200	--	
		LSW_RDIS[1:0] = 00	--	500	--	
I^2C for Fast Mode						
SCL, SDA High-Level Input Threshold Voltage	V_{IH_I2C}		1.2	--	--	V
SCL, SDA Low-Level Input Threshold Voltage	V_{IL_I2C}		--	--	0.4	V
SCL Clock Frequency	f_{SCL}		--	--	400	kHz
(Repeated) Start Hold Time	$t_{HD;STA}$	After this period, the first clock pulse is generated.	0.6	--	--	μs
SCL Clock Low Period	t_{LOW}		1.3	--	--	μs
SCL Clock High Period	t_{HIGH}		0.6	--	--	μs
(Repeated) Start Setup Time	$t_{SU;STA}$		0.6	--	--	μs
SDA Data Hold Time	$t_{HD;DAT}$		0	--	0.9	μs
SDA Setup Time	$t_{SU;DAT}$		100	--	--	ns

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
STOP Condition Setup Time	$t_{SU;STO}$		0.6	--	--	μs
Bus Free Time between Stop and Start	t_{BUF}		1.3	--	--	μs
Rise Time of SDA and SCL Signals	t_R		20	--	300	ns
Fall Time of SDA and SCL Signals	t_F		20	--	300	ns
SDA Output Low Sink Current	I_{OL_I2C}	SDA voltage = 0.4V	2	--	--	mA
I^2C for High Speed Mode						
SCL, SDA High-Level Input Threshold Voltage	V_{IH_I2C}		1.2	--	--	V
SCL, SDA Low-Level Input Threshold Voltage	V_{IL_I2C}		--	--	0.4	V
SCL Clock Frequency	f_{SCL}		--	--	3.4	MHz
(Repeated) Start Hold Time	$t_{HD;STA}$	After this period, the first clock pulse is generated.	160	--	--	ns
SCL Clock Low Period	t_{LOW}		160	--	--	ns
SCL Clock High Period	t_{HIGH}		60	--	--	ns
(Repeated) Start Setup Time	$t_{SU;STA}$		60	--	--	ns
SDA Data Hold Time	$t_{HD;DAT}$		0	--	70	ns
SDA Setup Time	$t_{SU;DAT}$		10	--	--	ns
STOP Condition Setup Time	$t_{SU;STO}$		160	--	--	ns
Rise Time of SDA and SCL Signals	t_R		10	--	80	ns
Fall Time of SDA and SCL Signals	t_F		10	--	80	ns
SDA Output Low Sink Current	I_{OL_I2C}	SDA voltage = 0.4V	2	--	--	mA

13 Typical Application Circuit

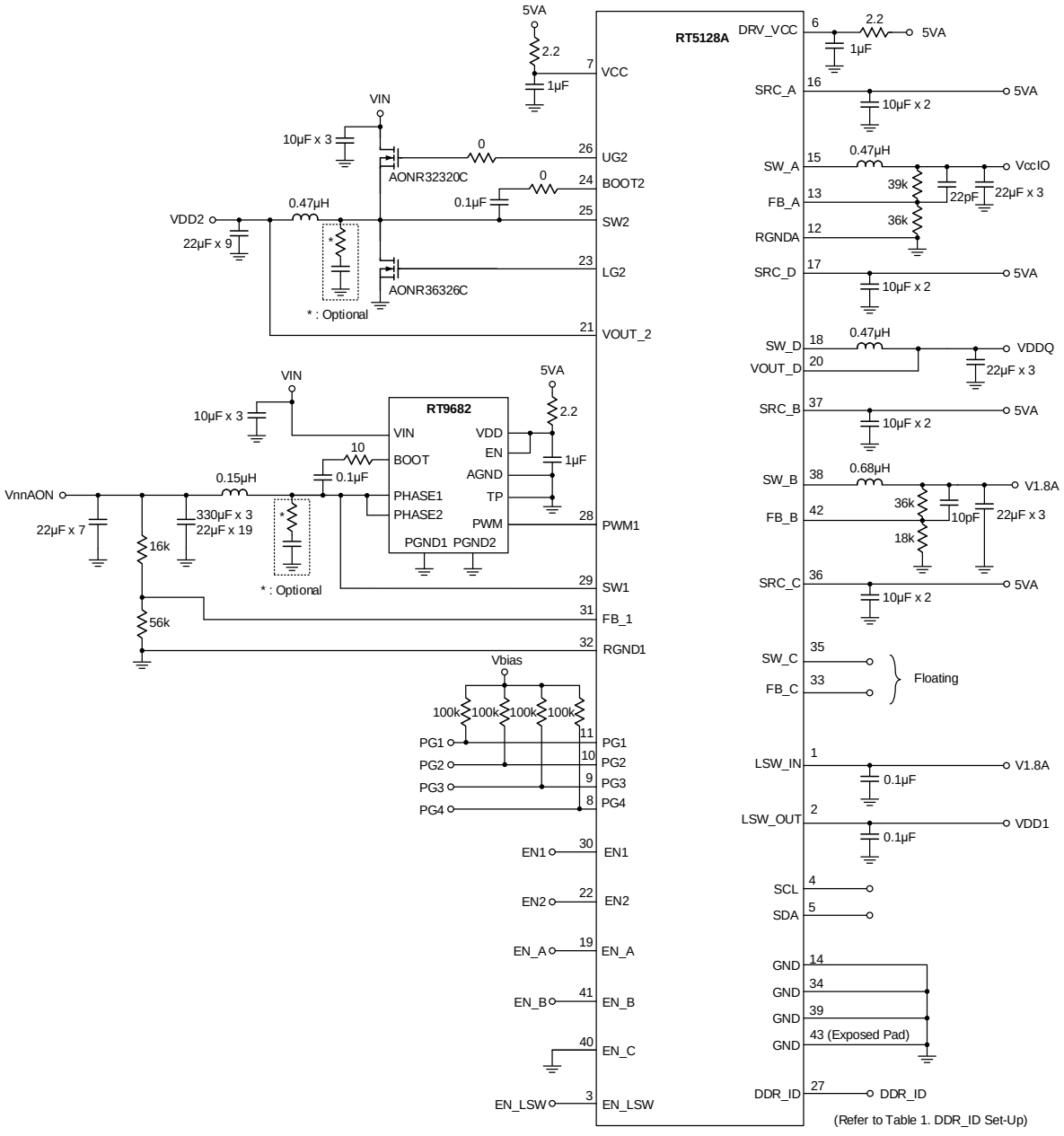


Figure 3. Typical Application Circuit for Intel MTL-UPH

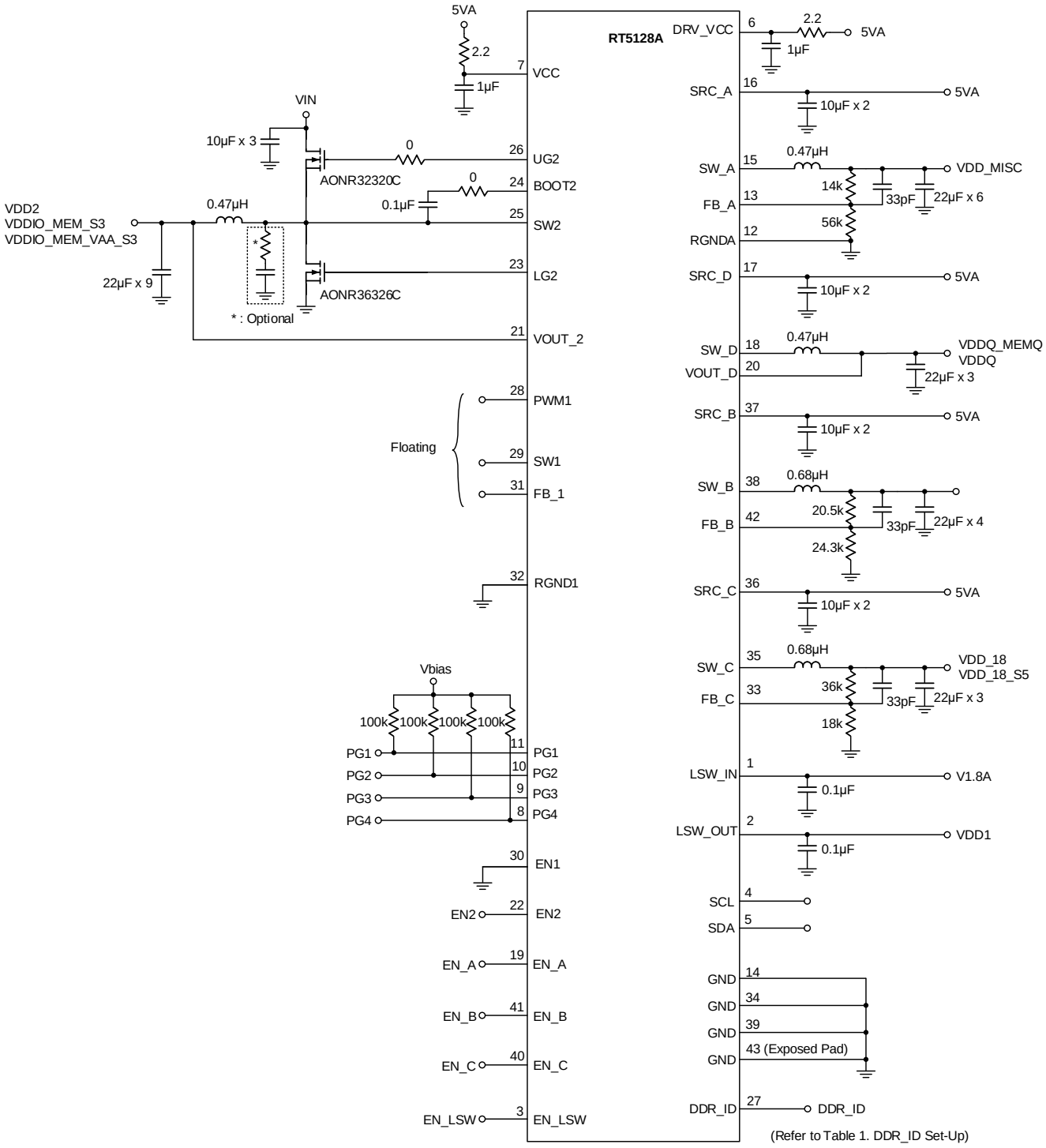
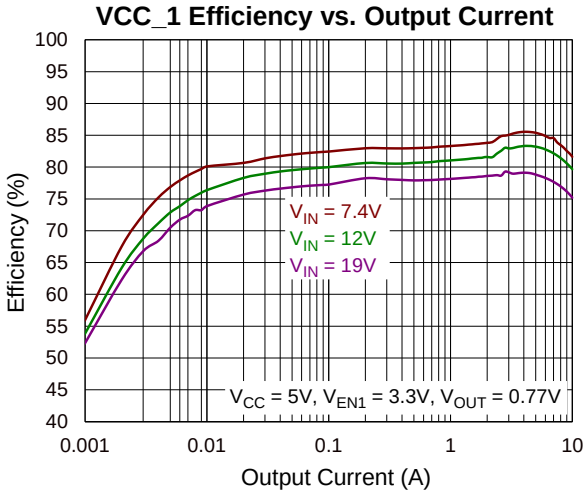


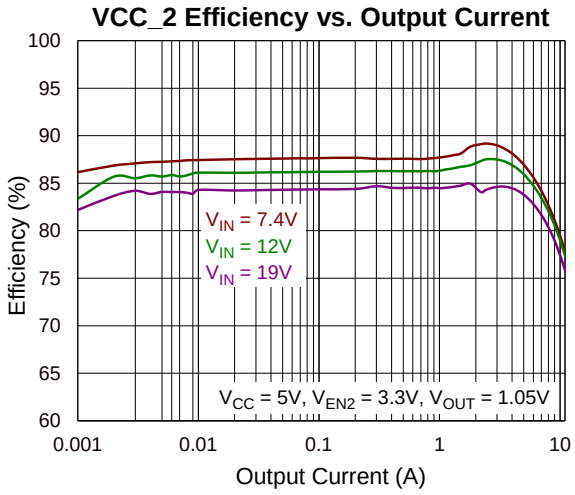
Figure 4. Typical Application Circuit for AMD SVI3

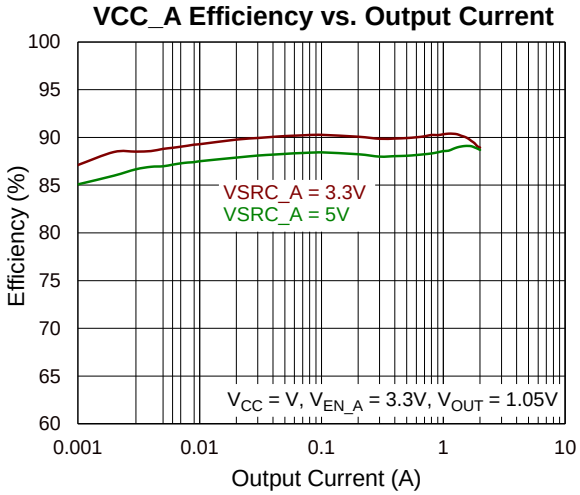
Table 1. DDR_ID Set-Up

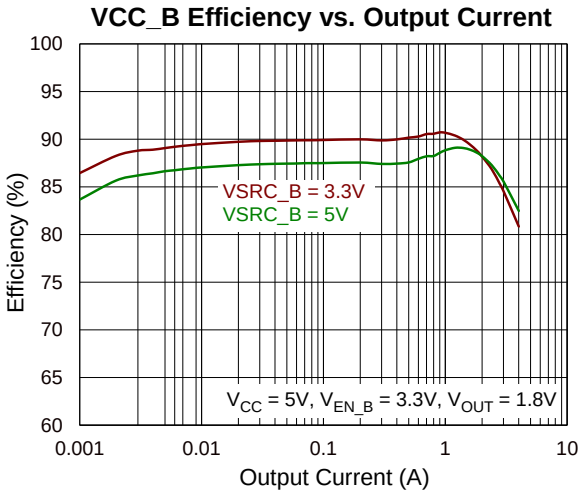
DDR_ID	Memory Type	Suggestion
High (> 1V)	LPDDR5	Connect to VCC
Low (< 0.4V)	DDR5	Connect to GND

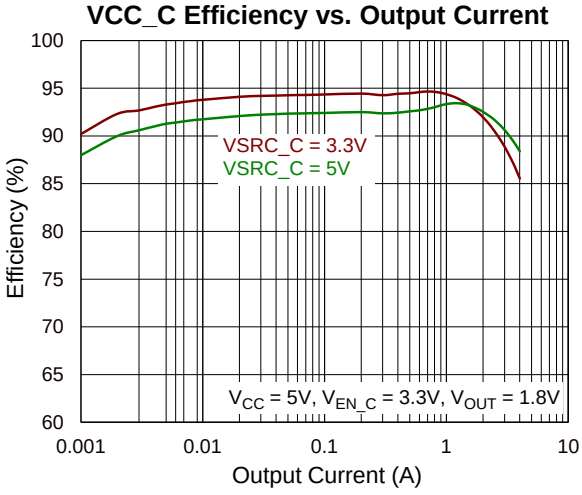
14 Typical Operating Characteristics

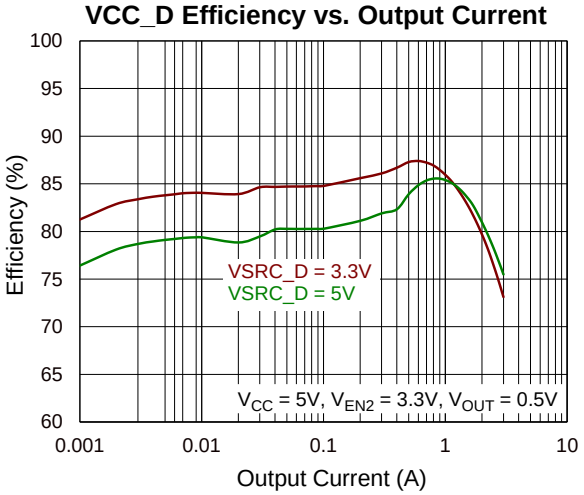




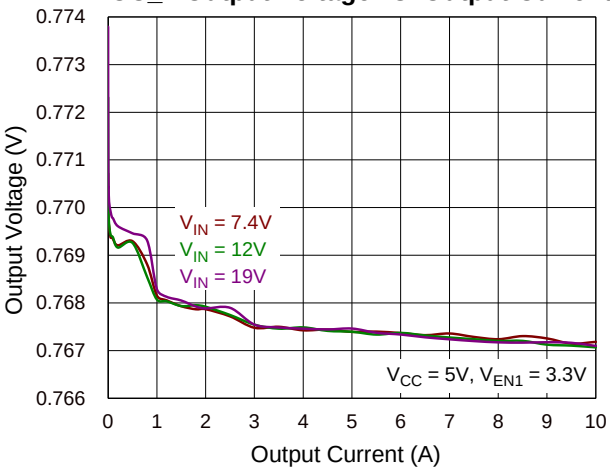




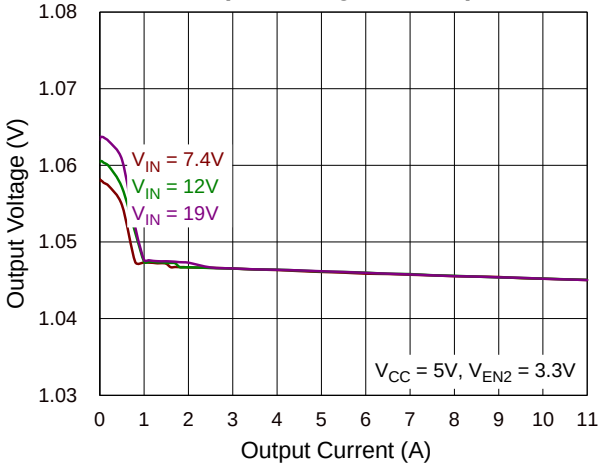




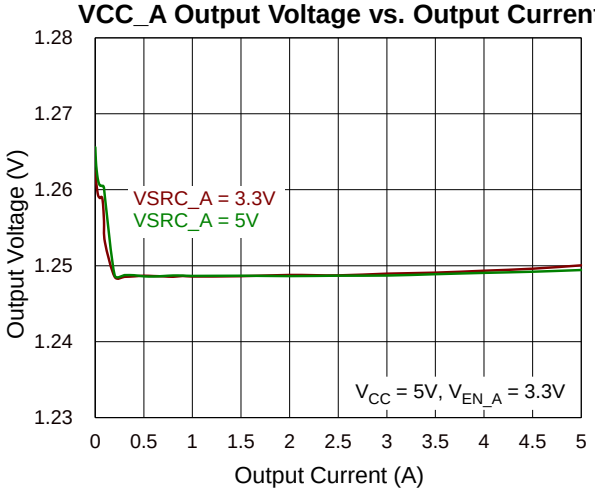
VCC_1 Output Voltage vs. Output Current



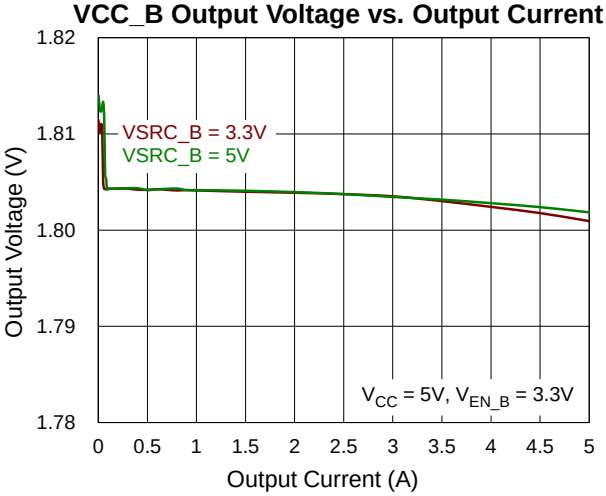
VCC_2 Output Voltage vs. Output Current



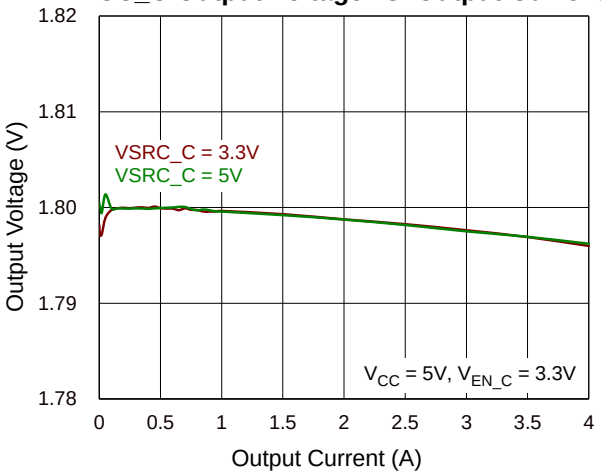
VCC_A Output Voltage vs. Output Current



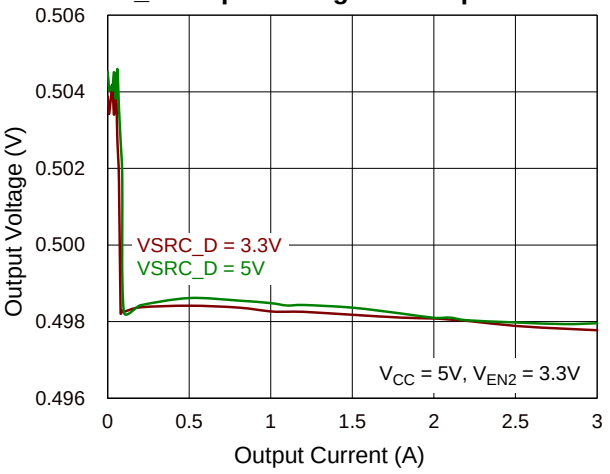
VCC_B Output Voltage vs. Output Current



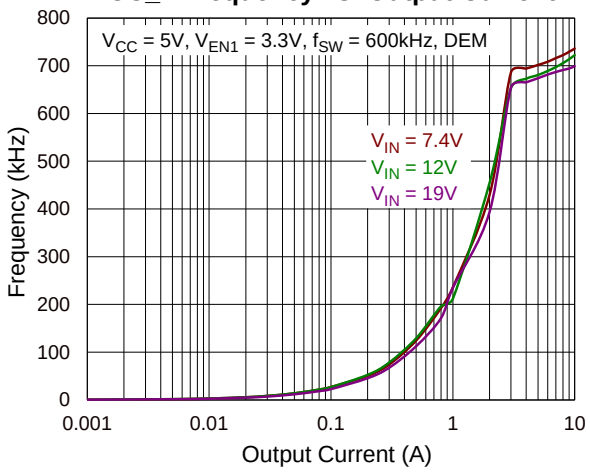
VCC_C Output Voltage vs. Output Current



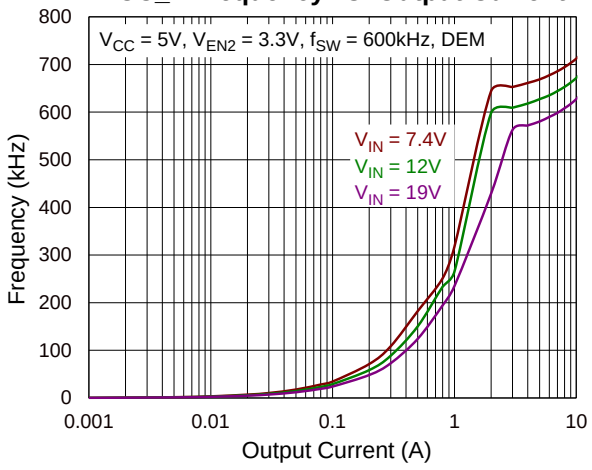
VCC_D Output Voltage vs. Output Current



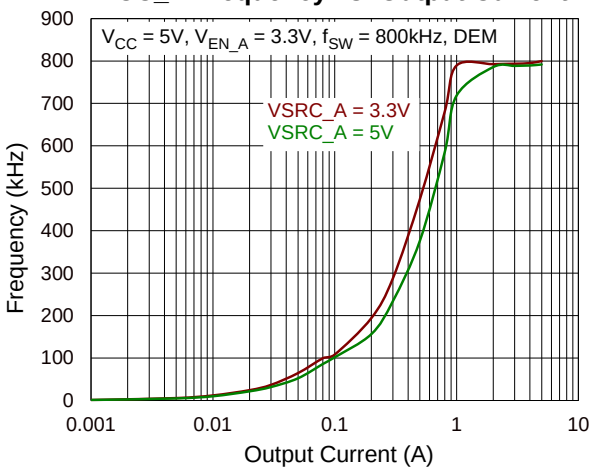
VCC_1 Frequency vs. Output Current



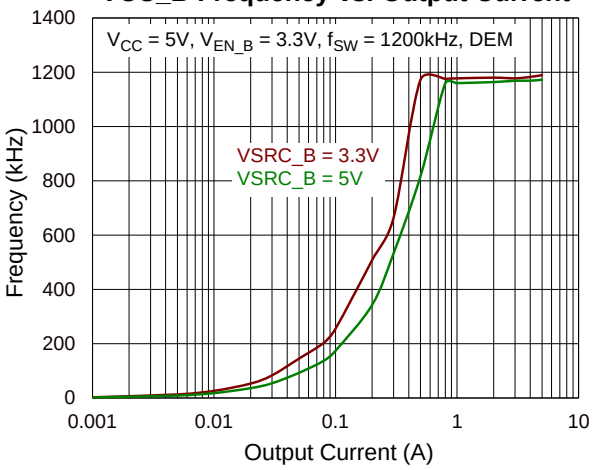
VCC_2 Frequency vs. Output Current



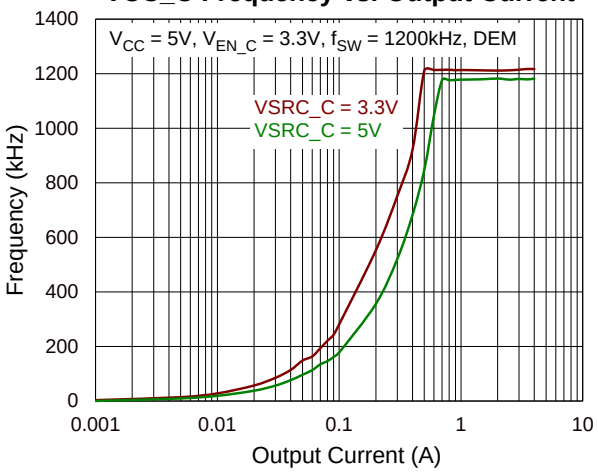
VCC_A Frequency vs. Output Current



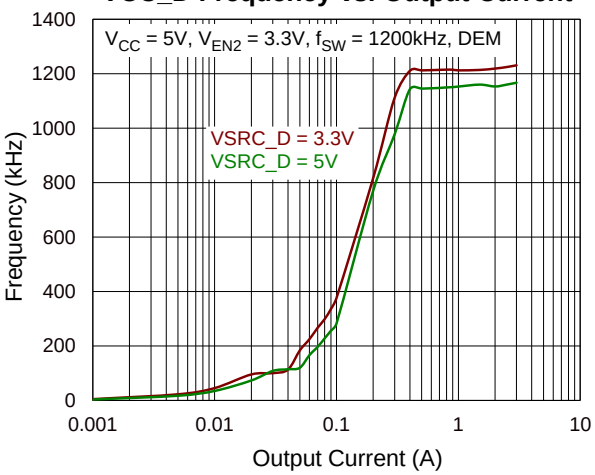
VCC_B Frequency vs. Output Current



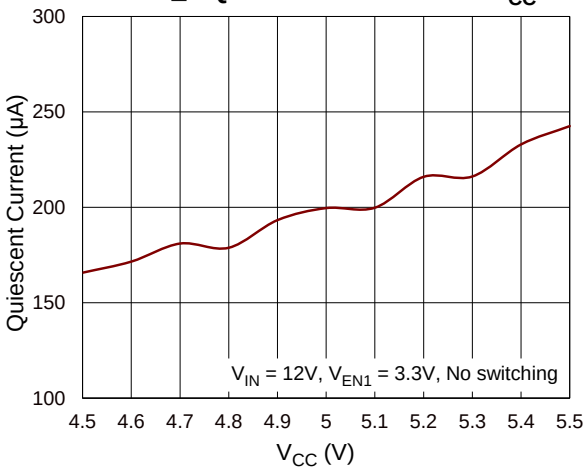
VCC_C Frequency vs. Output Current



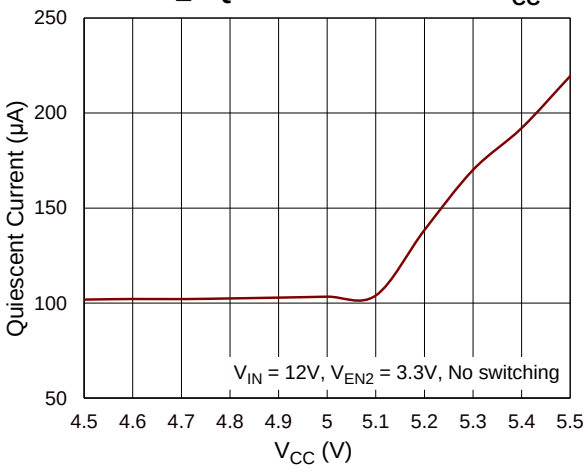
VCC_D Frequency vs. Output Current



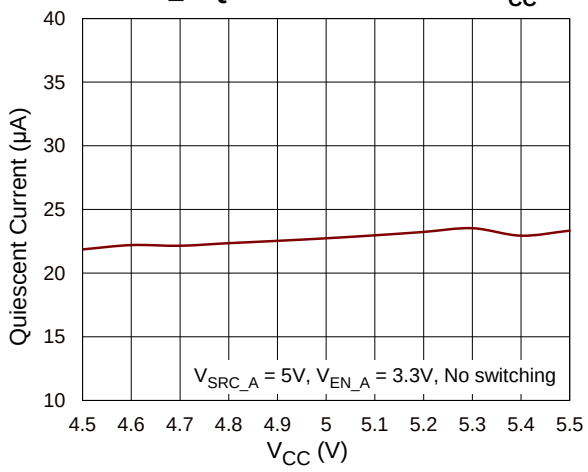
VCC_1 Quiescent Current vs. V_{CC}



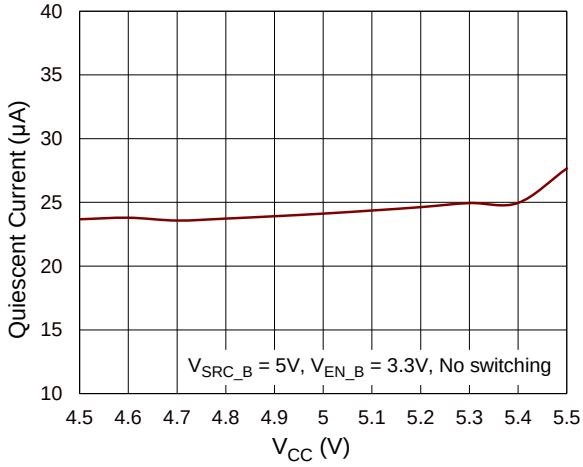
VCC_2 Quiescent Current vs. V_{CC}



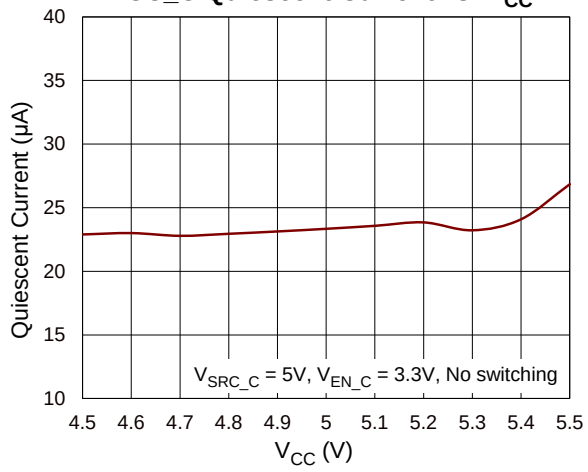
VCC_A Quiescent Current vs. V_{CC}



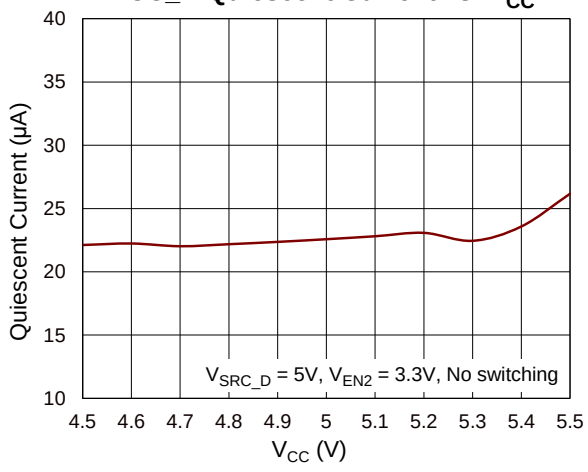
VCC_B Quiescent Current vs. V_{CC}



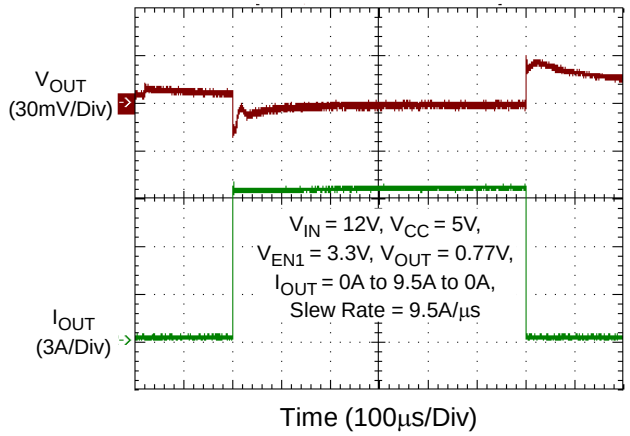
VCC_C Quiescent Current vs. V_{CC}



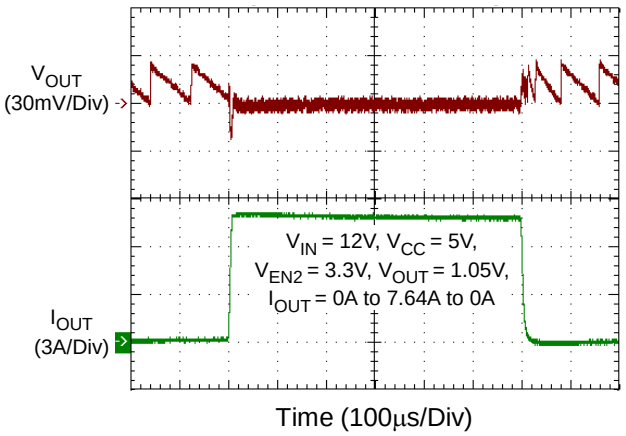
VCC_D Quiescent Current vs. V_{CC}



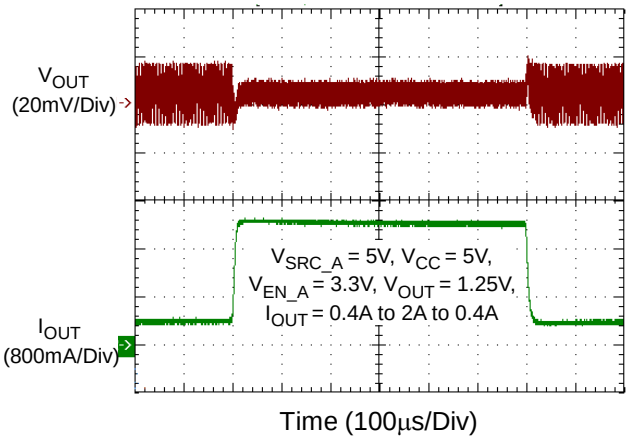
VCC_1 Load Transient Response



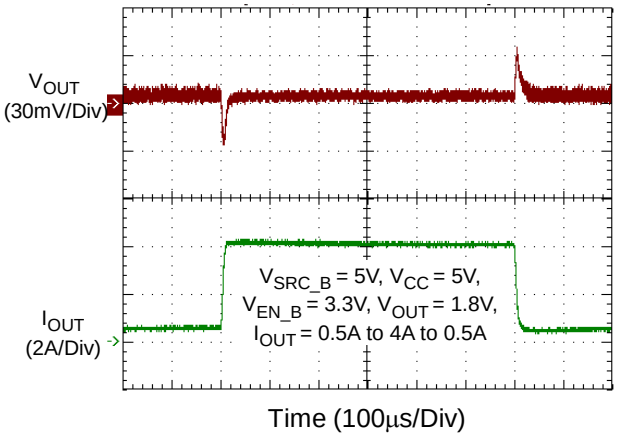
VCC_2 Load Transient Response



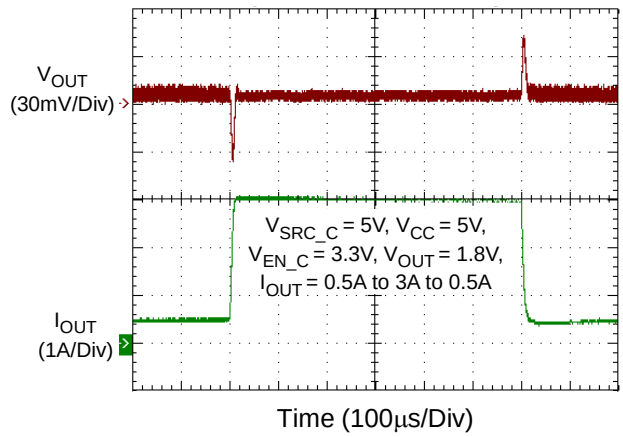
VCC_A Load Transient Response



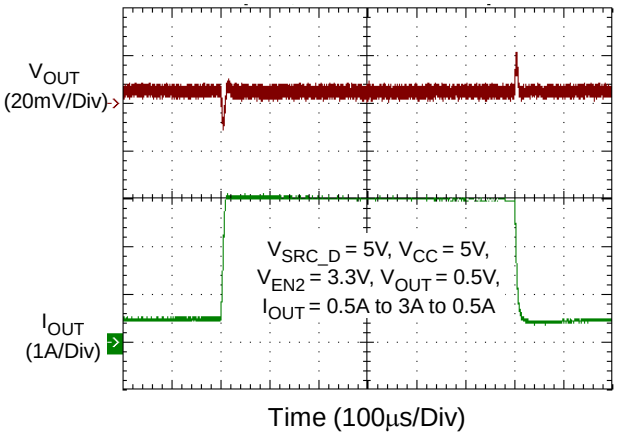
VCC_B Load Transient Response



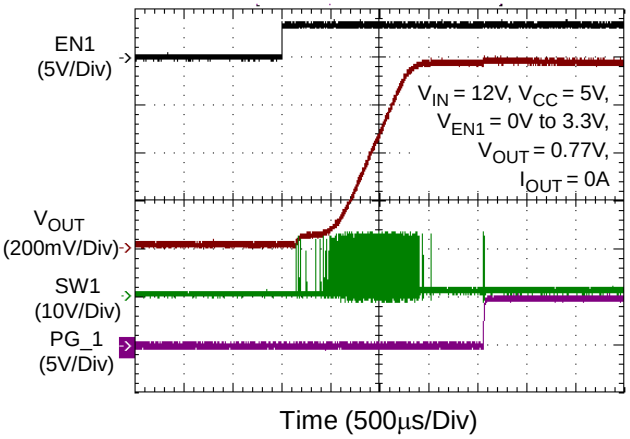
VCC_C Load Transient Response



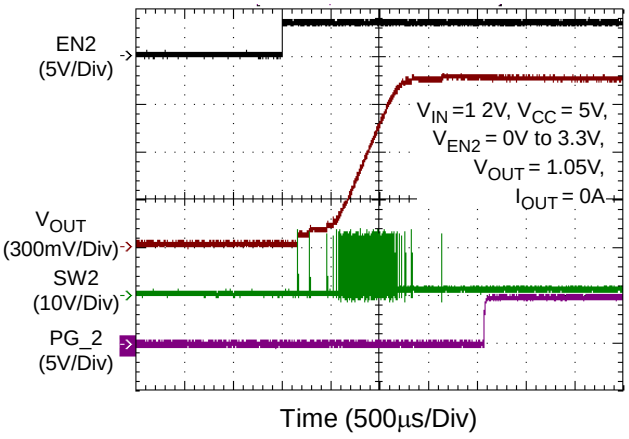
VCC_D Load Transient Response



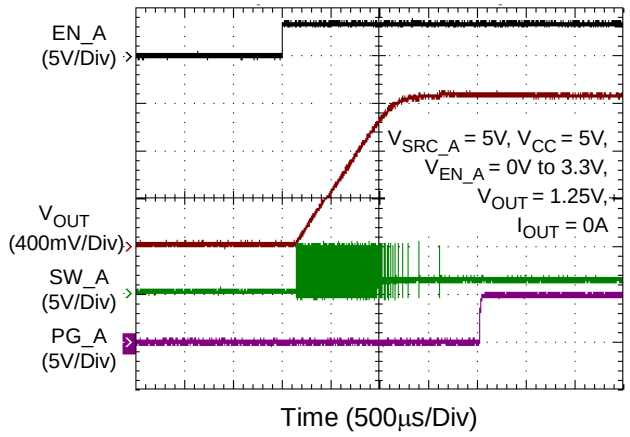
VCC_1 Power On from EN1



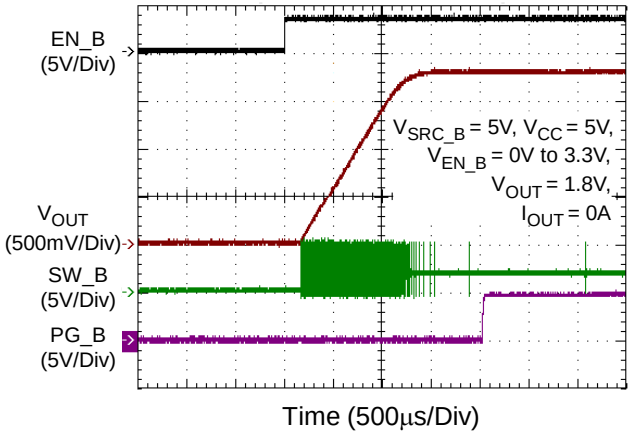
VCC_2 Power On from EN2



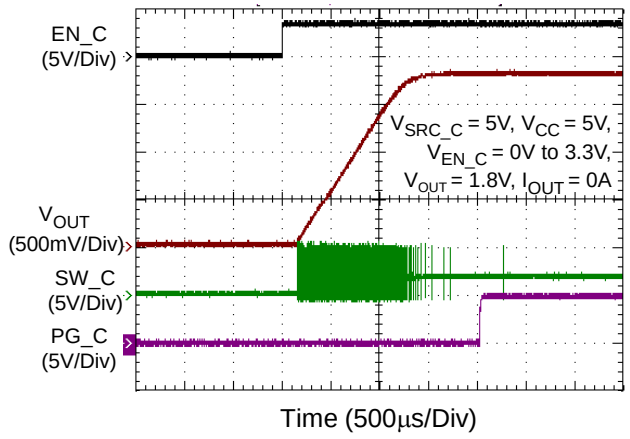
VCC_A Power On from EN_A



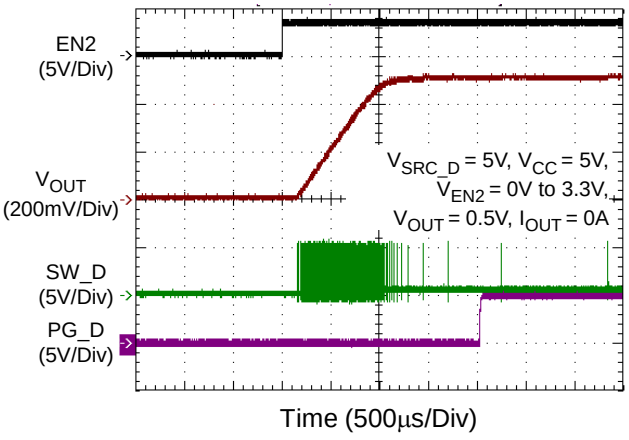
VCC_B Power On from EN_B



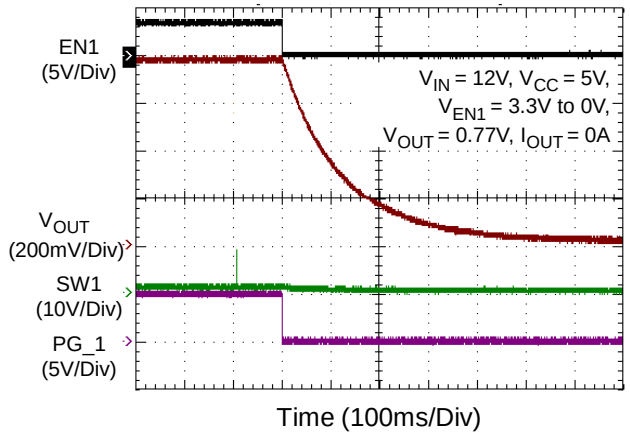
VCC_C Power On from EN_C



VCC_D Power On from EN2



VCC_1 Power Off from EN1



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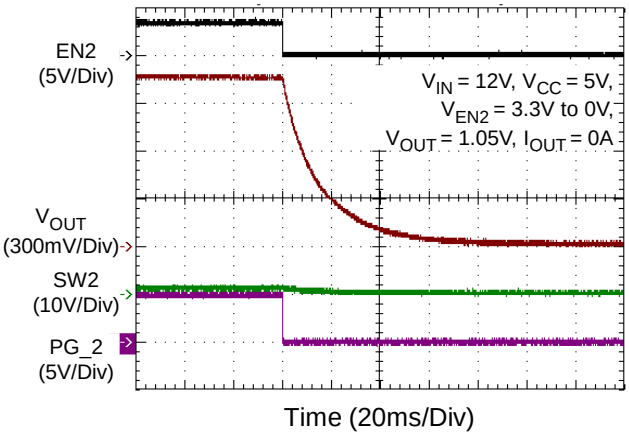
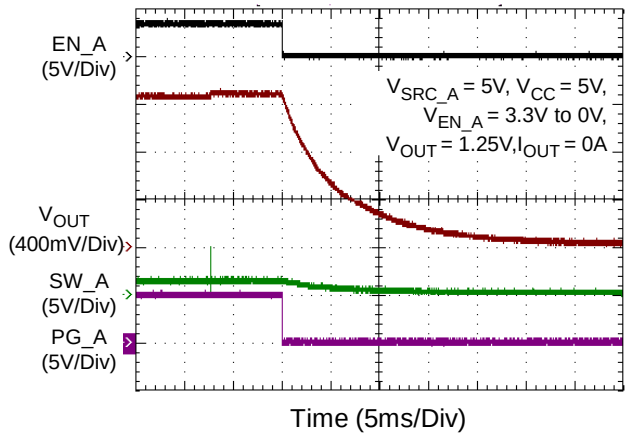
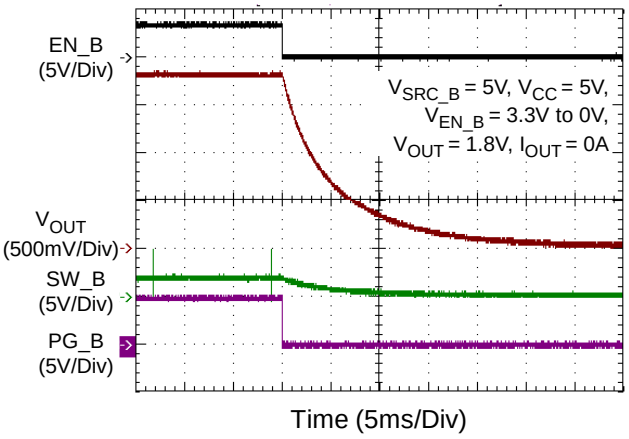


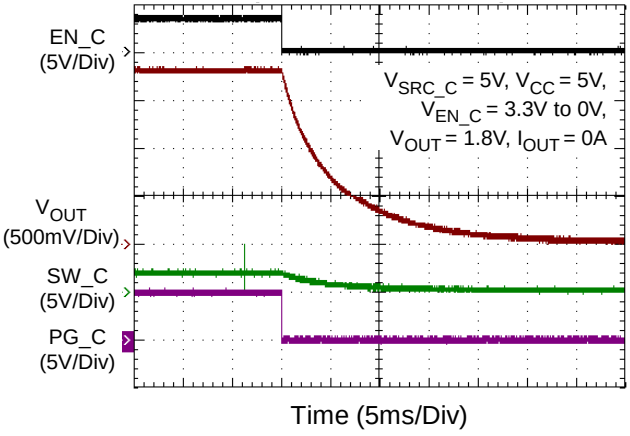
VCC_A Power Off from EN_A



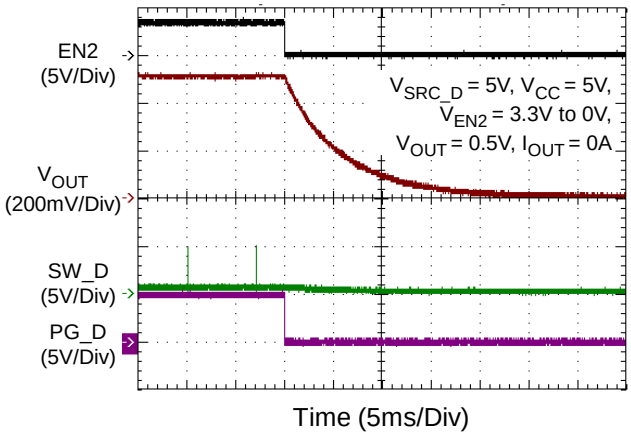
VCC_B Power Off from EN_B



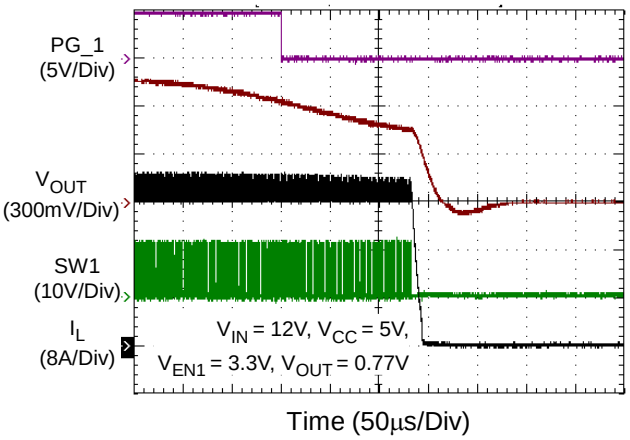
VCC_C Power Off from EN_C



VCC_D Power Off from EN2



VCC_1 Undervoltage Protection



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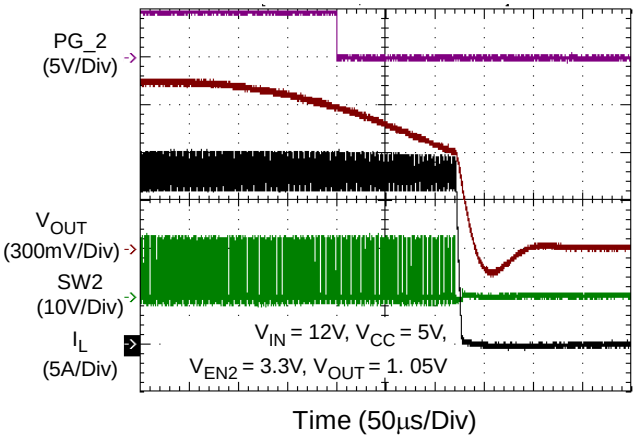
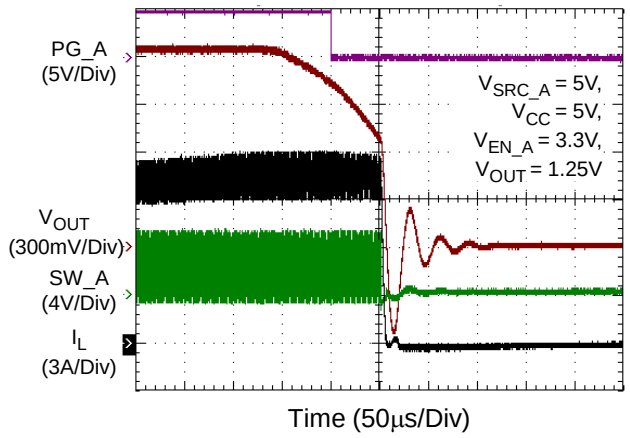
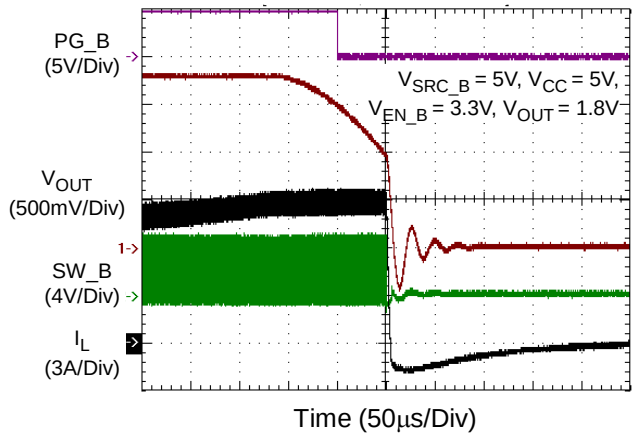


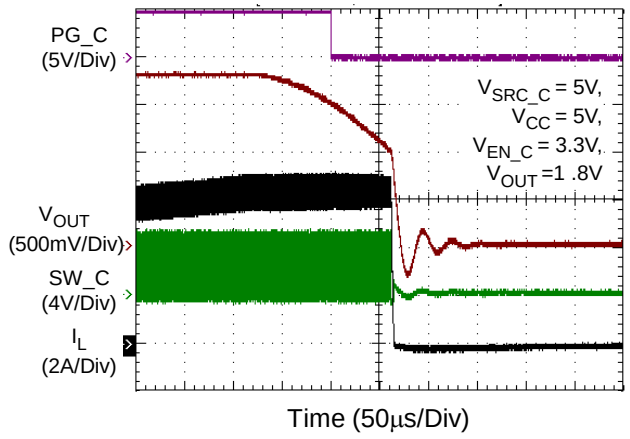
VCC_A Undervoltage Protection



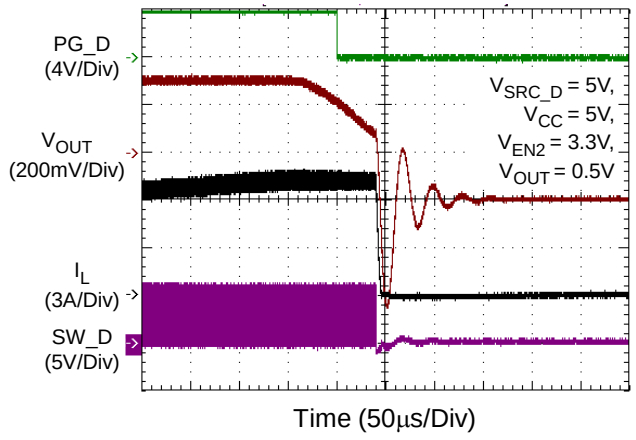
VCC_B Undervoltage Protection



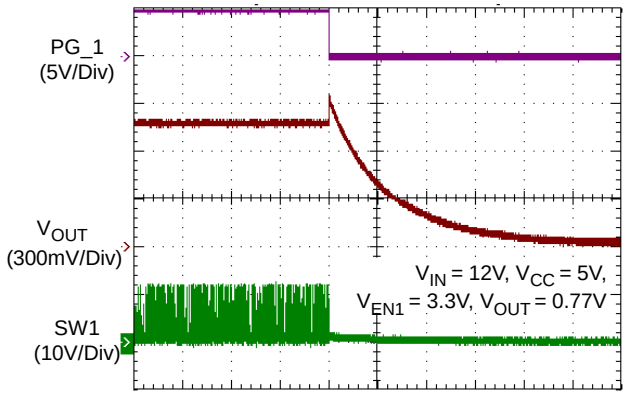
VCC_C Undervoltage Protection



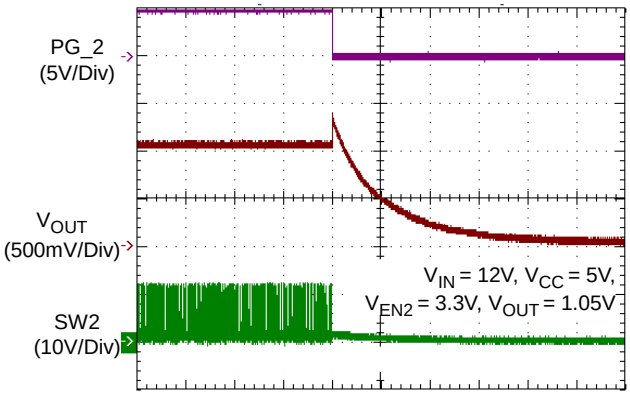
VCC_D Undervoltage Protection



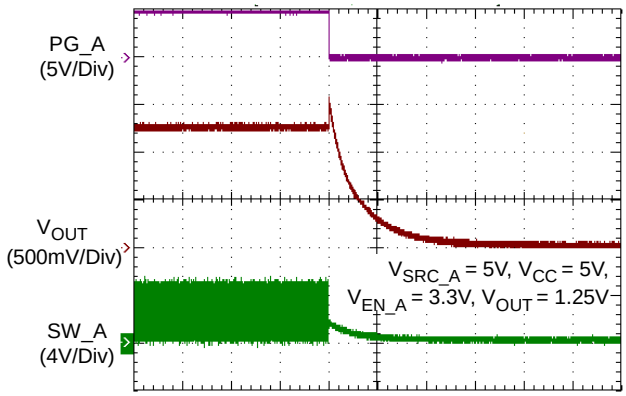
VCC_1 Overvoltage Protection



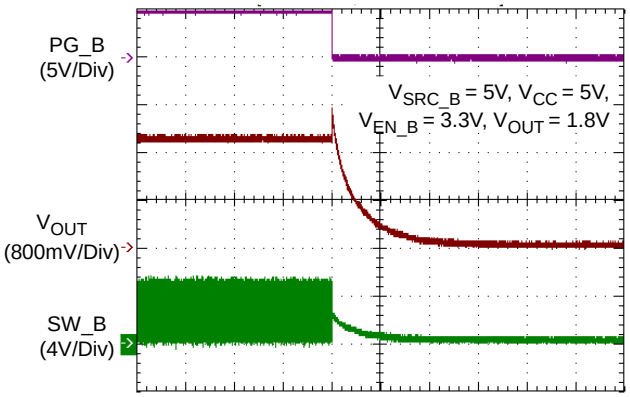
VCC_2 Overvoltage Protection



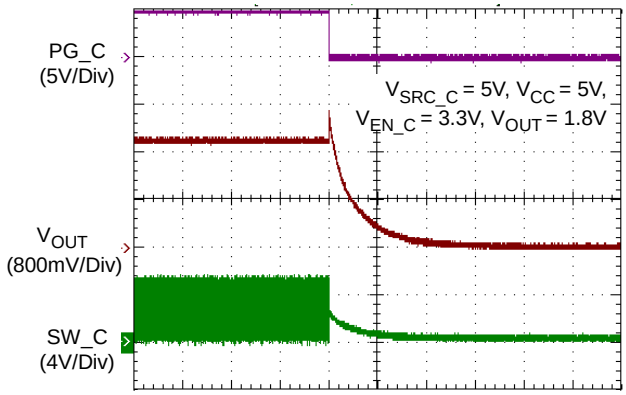
VCC_A Overvoltage Protection



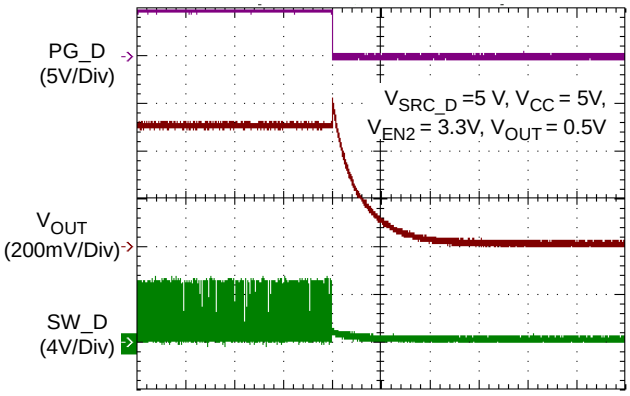
VCC_B Overvoltage Protection



VCC_C Overvoltage Protection



VCC_D Overvoltage Protection



15 Operation

The RT5128A is a multi-output integrated circuit (MOIC) for use with Intel MTL-UPH and AMD SVI3 mobile CPU platforms. The RT5128A integrates two buck controllers, four buck converters, and one load switch. Furthermore, the RT5128A supports both DDR5 and LPDDR5 applications.

15.1 Step-Down Converter

The VCC_A to VCC_D outputs are COT buck converters, while VCC_1 and VCC_2 function as controllers. Each of the VCC_A to VCC D converters integrates a high-side P-MOSFET and a low-side N-MOSFET. These COT buck converters are designed to provide a fast transient response and good stability with minimum output capacitance. To simplify the design and reduce costs, an internal compensation network is utilized, eliminating the need for an external compensation network for loop stability.

The feedback voltage is injected into the feedback network to generate a control signal for the one-shot on-time generator. The duration of the high-side turn-on is determined by the switching frequency, input voltage, and output voltage. Once the on-time duration expires, the low-side MOSFET turns on until the internal ramp is lower than the control signal. The duration of the low-side turn-on is therefore dependent on the output voltage level and the load current. A decrease in load current from a heavy load will cause the inductor current to reduce and eventually approach valley zero current, making the transition from continuous conduction mode to discontinuous conduction mode. To maintain high efficiency, the low-side MOSFET is turned off during off-time when the inductor current nears zero. If the load current continues to decrease, the switching frequency will reduce accordingly.

The buck converters and controllers are implement with OCP, OVP and undervoltage (UVP) to avoid the unexpected events.

15.2 Load Switch

The load switch (LSW) incorporates a low-resistance N-channel power switch MOSFET, which minimizes voltage drop. It features an adjustable slew rate to mitigate inrush current during power-up and boasts an extremely low quiescent current.

15.3 VCC Power-On Reset (POR), UVLO

The power-ready detection circuit, as shown in Figure 5, monitors the VCC voltage for a power-on reset with a typically rising-edge threshold of 3.8V and approximately 200mV of hysteresis voltage for the comparator. When VCC exceeds the POR threshold, the buck regulator initiates startup once EN exceeds 1V. In contrast, driving the EN pin below 0.4V turns off the buck regulator and clears all fault states. To prevent noise disturbance, the supplied bias voltage must be stable. An RC filter (R = 2.2Ω /0603 and C = 1μF/0603) should be connected from the bias voltage to the VCC pin and placed as close as possible to the VCC pin.

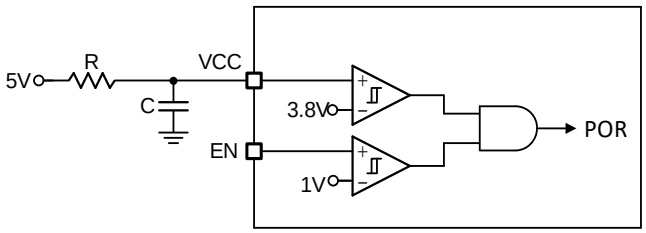


Figure 5. Circuit of Power Ready Detection

15.4 Power Good

The PG pin is an open-drain output and requires a pull-up resistor. During the soft-start period, PG remains low. When EN goes high and the output voltage exceeds the PG threshold for more than 2ms (typical), PG is pulled

high and latched. If the output voltage drops below the PG falling threshold, PG is immediately pulled low.

15.5 Buck Overcurrent Limit

The overcurrent limit is implemented using a cycle-by-cycle detected circuit. The switching current is monitored by measuring the low-side voltage between the SW pin and GND. The voltage is proportional to the switch current and the on-resistance of the low-side MOSFET.

If the sensed current exceeds the current-limit threshold, the converter maintains the low-side in the on state until the sensed voltage drops below the voltage proportional to the current limit, at which point a new switching cycle begins.

15.6 Undervoltage Protection (UVP)

The output voltages of all rails except for LSW, are continuously monitored for undervoltage protection. The UVP detection function is enabled after the soft-start process is completed to ensure a correct startup. If the output voltage drops below the UVP threshold, the UVP circuit will turn off the rail and latch it. In the meanwhile, PG will be pulled low if the output voltage is below the PG threshold. A typical Undervoltage Protection mechanism is shown in Figure 6.

The UVP thresholds for VCC_1/2/A/B/C/D are set at 60% of the output voltage.

To reset the latched state, either recycle the VCC power or toggle the enable pin.

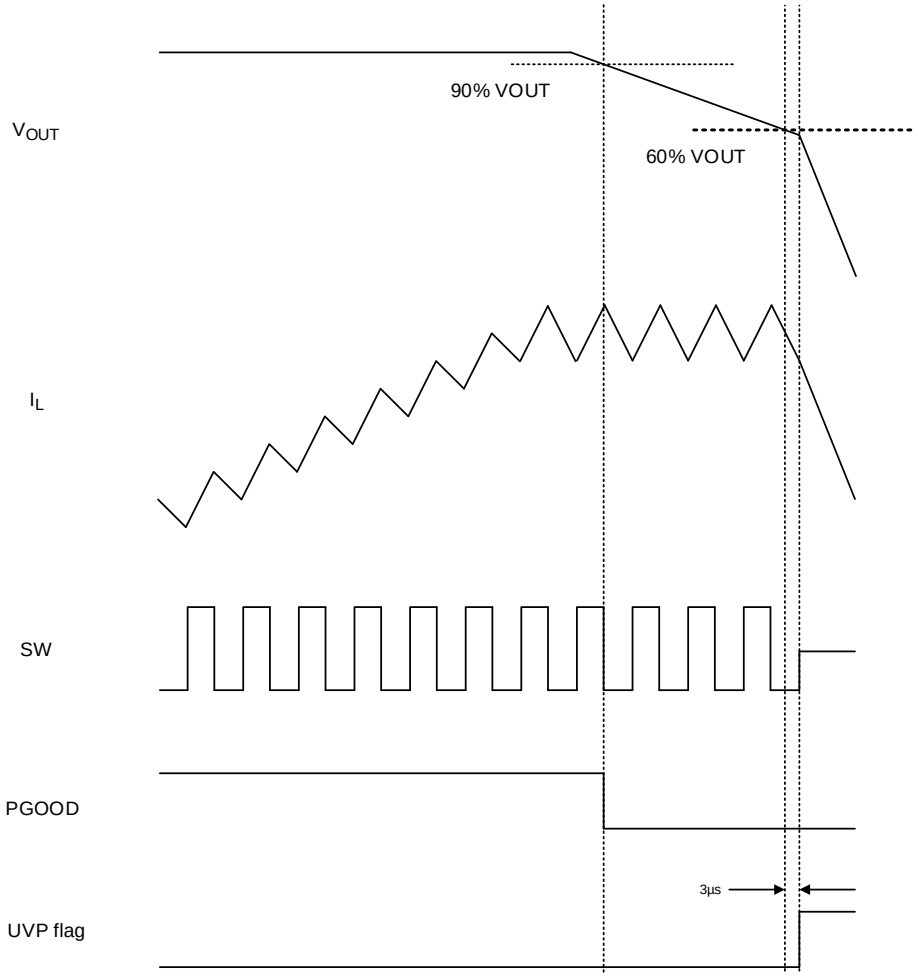


Figure 6. Typical UVP Mechanism

15.7 Overvoltage Protection (OVP)

The output voltage of all rails, except for LSW, is continuously monitored for overvoltage protection. The OVP detection is enabled after the soft-start process is completed to ensure a correct startup. Once the output voltage exceeds the OVP threshold, the OVP circuit will turn off the rail and become latched. Meanwhile, the PG will be pulled low. A typical Overvoltage Protection mechanism is shown in Figure 7. The OVP thresholds of VCC_1/2/A/B/C/D are set at 120% of the output voltage.

To cancel the latched behavior, either re-cycle VCC power or re-toggle the enable.

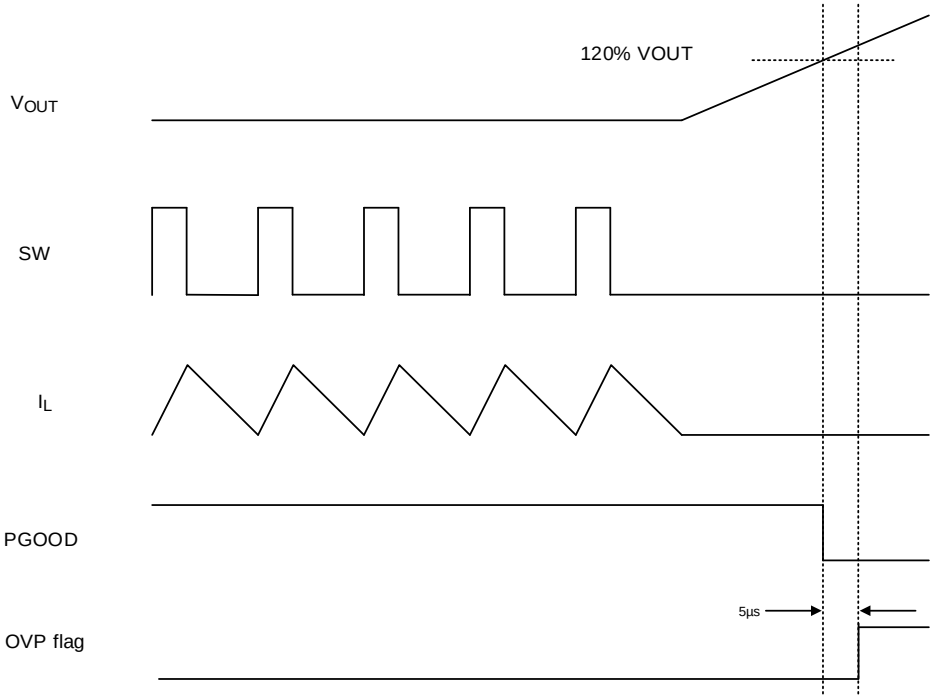


Figure 7. Typical OVP Mechanism

15.8 Over-Temperature Protection (OTP)

If the temperature of the IC exceeds 150°C, the OTP circuit activates, causing all power rails to shut down, and PG will go low. Recovery is possible by toggling the enable once the temperature of the PMIC drops below 125°C. A typical Over-Temperature Protection mechanism is shown in Figure 8.

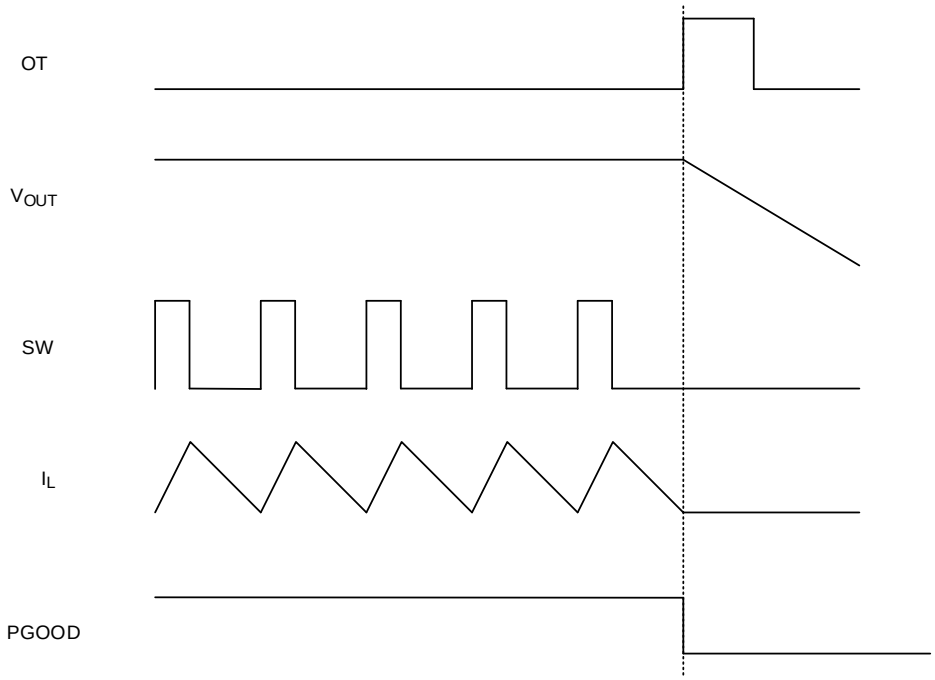


Figure 8. Typical OTP Mechanism

16 Application Information

Richtek's component specification does not include the following information in the Application Information section. Thereby no warranty is given regarding its validity and accuracy. Customers should take responsibility to verify their own designs and reserve suitable design margin to ensure the functional suitability of their components and systems.

The RT5128A provides two buck controllers, four buck converters, and one load switch to satisfy the power system requirements of both Intel or AMD processors. It operates in coordination with EC and communicates via an I^2C interface. The I^2C interface allows for flexible configuration of each power rail, including default switching frequency, power-up sequence, and fault handling, among other functions. Table 2 summarizes the key characteristics of the voltage rails. This section offers general application information and a detailed description of the RT5128A's features.

Table 2. Summary of Voltage Rails

Rail	Type	Input Voltage (V)		Switching frequency (kHz)	Output Voltage (V)			Current (A)
		Min	Max		Min	Default	Max	
VCC_1	Step-down Controller	4.5	23	600	0.6	Set by FB_1 Pin	1.1	By Ext-MOSFET
VCC_2	Step-down Controller	4.5	23	600	1.044	1.05 Set by DDR_ID	1.056	By Ext-MOSFET
VCC_A	Step-down Converter	2.7	5.5	800	0.6	Set by FB_A Pin	3.8	6
VCC_B	Step-down Converter	2.7	5.5	1200	0.6	Set by FB_B Pin	3.8	6
VCC_C	Step-down Converter	2.7	5.5	1200	0.6	Set by FB_C Pin	3.8	4
VCC_D	Step-down Converter	2.7	5.5	1200	0.497	0.5 Set by DDR_ID	0.503	3

16.1 Buck Regulator

The RT5128A features four high-efficiency, COT-based synchronous buck converters that deliver a range of output voltages.

Each switching regulator is optimized for extreme low quiescent current (<35μA) and maintains high efficiency across the full load range. The high-frequency switching allows for a smaller external LC filter, resulting in minimal output voltage ripple.

Additional features of these buck regulators include soft-start, discharge resistance, undervoltage protection, overvoltage protection, overcurrent protection, and thermal shutdown protection.

If one of the protections is activated or if EN is driven low during operation, the affected power rail will be shut down and require manual reset.

Other protections cause the rail's output voltage to discharge (if enabled) and will automatically reset once the fault condition no longer exists.

Through the I^2C interface, users can program the current-limit threshold, adjust the PWM frequency, and toggle the on/off state of each buck converter. Additionally, the PWM controller offers the flexibility to switch between forced PWM mode and PSM.

Note 5. For the power-up sequence of VCC1/2, ensure that V_{IN} is stable before applying power to EN and VCC.

16.2 Power-Up Sequencing and On/Off Controls (ENx)

EN1/2 and EN_A/B/C/LSW control the power-up sequencing of the two buck controllers, the four buck converters and the one load switch. Among these controls, EN_2 includes the enable control for both VCC_2 and VCC_D. The 0.4V falling edge threshold on ENx can be used to detect a specific analog voltage level and to shut down the rail. Upon shutdown, the 1V rising edge threshold becomes active, providing sufficient hysteresis for most applications. Additionally, the RT5128A EN_1/2 supports MLCC and POSCAP output capacitor types, determined by the EN_1/2 level. When EN_1/2 is between 1V to 1.5V, the operating mode is at MLCC mode. When EN_1/2 is above 1.7V, the RT5128A operates at POSCAP mode. The RT5128A also provides the enable software control. The compensation mode (Output capacitor type) can be controlled by I^2C.

When 0x48[0] is set to 1, the RT5128A rails can be powered on through I^2C setting.

16.3 DDR Voltage Selection

The output voltage of DDR can be set by the DDR_ID pin. The 0.4V falling edge threshold on DDR_ID can be used to detect a specific analog voltage level and to set DDR5. Upon reaching the 1V rising edge threshold, the settings switches to LPDDR5.

Table 3. DDR Voltage Selection Recommendation

DDR_ID	Memory type	VCC_2	VCC_D
High (>1V)	LPDDR5	1.05	0.5
Low (<0.4V)	DDR5	1.1	1.1

16.4 Current Limit

The RT5128A provides cycle-by-cycle current limit control by detecting the switch node voltage drop across the low-side MOSFET when it is turned on. The current limit circuit employs a "valley" current sensing algorithm, as shown in Figure 9.

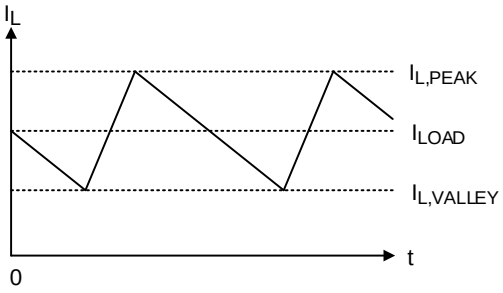


Figure 9. Valley Current Limit

In an overcurrent condition, the current to the load exceeds the average output inductor current. Thus, the output voltage falls and eventually crosses the undervoltage protection threshold, inducing IC shutdown.

16.5 Current Limit Setting

The OC level (V_{CL}) of the buck controller can be programmed via I^2C. The current limit can be calculated using the following equation:

$$I_{VALLEY} = \frac{V_{CL}}{R_{DS(ON)\_LG}}$$

where I_{VALLEY} represents the desired inductor limit current (valley inductor current). I_{VALLEY} value is based on the V_{CL} and $R_{DS(ON)\_LG}$.

16.6 Inductor Selection

Selecting the right inductor for a buck converter requires a balance among several factors: inductance, peak current capability, physical size, cost, and circuit efficiency. The choice of inductance is generally flexible, aimed at finding the optimal balance among these factors.

Lower inductor values benefit from reducing physical size and cost. They can also enhance the circuit's transient response. However, they lead to higher inductor ripple current and output voltage ripple, potentially reducing efficiency due to increased peak currents.

Conversely, higher inductor values can improve efficiency by reducing ripple currents but may lead to a larger physical size or higher resistance due to the need for more wire turns. This can also slow down the transient response due to the longer time required to change the inductor current (up or down).

To calculate the inductance value, consider the input and output voltages, switching frequency (f_{SW}), maximum output current ($I_{OUT(MAX)}$), and estimate a ripple current ΔI_L as a percentage of the full output load current. A good starting point is to aim for a ripple current (ΔI_L) of about 20-50% of the full output load current.

$$L = \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{f_{SW} \times \Delta I_L \times V_{IN(MAX)}}$$

Once an inductor value is determined, the ripple current (ΔI_L) is calculated to determine the required peak inductor current.

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{f_{SW} \times L \times V_{IN}} \text{ and } I_{PEAK} = I_{OUT(MAX)} + \frac{\Delta I_L}{2}$$

To ensure the required output current, the inductor should have a saturation current rating and a thermal rating that exceeds $I_{L(PEAK)}$. These are the minimum requirements. For controlling inductor current in overload and short-circuit conditions, some applications may require current ratings up to the current limit value. However, the IC's output undervoltage shutdown feature makes this unnecessary for most applications.

For optimal efficiency, select an inductor with a low DC resistance that meets the cost and size requirements. For reduced inductor core losses, shielded ferrite cores are usually preferable. Although they may be larger or more expensive, they tend to cause fewer EMI and other noise issues.

16.7 Output Capacitor Selection

The output ripple at the switching frequency is caused by the peak-to-peak inductor current ripple and its effect on the output capacitor's equivalent series resistance (ESR), ESL, and stored charge. These three ripple components are referred to as ESR ripple, ESL ripple, and capacitive ripple. Since ceramic capacitors have extremely low ESR and ESL, and relatively little capacitance, all these components should be considered if minimizing ripple is critical. The formulas to describe each component are listed below:

$$V_{RIPPLE} = V_{RIPPLE(ESR)} + V_{RIPPLE(ESL)} + V_{RIPPLE(C)}$$

$$V_{RIPPLE(ESR)} = \Delta I_L \times R_{ESR}$$

$$V_{RIPPLE(ESL)} = \frac{d}{dt} I_L \times ESL$$

$$V_{RIPPLE(C)} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

where the ΔI_L is the peak-to-peak inductor ripple current and R_{ESR} is the equivalent series resistance of C_{OUT}. The output ripple is highest at the maximum input voltage, as ΔI_L increases with input voltage. To meet the ESR and RMS current handling requirements, it may be necessary to place multiple capacitors in parallel. Regarding the transient loads, the V_{SAG} and V_{SOAR} requirements should be taken into account when selecting the output capacitance value. The magnitude of output sag is a function of the maximum duty cycle, which is determined by the on-time of the switch and the minimum off-time.

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times f_{SW}}$$

$$D_{MAX} = \frac{t_{ON}}{t_{ON} + t_{OFF\_MIN}}$$

The worst-case output sag voltage can be determined by the following equation:

$$\Delta V_{OUT\_SAG} = \frac{L \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times (V_{IN} \times D_{MAX} - V_{OUT})}$$

The amount of voltage overshoot due to stored inductor energy when the load is removed can be calculated as:

$$\Delta V_{OUT\_SOAR} = \frac{L \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times V_{OUT}}$$

Ceramic capacitors are known for their very low ESR and preferred for optimal ripple performance. However, it is important to consider the voltage coefficient of ceramic capacitors when selecting the appropriate value and case size. It should be noted that many ceramic capacitors can lose 50% or more of their rated capacitance when operated near their rated voltage.

16.8 Input Capacitor Selection

An input capacitance, C_{IN}, is required to filter the pulsating current at the drain of the high-side power MOSFET. C_{IN} should be sized to do this without causing a large variation in input voltage. The peak-to-peak voltage ripple

on the input capacitor can be estimated using the following equation:

$$\Delta V_{CIN} = D \times I_{OUT} \times \frac{1-D}{C_{IN} \times f_{SW}} + I_{OUT} \times ESR$$

where D is calculated as follows:

$$D = \frac{V_{OUT}}{V_{IN} \times \eta}$$

For ceramic capacitors, which have a very low equivalent series resistance (ESR), the ripple caused by ESR can be ignored, and the minimum input capacitance can be estimated using the following equation:

$$C_{IN\_MIN} = I_{OUT\_MAX} \times \frac{D(1-D)}{\Delta V_{CIN\_MAX} \times f_{SW}}$$

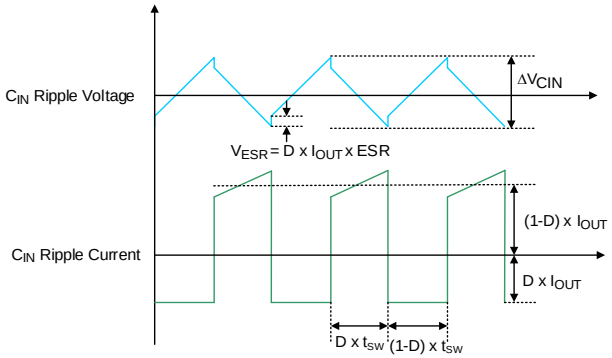


Figure 10. CIN Ripple Voltage and Ripple Current

Besides the ripple-voltage requirement, the ceramic capacitors should meet the thermal stress requirement as well. The input capacitor is used to supply the input RMS current, which can be approximately calculated using the following equation:

$$I_{RMS} = \sqrt{\frac{V_{OUT}}{V_{IN}} \left[\left(1 - \frac{V_{OUT}}{V_{IN}} \right) \times I_{OUT}^2 + \frac{\Delta I_L^2}{12} \right]}$$

Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life, which makes it advisable to either further de-rate the capacitor or choose a capacitor with a higher temperature rating than required.

Place the input capacitor as close as possible to the VIN and GND pins of the IC to minimize impedance and improve performance.

Besides, since the ESL of ceramic capacitors plays a significant role on voltage spike at the input and phase node, it is desirable to add a small capacitor with low ESL near the VIN pin.

16.9 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a UQFN-42L 5x5 (FC) package, the thermal resistance, θ_{JA}, is 19.52°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C – 25°C)/(19.52°C/W) = 5.12W for a UQFN-42L 5x5 (FC) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curve in Figure 11 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

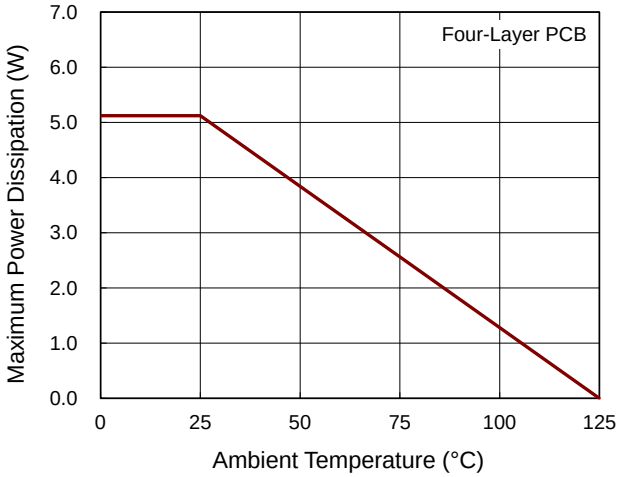


Figure 11. Derating Curve of Maximum Power Dissipation

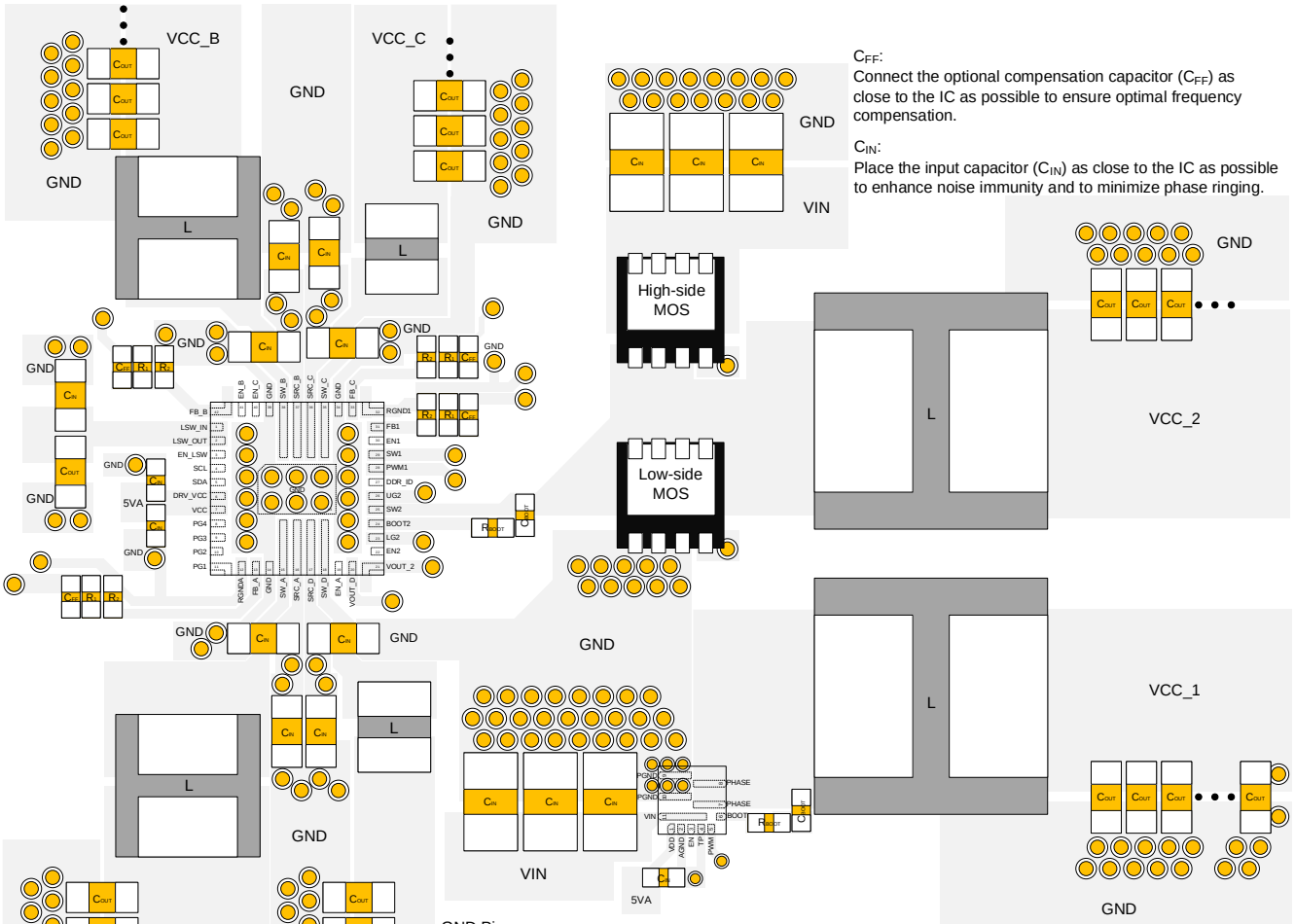
16.10 Layout Considerations

The design of printed circuit board (PCB) layouts for switch-mode power supply ICs is both critical and important. An improper PCB layout can cause numerous problems for the power supply, including poor output voltage regulation, switching jitter, bad thermal performance, excessive noise radiation, and reduced component reliability. To avoid those issues, designers have to understand current trace and signal flow in the switching power supply. The following suggestions are design considerations for PCB layouts in switching power supplies.

- Place the input capacitor close to VIN pin to suppress phase ringing and extra power losses, thereby enhancing device reliability by reducing the influence of parasitic inductance.
- Minimize thermal stress and power consumption by ensuring the current paths of V_{IN} and V_{OUT} are as short and wide as possible, thereby decreasing the trace impedance.
- Given the SW node voltage swings from V_{IN} to 0V with rapid rising and falling times, the switching power supply is prone to significant EMI issues. To eliminate EMI problems, the inductor must be put as close as possible to IC to narrow the SW node area. Besides, the SW node should be arranged in the same plate to reduce coupling noise path caused by parasitic capacitance.
- For system stability and coupling noise elimination, the sensitive components and signals, such as control signal and feedback loop, should be kept away from SW node.

- To enhance noise immunity on VCC pin, the decoupling capacitor must be connected from VCC to AGND, and the capacitor should be placed close to IC.
- The feedback signal path from VOUT to IC should be wide and kept away from high switching path.
- The trace width and numbers of via should be designed based on application current. Make sure the switching power supply has great thermal performance and good efficiency.

For reference, Figure 12 illustrates an example of PCB layout guidelines.



C_{FF}:
Connect the optional compensation capacitor (C_{FF}) as close to the IC as possible to ensure optimal frequency compensation.

C_{IN}:
Place the input capacitor (C_{IN}) as close to the IC as possible to enhance noise immunity and to minimize phase ringing.

GND Pin:
To improve thermal performance, ensure that the vias under the IC penetrate at least two layers of the GND plane.

AGND, AGND1 Pins:
Connect the AGND, AGND1, and GND pins using a single-point grounding technique to prevent ground potential differences.

SW1/2, SW_A/B/C/D Pins:
SW_A/B/C/D) to the inductor using wide and short traces to minimize impedance and avoid the use of vias, which can introduce inductance. Additionally, position sensitive components away from these areas to prevent interference.

Figure 12. Layout Suggestions for the RT5128A

16.11 I²C Interface

The I²C Interface facilitates communication with the RT5128A, which is assigned the address 0x34. Figure 13 shows the I²C communication format utilized by the RT5128A.

The bus enables both read and write access to the device's internal performance registers. Through these operation speeds of up to 1MHz, allowing for efficient adjustment of the operating parameters via the I²C interface.

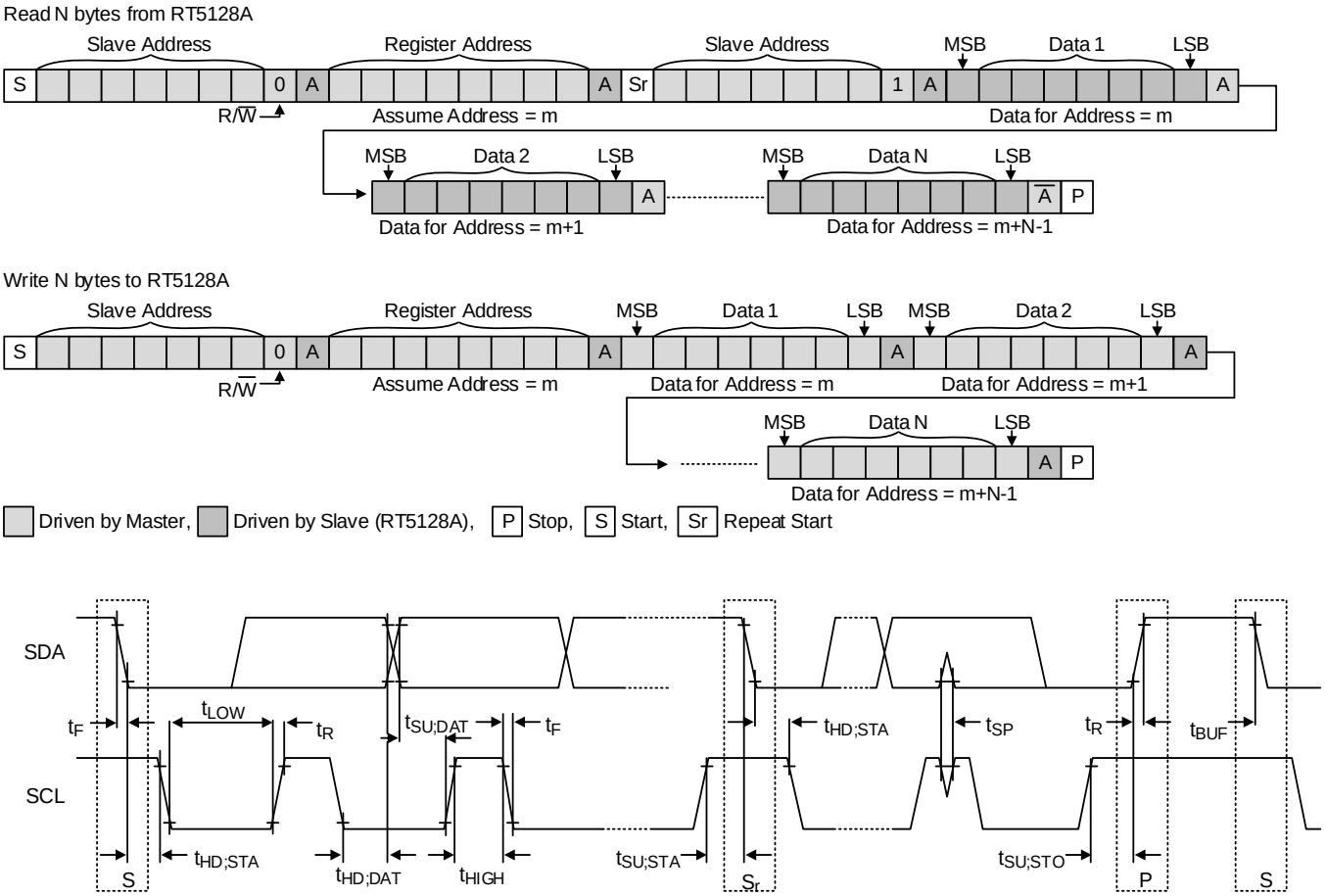


Figure 13. I²C Format and Waveform Information

17 Function Register Table

Table 4. I²C Register Map

Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	Type
0x00	VENDORID	VENDOR_ID								0x67	R
0x01	REVID	MAJREV				MINREV				0xA0	R
0x48	CONTROL	Reserved							SW_CTRL	0x00	R/W
0x49	RESET	Reserved						CLR_FAULT	SW_RST	0x00	R/W
0xD0	SW_MODE	VCC_2_COMP_MODE	VCC_1_COMP_MODE	VCC_D_MODE	VCC_C_MODE	VCC_B_MODE	VCC_A_MODE	VCC_2_MODE	VCC_1_MODE	0x00	R/W
0xD1	SW_EN	Reserved	SW_LSW_EN	SW_VCC_D_EN	SW_VCC_C_EN	SW_VCC_B_EN	SW_VCC_A_EN	SW_VCC_2_EN	SW_VCC_1_EN	0x00	R/W
0xD2	EN_STATE	Reserved	LSW_STATE	VCC_D_STATE	VCC_C_STATE	VCC_B_STATE	VCC_A_STATE	VCC_2_STATE	VCC_1_STATE	0x00	R
0xD3	PG_STATE	PROCHOT	VCC_UVLOB	VCC_D_PG	VCC_C_PG	VCC_B_PG	VCC_A_PG	VCC_2_PG	VCC_1_PG	0x00	R
0xD4	THSD_UVP_REC	Reserved	THSD_STS	VCC_D_UVP_STS	VCC_C_UVP_STS	VCC_B_UVP_STS	VCC_A_UVP_STS	VCC_2_UVP_STS	VCC_1_UVP_STS	0x00	R
0xD5	OVP_REC	Reserved	Reserved	VCC_D_OVP_STS	VCC_C_OVP_STS	VCC_B_OVP_STS	VCC_A_OVP_STS	VCC_2_OVP_STS	VCC_1_OVP_STS	0x00	R
0xD6	PROCHOT_VCC_2_OS	PROCHOT_EN	PROCHOT_SET		Reserved	VCC_2_OS				0xA8	R/W
0xD7	VCC_D_OS	Reserved					VCC_D_OS			0x02	R/W
0xD8	DISCH_CTRL1	VCC_D_RDIS		VCC_C_RDIS		VCC_B_RDIS		VCC_A_RDIS		0x55	R/W
0xD9	DISCH_CTRL2	Reserved		LSW_RDIS		VCC_2_RDIS		VCC_1_RDIS		0x25	R/W
0xDA	OC_CTRL1	VCC_D_CL		VCC_C_CL		VCC_B_CL		VCC_A_CL		0xF0	R/W
0xDB	OC_CTRL2	Reserved				VCC_2_VCL		VCC_1_VCL		0x09	R/W
0xDC	FSW_CTRL1	VCC_D_FSW		VCC_C_FSW		VCC_B_FSW		VCC_A_FSW		0x01	R/W
0xDD	FSW_CTRL2	VCC_2_FSW		VCC_2_SPREAD_EN	VCC_1_SPREAD_EN	VCC_1_TON_SHRINK		VCC_1_FSW		0x41	R/W
0xDE	PG_CONFIG1	PG1_TEST_SETTING	PG1_SETTING			PG2_TEST_SETTING	PG2_SETTING			0x01	R/W
0xDF	PG_CONFIG2	PG3_TEST_SETTING	PG3_SETTING			PG4_TEST_SETTING	PG4_SETTING			0x24	R/W

Table 5. VENDORID

Address: 0x0B Description: RT5128A ID Register.								
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field	VENDORID[7:0]							
Default	0	1	1	0	0	1	1	1
Type	R							

Bit	Name	Description
7:0	VENDORID	Vendor ID

Table 6. REVID

Address: 0x01 Description: PMIC Vendor ID Register.								
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field	MAJREV[7:4]				MINREV[3:0]			
Default	1	0	1	0	0	0	0	0
Type	R				R			

Bit	Name	Description
7:4	MAJREV	Major Si revision ID. (Hex Number) 1010: A 1011: B 1100: C
3:0	MINREV	Minor Si revision ID. 0000: 0 0001: 1 0010: 2

Table 7. CONTROL

Address: 0x48 Description: PMIC Enable Selection Control Register.								
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field	Reserved							SW_CTRL
Default	0	0	0	0	0	0	0	0
Type	R							R/W

Bit	Name	Description
0	SW_CTRL	Enable software control function: 0: External hardware enables pins control. (default) 1: Internal register SW_EN control.

Table 8. RESET

Address: 0x49 Description: PMIC Reset Register.								
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field	Reserved						CLR_FAULT	SW_RST
Default	0	0	0	0	0	0	0	0
Type	R						R/W	R/W

Bit	Name	Description
1	CLR_FAULT	0: None (default) 1: Clear the fault flags located at the address D4 and D5. Furthermore, the internal latch for fault detection is also reset through the software control configuration. The channel may be re-enabled via the register at address D1 or through the HW enable pin. This bit will automatically reset to 0 after the operation.
0	SW_RST	Setting reset: 0: None (default) 1: Reset the registers (address D0 and D6 to DF) back to the default values. This bit will automatically reset to 0 after the operation.

Table 9. SW_MODE

Address: 0xD0 Description: Controller MLCC/POSCAP, Converter PSM/FCCM Control Register.								
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field	VCC_2_COMP_MODE	VCC_1_COMP_MODE	VCC_D_MODE	VCC_C_MODE	VCC_B_MODE	VCC_A_MODE	VCC_2_MODE	VCC_1_MODE
Default	0	0	0	0	0	0	0	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Description
7	VCC_2_COMP_MODE	VCC_2 compensation mode: 0: MLCC mode (default) 1: POSCAP mode
6	VCC_1_COMP_MODE	VCC_1 compensation mode: 0: MLCC mode (default) 1: POSCAP mode
5	VCC_D_MODE	Operation mode: 0: PSM (default) 1: FCCM
4	VCC_C_MODE	Operation mode: 0: PSM (default) 1: FCCM
3	VCC_B_MODE	Operation mode: 0: PSM (default) 1: FCCM
2	VCC_A_MODE	Operation mode: 0: PSM (default) 1: FCCM
1	VCC_2_MODE	Operation mode: 0: PSM (default) 1: FCCM
0	VCC_1_MODE	Operation mode: 0: PSM (default) 1: FCCM

Table 10. SW_EN

Address: 0xD1 Description: PMIC I2C Enable Control Register.								
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field	Reserved	SW_ LSW_EN	SW_ VCC_ D _EN	SW_ VCC_C_ EN	SW_ VCC_B_ EN	SW_ VCC_A_ EN	SW_ VCC_2_ EN	SW_ VCC_1_ EN
Default	0	0	0	0	0	0	0	0
Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Description
6	SW_LSW_EN	Software LSW_EN: 0: Rail off (default) 1: Rail on
5	SW_VCC_D_EN	Software VCC_D_EN: 0: Rail off (default) 1: Rail on
4	SW_VCC_C_EN	Software VCC_C_EN: 0: Rail off (default) 1: Rail on
3	SW_VCC_B_EN	Software VCC_B_EN: 0: Rail off (default) 1: Rail on
2	SW_VCC_A_EN	Software VCC_A_EN: 0: Rail off (default) 1: Rail on
1	SW_VCC_2_EN	Software VCC_2_EN: 0: Rail off (default) 1: Rail on
0	SW_VCC_1_EN	Software VCC_1_EN: 0: Rail off (default) 1: Rail on

Table 11. EN_State

Address: 0xD2 Description: The Enable State of The Rails.								
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field	Reserved	LSW_ STATE	VCC_D_ STATE	VCC_C_ STATE	VCC_B_ STATE	VCC_A_ STATE	VCC_2_ STATE	VCC_1_ STATE
Default	0	0	0	0	0	0	0	0
Type	R	R	R	R	R	R	R	R

Bit	Name	Description
6	LSW_STATE	LSW_EN state (Real Time): 0: Off (default) 1: On
5	VCC_D_STATE	VCC_D state (Real Time): 0: Off (default) 1: On
4	VCC_C_STATE	VCC_C state (Real Time): 0: Off (default) 1: On
3	VCC_B_STATE	VCC_B state (Real Time): 0: Off (default) 1: On
2	VCC_A_STATE	VCC_A state (Real Time): 0: Off (default) 1: On
1	VCC_2_STATE	VCC_2 state (Real Time): 0: Off (default) 1: On
0	VCC_1_STATE	VCC_1 state (Real Time): 0: Off (default) 1: On

Table 12. PG_State

Address: 0xD3 Description: Power Good Indicator for Output Rails Status Register.								
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field	PROCHOT	VCC_ UVLOB	VCC_D_ PG	VCC_C_ PG	VCC_B_ PG	VCC_A_ PG	VCC_2_ PG	VCC_1_ PG
Default	0	0	0	0	0	0	0	0
Type	R	R	R	R	R	R	R	R

Bit	Name	Description
7	PROCHOT	Thermal alert: 0: No thermal alert 1: Thermal alert, IC temperature is high, it is a non-latched signal
6	VCC_UVLOB	PMIC control circuit supply VCC UVLOB: 0: In UVLO 1: Not in UVLO
5	VCC_D_PG	VCC_D rail's power good signal for both hardware and software control: 0: Power not ready 1: Power Good
4	VCC_C_PG	VCC_C rail's power good signal for both hardware and software control: 0: Power not ready 1: Power Good
3	VCC_B_PG	VCC_B rail's power good signal for both hardware and software control: 0: Power not ready 1: Power Good
2	VCC_A_PG	VCC_A rail's power good signal for both hardware and software control: 0: Power not ready 1: Power Good
1	VCC_2_PG	VCC_2 rail's power good signal for both hardware and software control: 0: Power not ready 1: Power Good
0	VCC_1_PG	VCC_1 rail's power good signal for both hardware and software control: 0: Power not ready 1: Power Good

Table 13. THSD_UVP_REC

Address: 0xD4
Description: Status Bits to Indicate Whether OT/UV Is Triggered.

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field	Reserved	THSD_ STS	VCC_D _UVP_ STS	VCC_C _UVP _STS	VCC_B _UVP _STS	VCC_A _UVP _STS	VCC_2 _UVP _STS	VCC_1 _UVP _STS
Default	0	0	0	0	0	0	0	0
Type	R	R	R	R	R	R	R	R

Bit	Name	Description
6	THSD_STS	Thermal shutdown protection: 0: No thermal shutdown event occurred 1: An OTP event occurred
5	VCC_D_ UVP_STS	VCC_D's undervoltage protection: 0: No UVP event occurred 1: An UVP event occurred
4	VCC_C_ UVP_STS	VCC_C's undervoltage protection: 0: No UVP event occurred 1: An UVP event occurred
3	VCC_B_ UVP_STS	VCC_B's undervoltage protection: 0: No UVP event occurred 1: An UVP event occurred
2	VCC_A_ UVP_STS	VCC_A's undervoltage protection: 0: No UVP event occurred 1: An UVP event occurred
1	VCC_2_ UVP_STS	VCC_2's undervoltage protection: 0: No UVP event occurred 1: An UVP event occurred
0	VCC_1_ UVP_STS	VCC_1's undervoltage protection: 0: No UVP event occurred 1: An UVP event occurred

Table 14. OVP_REC

Address: 0xD5 Description: Status Bits to Indicate Whether OV Is Triggered.								
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field	Reserved	Reserved	VCC_D _OVP _STS	VCC_C _OVP _STS	VCC_B _OVP _STS	VCC_A _OVP _STS	VCC_2 _OVP _STS	VCC_1 _OVP _STS
Default	0	0	0	0	0	0	0	0
Type	R	R	R	R	R	R	R	R

Bit	Name	Description
5	VCC_D_ OVP_STS	VCC_D's overvoltage protection: 0: No OVP event occurred 1: An OVP event occurred
4	VCC_C_ OVP_STS	VCC_C's overvoltage protection: 0: No OVP event occurred 1: An OVP event occurred
3	VCC_B_ OVP_STS	VCC_B's overvoltage protection: 0: No OVP event occurred 1: An OVP event occurred
2	VCC_A_ OVP_STS	VCC_A's overvoltage protection: 0: No OVP event occurred 1: An OVP event occurred
1	VCC_2_ OVP_STS	VCC_2's overvoltage protection: 0: No OVP event occurred 1: An OVP event occurred
0	VCC_1_ OVP_STS	VCC_1's overvoltage protection: 0: No OVP event occurred 1: An OVP event occurred

Table 15. PROCHOT_VCC_2_OS

Address: 0xD6
Description: Thermal Alert Setting and The Offset Setting of The VCC2.

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field	PROCHOT_EN	PROCHOT_SET		Reserved	VCC_2_OS			
Default	1	0	1	0	1	0	0	0
Type	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W

Bit	Name	Description
7	PROCHOT_EN	Enable of thermal alert function. The thermal alert function is controlled by the register 0xD3 bit<7>. Modifying this bit will enable and disable the function as follows: 0: Thermal alert function is disabled. 1: Thermal alert function is enabled. (default)
6:5	PROCHOT_SET	Thermal alert setting: 00:90°C 01:100°C (default) 10:110°C 11:120°C
3:0	VCC_2_OS	VCC_2 will be 1.1V/1.065V plus the following offset: 1111: +35mV 1110: +30mV 1101: +25mV 1100: +20mV 1011: +15mV 1010: +10mV 1001: +5mV 1000: +0mV (default) 0111: –5mV 0110: –10mV 0101: –15mV 0100: –20mV 0011: –25mV 0010: –30mV 0001: –35mV 0000: –40mV

Table 16. VCC_D_OS

Address: 0xD7 Description: The Offset Setting of the VCC_D.								
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field	Reserved					VCC_D_OS		
Default	0	0	0	0	0	0	1	0
Type	R					R/W		

Bit	Name	Description
2:0	VCC_D_OS	VCC_D will be 1.1V/0.5V plus the following offset: 111: +50mV 110: +40mV 101: +30mV 100: +20mV 011: +10mV 010: +0mV (default) 001: −10mV 000: −20mV

Table 17. DISCH_CTRL1

Address: 0xD8 Description: The Discharge Resistor Setting of VCC_A/B/C/D.								
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field	VCC_D_RDIS		VCC_C_RDIS		VCC_B_RDIS		VCC_A_RDIS	
Default	0	1	0	1	0	1	0	1
Type	R/W		R/W		R/W		R/W	

Bit	Name	Description
7:6	VCC_D_RDIS	Dummy loading at output when rail is OFF: 11: 500Ω 10: 200Ω 01: 100Ω (default) 00: Hi-Z
5:4	VCC_C_RDIS	Dummy loading at output when rail is OFF: 11: 500Ω 10: 200Ω 01: 100Ω (default) 00: Hi-Z
3:2	VCC_B_RDIS	Dummy loading at output when rail is OFF: 11: 500Ω 10: 200Ω 01: 100Ω (default) 00: Hi-Z
1:0	VCC_A_RDIS	Dummy loading at output when rail is OFF: 11: 500Ω 10: 200Ω 01: 100Ω (default) 00: Hi-Z

Table 18. DISCH_CTRL2

Address: 0xD9
Description: The Discharge Resistor Setting of LSW and VCC_1/2.

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field	Reserved		LSW_RDIS		VCC_2_RDIS		VCC_1_RDIS	
Default	0	0	1	0	0	1	0	1
Type	R		R/W		R/W		R/W	

Bit	Name	Description
5:4	LSW_RDIS	Dummy loading at output when rail is OFF: 11: 500Ω 10: 200Ω 01: 100Ω (default) 00: Hi-Z
3:2	VCC_2_RDIS	Dummy loading at output when rail is OFF: 11: 500Ω 10: 200Ω 01: 100Ω (default) 00: Hi-Z
1:0	VCC_1_RDIS	Dummy loading at output when rail is OFF: 11: 500Ω 10: 200Ω 01: 100Ω (default) 00: Hi-Z

Table 19. OC_CTRL1

Address: 0xDA Description: The Current Limit Setting of VCC_A/B/C/D.								
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field	VCC_D_CL		VCC_C_CL		VCC_B_CL		VCC_A_CL	
Default	1	1	1	1	0	0	0	0
Type	R/W		R/W		R/W		R/W	

Bit	Name	Description
7:6	VCC_D_CL	OC Setting: 00: 6A 01: 5A 10: 4A 11: 3A (default)
5:4	VCC_C_CL	OC Setting: 00: 6A 01: 5A 10: 4A 11: 3A (default)
3:2	VCC_B_CL	OC Setting: 00: 9A (default) 01: 7.8A 10: 6.6A 11: 5.3A
1:0	VCC_A_CL	OC Setting: 00: 9A (default) 01: 7.8A 10: 6.6A 11: 5.3A

Table 20. OC_CTRL2

Address: 0xDB Description: The Current Limit Setting of VCC_1/2.								
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field	Reserved				VCC_2_VCL		VCC_1_VCL	
Default	0	0	0	0	1	0	0	1
Type	R				R/W		R/W	

Bit	Name	Description
3:2	VCC_2_VCL	VCC_2 current limit setting: 11: 230mV 10: 200mV (default) 01: 125mV 00: 75mV
1:0	VCC_1_VCL	VCC_1 current limit setting: 11: 230mV 10: 200mV 01: 125mV (default) 00: 75mV

Table 21. FSW_CTRL1

Address: 0xDC Description: The Frequency Setting of VCC_A/B/C/D.								
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field	VCC_D_FSW		VCC_C_FSW		VCC_B_FSW		VCC_A_FSW	
Default	0	0	0	0	0	0	0	1
Type	R/W		R/W		R/W		R/W	

Bit	Name	Description
7:6	VCC_D_FSW	Rail switching frequency setting: 11: 1.8MHz 10: 1.6MHz 01: 1.4MHz 00: 1.2MHz (default)
5:4	VCC_C_FSW	Rail switching frequency setting: 11: 1.8MHz 10: 1.6MHz 01: 1.4MHz 00: 1.2MHz (default)
3:2	VCC_B_FSW	Rail switching frequency setting: 11: 1.8MHz 10: 1.6MHz 01: 1.4MHz 00: 1.2MHz (default)
1:0	VCC_A_FSW	Rail switching frequency setting: 11: 1200kHz 10: 1000kHz 01: 800kHz (default) 00: 600kHz

Table 22. FSW_CTRL2

Address: 0xDD Description: The Frequency Setting of VCC_1/2.								
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field	VCC_2_FSW		VCC_2_SPREAD_EN	VCC_1_SPREAD_EN	VCC_1_TON_SHRINK		VCC_1_FSW	
Default	0	1	0	0	0	0	0	1
Type	R/W		R/W		R/W		R/W	

Bit	Name	Description
7:6	VCC_2_FSW	Rail switching frequency setting: 11: 1MHz 10: 800kHz 01: 600kHz (default) 00: 400kHz
5	VCC_2_SPREAD_EN	Rail PSM spread spectrum enable: 0: Disable (default) 1: Enable
4	VCC_1_SPREAD_EN	Rail PSM spread spectrum enable: 0: Disable (default) 1: Enable
3:2	VCC_1_TON_SHRINK	VCC_1 TON width shrink percent in PSM: 11: 60% 10: 80% 01: 90% 00: 100% --- No shrink (default)
1:0	VCC_1_FSW	Rail switching frequency setting: 11: 1MHz 10: 800kHz 01: 600kHz (default) 00: 400kHz

Table 23. PG_CONFIG1

Address: 0xDE
Description: The PG1/2 Setting of VCC_1/2/A/B/C/D.

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field	PG1_ TEST_ SETTING	PG1_SETTING			PG2_ TEST_SETTING	PG2_ SETTING		
Default	0	0	0	0	0	0	0	1
Type	R/W	R/W			R/W	R/W		

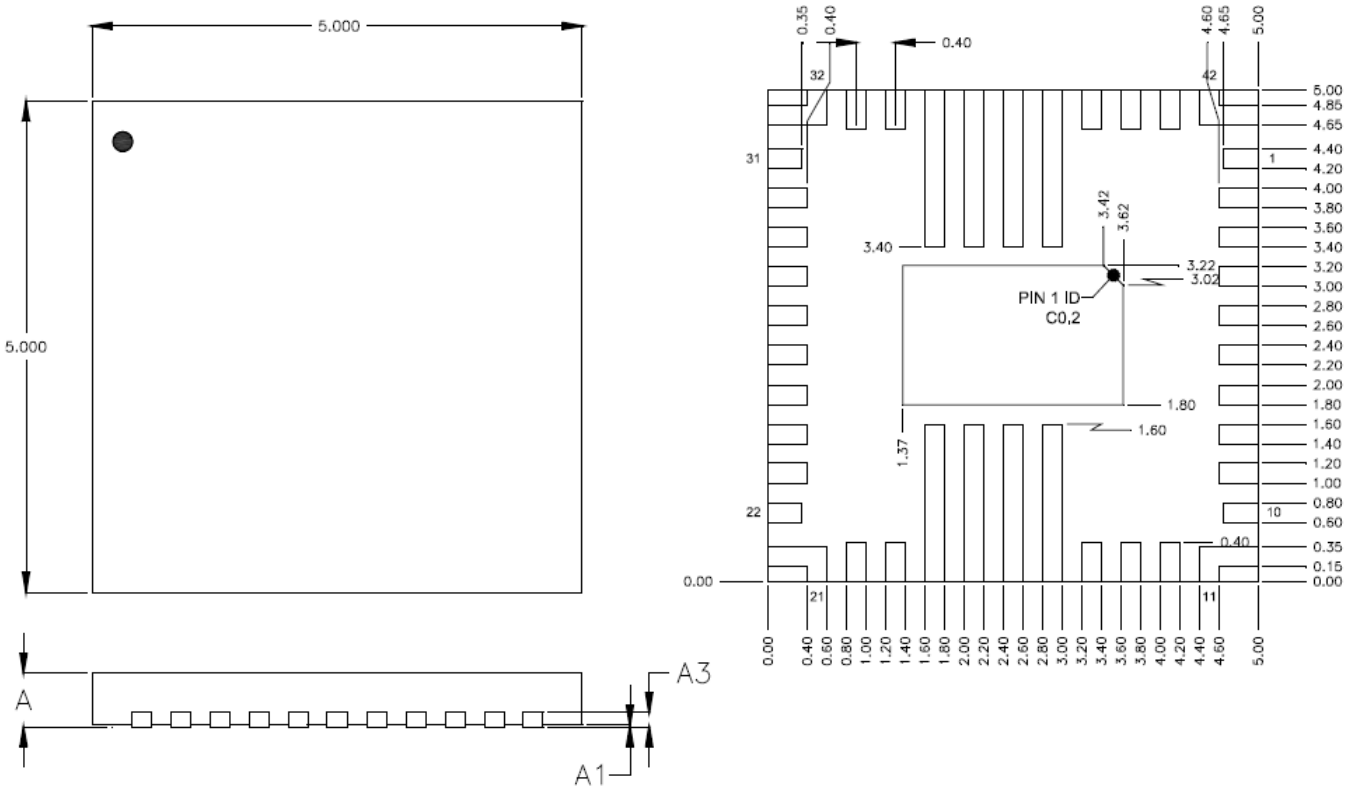
Bit	Name	Description
7	PG1_TEST_ SETTING	This pin can be written in test mode only. When this bit = 1, DO_PG_1 listens to 010: DI_EN_A 001: DI_EN1 000: DI_UVLO_BK12
6:4	PG1_SETTING	DO_PG_1 listen to 101: VCC_D_PG 100: VCC_C_PG 011: VCC_B_PG 010: VCC_A_PG 001: VCC_2_PG 000: VCC_1_PG (default)
3	PG2_TEST_ SETTING	This pin can be written in test mode only. When this bit = 1, DO_PG_2 listens to 010: DI_EN_B 001: DI_EN2 000: DI_UVLO_BKAD
2:0	PG2_SETTING	DO_PG_2 listen to 110: VCC_2_PG AND VCC_D_PG 101: VCC_D_PG 100: VCC_C_PG 011: VCC_B_PG 010: VCC_A_PG 001: VCC_2_PG (default) 000: VCC_1_PG

Table 24. PG_CONFIG2

Address: 0xDF Description: The PG3/4 Setting of VCC_1/2/A/B/C/D.								
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field	PG3_ TEST_ SETTING	PG3_SETTING			PG4_ TEST_SETTING	PG4_ SETTING		
Default	0	0	1	0	0	1	0	0
Type	R/W	R/W			R/W	R/W		

Bit	Name	Description
7	PG3_TEST_ SETTING	This pin can be written in test mode only. When this bit = 1, DO_PG_3 listen to 010: DI_EN_C 001: DI_DDR_ID 000: DI_UVLO_BKBC
6:4	PG3_SETTING	DO_PG_3 listens to 101: VCC_D_PG 100: VCC_C_PG 011: VCC_B_PG 010: VCC_A_PG (default) 001: VCC_2_PG 000: VCC_1_PG
3	PG4_TEST_ SETTING	This pin can be written in test mode only. When this bit = 1, DO_PG_4 listen to 010: DI_EN_LSW 001: DI_PROCHOT 000: DI_OTP
2:0	PG4_SETTING	DO_PG_4 listens to 110: VCC_B_PG AND VCC_C_PG 101: VCC_D_PG 100: VCC_C_PG (default) 011: VCC_B_PG 010: VCC_A_PG 001: VCC_2_PG 000: VCC_1_PG

18 Outline Dimension

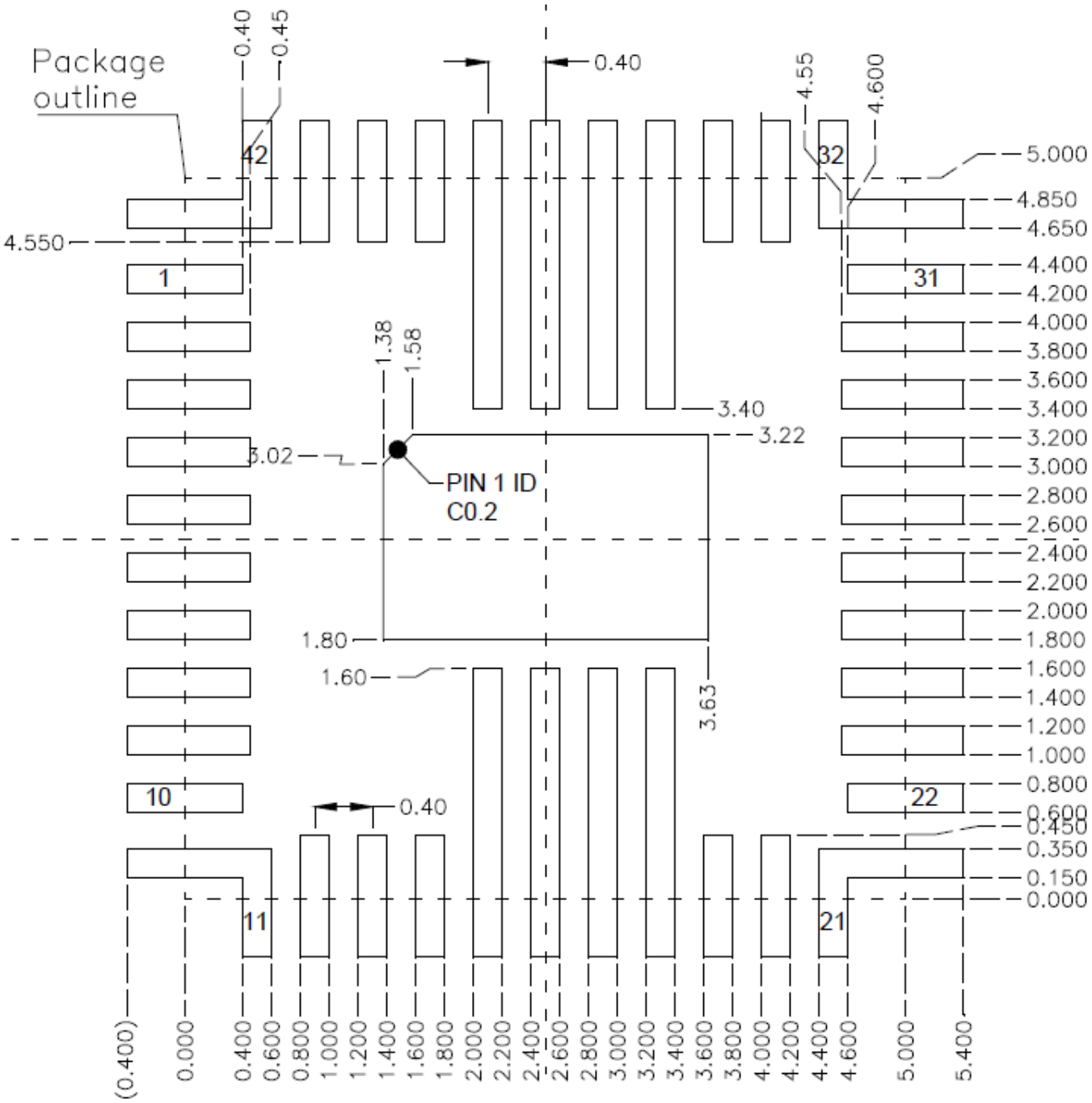


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.500	0.600	0.020	0.024
A1	0.000	0.050	0.000	0.002
A3	0.100	0.200	0.004	0.008

Tolerance
±0.050

U-Type 42L QFN 5x5 Package (FC)

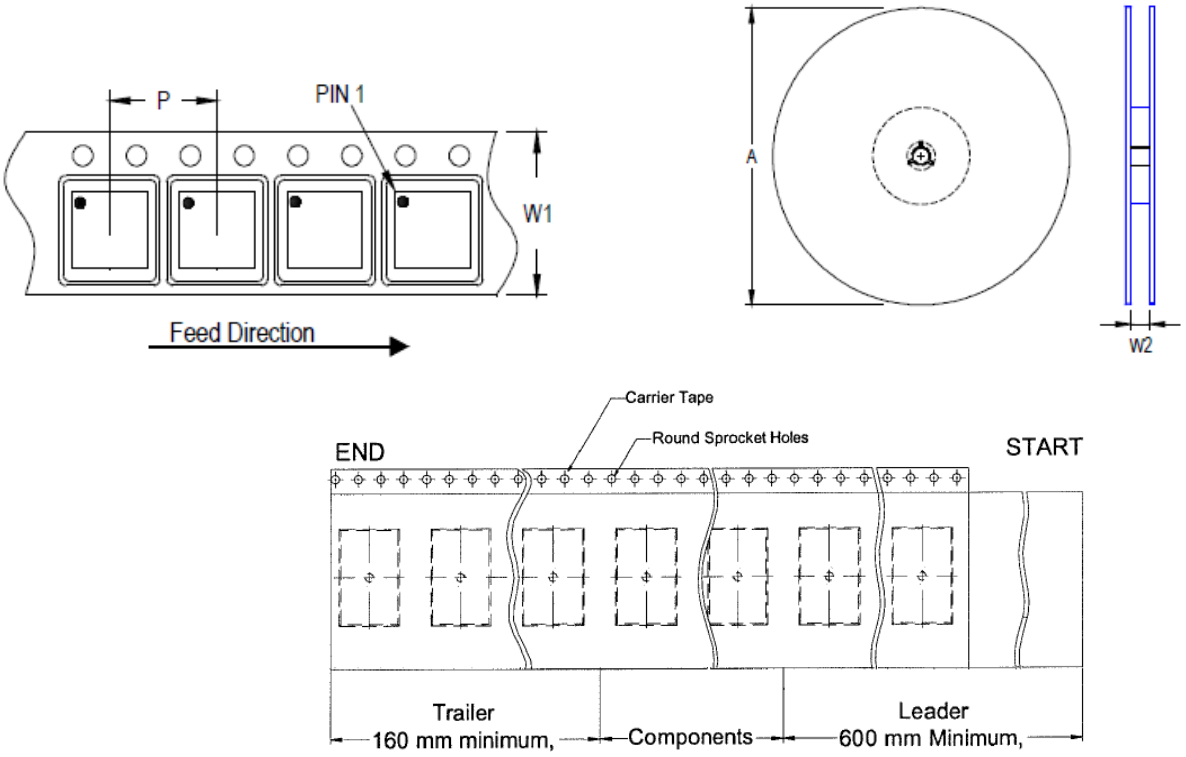
19 Footprint Information



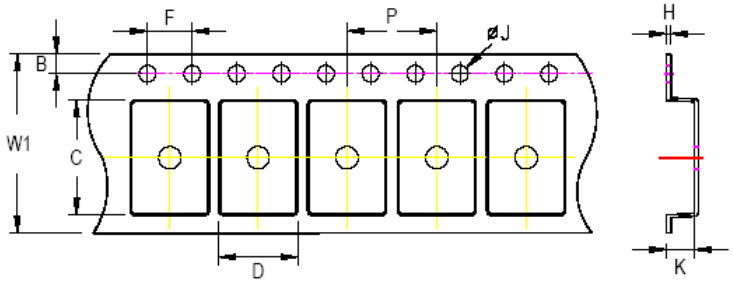
Package	Number of Pin	Tolerance
V/W/U/XQFN5x5-42(FC)	42	±0.05 mm

20 Packing Information

20.1 Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader(mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
QFN/DFN 5x5	12	8	180	7	1,500	160	600	12.4/14.4



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

20.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box					Carton			
	Size	Units	Item	Size(cm)	Weight(Kg)	Reels	Units	Item	Size(cm)	Boxes	Unit
QFN/DFN 5x5	7”	1,500	Box A	18.3*18.3*8.0	0.1	3	4,500	Carton A	38.3*27.2*40.0	12	54,000
			Box E	18.6*18.6*3.5	0.03	1	1,500	For Combined or Partial Reel.			

20.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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21 Datasheet Revision History

Version	Date	Description	Item
00	2024/3/29	Final	