Power Management Unit Total Power Solution for SSD

General Description

The RT5045A is a total power management solution for SSD (Solid State Drive) and applicable the dedicated powered by 3.3V or 5V input. RT5045A provides six step-down converters, one LDO and is designed to be flexible PMIC for supporting different output load applications with regulated power sequence.

RT5045A provides configurable outputs for core power of SSD controller, NAND Flash memory, I/O power and DRAM power. It supports dynamic voltage scaling by a dedicated I^2C interface and also apply low power mode to minimize the standby power consumption.

Applications

- Solid State Devices

Ordering Information

RT5045A□

└Package Type
WSC : WL-CSP-52B 3.19x3.59 (BSC)

Note :

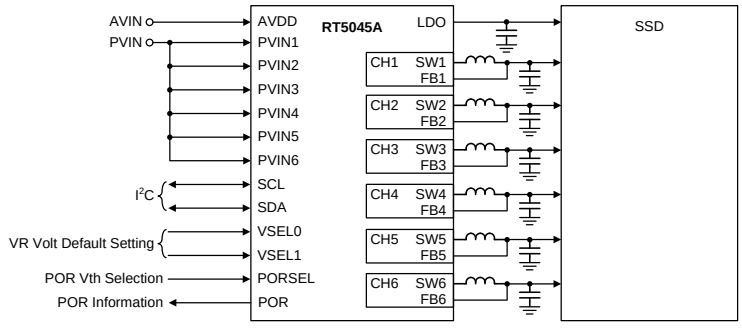
Richtek products are :

- ▸ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▸ SuiTable for use in SnPb or Pb-free soldering processes.

Features

- **Supply Input Voltage Range : 2.9V to 5.5V**
- **Six High Efficiency, Low Voltage Buck Converters**
  - ▸ **Up to 85% Efficiency at 10mA, and at Half Rated Output Current**
  - ▸ **CH1 : 2.3V to 3V in 25mV step, Output 4A max.**
  - ▸ **CH2 : 0.9V to 1.6V in 25mV step, Output 1A max.**
  - ▸ **CH3 : 1.5V to 2.1V in 25mV step, Output 1A max.**
  - ▸ **CH4 : 0.7V to 1.3V in 25mV step, Output 2A max.**
  - ▸ **CH5 : 0.7V to 1.3V in 25mV step, Output 1A max.**
  - ▸ **CH6 : 0.7V to 1.3V in 25mV step, Output 3.5A max.**
  - ▸ **CH2/3 2MHz CH4/5/6 2.5MHz Default Switching Frequency and Programmable 1 to 3MHz**
  - ▸ **2MHz Default Switching Frequency and Programmable 0.8 to 2.3MHz (CH1)**
- **VSEL0 & VSEL1 for Programmable Default Output Voltage**
- **One low quiescent current LDO with Output 200mA max.**
- **Low Power Mode (LPM) for Ultra Low Quiescent Current**
- **High-speed I^2C Interfaces for Programming Outputs**
- **POR Threshold Selection and Open-Drain POR Indicator**
- **Power Sequence Control During Startup**
- **OVP, UVP, UVLO**
- **Thermal Shutdown Protection**

Simplified Application Circuit



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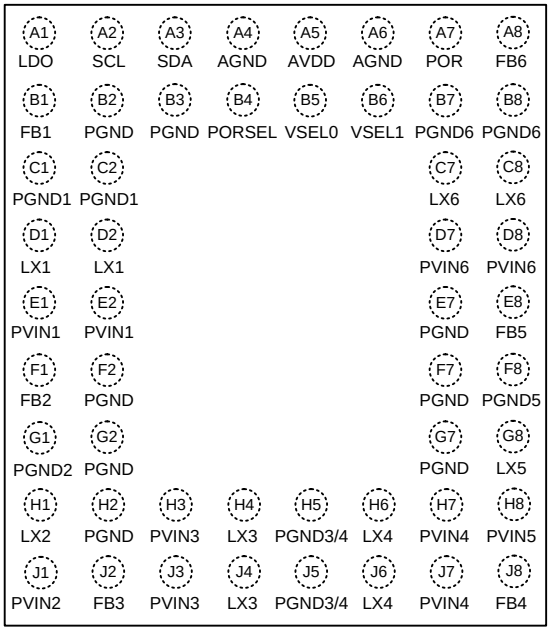
Pin Configurations

(TOP VIEW)



WL-CSP-52B 3.19x3.59 (BSC)

Marking Information

RT5045AWSC : Product Number
YMDNN : Date Code

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Functional Pin Description

Pin No.	Pin Name	Pin Function
A1	LDO	LDO Output.
A2	SCL	I^2C Interface Clock Signal.
A3	SDA	I^2C Interface Data Signal.
A4, A6	AGND	Analog Ground.
A5	AVDD	Analog Power Input for Control Logic and LDO Input.
A7	POR	Power On Reset Information. When AVDD > V_{PORTH}, POR = high level. When AVDD < V_{PORTH} – 100mV, POR = low level.
A8	FB6	CH6 Buck Converter Output Voltage Feedback Input.
B1	FB1	CH1 Buck Converter Output Voltage Feedback Input.
B2, B3, E7, F2, F7, G2, G7, H2	PGND	Power Ground.
B4	PORSEL	POR Threshold Voltage Select.
B5	VSEL0	Power Rails Default Voltage Select Pin0. Pull down resistance 1.5MΩ typ.
B6	VSEL1	Power Rails Default Voltage Select Pin1. Pull down resistance 1.5MΩ typ.
B7, B8	PGND6	CH6 Buck Converter Power Ground.
C1, C2	PGND1	CH1 Buck Converter Power Ground.
C7, C8	LX6	CH6 Buck Converter Switched Output.
D1, D2	LX1	CH1 Buck Converter Switched Output.
D7, D8	PVIN6	CH6 Buck Converter Input.
E1, E2	PVIN1	CH1 Buck Converter Input.
E8	FB5	CH5 Buck Converter Output Voltage Feedback Input.
F1	FB2	CH2 Buck Converter Output Voltage Feedback Input.
F8	PGND5	CH5 Buck Converter Power Ground.
G1	PGND2	CH2 Buck Converter Power Ground.
G8	LX5	CH5 Buck Converter Switched Output.
H1	LX2	CH2 Buck Converter Switched Output.
H3, J3	PVIN3	CH3 Buck Converter Input.
H4, J4	LX3	CH3 Buck Converter Switched Output.
H5, J5	PGND3/4	CH3 and CH4 Buck Converter Power Ground.
H6, J6	LX4	CH4 Buck Converter Switched Output.
H7, J7	PVIN4	CH4 Buck Converter Input.
H8	PVIN5	CH5 Buck Converter Input.
J1	PVIN2	CH2 Buck Converter Input.
J2	FB3	CH3 Buck Converter Output Voltage Feedback Input.
J8	FB4	CH4 Buck Converter Output Voltage Feedback Input.

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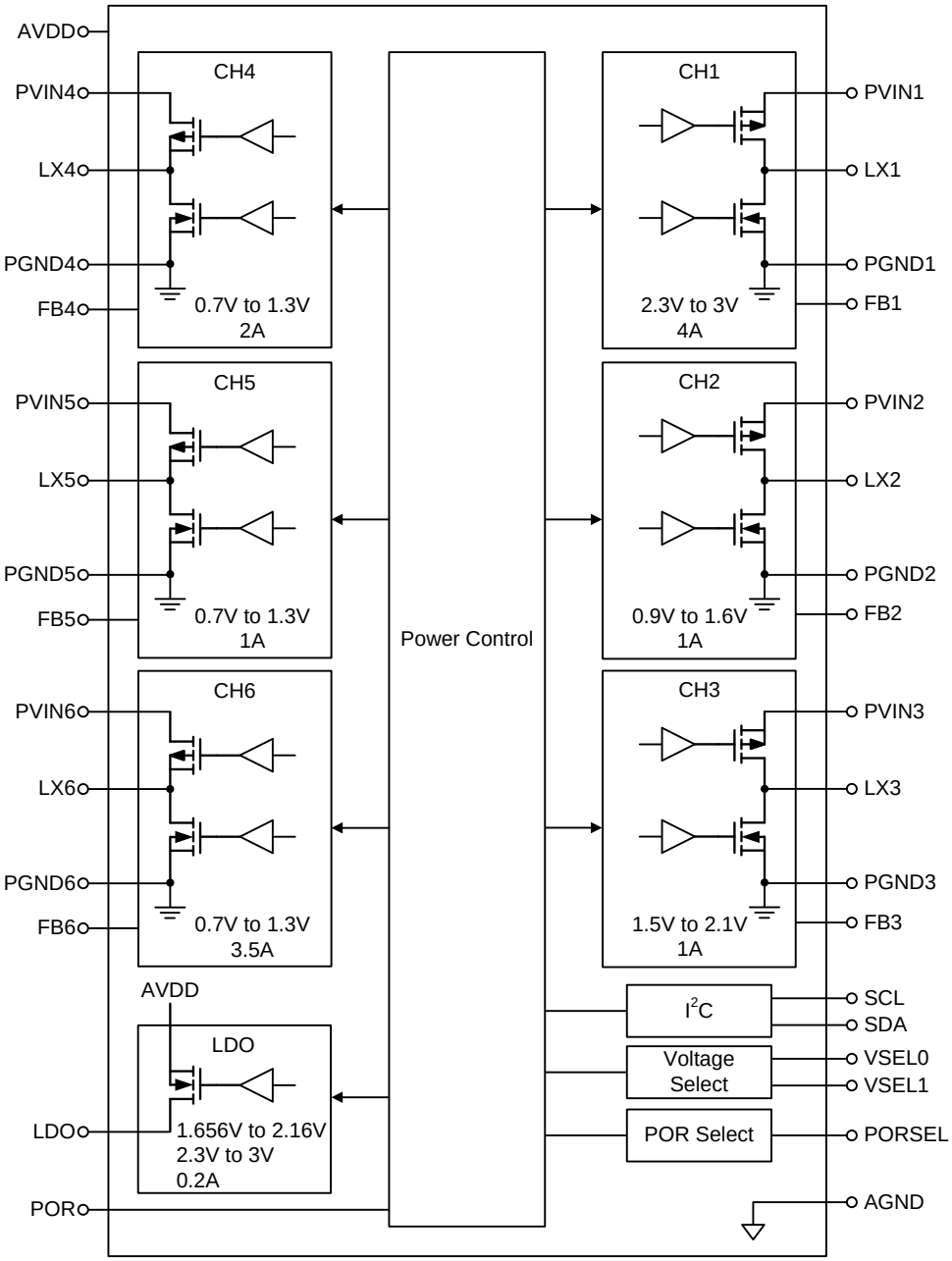
Function Block Diagram



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Operation

The RT5045A provides six synchronous Buck regulators and one LDO to satisfy the entire power system of SSD. This device can communicate with processors through I2C interface for programming the voltage, monitoring the status, or in/out the power saving mode.

Buck Converter

The RT5045A incorporates six high-efficiency synchronous switching Buck converters that deliver various voltages. CH1 features peak current mode architecture of Buck converter. For preventing the unstable when duty > 50% traditionally, it adds external ramp and compensation to reduce duty cycle perturbation and stabilize the current loop. CH1 can operate up to 100% duty to let the lowest input voltage still maintain the regulator work. And the output voltage will be the lowest input voltage decreases dropout voltage on the resistance of current path. Unlike CH1, the control scheme of other buck converters are constant-on-time current mode for low output voltage, quick transient response. The buck converters have a full set of protection.

Buck Over-Current Protection

The buck converters provides over current protection by detecting low-side MOSFET valley inductor current for CH2~CH6 and by detection high-side MOSFET peak current for CH1. If the sensed inductor current is over the current limit threshold, the OCP will be triggered. When OCP is tripped, the buck converter will keep the over current threshold level until the over current condition is removed.

Buck Under Voltage Protection

The output voltages are continuously monitored for under voltage protection. If the output voltage falls below 60% of the reference voltage, under voltage protection is triggered and then the high-side and low-side MOSFET will turn off. The UVP circuit will turn off all rails and latched. The way to cannel the latched behavior is to re-give AVDD power of RT5045A.

Buck Output Over Voltage Protection

The output voltages are continuously monitored for over voltage protection. If the output voltage exceeds 120% of the reference, over voltage protection is triggered and then the high-side and low-side MOSFET will turn off. The power MOS will keep turn off until the over voltage condition is removed.

Linear Dropout Regulator

The RT5045A includes one performance linear dropout regulators. The LDO contains an independent current limit and under voltage protection circuit to prevent unexpected applications.

When the path current is over the current limit, the current limit circuit fixes the gate voltage to limit the output current. And if the output voltage is less than 60% of reference voltage, the UVP circuit will shut-down all rails and latched. The way to cannel the latched behavior is to re-give AVDD power of RT5045A.

Over-Temperature Protection

If the temperature of the buck converter is over 150°C, the OTP circuit acts and makes all power rails shutdown. They recover back with power-up sequence when the temperature of PMIC is low to 125°C.

VSEL0, VSEL1

The RT5045A applies four set default output voltages for all power rails when the device starts a power up sequence.

PORSEL

PORSEL is a logic pin to select the threshold voltage of AVDD to raise POR signal. If AVDD voltage is over the threshold voltage, the device starts a POR rising function. When set PORSEL = 1, the threshold voltage of AVDD is 3.8V, else the threshold voltage is 2.8V.

POR

POR pin is a signal to inform the system that the power up sequence of the RT5045A is completed. If AVDD voltage is larger than the POR rising threshold voltage, the POR will go high with a timing delay. If AVDD voltage is less than POR falling threshold voltage, the POR falls right away.

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Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, AVDD, PVIN1, PVIN2, PVIN3, PVIN4, PVIN5, PVIN6 ---------- –0.3V to 6V
- Switch Node Voltage, LX1, LX2, LX3, LX4, LX5, LX6 ---------- –0.3V to 6V
- Other Pins ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C

  WL-CSP-52B 3.19x3.59 (BSC) ---------- 3.84W
- Package Thermal Resistance (Note 2)

  WL-CSP-52B 3.19x3.59 (BSC), θ_{JA} ---------- 26°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C

  ESD Susceptibility (Note 3)

  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, AVDD, PVIN1, PVIN2, PVIN3, PVIN4, PVIN5, PVIN6 ---------- 2.9V to 5.5V
- Other Pins, VSEL0, VSEL1, SCL, SDA, PORSEL, POR ---------- 0V to 5.5V
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(AVDD = 3.3V, PVIN = 3.3V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
PMIC						
AVDD Supply Voltage	V_{AVIN}		2.9	3.3	5.5	V
AVDD Supply Current	I_{AVIN}	All Voltage Rails off	--	15	25	μA
AVDD Supply Current in Sleep Mode		CH5 = LPM, other voltage rails off	--	15	25	μA
VSEL0, VSEL1, PORSEL High	V_{IH}	Logic signal rising threshold	1.2	--	--	V
VSEL0, VSEL1, PORSEL Low	V_{IL}	Logic signal falling threshold	--	--	0.4	V
AVDD UVLO Hysteresis		Hysteresis	--	100	--	mV
AVDD UVLO Threshold	V_{AVUV}	POR_OPTION = 0, PORSEL = 0, UVLO falling	2.673	2.7	2.727	V
		POR_OPTION = 0, PORSEL = 1, UVLO falling	3.663	3.7	3.737	
AVDD UVLO Hysteresis		Hysteresis	--	100	--	mV
POR Threshold	V_{PORTH}	POR_OPTION = 0, PORSEL = 0, POR falling	2.673	2.7	2.727	V
		POR_OPTION = 0, PORSEL = 1, POR falling	3.663	3.7	3.737	
POR Hysteresis		Hysteresis	--	100	--	mV
POR Output Low	V_{PORLO}	Sink current = 5mA	--	--	0.4	V

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
POR Rising Delay Time		AVDD > V_{PORTH}, detect the POR rising edge. VSEL = 0, VSEL1 = 0	9	10	11	ms
Thermal Shutdown Threshold	T_{SD}		--	150	--	°C
Thermal Shutdown Hysteresis			--	25	--	°C
CH1 (4A)						
AVDD Quiescent Current	I_{INQ}	Enable, no switching, not include I_{AVIN}	--	25	35	μA
AVDD LPM Quiescent	I_{INLP}	LPM enable, not include I_{AVIN}	--	10	20	μA
Output Voltage Scaling		Controlled by I^2C	2.3	--	3	V
Output Voltage Default	V_{OUT}	VSEL0 = 0, VSEL1 = 0	–2%	2.5	+2%	V
DC Output Voltage Programmable step	V_{STEP}		--	25	--	mV
Line Regulation			--	0.5	--	%/V
Load Regulation		Force PWM	--	0.5	--	%/A
Transient Load Regulation		V_{IN} = 3.3V, V_{OUT} = 2.5V, L = 0.47μH, C_{OUT} = 22μF x 2, I_{OUT} = 0.2 to 1.5A at SR = 0.13A/μs	--	--	84	mV
H/S Switch On Resistance	$R_{DS(ON)H}$	V_{IN} = 5V	--	35	--	mΩ
L/S Switch On Resistance	$R_{DS(ON)L}$	V_{IN} = 5V	--	18	--	mΩ
Current Limit	I_{OC}	Peak current, IMAX[6:5] = 10	5	5.8	--	A
Switching Frequency	F_{SW}	FREQ[2:0] = 110	1.8	2	2.2	MHz
Minimum On-Time	T_{ON}		--	150	200	ns
OVP Trip Threshold	V_{OVP}	OVP detected	115	120	125	%
OVP Propagation Delay	T_{OVPDLY}		--	1	--	μs
UVP Trip Threshold	V_{UVP}	UVP detected	55	60	65	%
UVP Propagation Delay (Note 5)	T_{UVPDLY}		--	2	--	μs
Soft-Start Time	T_{SS}		--	0.5	0.8	ms
Discharge Resistance			--	50	--	Ω
Efficiency		V_{IN} = 3.3V, V_{OUT} = 2.5V, Load = 10mA	85	--	--	%
		V_{IN} = 3.3V, V_{OUT} = 2.5V, Load = 1A	90	--	--	
CH2 (1A)						
AVDD Quiescent Current	I_{INQ}	Enable, no switching, not include I_{AVIN}	--	25	35	μA
AVDD LPM Quiescent	I_{INLP}	LPM enable, not include I_{AVIN}	--	10	20	μA
Output Voltage Scaling		Controlled by I^2C	0.9	--	1.6	V
Output Voltage Default	V_{OUT}	VSEL0 = 0, VSEL1 = 0	–2%	1.35	+2%	V
DC Output Voltage Programmable Step	V_{STEP}		--	25	--	mV
Line Regulation			--	0.5	--	%/V
Load Regulation		Force PWM	--	0.5	--	%/A

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Transient Load Regulation		V_{IN} = 3.3V, V_{OUT} = 1.5V	--	--	75	mV
H/S Switch On Resistance	$R_{DS(ON)H}$	V_{IN} = 5V	--	40	--	mΩ
L/S Switch On Resistance	$R_{DS(ON)L}$	V_{IN} = 5V	--	20	--	mΩ
Current Limit	I_{OC}	Valley current, IMAX[6:5] = 10,	2	2.5	--	A
Switching Frequency	F_{SW}	FREQ[2:0] = 101	1.8	2	2.2	MHz
Minimum Off-Time	T_{OFF}		--	120	160	ns
OVP Trip Threshold	V_{OVP}	OVP detected	120	125	130	%
OVP Propagation Delay	T_{OVPDLY}			1	--	µs
UVP Trip Threshold	V_{UVP}	UVP detected	55	60	65	%
UVP Propagation Delay (Note 5)	T_{UVPDLY}		--	2	--	µs
Soft-Start Time	T_{SS}		--	0.5	0.8	ms
Discharge Resistance			--	100	--	Ω
Efficiency		V_{IN} = 3.3V, V_{OUT} = 1.5V, Load = 10mA	85	--	--	%
		V_{IN} = 3.3V, V_{OUT} = 1.5V, Load = 500mA	85	--	--	
CH3 (1A)						
AVDD Quiescent Current	I_{INQ}	Enable, no switching, not include I_{AVIN}	--	25	35	µA
AVDD LPM Quiescent	I_{INLP}	LPM enable, not include I_{AVIN}	--	10	20	µA
Output Voltage Scaling		Controlled by I^2C	1.5	--	2.1	V
Output Voltage Default	V_{OUT}	VSEL0 = 0, VSEL1 = 0	–2%	1.8	+2%	V
DC Output Voltage Programmable step	V_{STEP}		--	25	--	mV
Line Regulation			--	0.5	--	%/V
Load Regulation		Force PWM	--	0.5	--	%/A
Transient Load Regulation		V_{IN} = 3.3V, V_{OUT} = 1.8V	--	--	90	mV
H/S Switch On Resistance	$R_{DS(ON)H}$	V_{IN} = 5V	--	45	--	mΩ
L/S Switch On Resistance	$R_{DS(ON)L}$	V_{IN} = 5V	--	25	--	mΩ
Current Limit	I_{OC}	Valley current, IMAX[6:5] = 10	2	2.5	--	A
Switching Frequency	F_{SW}	FREQ[2:0] = 101	1.8	2	2.2	MHz
Minimum Off-Time	T_{OFF}		--	120	160	ns
OVP Trip Threshold	V_{OVP}	OVP detected	120	125	130	%
OVP Propagation Delay	T_{OVPDLY}		--	1	--	µs
UVP Trip Threshold	V_{UVP}	UVP detected	55	60	65	%
UVP Propagation Delay (Note 5)	T_{UVPDLY}		--	2	--	µs
Soft-Start Time	T_{SS}		--	0.5	0.8	ms
Discharge Resistance			--	50	--	Ω
Efficiency		V_{IN} = 3.3V, V_{OUT} = 1.8V, Load = 10mA	85	--	--	%
		V_{IN} = 3.3V, V_{OUT} = 1.8V, Load = 500mA	85	--	--	

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
CH4 (2A)						
AVDD Quiescent Current	I_{INQ}	Enable, no switching, not include I_{AVIN}	--	25	35	μA
AVDD LPM Quiescent	I_{INLP}	LPM enable, not include I_{AVIN}	--	10	20	μA
Output Voltage Scaling		Controlled by I^2C	0.7	--	1.3	V
Output Voltage Default	V_{OUT}	VSEL0 = 0, VSEL1 = 0	–2%	1	+2%	V
DC Output Voltage Programmable step	V_{STEP}		--	25	--	mV
Line Regulation			--	0.5	--	%/V
Load Regulation		Force PWM	--	0.5	--	%/A
Transient Load Regulation		V_{IN} = 3.3V, V_{OUT} = 1V	--	--	50	mV
H/S Switch On Resistance	$R_{DS(ON)H}$	V_{IN} = 5V	--	45	--	mΩ
L/S Switch On Resistance	$R_{DS(ON)L}$	V_{IN} = 5V	--	25	--	mΩ
Current Limit	I_{OC}	Valley current, IMAX[6:5] = 10	2.5	3	--	A
Switching Frequency	F_{SW}	FREQ[2:0] = 110	2.2	2.5	2.75	MHz
Minimum Off-Time	T_{OFF}		--	120	160	ns
OVP Trip Threshold	V_{OVP}	OVP detected	120	125	130	%
OVP Propagation Delay	T_{OVPDLY}		--	1	--	μs
UVP Trip Threshold	V_{UVP}	UVP detected	55	60	65	%
UVP Propagation Delay (Note 5)	T_{UVPDLY}		--	2	--	μs
Soft-Start Time	T_{SS}		--	0.5	0.8	ms
Discharge Resistance	T_{DIS}		--	150	--	Ω
Efficiency		V_{IN} = 3.3V, V_{OUT} = 1V, Load = 10mA	85	--	--	%
		V_{IN} = 3.3V, V_{OUT} = 1V, Load = 1A	85	--	--	
CH5 (1A)						
AVDD Quiescent Current	I_{INQ}	Enable, no switching, not include I_{AVIN}	--	25	35	μA
AVDD LPM Quiescent	I_{INLP}	LPM enable, not include I_{AVIN}	--	10	20	μA
Output Voltage Scaling		Controlled by I^2C	0.7	--	1.3	V
Output Voltage Default	V_{OUT}	VSEL0 = 0, VSEL1 = 0	–2%	1	+2%	V
DC Output Voltage Programmable Step	V_{STEP}		--	25	--	mV
Line Regulation			--	0.5	--	%/V
Load Regulation		Force PWM	--	0.5	--	%/A
Transient Load Regulation		V_{IN} = 3.3V, V_{OUT} = 1V	--	--	50	mV
H/S Switch On Resistance	$R_{DS(ON)H}$	V_{IN} = 5V	--	50	--	mΩ
L/S Switch On Resistance	$R_{DS(ON)L}$	V_{IN} = 5V	--	30	--	mΩ
Current Limit	I_{OC}	Valley current, IMAX[6:5] = 10	2	2.5	--	A
Switching Frequency	F_{SW}	FREQ[2:0] = 110	2.2	2.5	2.75	MHz
Minimum Off-Time	T_{OFF}		--	120	160	ns

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OVP Trip Threshold	V_{OVP}	OVP detected	120	125	130	%
OVP Propagation Delay	T_{OVPDLY}		--	1	--	μs
UVP Trip Threshold	V_{UVP}	UVP detected	55	60	65	%
UVP Propagation Delay (Note 5)	T_{UVPDLY}		--	2	--	μs
Soft-Start Time	T_{SS}		--	0.5	0.8	ms
Discharge Resistance			--	150	--	Ω
Efficiency		V_{IN} = 3.3V, V_{OUT} = 1V, Load = 1mA, LPM	85	--	--	%
		V_{IN} = 3.3V, V_{OUT} = 1V, Load = 500mA	85	--	--	
CH6 (3.5A)						
AVDD Quiescent Current	I_{INQ}	Enable, no switching, not include I_{AVIN}	--	25	35	μA
AVDD LPM Quiescent	I_{INLP}	LPM enable, not include I_{AVIN}	--	10	20	μA
Output Voltage Scaling		Controlled by I^2C	0.7	--	1.3	V
Output Voltage Default	V_{OUT}	VSEL0 = 0, VSEL1 = 0	–2%	1	+2%	V
DC Output Voltage Programmable Step	V_{STEP}		--	25	--	mV
Line Regulation			--	0.5	--	%/V
Load Regulation		Force PWM	--	0.5	--	%/A
Transient Load Regulation		V_{IN} = 3.3V, V_{OUT} = 1V	--	--	50	mV
H/S Switch On Resistance	$R_{DS(ON)H}$	V_{IN} = 5V	--	40	--	mΩ
L/S Switch On Resistance	$R_{DS(ON)L}$	V_{IN} = 5V	--	20	--	mΩ
Current Limit	I_{OC}	Valley current, IMAX[6:5] = 10	4.5	5	--	A
Switching Frequency	F_{SW}	FREQ[2:0] = 110	2.2	2.5	2.75	MHz
Minimum Off-Time	T_{OFF}		--	120	160	ns
OVP Trip Threshold	V_{OVP}	OVP detected	120	125	130	%
OVP Propagation Delay	T_{OVPDLY}		--	1	--	μs
UVP Trip Threshold	V_{UVP}	UVP detected	55	60	65	%
UVP Propagation Delay (Note 5)	T_{UVPDLY}		--	2	--	μs
Soft-Start Time	T_{SS}		--	0.5	0.8	ms
Discharge Resistance			--	150	--	Ω
Efficiency		V_{IN} = 3.3V, V_{OUT} = 1V, Load = 10mA	85	--	--	%
		V_{IN} = 3.3V, V_{OUT} = 1V, Load = 1A	85	--	--	
LDO (0.2A)						
AVDD Quiescent Current	I_{INQ}	Enable, not include I_{AVIN}	--	28	38	μA
AVDD LPM Quiescent	I_{INLP}	LPM enable, not include I_{AVIN}	--	15	25	μA
Output Voltage Scaling		VSEL0 = 0, VSEL1 = 0 VSEL0 = 0, VSEL1 = 1	2.3	--	3	V
		VSEL0 = 1, VSEL1 = 0 VSEL0 = 1, VSEL1 = 1	1.656	--	2.16	

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage Default	V_{OUT}	VSEL0 = 0, VSEL1 = 0	–2%	2.5	+2%	V
DC Output Voltage Programmable Step	V_{STEP}		--	25	--	mV
Line Regulation			--	0.5	--	%/V
Load Regulation			--	0.5	--	%/A
Transient Load Regulation		V_{IN} = 3.3V, V_{OUT} = 2.5V, Load = 20mA to 180mA during 5μs	--	--	125	mV
Dropout Voltage	V_{DROP}	V_{IN} = 3.3V, V_{OUT} = 2.5V Load = 200mA	--	100	200	mV
Current Limit	I_{OC}		--	0.4	--	A
UVP Trip Threshold	V_{UVP}	UVP detected	55	60	65	%
UVP Propagation Delay (Note 5)	T_{UVPDLY}		--	2	--	μs
Soft-Start Time	T_{SS}		--	0.3	0.6	ms
Discharge Resistance	T_{DIS}		--	100	--	Ω
Power Supply Rejection Rate	PSRR	Load = 100mA, F = 100Hz	--	–50	--	dB
		Load = 100mA, F = 100kHz	--	–28	--	

I²C for Fast Mode

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
SDA, SCL Input Voltage	High-Level			1.2	--	--	V
	Low-Level			--	--	0.4	
Fast Mode							
SCL Clock Rate		f_{SCL}		--	--	400	kHz
Hold Time (Repeated) START Condition. After this Period, the First Clock Pulse is Generated		$t_{HD;STA}$		0.6	--	--	μs
LOW Period of the SCL Clock		t_{LOW}		1.3	--	--	μs
HIGH Period of the SCL Clock		t_{HIGH}		0.6	--	--	μs
Set-Up Time for a Repeated START Condition		$t_{SU;STA}$		0.6	--	--	μs
Data Hold Time		$t_{HD;DAT}$		0	--	0.9	μs
Data Set-Up Time		$t_{SU;DAT}$		100	--	--	ns
Set-Up Time for STOP Condition		$t_{SU;STO}$		0.6	--	--	μs
Bus Free Time between a STOP and START Condition		t_{BUF}		1.3	--	--	μs
Rising Time of both SDA and SCL Signals		t_r		20	--	300	ns
Falling Time of both SDA and SCL Signals		t_f		20	--	300	ns
SDA and SCL Output Low Sink Current		I_{OL}	SDA or SCL Voltage = 0.4V	2	--	--	mA

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I²C High Speed Mode

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
SDA, SCL Input Voltage	High-Level			1.2	--	--	V
	Low-Level			--	--	0.4	
High Speed Mode							
SCL Clock Rate		f_{SCL}		--	--	3.4	MHz
Hold Time (Repeated) START Condition. After this Period, the First Clock Pulse is Generated		$t_{HD;STA}$		160	--	--	ns
LOW Period of the SCL Clock		t_{LOW}		160	--	--	ns
HIGH Period of the SCL Clock		t_{HIGH}		60	--	--	ns
Set-Up Time for a Repeated START Condition		$t_{SU;STA}$		60	--	--	ns
Data Hold Time		$t_{HD;DAT}$		0	--	70	ns
Data Set-Up Time		$t_{SU;DAT}$		10	--	--	ns
Set-Up Time for STOP Condition		$t_{SU;STO}$		160	--	--	ns
Rising Time of both SDA and SCL Signals		t_r		10	--	80	ns
Falling Time of both SDA and SCL Signals		t_f		10	--	80	ns
SDA and SCL Output Low Sink Current		I_{OL}	SDA or SCL Voltage = 0.4V	2	--	--	mA

Note 1. Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7.

Note 3. Devices are ESD sensitive. Handling precaution recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Design Guaranteed.

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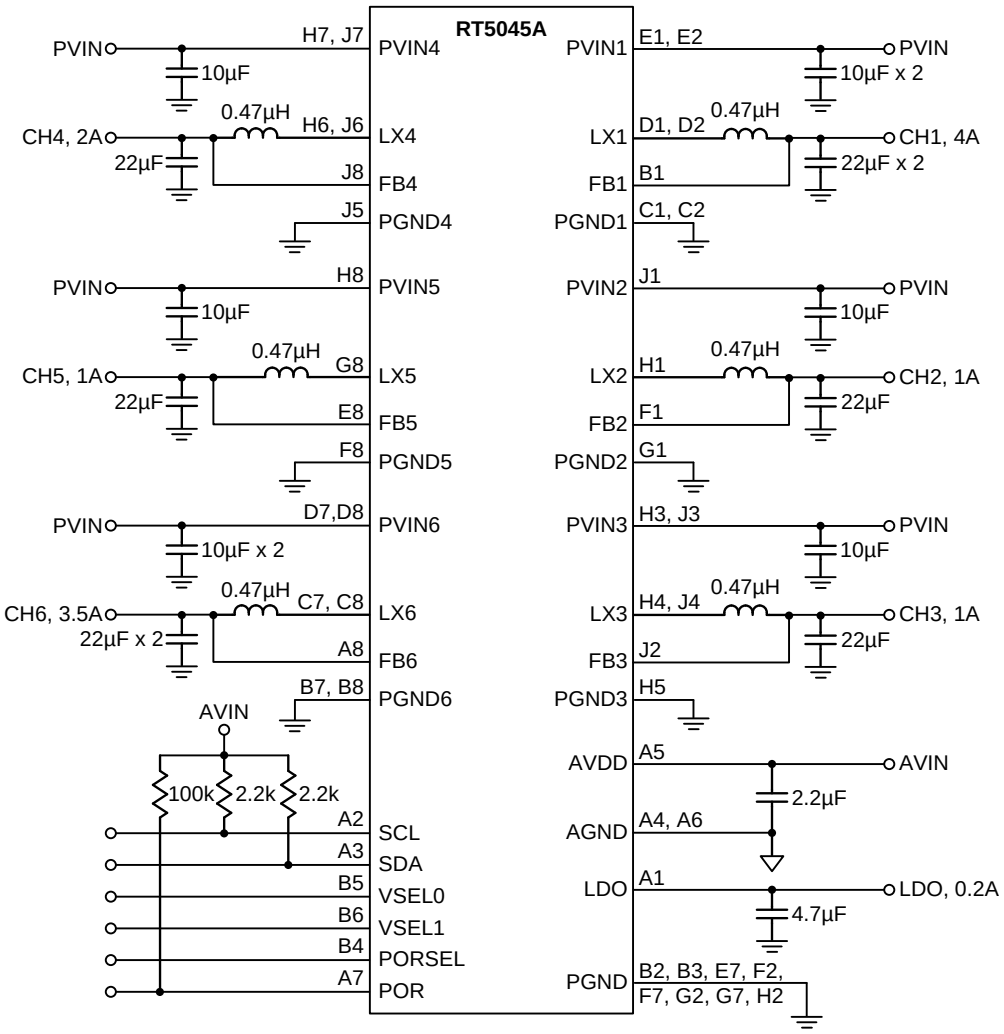
Typical Application Circuit



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Functional Register Table

Table 1. RT5045A Register Summary

Name	Type	Register Reset	Address Offset
POWER_GOOD	RO	0x00	0x00
CH1_CFG_REG	RW	0x56	0x01
CH1_SEL_REG	RW	0x00	0x02
CH2_CFG_REG	RW	0x55	0x03
CH2_SEL_REG	RW	0x00	0x04
CH3_CFG_REG	RW	0x55	0x05
CH3_SEL_REG	RW	0x00	0x06
CH4_CFG_REG	RW	0x56	0x07
CH4_SEL_REG	RW	0x00	0x08
CH5_CFG_REG	RW	0x56	0x09
CH5_SEL_REG	RW	0x00	0x0A
CH6_CFG_REG	RW	0x56	0x0B
CH6_SEL_REG	RW	0x00	0x0C
LDO_SEL_REG	RW	0x00	0x0D
DCDCCTRL0_REG	RW	0x00	0x11
SLEEP_REG	RW	0x00	0x12
DCDCCTRL1_REG	RW	0x00	0x13
DISCHARGE_REG	RW	0xFE	0x14
POR_OPTION_REG	RW	0x00	0x17
DCDCTRL2_REG	RW	0x00	0x18
WK_TIME1	RW	0x00	0x19
WK_TIME2	RW	0x00	0x1A
WK_TIME3	RW	0x00	0x1B
WK_TIME4	RW	0x00	0x1C
PRODUCT_ID_REG	RO	0x01	0x20
MANUFACTURER_ID	RO	0x01	0x21
REVISION_NUMBER	RO	0x00	0x22

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Table 2. POWER_GOOD_REG

Address : 0x00
Description : Power good information register.
When Voltage Rails achieve 90% of VID target, the relative bit will set to 1.

Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	CH1_PG	CH2_PG	CH3_PG	CH4_PG	CH5_PG	CH6_PG	LDO_PG	POR
Reset Value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

Bits	Name	Description
7	CH1_PG	Status bit. Indicates power good on CH1
6	CH2_PG	Status bit. Indicates power good on CH2
5	CH3_PG	Status bit. Indicates power good on CH3
4	CH4_PG	Status bit. Indicates power good on CH4
3	CH5_PG	Status bit. Indicates power good on CH5
2	CH6_PG	Status bit. Indicates power good on CH6
1	LDO_PG	Status bit. Indicates power good on LDO
0	POR	Status bit. Indicates POR

Table 3. CH1_CFG_REG

Address : 0x01
Description : CH1 config register.
Set CH1 current limited, VID change slew rate, PWM frequency.

Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	Reserved	ILMAX		TSTEP		FREQ		
Reset Value	0	1	0	1	0	1	1	0
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
7	Reserved	Reserved bit
6 : 5	ILMAX	ILMAX[6:5] = 00 : 3.8A ILMAX[6:5] = 01 : 4.8A ILMAX[6:5] = 10 : 5.8A (default) ILMAX[6:5] = 11 : 6.8A
4 : 3	TSTEP	TSTEP[4:3] = 00 : 20mV/μs TSTEP[4:3] = 01 : 15mV/μs TSTEP[4:3] = 10 : 10mV/μs (default) TSTEP[4:3] = 11 : 5mV/μs
2 : 0	FREQ	FREQ[2:0] = 000 to 010, 0.8MHz FREQ[2:0] = 011, 1.1MHz FREQ[2:0] = 100, 1.4MHz FREQ[2:0] = 101, 1.7MHz FREQ[2:0] = 110, 2.0MHz (default) FREQ[2:0] = 111, 2.3MHz

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Table 4. CH1_SEL_REG

Address : 0x02
Description : CH1 VID setting register.
CH1 VID setting and power on/off status and control.

Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	Reserved	SEL					Reserved	
Reset Value	0	0	0	0	0	0	0	0
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
7	Reserved	Reserved bit
6 : 2	SEL	Supply voltage, SEL[6:2] = 00000 to 00011 : 2.3V SEL[6:2] = 100 : 2.325V SEL[6:2] = 101 : 2.35V SEL[6:2] = 110 : 2.375V SEL[6:2] = 111 : 2.4V SEL[6:2] = 1000 : 2.425V SEL[6:2] = 1001 : 2.45V SEL[6:2] = 1010 : 2.475V SEL[6:2] = 1011 : 2.5V SEL[6:2] = 1100 : 2.525V SEL[6:2] = 1110 : 2.575V SEL[6:2] = 1111 : 2.6V SEL[6:2] = 10000 : 2.625V SEL[6:2] = 10001 : 2.65V SEL[6:2] = 10010 : 2.675V SEL[6:2] = 10011 : 2.7V SEL[6:2] = 10100 : 2.725V SEL[6:2] = 10101 : 2.75V SEL[6:2] = 10110 : 2.775V SEL[6:2] = 10111 : 2.8V SEL[6:2] = 11000 : 2.825V SEL[6:2] = 11001 : 2.85V SEL[6:2] = 11010 : 2.875V SEL[6:2] = 11011 : 2.9V SEL[6:2] = 11100 : 2.925V SEL[6:2] = 11111 : 3V VOUT = SEL[6:2] x 0.025V + 2.225V, from SEL[6:2] = 3 to 1F (hex) (After each UVLO rising, the voltage is set to the value by VSEL0/VSEL1 setting : VSEL0 = 0, VSEL1 = 0, VOUT = 2.5V VSEL0 = 0, VSEL1 = 1, VOUT = 2.5V VSEL0 = 1, VSEL1 = 0, VOUT = 2.5V VSEL0 = 1, VSEL1 = 1, VOUT = 2.5V)
1 : 0	Reserved	Reserved bit

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Table 5. CH2_CFG_REG

Address : 0x03
Description : CH2 config register.
Set CH2 current limited, VID change slew rate, PWM frequency.

Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	Reserved	ILMAX		TSTEP		FREQ		
Reset Value	0	1	0	1	0	1	0	1
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
7	Reserved	Reserved bit
6 : 5	ILMAX	ILMAX[6:5] = 00 : 1.5A ILMAX[6:5] = 01 : 2A ILMAX[6:5] = 10 : 2.5A (default) ILMAX[6:5] = 11 : 3A
4 : 3	TSTEP	TSTEP[4:3] = 00 : 20mV/μs TSTEP[4:3] = 01 : 15mV/μs TSTEP[4:3] = 10 : 10mV/μs (default) TSTEP[4:3] = 11 : 5mV/μs
2 : 0	FREQ	FREQ[2:0] = 000 to 011, 1MHz FREQ[2:0] = 100, 1.5MHz FREQ[2:0] = 101, 2.0MHz (default) FREQ[2:0] = 110, 2.5MHz FREQ[2:0] = 111, 3.0MHz

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Table 6. CH2_SEL_REG

Address : 0x04
Description : CH2 VID setting register.
CH2 VID setting and power on/off status and control.

Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	Reserved	SEL					Reserved	
Reset Value	0	0	0	0	0	0	0	0
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
7	Reserved	Reserved bit
6 : 2	SEL	Supply voltage, SEL[6:2] = 00000 to 00011 : 0.9V SEL[6:2] = 100 : 0.925V SEL[6:2] = 101 : 0.95V SEL[6:2] = 110 : 0.975V SEL[6:2] = 111 : 1V SEL[6:2] = 1000 : 1.025V SEL[6:2] = 1001 : 1.05V SEL[6:2] = 1010 : 1.075V SEL[6:2] = 1011 : 1.1V SEL[6:2] = 1100 : 1.125V SEL[6:2] = 1110 : 1.175V SEL[6:2] = 1111 : 1.2V SEL[6:2] = 10000 : 1.225V SEL[6:2] = 10001 : 1.25V SEL[6:2] = 10010 : 1.275V SEL[6:2] = 10011 : 1.3V SEL[6:2] = 10100 : 1.325V SEL[6:2] = 10101 : 1.35V SEL[6:2] = 10110 : 1.375V SEL[6:2] = 10111 : 1.4V SEL[6:2] = 11000 : 1.425V SEL[6:2] = 11001 : 1.45V SEL[6:2] = 11010 : 1.475V SEL[6:2] = 11011 : 1.5V SEL[6:2] = 11100 : 1.525V SEL[6:2] = 11111 : 1.6V VOUT = SEL[6:2] x 0.025V + 0.825V, from SEL[6:2] = 3 to 1F (hex) (After each UVLO rising, the voltage is set to the value by VSEL0/VSEL1 setting : VSEL0 = 0, VSEL1 = 0, VOUT = 1.35V VSEL0 = 0, VSEL1 = 1, VOUT = 1.35V VSEL0 = 1, VSEL1 = 0, VOUT = 1.35V VSEL0 = 1, VSEL1 = 1, VOUT = 1.2V)
1 : 0	Reserved	Reserved bit

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Table 7. CH3_CFG_REG

Address : 0x05
Description : CH3 config register.
Set CH3 current limited, VID change slew rate, PWM frequency.

Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	Reserved	ILMAX		TSTEP		FREQ		
Reset Value	0	1	0	1	0	1	0	1
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
7	Reserved	Reserved bit
6 : 5	ILMAX	ILMAX[6:5] = 00 : 1.5A ILMAX[6:5] = 01 : 2A ILMAX[6:5] = 10 : 2.5A (default) ILMAX[6:5] = 11 : 3A
4 : 3	TSTEP	TSTEP[4:3] = 00 : 20mV/μs TSTEP[4:3] = 01 : 15mV/μs TSTEP[4:3] = 10 : 10mV/μs (default) TSTEP[4:3] = 11 : 5mV/μs
2 : 0	FREQ	FREQ[2:0] = 000 to 011, 1MHz FREQ[2:0] = 100, 1.5MHz FREQ[2:0] = 101, 2.0MHz (default) FREQ[2:0] = 110, 2.5MHz FREQ[2:0] = 111, 3.0MHz

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Table 8. CH3_SEL_REG

Address : 0x06
Description : CH3 VID setting register.
CH3 VID setting and power on/off status and control.

Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	Reserved	SEL					Reserved	
Reset Value	0	0	0	0	0	0	0	0
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
7	Reserved	Reserved bit
6 : 2	SEL	Supply voltage, SEL[6:2] = 00000 to 00011 : 1.5V SEL[6:2] = 100 : 1.525V SEL[6:2] = 101 : 1.55V SEL[6:2] = 110 : 1.575V SEL[6:2] = 111 : 1.6V SEL[6:2] = 1000 : 1.625V SEL[6:2] = 1001 : 1.65V SEL[6:2] = 1010 : 1.675V SEL[6:2] = 1011 : 1.7V SEL[6:2] = 1100 : 1.725V SEL[6:2] = 1110 : 1.775V SEL[6:2] = 1111 : 1.8V SEL[6:2] = 10000 : 1.825V SEL[6:2] = 10001 : 1.85V SEL[6:2] = 10010 : 1.875V SEL[6:2] = 10011 : 1.9V SEL[6:2] = 10100 : 1.925V SEL[6:2] = 10101 : 1.95V SEL[6:2] = 10110 : 1.975V SEL[6:2] = 10111 : 2V SEL[6:2] = 11000 : 2.025V SEL[6:2] = 11001 : 2.05V SEL[6:2] = 11010 : 2.075V SEL[6:2] = 11011 to 11111 : 2.1V VOUT = SEL[6:2] x 0.025V + 1.425V, from SEL[6:2] = 3 to 1B (hex) (After each UVLO rising, the voltage is set to the value by VSEL0/VSEL1 setting : VSEL0 = 0, VSEL1 = 0, VOUT = 1.8V VSEL0 = 0, VSEL1 = 1, VOUT = 1.8V VSEL0 = 1, VSEL1 = 0, VOUT = 1.8V VSEL0 = 1, VSEL1 = 1, VOUT = 1.8V)
1 : 0	Reserved	Reserved bit

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Table 9. CH4_CFG_REG

Address : 0x07
Description : CH4 config register.
Set CH4 current limited, VID change slew rate, PWM frequency.

Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	Reserved	ILMAX		TSTEP		FREQ		
Reset Value	0	1	0	1	0	1	1	0
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
7	Reserved	Reserved bit
6 : 5	ILMAX	ILMAX[6:5] = 00 : 2A ILMAX[6:5] = 01 : 2.5A ILMAX[6:5] = 10 : 3A (default) ILMAX[6:5] = 11 : 3.5A
4 : 3	TSTEP	TSTEP[4:3] = 00 : 20mV/μs TSTEP[4:3] = 01 : 15mV/μs TSTEP[4:3] = 10 : 10mV/μs (default) TSTEP[4:3] = 11 : 5mV/μs
2 : 0	FREQ	FREQ[2:0] = 000 to 011, 1MHz FREQ[2:0] = 100, 1.5MHz FREQ[2:0] = 101, 2.0MHz FREQ[2:0] = 110, 2.5MHz (default) FREQ[2:0] = 111, 3.0MHz

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Table 10. CH4_SEL_REG

Address : 0x08
Description : CH4 VID setting register.
CH4 VID setting and power on/off status and control.

Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	Reserved	SEL					Reserved	
Reset Value	0	0	0	0	0	0	0	0
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
7	Reserved	Reserved bit
6 : 2	SEL	Supply voltage, SEL[6:2] = 00000 : 0.7V SEL[6:2] = 1 : 0.725V SEL[6:2] = 10 : 0.75V SEL[6:2] = 11 : 0.775V SEL[6:2] = 100 : 0.8V SEL[6:2] = 101 : 0.825V SEL[6:2] = 110 : 0.85V SEL[6:2] = 111 : 0.875V SEL[6:2] = 1000 : 0.9V SEL[6:2] = 1001 : 0.925V SEL[6:2] = 1010 : 0.95V SEL[6:2] = 1011 : 0.975V SEL[6:2] = 1100 : 1V SEL[6:2] = 1110 : 1.05V SEL[6:2] = 1111 : 1.075V SEL[6:2] = 10000 : 1.1V SEL[6:2] = 10001 : 1.125V SEL[6:2] = 10010 : 1.15V SEL[6:2] = 10011 : 1.175V SEL[6:2] = 10100 : 1.2V SEL[6:2] = 10101 : 1.225V SEL[6:2] = 10110 : 1.25V SEL[6:2] = 10111 : 1.275V SEL[6:2] = 11000 to 11111 : 1.3V VOUT = SEL[6:2] x 0.025V + 0.7V, from SEL[6:2] = 0 to 18 (hex) (After each UVLO rising, the voltage is set to the value by VSEL0/VSEL1 setting : VSEL0 = 0, VSEL1 = 0, VOUT = 1.0V VSEL0 = 0, VSEL1 = 1, VOUT = 1.0V VSEL0 = 1, VSEL1 = 0, VOUT = 1.2V VSEL0 = 1, VSEL1 = 1, VOUT = 1.2V)
1 : 0	Reserved	Reserved bit

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Table 11. CH5_CFG_REG

Address : 0x09
Description : CH5 config register.
Set CH5 current limited, VID change slew rate, PWM frequency.

Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	Reserved	ILMAX		TSTEP		FREQ		
Reset Value	0	1	0	1	0	1	1	0
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
7	Reserved	Reserved bit
6 : 5	ILMAX	ILMAX[6:5] = 00 : 1.5A ILMAX[6:5] = 01 : 2.0A ILMAX[6:5]= 10 : 2.5A (default) ILMAX[6:5] = 11 : 3A
4 : 3	TSTEP	TSTEP[4:3] = 00 : 20mV/μs TSTEP[4:3] = 01 : 15mV/μs TSTEP[4:3] = 10 : 10mV/μs (default) TSTEP[4:3] = 11 : 5mV/μs
2 : 0	FREQ	FREQ[2:0] = 000 to 011, 1MHz FREQ[2:0] = 100, 1.5MHz FREQ[2:0] = 101, 2.0MHz FREQ[2:0] = 110, 2.5MHz (default) FREQ[2:0] = 111, 3.0MHz

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Table 12. CH5_SEL_REG

Address : 0x0A
Description : CH5 VID setting register.
CH5 VID setting and power on/off status and control.

Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	Reserved	SEL					Reserved	
Reset Value	0	0	0	0	0	0	0	0
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
7	Reserved	Reserved bit
6 : 2	SEL	Supply voltage, SEL[6:2] = 00000 : 0.7V SEL[6:2] = 1 : 0.725V SEL[6:2] = 10 : 0.75V SEL[6:2] = 11 : 0.775V SEL[6:2] = 100 : 0.8V SEL[6:2] = 101 : 0.825V SEL[6:2] = 110 : 0.85V SEL[6:2] = 111 : 0.875V SEL[6:2] = 1000 : 0.9V SEL[6:2] = 1001 : 0.925V SEL[6:2] = 1010 : 0.95V SEL[6:2] = 1011 : 0.975V SEL[6:2] = 1100 : 1V SEL[6:2] = 1110 : 1.05V SEL[6:2] = 1111 : 1.075V SEL[6:2] = 10000 : 1.1V SEL[6:2] = 10001 : 1.125V SEL[6:2] = 10010 : 1.15V SEL[6:2] = 10011 : 1.175V SEL[6:2] = 10100 : 1.2V SEL[6:2] = 10101 : 1.225V SEL[6:2] = 10110 : 1.25V SEL[6:2] = 10111 : 1.275V SEL[6:2] = 11000 to 11111 : 1.3V VOUT = SEL[6:2] x 0.025V + 0.7V, from SEL[6:2] = 0 to 18 (hex) (After each UVLO rising, the voltage is set to the value by VSEL0/VSEL1 setting : VSEL0 = 0, VSEL1 = 0, VOUT = 1.0V VSEL0 = 0, VSEL1 = 1, VOUT = 1.0V VSEL0 = 1, VSEL1 = 0, VOUT = 0.9V VSEL0 = 1, VSEL1 = 1, VOUT = 0.9V)
1 : 0	Reserved	Reserved bit

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Table 13. CH6_CFG_REG

Address : 0x0B
Description : CH6 config register.
Set CH6 current limited, VID change slew rate, PWM frequency.

Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	Reserved	ILMAX		TSTEP		FREQ		
Reset Value	0	1	0	1	0	1	1	0
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
7	Reserved	Reserved bit
6 : 5	ILMAX	ILMAX[6:5] = 00 : 4A ILMAX[6:5] = 01 : 4.5A ILMAX[6:5] = 10 : 5A (default) ILMAX[6:5] = 11 : 5.5A
4 : 3	TSTEP	TSTEP[4:3] = 00 : 20mV/μs TSTEP[4:3] = 01 : 15mV/μs TSTEP[4:3] = 10 : 10mV/μs (default) TSTEP[4:3]= 11 : 5mV/μs
2 : 0	FREQ	FREQ[2:0] = 000 to 011, 1MHz FREQ[2:0] = 100, 1.5MHz FREQ[2:0] = 101, 2.0MHz FREQ[2:0] = 110, 2.5MHz (default) FREQ[2:0] = 111, 3.0MHz

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Table 14. CH6_SEL_REG

Address : 0x0C
Description : CH6 VID setting register.
CH5 VID setting and power on/off status and control.

Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	Reserved	SEL					Reserved	
Reset Value	0	0	0	0	0	0	0	0
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
7	Reserved	Reserved bit
6 : 2	SEL	Supply voltage, SEL[6:2] = 00000 : 0.7V SEL[6:2] = 1 : 0.725V SEL[6:2] = 10 : 0.75V SEL[6:2] = 11 : 0.775V SEL[6:2] = 100 : 0.8V SEL[6:2] = 101 : 0.825V SEL[6:2] = 110 : 0.85V SEL[6:2] = 111 : 0.875V SEL[6:2] = 1000 : 0.9V SEL[6:2] = 1001 : 0.925V SEL[6:2] = 1010 : 0.95V SEL[6:2] = 1011 : 0.975V SEL[6:2] = 1100 : 1V SEL[6:2] = 1110 : 1.05V SEL[6:2] = 1111 : 1.075V SEL[6:2] = 10000 : 1.1V SEL[6:2] = 10001 : 1.125V SEL[6:2] = 10010 : 1.15V SEL[6:2] = 10011 : 1.175V SEL[6:2] = 10100 : 1.2V SEL[6:2] = 10101 : 1.225V SEL[6:2] = 10110 : 1.25V SEL[6:2] = 10111 : 1.275V SEL[6:2] = 11000 to 11111 : 1.3V VOUT = SEL[6:2] x 0.025V + 0.7V, from SEL[6:2] = 0 to 18 (hex) (After each UVLO rising, the voltage is set to the value by VSEL0/VSEL1 setting : VSEL0 = 0, VSEL1 = 0, VOUT = 1.0V VSEL0 = 0, VSEL1 = 1, VOUT = 1.0V VSEL0 = 1, VSEL1 = 0, VOUT = 0.9V VSEL0 = 1, VSEL1 = 1, VOUT = 0.9V)
1 : 0	Reserved	Reserved bit

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Table 15. LDO_SEL_REG

Address : 0x0D
Description : LDO VID setting register.
LDO VID setting and power on/off status and control.

Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	Reserved	SEL					Reserved	
Reset Value	0	0	0	0	0	0	0	0
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
7	Reserved	Reserved bit
6 : 2	SEL	Supply voltage. After each UVLO rising, the voltage is set to the value by VSEL0/VSEL1 setting : VSEL0 = 0, VSEL1 = 0, VOUT = 2.5V VSEL0 = 0, VSEL1 = 1, VOUT = 2.5V SEL[6:2] = 00000 to 00011 : 2.3V SEL[6:2] = 100 : 2.325V SEL[6:2] = 101 : 2.35V SEL[6:2] = 110 : 2.375V SEL[6:2] = 111 : 2.4V SEL[6:2] = 1000 : 2.425V SEL[6:2] = 1001 : 2.45V SEL[6:2] = 1010 : 2.475V SEL[6:2] = 1011 : 2.5V SEL[6:2] = 1100 : 2.525V SEL[6:2] = 1110 : 2.575V SEL[6:2] = 1111 : 2.6V SEL[6:2] = 10000 : 2.625V SEL[6:2] = 10001 : 2.65V SEL[6:2] = 10010 : 2.675V SEL[6:2] = 10011 : 2.7V SEL[6:2] = 10100 : 2.725V SEL[6:2] = 10101 : 2.75V SEL[6:2] = 10110 : 2.775V SEL[6:2] = 10111 : 2.8V SEL[6:2] = 11000 : 2.825V SEL[6:2] = 11001 : 2.85V SEL[6:2] = 11010 : 2.875V SEL[6:2] = 11011 : 2.9V SEL[6:2] = 11100 : 2.925V SEL[6:2] = 11101 : 2.95V SEL[6:2] = 11110 : 2.975V SEL[6:2] = 11111 : 3V VOUT = SEL[6:2] x 0.025V + 2.225V, from SEL[6:2] = 3 to 1F (hex) After each UVLO rising, the voltage is set to the value by VSEL0/VSEL1 setting : VSEL0 = 1, VSEL1 = 0, VOUT = 1.8V VSEL0 = 1, VSEL1 = 1, VOUT = 1.8V SEL[6:2] = 00000 to 00011 : 1.656V SEL[6:2] = 100 : 1.674V SEL[6:2] = 101 : 1.692V SEL[6:2] = 110 : 1.71V SEL[6:2] = 111 : 1.728V SEL[6:2] = 1000 : 1.746V SEL[6:2] = 1001 : 1.764V

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6 : 2	SEL	SEL[6:2] = 1010 : 1.782V SEL[6:2] = 1011 : 1.8V SEL[6:2] = 1100 : 1.818V SEL[6:2] = 1101 : 1.836V SEL[6:2] = 1110 : 1.854V SEL[6:2] = 1111 : 1.872V SEL[6:2] = 10000 : 1.89V SEL[6:2] = 10001 : 1.908V SEL[6:2] = 10010 : 1.926V SEL[6:2] = 10011 : 1.944V SEL[6:2] = 10100 : 1.962V SEL[6:2] = 10101 : 1.98V SEL[6:2] = 10110 : 1.998V SEL[6:2] = 10111 : 2.016V SEL[6:2] = 11000 : 2.034V SEL[6:2] = 11001 : 2.052V SEL[6:2] = 11010 : 2.07V SEL[6:2] = 11011 : 2.088V SEL[6:2] = 11100 : 2.106V SEL[6:2] = 11101 : 2.124V SEL[6:2] = 11110 : 2.142V SEL[6:2] = 11111 : 2.16V
1 : 0	Reserved	Reserved bit

Table 16. DCDCCTRL0_REG

Address : 0x11
Description : DCDC high/low power mode control register.

Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	CH1_ EN	CH2_ EN	CH3_ EN	CH4_ EN	CH5_ EN	CH6_ EN	LDO_ EN	Reserved
Reset Value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R

Bits	**Name**	**Description**
7	CH1_ EN	0 : Disable 1 : Enable (After each UVLO rising, the value is set to 1)
6	CH2_ EN	0 : Disable 1 : Enable (After each UVLO rising, the value is set to 1)
5	CH3_ EN	0 : Disable 1 : Enable (After each UVLO rising, the value is set to 1)
4	CH4_ EN	0 : Disable 1 : Enable (After each UVLO rising, the value is set to 1)
3	CH5_ EN	0 : Disable 1 : Enable (After each UVLO rising, the value is set to 1)
2	CH6_ EN	0 : Disable 1 : Enable (After each UVLO rising, the value is set to 1)
1	LDO_ EN	0 : Disable 1 : Enable (After each UVLO rising, the value is set to 1)
0	Reserved	Reserved bit

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Table 17. SLEEP_REG

Address : 0x12 **Description :** Sleep mode control register.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	CH1_ ALIVE	CH2_ ALIVE	CH3_ ALIVE	CH4_ ALIVE	CH5_ ALIVE	CH6_ ALIVE	LDO_ ALIVE	SLEEP
Reset Value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
7	CH1_ ALIVE	0 : When Sleep bit = 1 , CH1 turn off 1 : When Sleep bit = 1, CH1 alive and enter low power mode
6	CH2_ ALIVE	0 : When Sleep bit = 1 , CH2 turn off 1 : When Sleep bit = 1, CH2 alive and enter low power mode
5	CH3_ ALIVE	0 : When Sleep bit = 1 , CH3 turn off 1 : When Sleep bit = 1, CH3 alive and enter low power mode
4	CH4_ ALIVE	0 : When Sleep bit = 1 , CH4 turn off 1 : When Sleep bit = 1, CH4 alive and enter low power mode
3	CH5_ ALIVE	0 : When Sleep bit = 1 , CH5 turn off 1 : When Sleep bit = 1, CH5 alive and enter low power mode
2	CH6_ ALIVE	0 : When Sleep bit = 1 , CH6 turn off 1 : When Sleep bit = 1, CH6 alive and enter low power mode
1	LDO_ ALIVE	0 : When Sleep bit = 1 , LDO turn off 1 : When Sleep bit = 1, LDO alive and enter low power mode
0	SLEEP	0 : Exit sleep mode 1 : Enter sleep mode

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Table 18. DCDCCTRL1_REG

Address : 0x13 **Description :** DCDC PSKIP/PWM mode control register.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	CH1_ PWM	CH2_ PWM	CH3_ PWM	CH4_ PWM	CH5_ PWM	CH6_ PWM	Reserved	
Reset Value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Bits	Name	Description
7	CH1_PWM	CH1_PWM[7] = 0 : PSKIP mode. CH1_PWM[7] = 1 : Forced PWM mode
6	CH2_ PWM	CH2_PWM[6] = 0 : PSKIP mode. CH2_PWM[6] = 1 : Forced PWM mode
5	CH3_ PWM	CH3_PWM[5] = 0 : PSKIP mode. CH3_PWM[5] = 1 : Forced PWM mode
4	CH4_ PWM	CH4_PWM[4] = 0 : PSKIP mode. CH4_PWM[4] = 1 : Forced PWM mode
3	CH5_ PWM	CH5_PWM[3] = 0 : PSKIP mode. CH5_PWM[3] = 1 : Forced PWM mode
2	CH6_ PWM	CH6_PWM[2] = 0 : PSKIP mode. CH6_PWM[2] = 1 : Forced PWM mode
1 : 0	Reserved	Reserved bit

Table 19. DISCHARGE_REG

Address : 0x14 **Description :** Discharge enable register.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	CH1_DIS	CH2_DIS	CH3_DIS	CH4_DIS	CH5_DIS	CH6_DIS	LDO_DIS	Reserved
Reset Value	1	1	1	1	1	1	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R

Bits	Name	Description
7	CH1_DIS	CH1_DIS[7] = 0 : discharge path disable CH1_DIS[7] = 1 : discharge path enable
6	CH2_DIS	CH2_DIS[6] = 0 : discharge path disable CH2_DIS[6] = 1 : discharge path enable
5	CH3_DIS	CH3_DIS[5] = 0 : discharge path disable CH3_DIS[5] = 1 : discharge path enable
4	CH4_DIS	CH4_DIS[4] = 0 : discharge path disable CH4_DIS[4] = 1 : discharge path enable
3	CH5_DIS	CH5_DIS[3] = 0 : discharge path disable CH5_DIS[3] = 1 : discharge path enable
2	CH6_DIS	CH6_DIS[2] = 0 : discharge path disable CH6_DIS[2] = 1 : discharge path enable
1	LDO_DIS	LDO_DIS[1] = 0 : discharge path disable LDO_DIS[1] = 1 : discharge path enable
0	Reserved	Reserved bit

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Table 20. POR_OPTION_REG

Address : 0x17 **Description :** POR_OPTION select register.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	Reserved						POR_OPTION_SEL	
Reset Value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R/W	R/W

Bits	Name	Description
7 : 2	Reserved	Reserved bit
0 : 1	POR_OPTION_SEL	Supply state POR_OPTION_SEL[1:0] = 00, depended on AVDD POR rising with delay time POR_OPTION_SEL[1:0] = 01, reserved. POR_OPTION_SEL[1:0] = 10, POR_OPTION = 0 POR_OPTION_SEL[1:0] = 11, POR_OPTION = 1

Table 21. DCDCTRL2_REG

Address : 0x18 **Description :** DCDC high/low power mode control register.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	CH1_LPM	CH2_LPM	CH3_LPM	CH4_LPM	CH5_LPM	CH6_LPM	LDO_LPM	Reserved
Reset Value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R

Bits	Name	Description
7	CH1_LPM	CH1_LPM[7] = 0 : active high power mode. CH1_LPM[7] = 1 : active low power mode.
6	CH2_LPM	CH2_LPM[6] = 0 : active high power mode. CH2_LPM[6] = 1 : active low power mode.
5	CH3_LPM	CH3_LPM[5] = 0 : active high power mode. CH3_LPM[5] = 1 : active low power mode.
4	CH4_LPM	CH4_LPM[4] = 0 : active high power mode. CH4_LPM[4] = 1 : active low power mode.
3	CH5_LPM	CH5_LPM[3] = 0 : active high power mode. CH5_LPM[3] = 1 : active low power mode.
2	CH6_LPM	CH6_LPM[2] = 0 : active high power mode. CH6_LPM[2] = 1 : active low power mode.
1	LDO_LPM	LDO_LPM[1] = 0 : active high power mode. LDO_LPM[1] = 1 : active low power mode.
0	Reserved	Reserved bit

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Table 22. Ch1/Ch2_Wake-up_time

Address : 0x19
Description :. Ch1/Ch2_Wake-up_time

Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	Ch1_Wake-up_time				Ch2_Wake-up_time			
Reset Value	0	0	0	0	0	0	0	0
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
7:4	Ch1_Wake-up_time	CH1 sleep wake-up sequence Disable = 0000 Time slot1 = 0001 Time slot2 = 0010 Time slot3 = 0011 Time slot4 = 0100 Time slot5 = 0101 Time slot6 = 0110 Time slot7 = 0111 Time slot8 = 1000 Time slot9 = 1001 Time slot10 = 1010 Time slot11 = 1011 Time slot12 = 1100 Time slot13 = 1101 Time slot14 = 1110 Time slot15 = 1111 Time slot time = 512μs
3:0	Ch2_Wake-up_time	CH2 sleep wake-up sequence Disable = 0000 Time slot1 = 0001 Time slot2 = 0010 Time slot3 = 0011 Time slot4 = 0100 Time slot5 = 0101 Time slot6 = 0110 Time slot7 = 0111 Time slot8 = 1000 Time slot9 = 1001 Time slot10 = 1010 Time slot11 = 1011 Time slot12 = 1100 Time slot13 = 1101 Time slot14 = 1110 Time slot15 = 1111 Time slot time = 512μs

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Table 23. Ch3/Ch4_Wake-up_time

Address : 0x1A
Description :. Ch3/Ch4_Wake-up_time

Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	Ch3_Wake-up_time				Ch4_Wake-up_time			
Reset Value	0	0	0	0	0	0	0	0
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
7:4	Ch3_Wake-up_time	CH3 sleep wake-up sequence Disable = 0000 Time slot1 = 0001 Time slot2 = 0010 Time slot3 = 0011 Time slot4 = 0100 Time slot5 = 0101 Time slot6 = 0110 Time slot7 = 0111 Time slot8 = 1000 Time slot9 = 1001 Time slot10 = 1010 Time slot11 = 1011 Time slot12 = 1100 Time slot13 = 1101 Time slot14 = 1110 Time slot15 = 1111 Time slot time = 512μs
3:0	Ch4_Wake-up_time	CH4 sleep wake-up sequence Disable = 0000 Time slot1 = 0001 Time slot2 = 0010 Time slot3 = 0011 Time slot4 = 0100 Time slot5 = 0101 Time slot6 = 0110 Time slot7 = 0111 Time slot8 = 1000 Time slot9 = 1001 Time slot10 = 1010 Time slot11 = 1011 Time slot12 = 1100 Time slot13 = 1101 Time slot14 = 1110 Time slot15 = 1111 Time slot time = 512μs

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Table 24. Ch5/Ch6_Wake-up_time

Address : 0x1b **Description :**. Ch5/Ch6_Wake-up_time								
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	Ch5_Wake-up_time				Ch6_Wake-up_time			
Reset Value	0	0	0	0	0	0	0	0
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
7:4	Ch5_Wake-up_time	CH5 sleep wake-up sequence Disable = 0000 Time slot1 = 0001 Time slot2 = 0010 Time slot3 = 0011 Time slot4 = 0100 Time slot5 = 0101 Time slot6 = 0110 Time slot7 = 0111 Time slot8 = 1000 Time slot9 = 1001 Time slot10 = 1010 Time slot11 = 1011 Time slot12 = 1100 Time slot13 = 1101 Time slot14 = 1110 Time slot15 = 1111 Time slot time = 512μs
3:0	Ch6_Wake-up_time	CH6 sleep wake-up sequence Disable = 0000 Time slot1 = 0001 Time slot2 = 0010 Time slot3 = 0011 Time slot4 = 0100 Time slot5 = 0101 Time slot6 = 0110 Time slot7 = 0111 Time slot8 = 1000 Time slot9 = 1001 Time slot10 = 1010 Time slot11 = 1011 Time slot12 = 1100 Time slot13 = 1101 Time slot14 = 1110 Time slot15 = 1111 Time slot time = 512μs

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Table 25. LDO Wake-up_time

Address : 0x1C **Description :**LDO_Wake-up_time								
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	LDO_Wake-up_time				Reserved			
Reset Value	0	0	0	0	0	0	0	0
Read/Write	RW	RW	RW	RW	R	R	R	R

Bits	Name	Description
7:4	LDO_Wake-up_time	LDO sleep wake-up sequence Disable = 0000 Time slot1 = 0001 Time slot2 = 0010 Time slot3 = 0011 Time slot4 = 0100 Time slot5 = 0101 Time slot6 = 0110 Time slot7 = 0111 Time slot8 = 1000 Time slot9 = 1001 Time slot10 = 1010 Time slot11 = 1011 Time slot12 = 1100 Time slot13 = 1101 Time slot14 = 1110 Time slot15 = 1111 Time slot time = 512μs
3:0	Reserved	Reserved bits

Table 26. PRODUCT_ID_REG

Address : 0x20 **Description :** Product ID number register.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	PRODUCT_ID							
Reset Value	0x01							
Read/Write	R	R	R	R	R	R	R	R

Bits	Name	Description
7 : 0	PRODUCT_ID	Return the product ID number : 0x01

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Table 27. MANUFACTURER_ID_REG

Address : 0x21 **Description :** Manufacturer ID number register.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	MANUFACTURER_ID							
Reset Value	0x01							
Read/Write	R	R	R	R	R	R	R	R

Bits	Name	Description
7 : 0	MANUFACTURER_ID	Return the manufacturer ID number : 0x01

Table 28. REVISION_NUMBER_REG

Address : 0x22 **Description :** Revision number register.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	REVISION_NUMBER							
Reset Value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

Bits	Name	Description
7 : 0	REVISION_NUMBER	Return the revision number : 0x00

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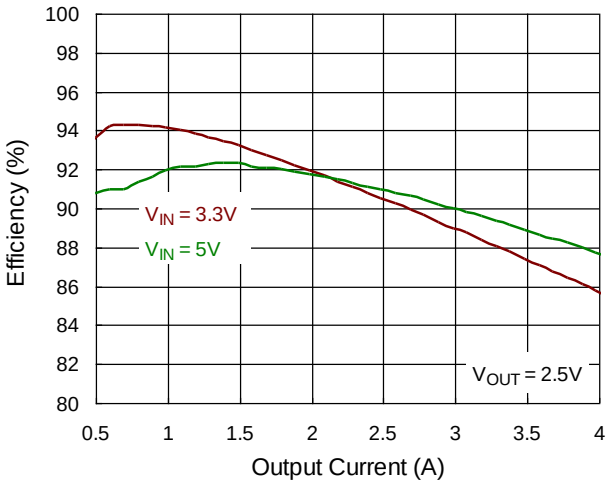
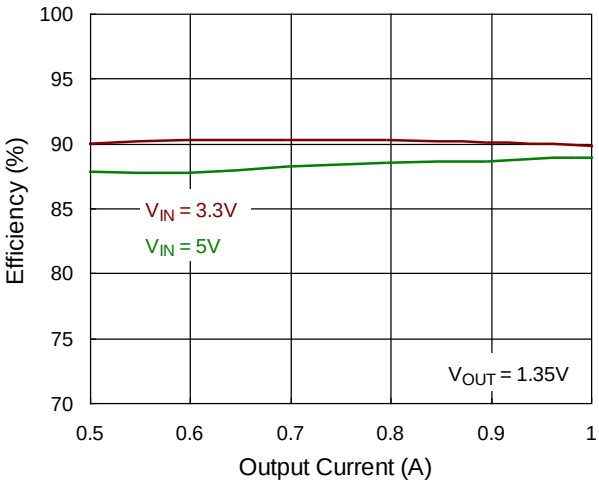
Typical Operating Characteristics

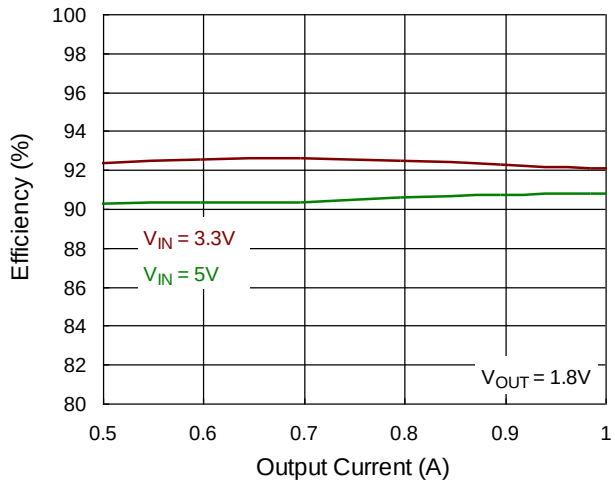
CH1 Efficiency vs. Output Current



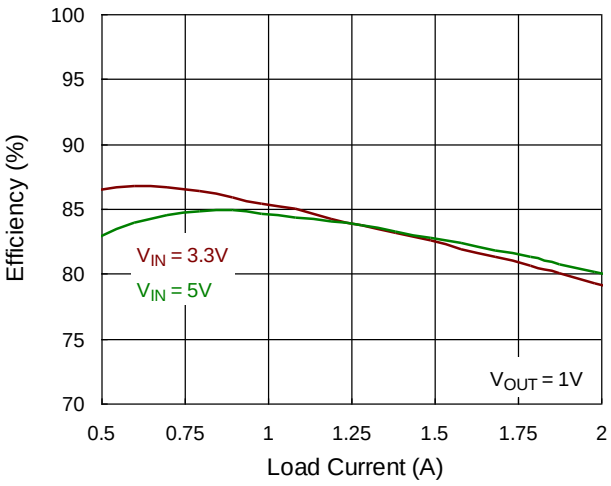
CH2 Efficiency vs. OutputCurrent



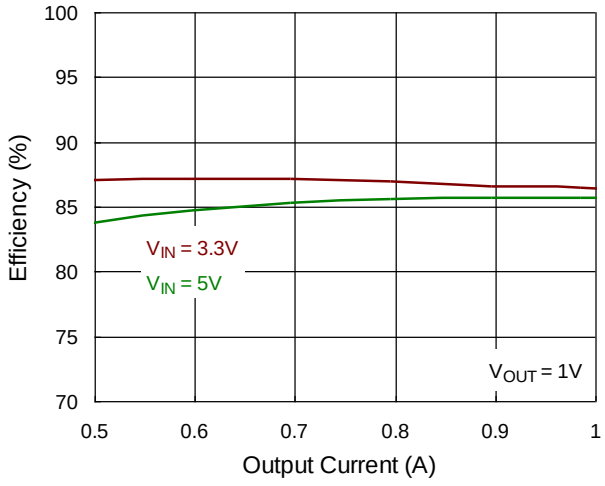
CH3 Efficiency vs. Output Current



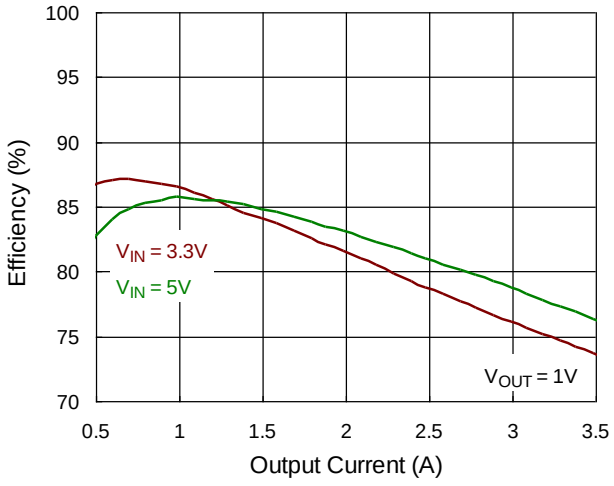
CH4 Efficiency vs. Load Current



CH5 Efficiency vs. Output Current



CH6 Efficiency vs. Output Current



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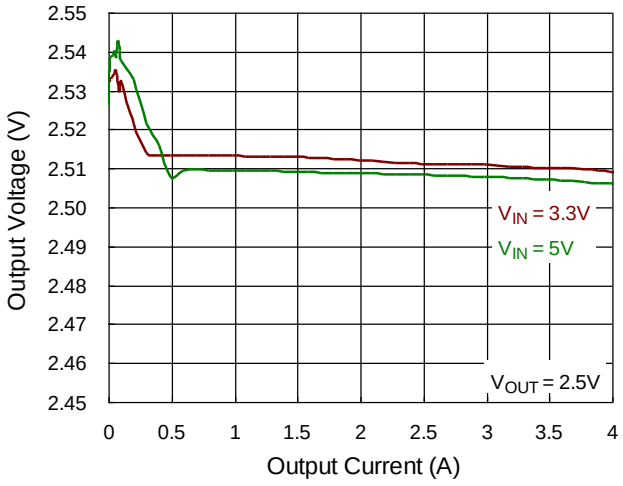
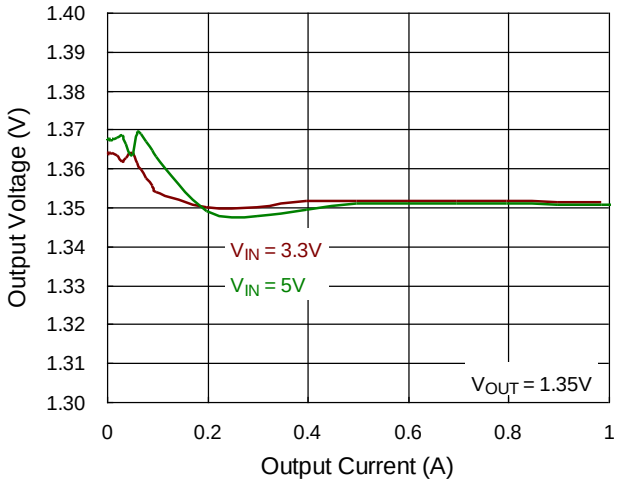
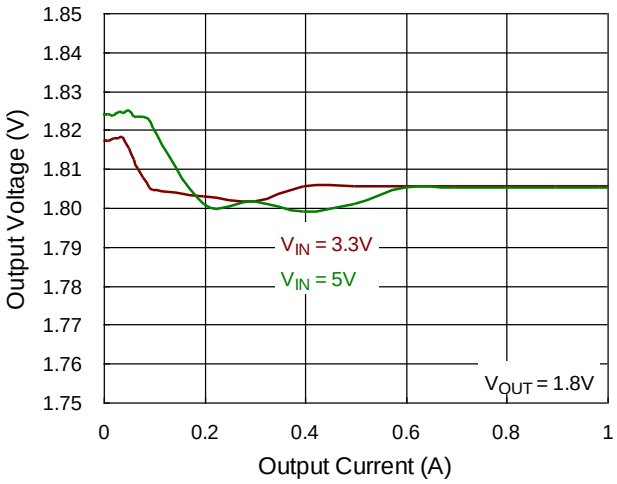
CH1 Output Voltage vs. Output Current



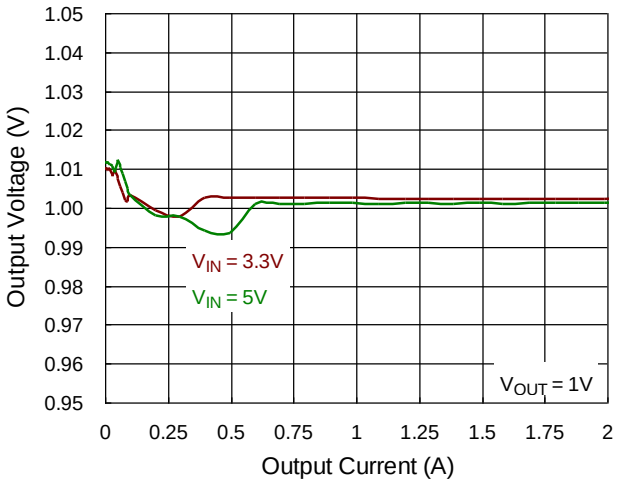
CH2 Output Voltage vs. Output Current



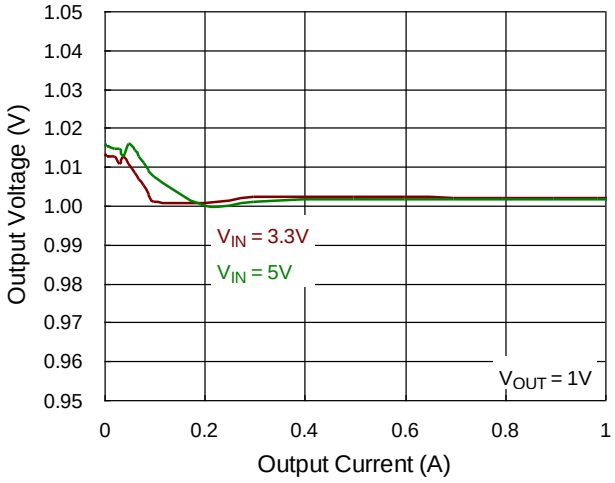
CH3 Output Voltage vs. Output Current



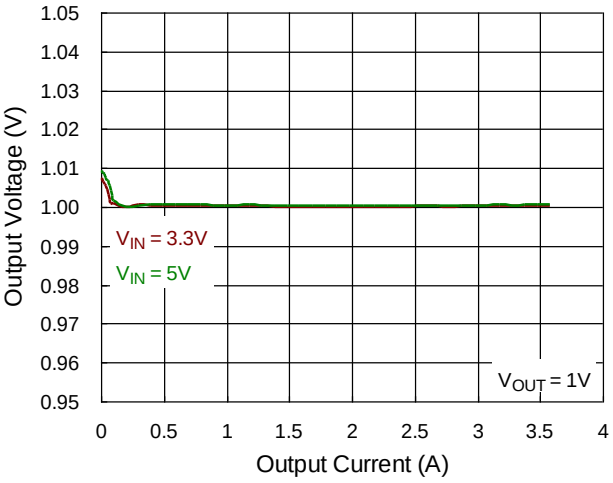
CH4 Output Voltage vs. Output Current



CH5 Output Voltage vs. Output Current



CH6 Output Voltage vs. Output Current



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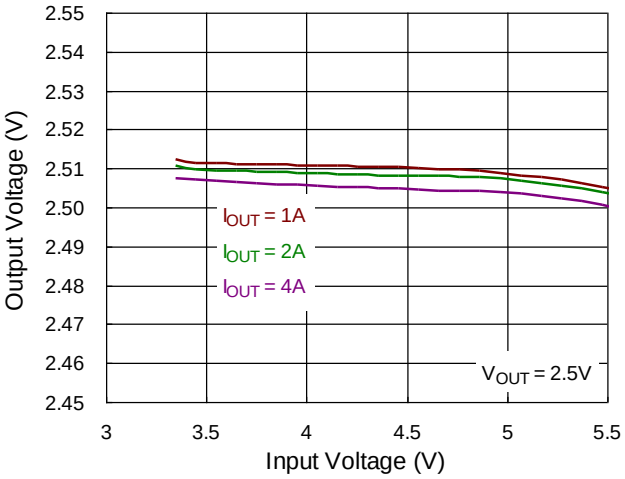
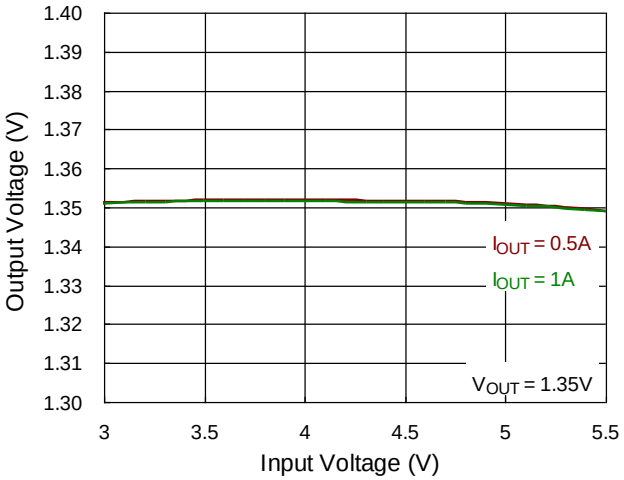
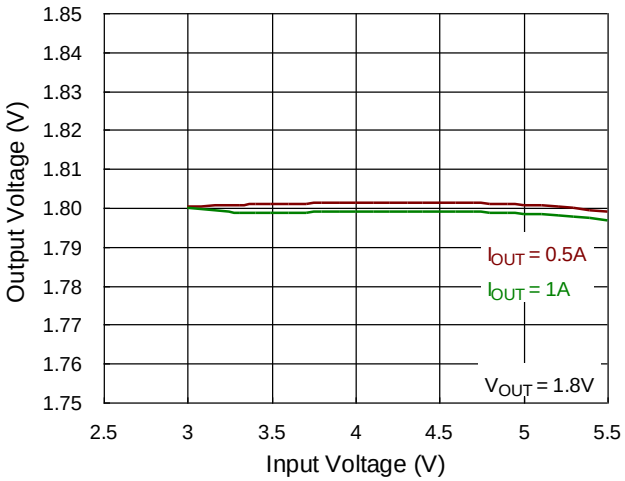
CH1 Output Voltage vs. Input Voltage



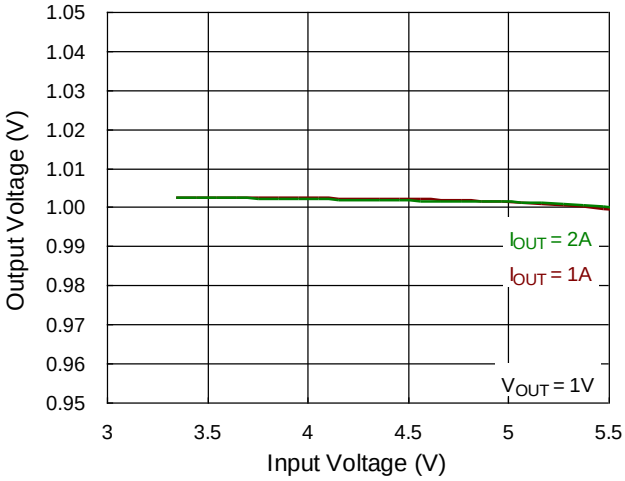
CH2 Output Voltage vs. Input Voltage



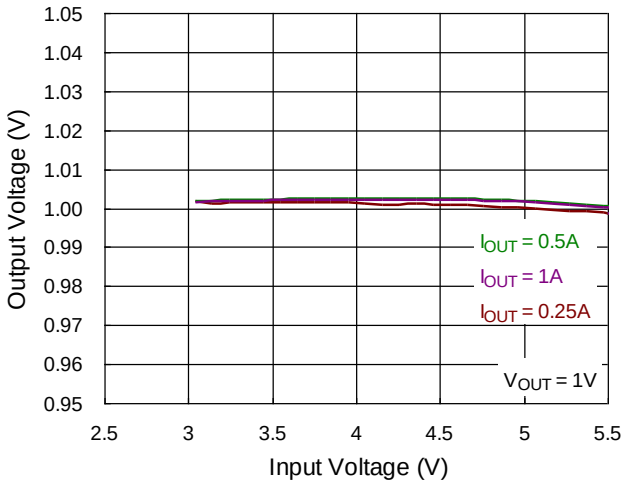
CH3 Output Voltage vs. Input Voltage



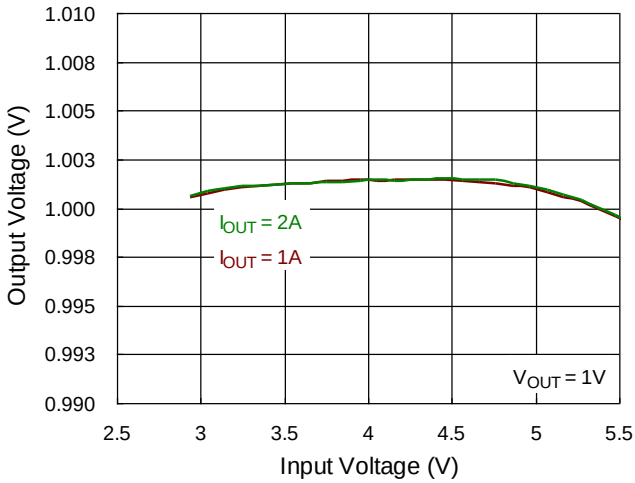
CH4 Output Voltage vs. Input Voltage



CH5 Output Voltage vs. Input Voltage



CH6 Output Voltage vs. Input Voltage



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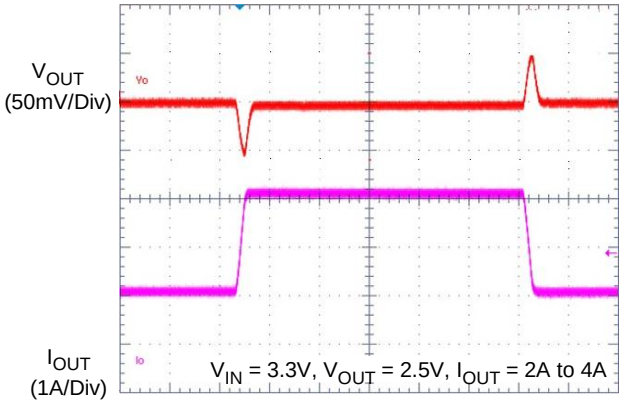
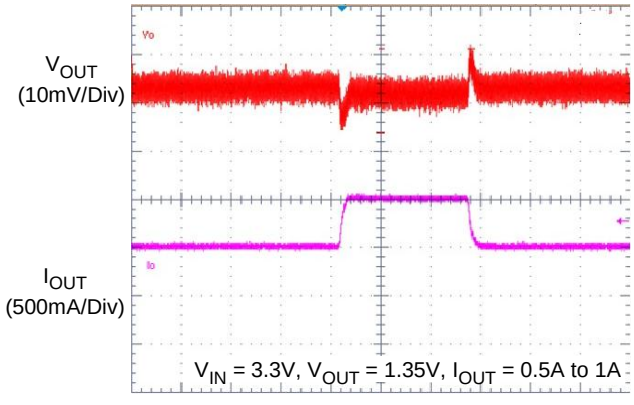
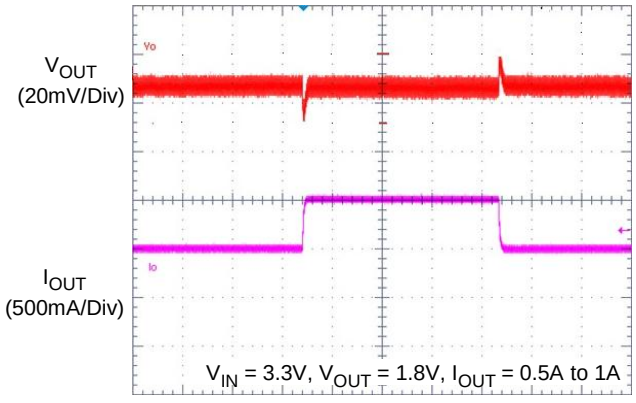
CH1 Load Transient Response



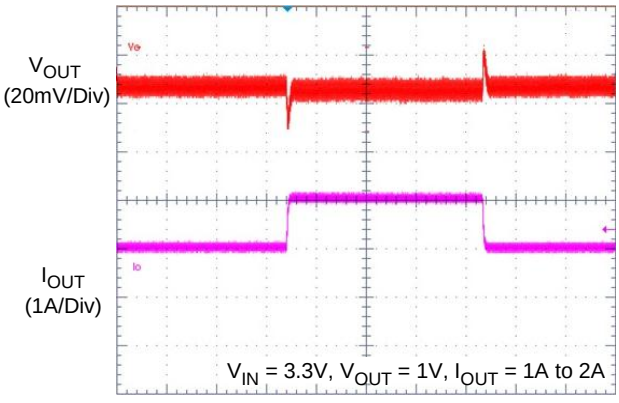
CH2 Load Transient Response



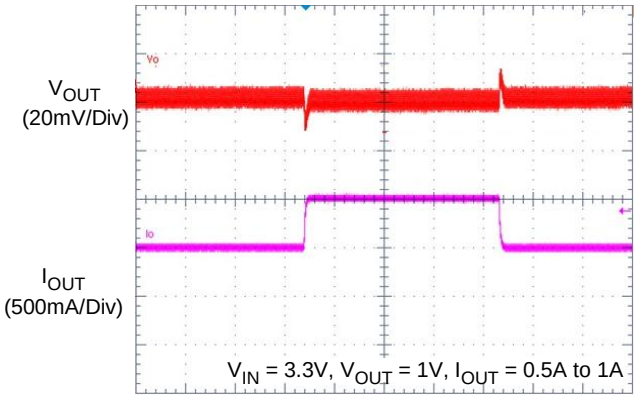
CH3 Load Transient Response



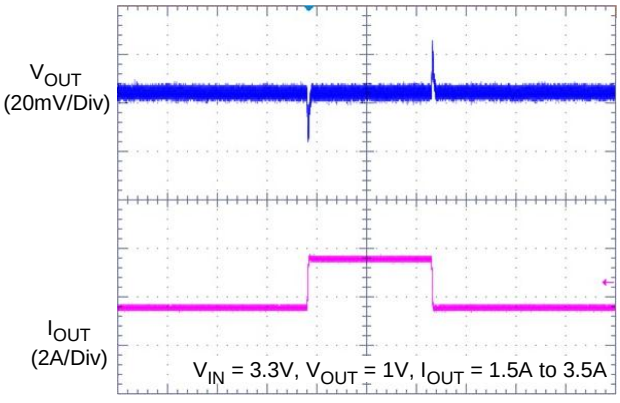
CH4 Load Transient Response



CH5 Load Transient Response



CH6 Load Transient Response



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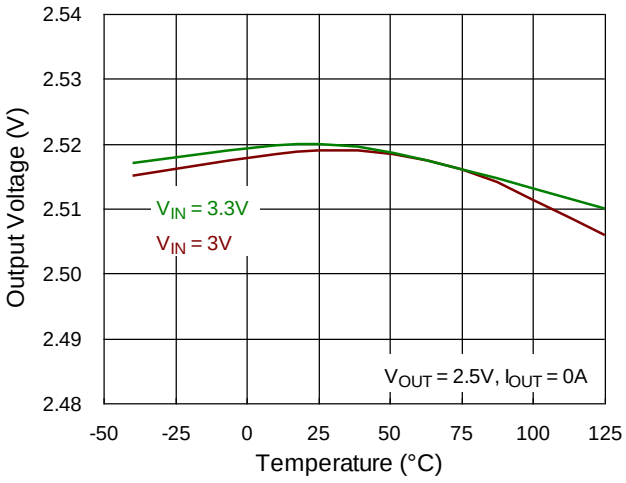
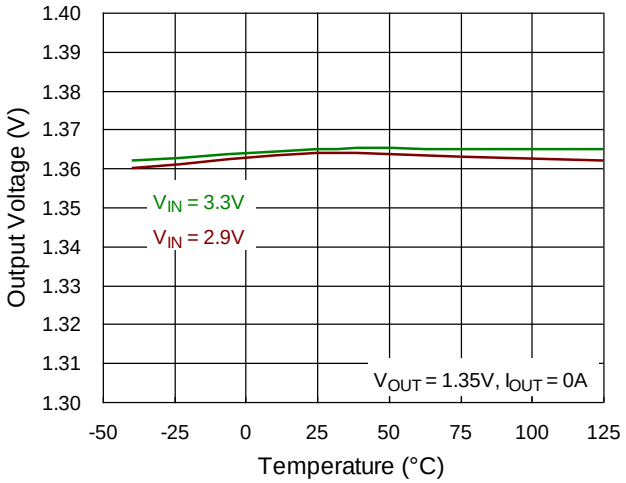
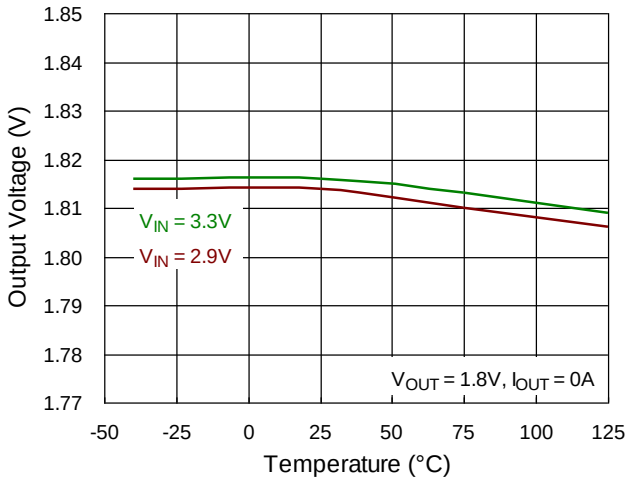
CH1 Output Voltage vs. Temperature



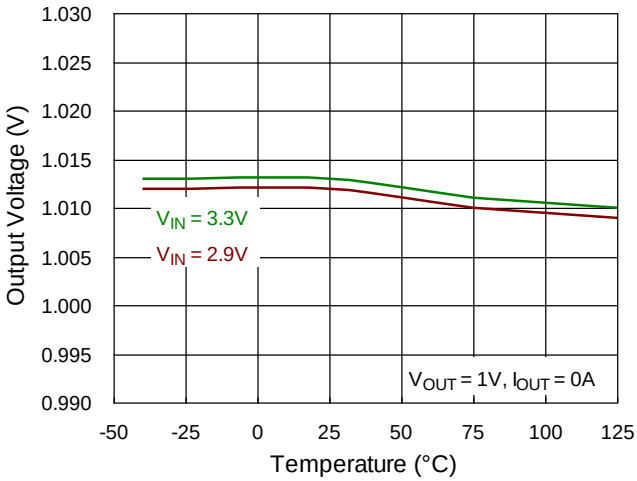
CH2 Output Voltage vs. Temperature



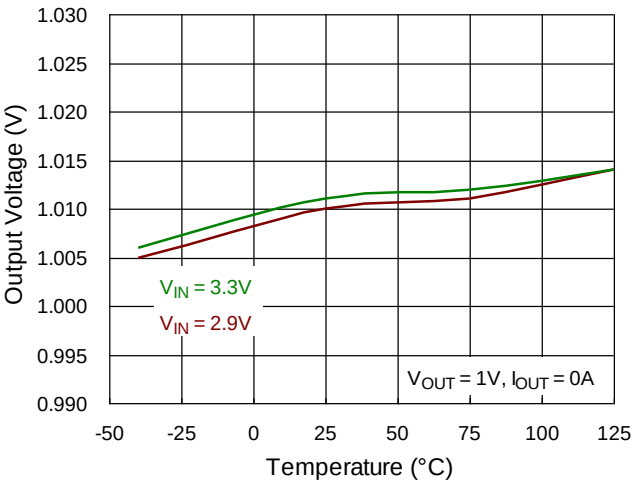
CH3 Output Voltage vs. Temperature



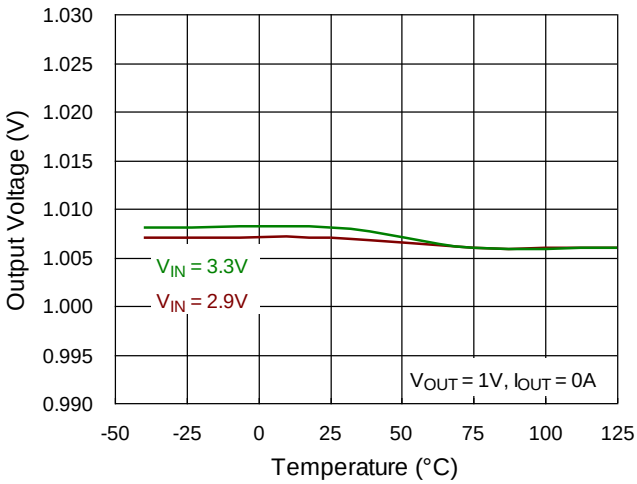
CH4 Output Voltage vs. Temperature



CH5 Output Voltage vs. Temperature



CH6 Output Voltage vs. Temperature



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Application Information

The RT5045A provides six synchronous Buck regulators and one LDO to satisfy the entire power system of SSD. This device can communicate with processors through I^{2}C interface for programming the voltage, monitoring the status, or in/out the power saving mode. Table 29 lists the power rails provided by the RT5045A.

Table 29. Detail of Power Rails

Resource Name	Type	Voltage Range	Current Rating
CH1	Buck Converter	2.3V – 3.0V, 25mV step	4000mA
CH2	Buck Converter	0.9V – 1.6V, 25mV step	1000mA
CH3	Buck Converter	1.5V – 2.1V, 25mV step	1000mA
CH4	Buck Converter	0.7V – 1.3V, 25mV step	2000mA
CH5	Buck Converter	0.7V – 1.3V, 25mV step	1000mA
CH6	Buck Converter	0.7V – 1.3V, 25mV step	3500mA
LDO	LDO	2.3V – 3.0V, 25mV step 1.656V-2.16V,18mV step	200mA

Buck Converter

The RT5045A incorporates six high-efficiency synchronous switching Buck converters that deliver various voltages. CH1 features peak current mode architecture of Buck converter. For preventing the unstable when duty > 50% traditionally, it adds external ramp and compensation to reduce duty cycle perturbation and stabilize the current loop. CH1 can operate up to 100% duty to let the lowest input voltage still maintain the regulator work. And the output voltage will be the lowest input voltage decreases dropout voltage on the resistance of current path. Unlike CH1, the control scheme of other buck converters are constant-on-time current mode for low output voltage, quick transient response.

Every switching regulator is specially designed for very low quiescent (<20μA), high-efficiency operation throughout the load range. With high switching frequency (1M to 3MHz), the external LC filter can be small and keeps very low output voltage ripple.

Additional features include soft-start, discharged, input UVLO protection, under-voltage protection, over voltage protection, over current protection and over thermal protection. Please note that the IC will latched when one power rail occurs under voltage protection. The other protections just make the rail output voltage drop and recovery when the faults disabled.

With I^{2}C interface, every Buck converter can program output voltage, adjust VID slew rate, change the PWM frequency, and control the on/off state. Even PWM can switch to forced PWM mode, PSKIP mode or LPM mode (quiescent < 10μA). Please see the back register tables for detail control.

Inductor Selection

For given input voltage (V_{IN}), output voltage (V_{OUT}), and operation frequency (F_{SW}), the inductor value (L) determines the inductor ripple current (ΔI_L) as shown in equation below :

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{F_{SW} \times L \times V_{IN}}$$

Having a lower ripple current reduces not only the ESR losses in the output capacitors, but also the output voltage ripple.

A reasonable starting point for selecting the ripple current is $\Delta I_L = 0.3 \times I_{MAX}$ to $0.4 \times I_{MAX}$. The largest ripple current occurs at the highest VIN. To guarantee that the ripple current stays below a specified maximum, the inductor value should be chosen according to the following equation :

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$$L=\frac{V_{OUT}\times\left(V_{IN(MAX)}-V_{OUT}\right)}{F_{SW}\times\Delta I_L\times V_{IN(MAX)}}$$

The current rating of the inductor must be large enough and will not saturate at the peak inductor current (I_{PEAK}) :

$$I_{PEAK}=I_{OUT(MAX)}+\frac{\Delta I_L}{2}$$

C_{IN} and C_{SYS} Selection

The input capacitance of every rail, C_{IN}, needs to filter the trapezoidal current at the source of the high-side MOSFET. To prevent large ripple voltage, a low ESR input capacitor for the maximum current should be used. The relation between C_{IN} ripple voltage and current ripple is shown as the Figure 1.

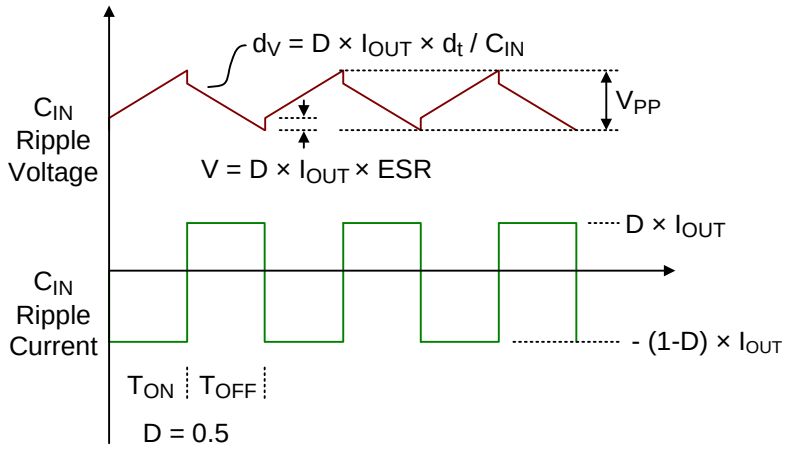

Figure 1. Relationship of C_{IN} Voltage Ripple and Current Ripple

The C_{IN} voltage ripple can use below equations to determine when F_{SW} works at CCM mode.

$$V_{CIN\_PP}=D\times I_{OUT(MAX)}\times\left(ESR+\frac{(1-D)}{C_{IN}\times F_{SW}}\right)$$

Where D = V_{OUT} / V_{IN}. If use MLCC as the input current, the ESR is almost equal to zero. And the minimum input capacitance requirement could be estimate as below :

$$C_{IN(MIN)}=I_{OUT(MAX)}\times\frac{D\times(1-D)}{V_{CIN\_PP(MAX)}\times F_{SW}}$$

Next, it needs to consider the input bulk capacitance, C_{SYS}, to ensure a stable input voltage during large load transient. The input host supply can not typically provide the enough input current for the converter to respond to a fast transient current. The input bulk capacitor will provide the energy necessary to source current until the host supply fill the demand, as shown as Figure 2.

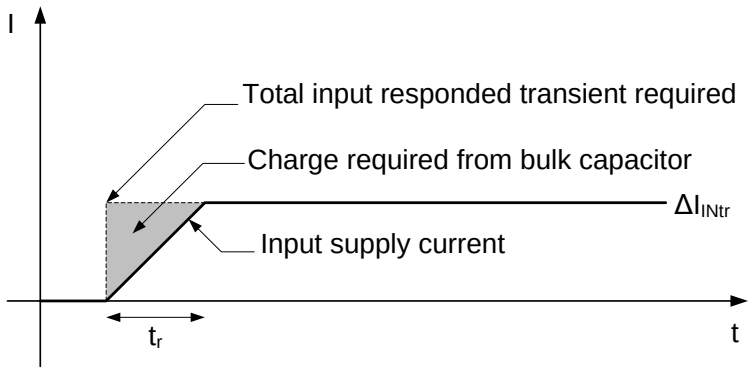

Figure 2. Charge Required from Input Bulk Capacitor During Transient.

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Figure 3 shows the diagram of every power rail of RT5045A sharing a single bank of bulk input capacitors. It can calculate the input required transient current using following equation :

$$\Delta I_{INtr} = \sum_{n=1}^{6} \frac{V_{OUTn} \times \Delta I_{OUTn(MAX)}}{V_{IN} \times \eta_n}$$

Where ΔI_{INtr} is the total input transient current required. ΔI_{OUT} is the maximum output transient current. η is the efficiency of the Buck at $I_{OUT(MAX)}$.

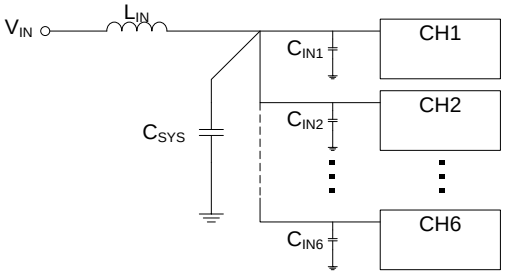

Figure 3. The Location of Bulk Input Capacitance Diagram

When ΔI_{INtr} is confirmed, the input bulk capacitance, C_{SYS}, can be decided with following estimating equation:

$$C_{SYS(MIN)} \cong \frac{1.21 \times \Delta I_{INtr}^2 \times L_{IN}}{\Delta V_{INPP(MAX)}^2}$$

where $\Delta V_{INPP(MAX)}$ is the maximum ac voltage allowable. L_{IN} is the input series filter inductance, if not used, put a reasonable value 50nH due to PCB layout.

C_{OUT} selection

The output capacitor and the inductor form a low pass filter in the buck topology. In steady state condition, the ripple current flowing into/out of the capacitor results in ripple voltage. The output voltage ripple (ΔV_{OUTPP}) can be calculated by the following equation:

$$\Delta V_{OUTPP} = \Delta I_L \left(ESR + \frac{1}{8 \times C_{OUT} \times F_{SW}} \right)$$

When load transient occurs, the output capacitor supplies the load current before the controller can respond. Therefore, the ESR will dominate the output voltage sag during load transient. The output voltage under-shoot (V_{SAG}) can be calculated by the following equation :

$$V_{SAG} = \Delta I_{LOAD} \times ESR$$

For a given output voltage sag specification, the ESR value can be determined.

Another parameter that has influence on the output voltage sag is the equivalent series inductance (ESL). The rapid change in load current results in di/dt during transient. Therefore, the ESL contributes to part of the voltage sag. Using a capacitor with low ESL can obtain better transient performance. Generally, using several capacitors connected in parallel can have better transient performance than using a single capacitor for the same total ESR.

Unlike the electrolytic capacitor, the ceramic capacitor has relatively low ESR and can reduce the voltage deviation during load transient. However, the ceramic capacitor can only provide low capacitance value. Therefore, use a mixed combination of electrolytic capacitor and ceramic capacitor to obtain better transient performance.

VSEL0, VSEL1

The RT5045A applies four set default output voltages for all power rails when the device starts a power up sequence. The detail of the initial output voltages shows in Table 30 lists the power rails provide by the RT5045A.

Table 30

VSEL0	**0**	**0**	**1**	**1**
VSEL1	**0**	**1**	**0**	**1**
CH1	2.5V	2.5V	2.5V	2.5V
CH2	1.35V	1.35V	1.35V	1.2V
CH3	1.8V	1.8V	1.8V	1.8V
CH4	1.0V	1.0V	1.2V	1.2V
CH5	1.0V	1.0V	0.9V	0.9V
CH6	1.0V	1.0V	0.9V	0.9V
LDO	2.5V	2.5V	1.8V	1.8V
POR delay time	10ms	10ms	6ms	6ms

PORSEL

PORSEL is a logic pin to select the threshold voltage of AVDD to raise POR signal. If AVDD voltage is over the threshold voltage, the device starts a POR rising function. When set PORSEL = 1, the threshold voltage of AVDD is 3.8V, else the threshold voltage is 2.8V.

POR_OPTION

Please refer to the following table to realize the POR_OPTION setting.

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Table 31. POR_OPTION Value Setting Condition

POR_OPTION_REG POR_OPTION_SEL [0:1]	Description
0x00	POR_OPTION = 0
0x01	Reversed.
0x02	POR_OPTION = 0
0x03	POR_OPTION = 1

POR

POR pin is a signal to inform the system that the power up sequence of the RT5045A is completed. At POR_OPTION = 0 situation. If AVDD voltage is less than 100mV than VPORTH, the POR falls right away.

When the device gets POR_OPTION = 1, POR will fall after SLEEP[0] = 0 turns to SLEEP[0] = 1, and POR comes after SLEEP [0] = 1 turn to SLEEP[0] = 0 with a 8ms delay.

I²C Interface

The RT5045A I²C slave address = 0x1b (hex). I²C interface supports standard slave mode (100kbps), and fast mode (400kbps). The write or read bit stream (N ≥ 1) is shown below :

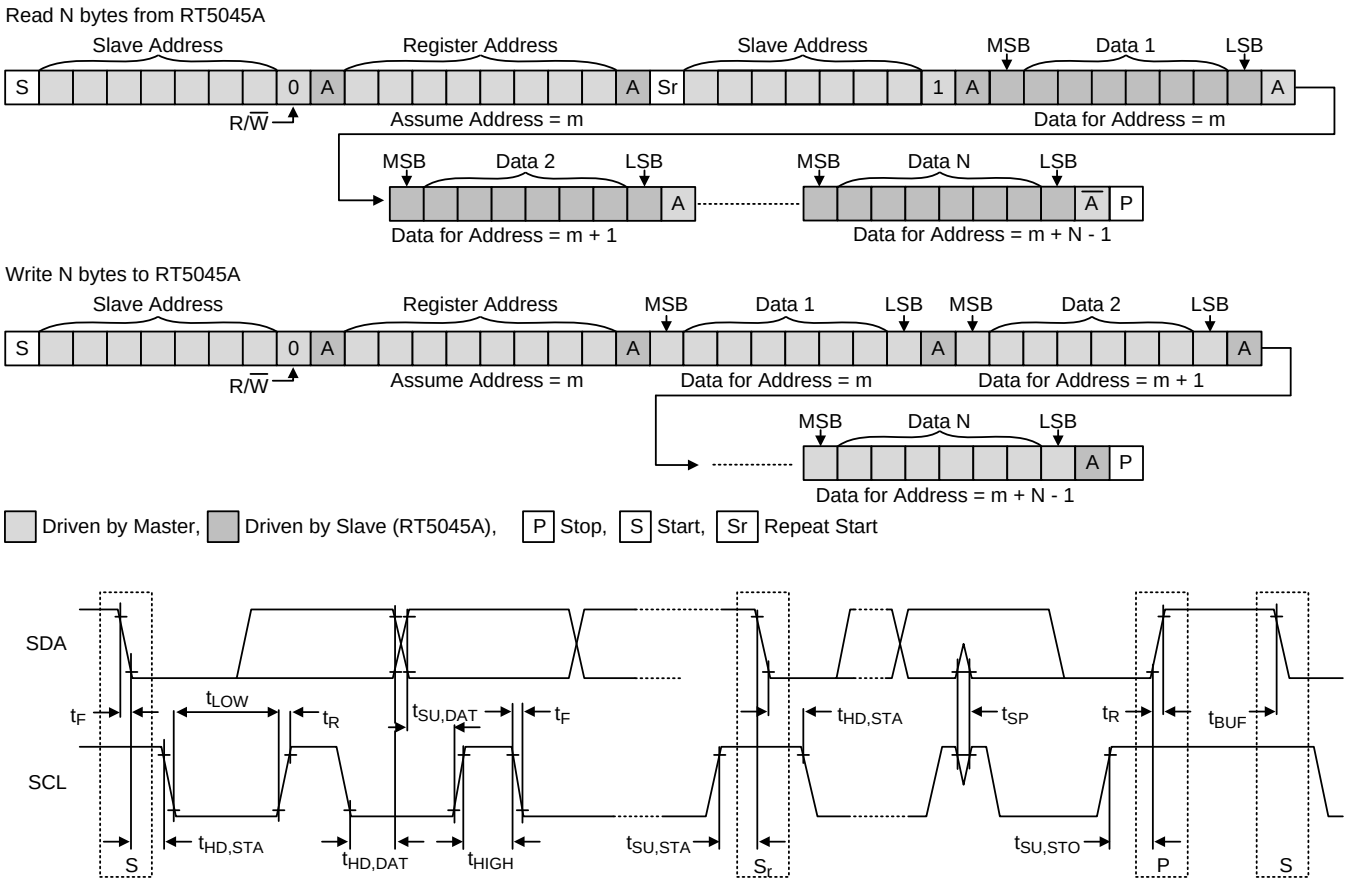

Figure 4. I²C Read and Write Stream and Timing Diagram

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Serial Data Transfer Format in Hs-Mode

Serial data transfer format in Hs-mode meets the Standard-mode I²C-bus specification. Hs-mode can only commence after the following conditions (all of which are in F/S-mode) :

- ► START condition (S)
- ► 8-bit master code (00001xxx)
- ► not-acknowledge bit ($\overline{A}$)

Figures 5 and Figure 6 show this in more detail. This master

code has two main functions:

- ► It allows arbitration and synchronization between competing masters at F/S-mode speeds, resulting in one winning master.
- ► It indicates the beginning of an Hs-mode transfer.

Hs-mode master codes are reserved 8-bit codes, which are not used for slave addressing or other purposes.

Furthermore, as each master has its own unique master code, up to eight Hs-mode masters can be present on the one I²C-bus system (although master code 0000 1000 should be reserved for test and diagnostic purposes). The master code for an Hs-mode master device is software programmable and is chosen by the System Designer.

Arbitration and clock synchronization only take place during the transmission of the master code and not-acknowledge bit ($\overline{A}$), after which one winning master remains active. The master code indicates to other devices that an Hs-mode transfer is to begin and the connected devices must meet the Hs-mode specification. As no device is allowed to acknowledge the master code, the master code is followed by a not-acknowledge ($\overline{A}$).

After the not-acknowledge bit ($\overline{A}$), and the SCLH line has been pulled-up to a HIGH level, the active master switches to Hs-mode and enables (at time t_H, see Figure 6) the current-source pull-up circuit for the SCLH signal. As other devices can delay the serial transfer before t_H by stretching the LOW period of the SCLH signal, the active master will enable its current-source pull-up circuit when all devices have released the SCLH line and the SCLH signal has reached a HIGH level, thus speeding up the last part of the rise time of the SCLH signal.

The active master then sends a repeated START condition (Sr) followed by a 7-bit slave address (or 10-bit slave address, see Section 14) with a R/W bit address, and receives an acknowledge bit ($\overline{A}$) from the selected slave.

After a repeated START condition and after each acknowledge bit ($\overline{A}$) or not-acknowledge bit ($\overline{A}$), the active master disables its current-source pull-up circuit. This enables other devices to delay the serial transfer by stretching the LOW period of the SCLH signal. The active master re-enables its current-source pull-up circuit again.

When all devices have released and the SCLH signal reaches a HIGH level, and so speeds up the last part of the SCLH signal's rise time.

Data transfer continues in Hs-mode after the next repeated START (Sr), and only switches back to F/S-mode after a STOP condition (P). To reduce the overhead of the master code, it's possible that a master links a number of Hs-mode transfers, separated by repeated START conditions (Sr).

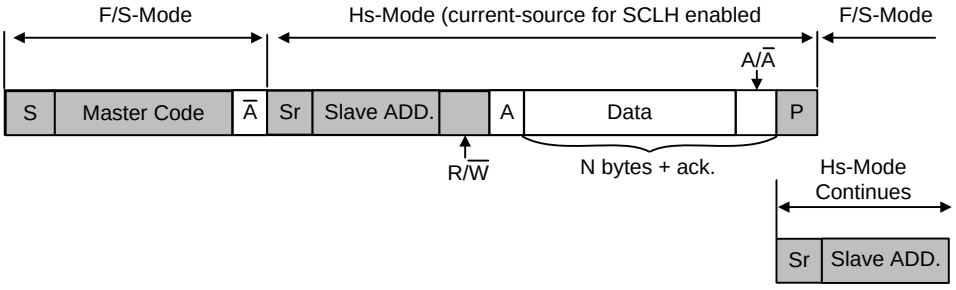

Figure 5. Data Transfer Format in Hs-mode

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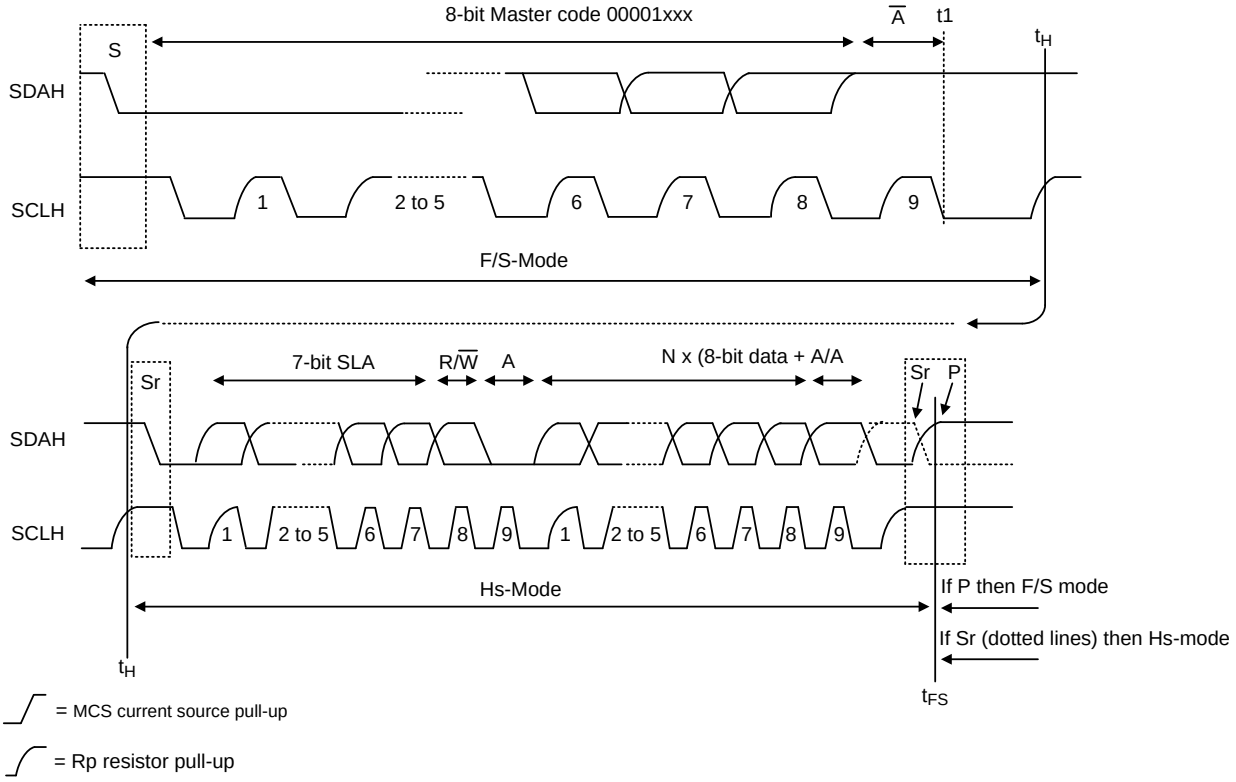

Figure 6. A Complete Hs-mode Transfer

Power On/Off Sequence

The RT5045A starts a power up sequence when AVDD > UVLO rising threshold voltage, and the device shuts down with AVDD < UVLO falling threshold voltage. The RT5045A applies sleep mode of PMIC to save power consumption with setting the SLEEP bit of SLEEP_REG to 1. If the device goes to sleep mode, power rails are set to LPM and the alive rails depend on sleep mode control register setting. The power rails will exit from LPM to normal mode and wake up with a sequence as the same as the power-up-sequence when SLEEP bit = 0. The relations of all power rails of RT5045A and sleep off / wake up sequence with different POR_OPTION on V_{IN} = 3.3V are shown as following Figure 7. The relations of all power rails of RT5045A and sleep off / wake up sequence with different POR_OPTION on V_{IN} = 5V are shown as following Figure 8.

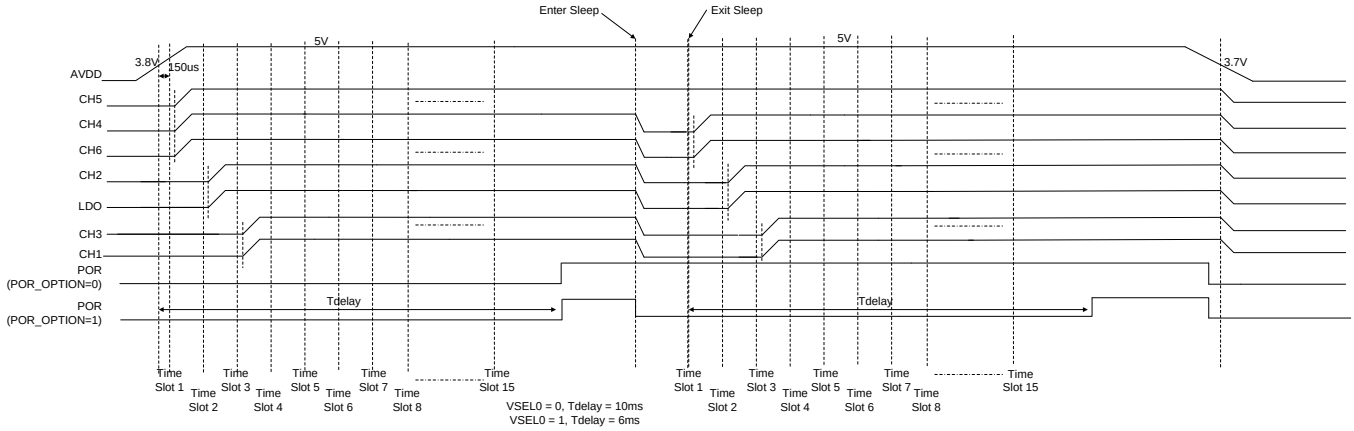

Figure 7. For example : Power On/Off Sequence and Sleep Off / Wake up Sequence with Different POR_OPTION on V_{IN} = 5V

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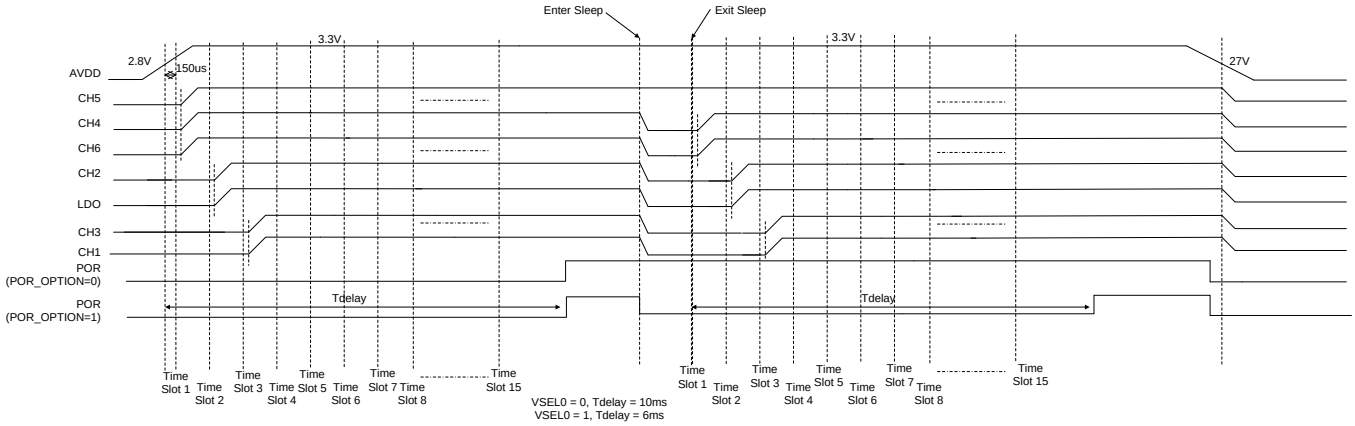

Figure 8. For example : Power On/Off Sequence and Sleep off / Wake up Sequence with Different POR_OPTION on V_{IN} = 3.3V

The relations quiescent current and LPM current of each channel table are shown as below.

RT5045	PMODE1	PMODE2	PMODE3	PMODE4	PMODE5	PMODE6	PMODE7	PMODE8
Buck1 2.5V	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF
Buck2 1.35V	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF
Buck3 1.8V	ON	ON	ON	OFF	OFF	OFF	OFF	OFF
Buck4 1.0V	ON	ON	ON	ON	OFF	OFF	OFF	OFF
Buck5 1.0V	ON	ON	ON	ON	ON	ON	ON	ON
Buck6 1.0V	ON	ON	ON	ON	ON	ON	OFF	OFF
LDO 2.5V	ON	ON	ON	ON	ON	OFF	OFF	OFF
LPM	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON
LPM ALL OFF Total (μA)	184	155	135	110	87	50		25

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Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WL-CSP-52B 3.19x3.59 (BSC) package, the thermal resistance, θ_{JA}, is 26°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (26°C/W) = 3.84W for WL-CSP-52B 3.19x3.59 (BSC)

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 9 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

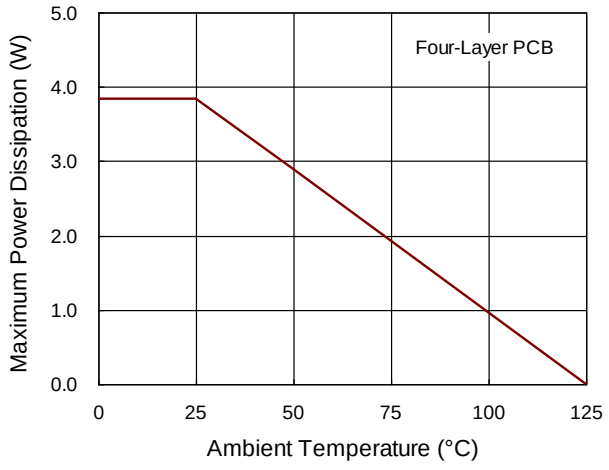

Figure 9. Derating Curve of Maximum Power Dissipation

Layout Considerations

Layout is very important in high frequency switching converter design. The PCB can radiate excessive noise and contribute to converter instability with improper layout.

Power components should be placed on the same side of board, with power traces routed on the same layer. If it is necessary to route a power trace to another layer, choose a trace in low di/dt paths and use multiple vias for interconnection. When vias are used to connect PCB layers in the high current loop, multiple vias should be used to minimize via impedance.

Certain points must be considered before starting a layout using the RT5045A.

- Make the traces of the main current paths as short and wide as possible.
- Place input decoupling capacitors as close as ossible as to PVIN1、PVIN2、PVIN3、PVIN4、PVIN5、PVIN6. This cap provide the instant current into this pin when the internal MOSFET switching. It is preferable to connect the decoupling capacitors directly to the pins without using vias.
- Place the inductors close LX1、LX2、LX3、LX4、LX5、LX6. To minimize the radiation noise, and the copper area should be minimized. However, the copper area is provided a heat sink to the internal MOSFET. Don't make the area of the node small by using narrow traces, using wide and short traces instead.
- For feedback signals FB1、FB2、FB3、FB4、FB5、FB6, the sensing point which detects the output voltage must be connected after output capacitor and keep the trace far away from the switching node or inductor. Place the feedback network as close to the chip as possible.
- Place the bypass capacitor close to AVDD.
- Place the filter capacitor close to LDO、LX1、LX2、LX3、LX4、LX5、LX6 to minimize trace inductance.
- The GND pin and Exposed Pad should be connected to a strong ground plane for heat sinking and noise protection.

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- An example of PCB layout guide is shown in Figure 7.for reference.

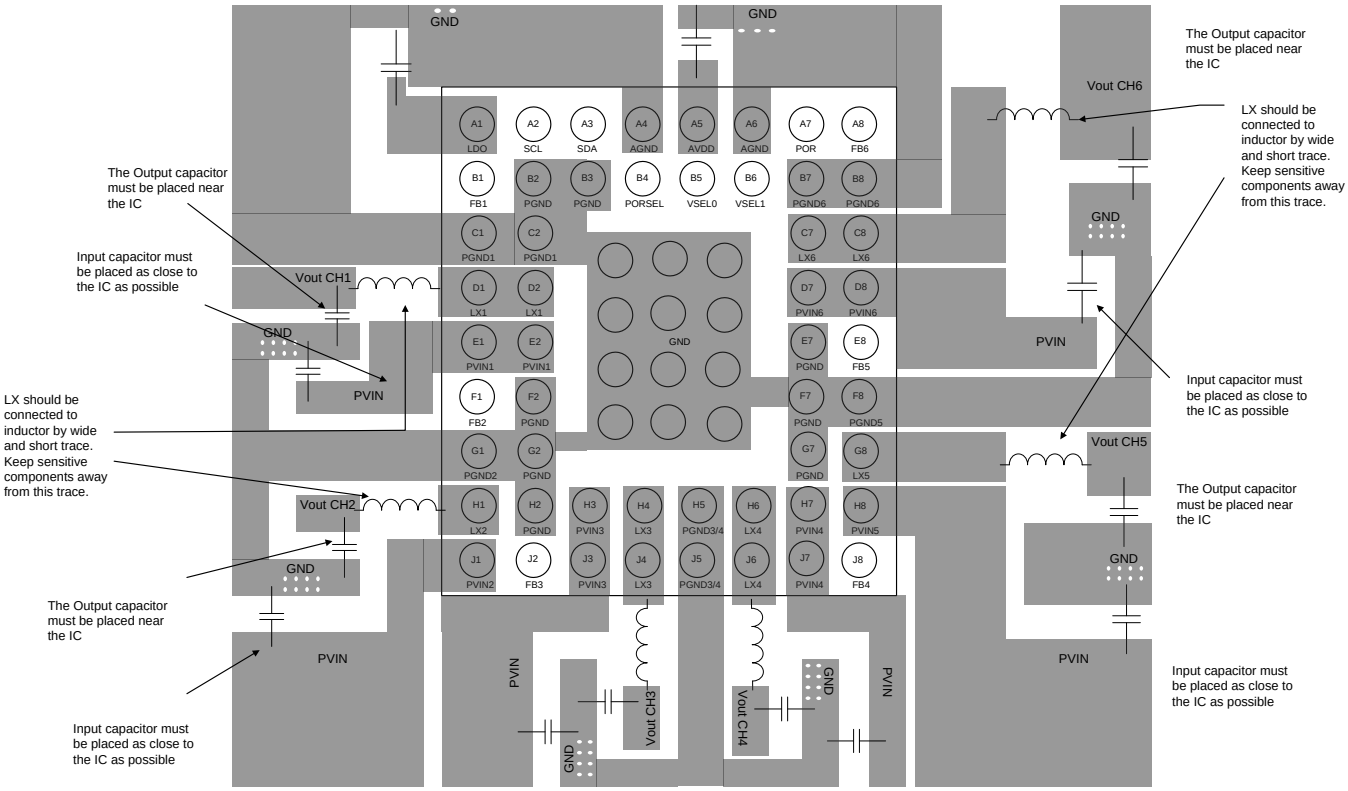

Figure 10. PCB Layout Guide

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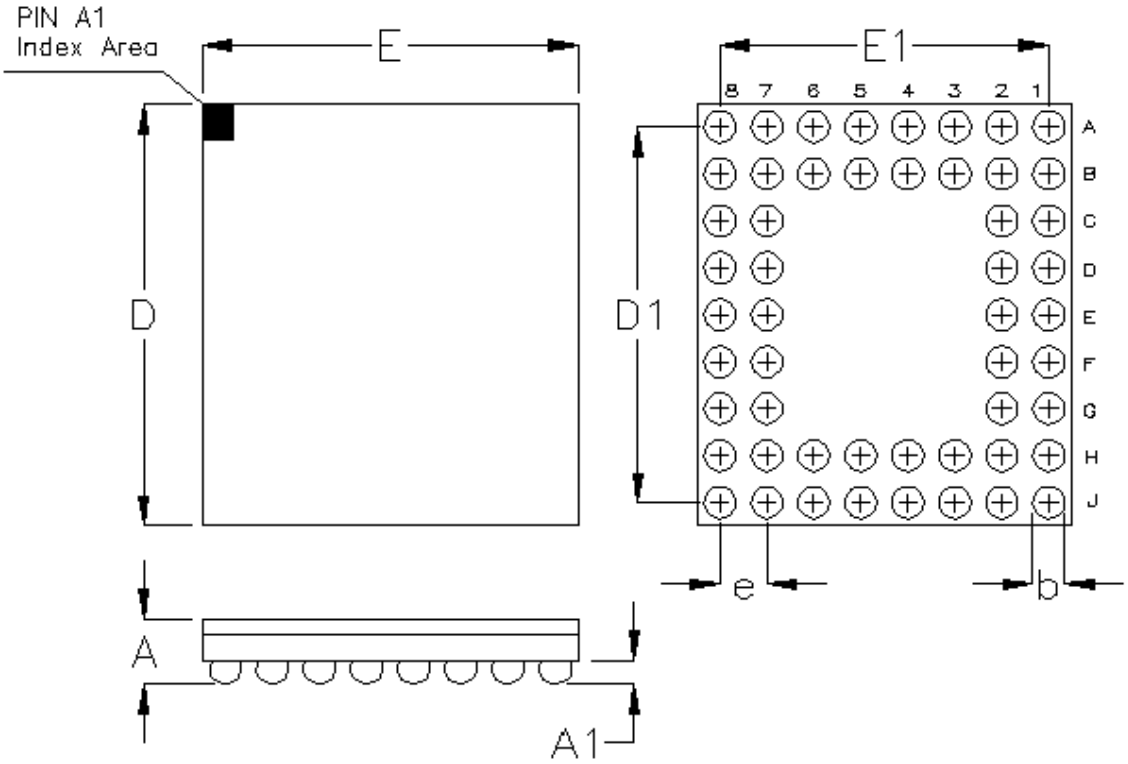
Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.500	0.600	0.020	0.024
A1	0.170	0.230	0.007	0.009
b	0.240	0.300	0.009	0.012
D	3.540	3.640	0.139	0.143
D1	3.200		0.126	
E	3.140	3.240	0.124	0.128
E1	2.800		0.110	
e	0.400		0.016	

52B WL-CSP 3.19x3.59 Package (BSC)

Richtek Technology Corporation
14F, No. 8, Tai Yuen 1st Street, Chupei City
Hsinchu, Taiwan, R.O.C.
Tel: (8863)5526789

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