

## High Efficiency Boost Converter

### General Description

The RT4813 allows systems to take advantage of new battery chemistries that can supply significant energy when the battery voltage is lower than the required voltage for system power ICs. By combining built-in power transistors, synchronous rectification, and low supply current; this IC provides a compact solution for systems using advanced Li-Ion battery chemistries.

The RT4813 is a boost regulator designed to provide a minimum output voltage from a single-cell Li-Ion battery, even when the battery voltage is below system minimum. In boost mode, output voltage regulation is guaranteed to a maximum load current of 3.1A. Quiescent current in Shutdown Mode is less than 1 $\mu$ A, which maximizes battery life.

### Ordering Information

RT4813	□□
	Package Type
	QUF : UQFN-9L 2x2 (FC) (U-Type)
	Lead Plating System
	G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- ▶ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▶ Suitable for use in SnPb or Pb-free soldering processes.

### Features

- CMCOT Topology and Small Output Ripple when VIN Close VOUT Voltage
- Operates from a Single Li-ion Cell : 1.8V to 5.5V
- Adjustable Output Voltage : 1.8V to 5.5V
- PSM Operation
- Up to 96% Efficiency
- Input Over Current Limit
- Input / Output Over Voltage Protection
- Programmable Average Output Current Limit Range : 3100mA to 550mA
- Internal Compensation
- Output Discharge
- Output Short Protection
- True Load Disconnect

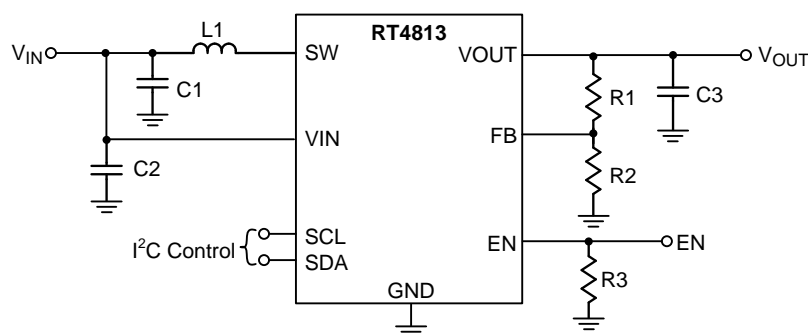
### Applications

- Single-Cell Li-Ion, LiFePO4 Smart-Phones
- Portable Equipment

### Marking Information

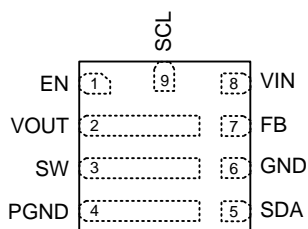
3VW	3V : Product Code
●	W : Date Code

## Simplified Application Circuit



## Pin Configuration

(TOP VIEW)

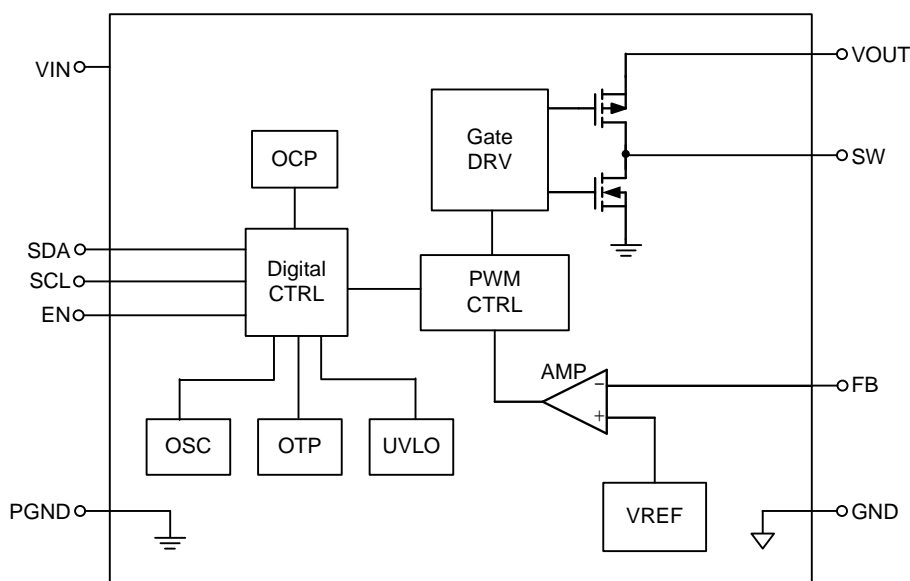


UQFN-9L 2x2 (FC)

## Functional Pin Description

Pin No.	Pin Name	Pin Function
1	EN	Enable input (1 enabled, 0 disabled), must not be left floating.
2	VOUT	Boost converter output.
3	SW	Switching node.
4	PGND	Power ground.
5	SDA	I <sup>2</sup> C interface data input.
6	GND	Analog ground.
7	FB	Voltage feedback.
8	VIN	Power input. Input capacitor CIN must be placed as close to IC as possible.
9	SCL	I <sup>2</sup> C interface clock input.

## Functional Block Diagram



## Operation

The RT4813 combined built-in power transistors, synchronous rectification, and low supply current, it provides a compact solution for system using advanced Li-Ion battery chemistries.

In boost mode, output voltage regulation is guaranteed to a maximum load current of 3.1A. Quiescent current in Shutdown mode is less than 1 $\mu$ A, which maximizes battery life.

Mode		Depiction	Condition
LIN	LIN 1	Linear startup 1	$V_{OUT} < V_{IN} - 300mV$
	LIN 2	Linear startup 2	$V_{OUT} < V_{IN} - 300mV$
Soft-Start		Boost soft-start	$0.95 \times V_{OUT\_Target} > V_{OUT} \geq V_{IN} - 300mV$
Boost		Boost mode	$V_{OUT} \geq 0.95 \times V_{OUT\_Target}$

### LIN State

When  $V_{IN}$  is rising, it enters the LIN State. There are two parts for the LIN state. It provides maximum current for 1A to charge the  $C_{OUT}$  in LIN1, and the other one is for 2A in LIN2. By the way, the EN is pulled high and  $V_{IN} > UVLO$ .

As the figure shown, if the timeout is over the specification, it will enter the Fault mode.

### Startup and Shutdown State

When  $V_{IN}$  is rising and through the LIN state, it will enter the Startup state. If EN is pulled low, any function is turned-off in shutdown mode.

### Soft-Start State

It starts to switch in Soft-start state. After the LIN state, output voltage is rising with the internal reference voltage.

### Fault State

As the Figure 1 shown, it will enter to the Fault state as below,

- The timeout of LIN2 is over the 1560 $\mu$ s.

It will be the high impedance between the input and output when the fault is triggered. A restart will be start after 20ms.

### OCP

The converter senses the current signal when the high-side P-MOSFET turns on. As a result, the OCP is cycle by-cycle current limitation. If the OCP occurs, the converter holds off the next on pulse until inductor current drops below the OCP limit.

### OTP

The converter has an over-temperature protection. When the junction temperature is higher than the thermal shutdown rising threshold, the system will be latched and the output voltage will no longer be regulated until the junction temperature drops under the falling threshold.

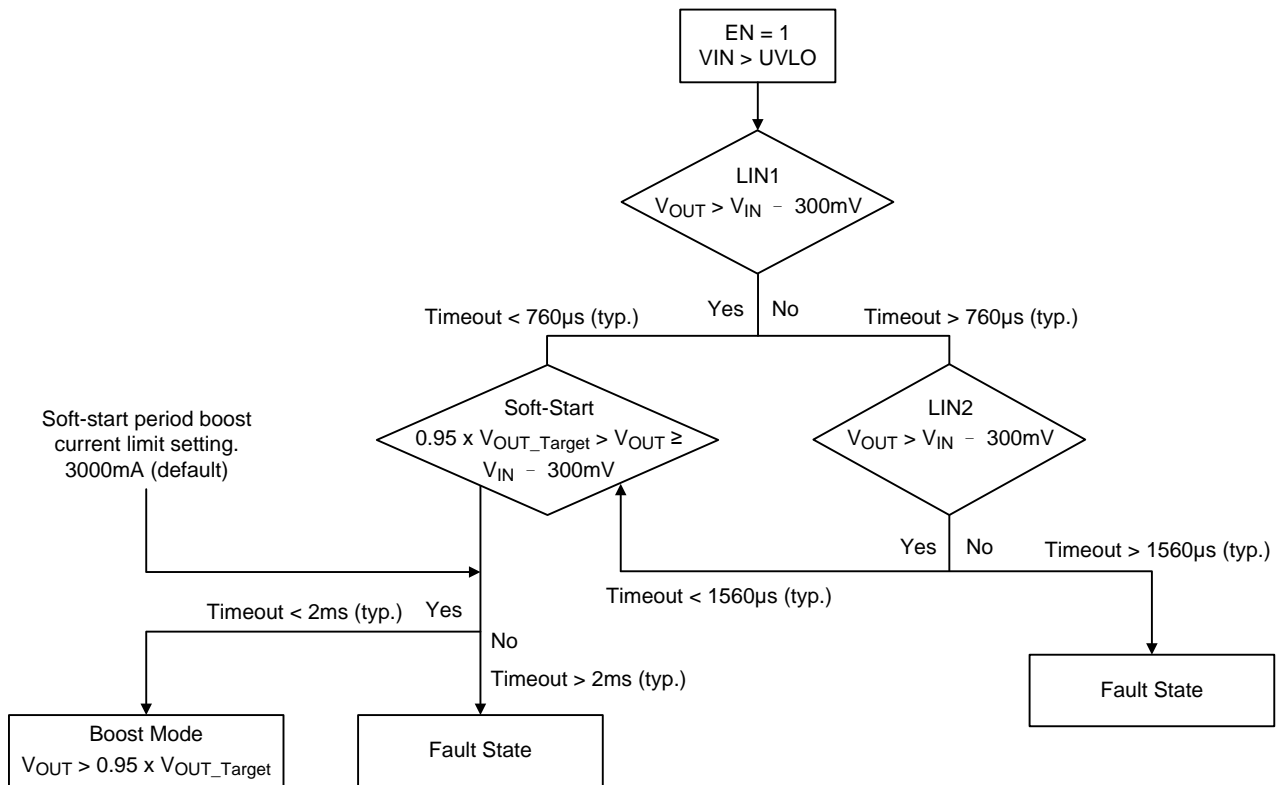


Figure 1. RT4813 State Chart

## Absolute Maximum Ratings (Note 1)

- VIN, FB, EN, SDA, SCL to GND----- -0.2V to 6V
- SW to GND ----- -0.2V to 6V  
     < 20ns----- -2V to 9.4V
- VOUT to GND----- 6V
- Power Dissipation,  $P_D$  @  $T_A = 25^\circ\text{C}$   
     UQFN-9L 2x2 (FC)----- 0.89W
- Package Thermal Resistance (Note 2)  
     UQFN-9L 2x2 (FC),  $\theta_{JA}$ ----- 111.5°C/W  
     UQFN-9L 2x2 (FC),  $\theta_{JC}$ ----- 19.6 °C/W
- Lead Temperature (Soldering, 10 sec.)----- 260°C
- Junction Temperature----- 150°C
- Storage Temperature Range----- -65°C to 150°C
- ESD Susceptibility (Note 3)  
     HBM (Human Body Model) ----- 2kV

## Recommended Operating Conditions (Note 4)

- Input Voltage Range----- 1.8V to 5.5V
- Output Voltage Range ----- 1.8V to 5.5V
- Ambient Temperature Range----- -40°C to 85°C
- Junction Temperature Range ----- -40°C to 125°C

## Electrical Characteristics

(VIN = 3.6V, TA = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Under Voltage Lockout Rising Threshold	VUVLOR		1.6	1.7	1.8	V
Under Voltage Lockout Falling Threshold	VUVLOF		1.5	1.6	1.7	V
FB Voltage	VFB	CCM	0.495	0.5	0.505	V
VOUT Voltage (I <sup>2</sup> C)	VOUT	CCM	-1	0	1	%
Shutdown Current	ISHDN	EN = 0V	--	0.1	2	μA
Quiescent Current		Close loop, no load	--	120	--	μA
Pre-Charge Current	IPre		--	1	--	A
Switching Frequency	fsw	VOUT – VIN > 1V, CCM	--	0.5	--	MHz
Valley Current Limit	Ioc		--	6	--	A
High Side Switch RON		VIN = 5V	--	43	55	mΩ
Low Side Switch RON		VIN = 5V	--	26	35	mΩ
FB Pin Input Leakage	IFB		-1	--	1	μA
Leakage of SW	ISW		--	--	5	μA

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Line Regulation		$\Delta V_{OUT, LINE}$	CCM, $V_{IN} = 2.7V$ to $4.5V$ , $V_{OUT} = 5V$ , $I_{OUT} = 500mA$	--	0.5	--	%
Load Regulation		$\Delta V_{OUT, LOAD}$	CCM, $I_{OUT} < 3.1A$ , $V_{IN} = 3.6V$ , $V_{OUT} = 5V$	--	0.5	--	%
Output Over Voltage Protection		$V_{OVP}$		--	6	--	V
Average Output Current Limit		$I_{LM}$	$V_{IN} = 3.6V$ (Default)	--	3.4	--	A
EN Input Voltage	Low-Level	$V_{IL}$		--	--	0.4	V
	High-Level	$V_{IH}$		1.2	--	--	V
EN Sink Current				--	0.1	1	$\mu A$
Thermal Shutdown		$T_{SD}$		--	160	--	$^{\circ}C$
Thermal Shutdown Hysteresis		$\Delta T_{SD}$		--	30	--	$^{\circ}C$
<b>I<sup>2</sup>C Characteristics</b>							
SCL, SDA High-Level Input Threshold Voltage		$V_{IH\_I2C}$	Fast-mode	2.31	--	3.8	V
SCL, SDA Low-Level Input Threshold Voltage		$V_{IL\_I2C}$	Fast-mode	--	--	0.4	V
SDA Digital Output Low		$V_{OL\_I2C}$	Fast-mode	--	--	0.4	V
SCL Clock Frequency		$f_{CLK}$	Fast-mode	--	--	400	kHz
Bus Free Time between Stop and Start Condition		$t_{BUF}$	Fast-mode	1.3	--	--	$\mu s$
(Repeated) Start Hold Time		$t_{HD;STA}$	Fast-mode	0.6	--	--	$\mu s$
(Repeated) Start Setup Time		$t_{SU;STA}$	Fast-mode	0.6	--	--	$\mu s$
STOP Condition Setup Time		$t_{SU;STO}$	Fast-mode	0.6	--	--	$\mu s$
SDA Data Hold Time		$t_{HD;DAT}$	Fast-mode	0.1	--	--	ns
SDA Valid Acknowledge Time		$t_{VD;ACK}$	Fast-mode	--	--	0.9	$\mu s$
SDA Setup Time		$t_{SU;DAT}$	Fast-mode	100	--	--	ns
SCL Clock Low Time		$t_{LOW}$	Fast-mode	1.3	--	--	$\mu s$
SCL Clock High Time		$t_{HIGH}$	Fast-mode	0.6	--	--	$\mu s$

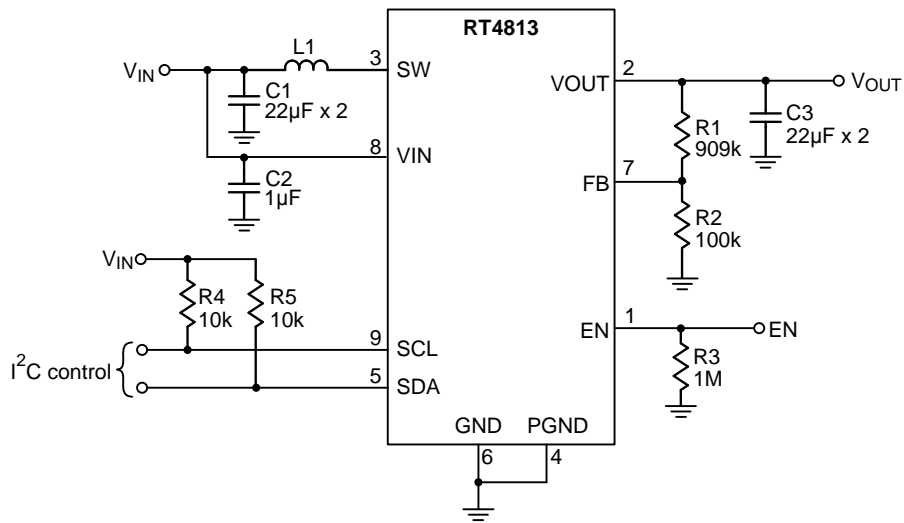
**Note 1.** Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

**Note 2.**  $\theta_{JA}$  is measured at  $T_A = 25^{\circ}C$  on a high effective thermal conductivity four-layer test board per JEDEC 51-7.  $\theta_{JC}$  is measured at the exposed pad of the package.

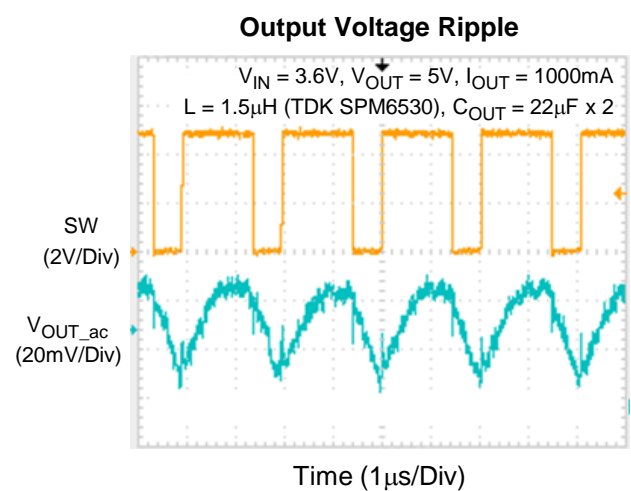
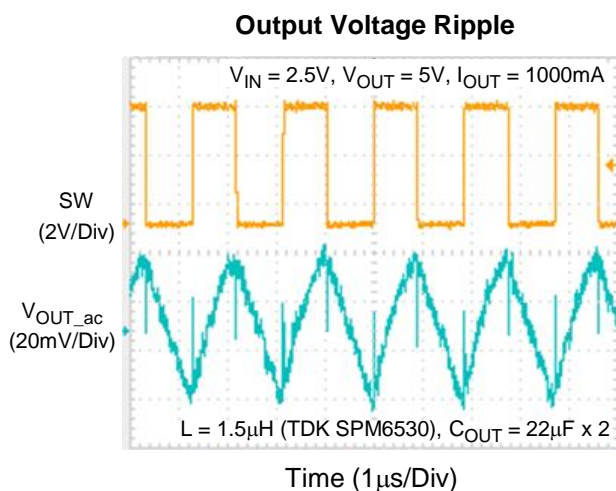
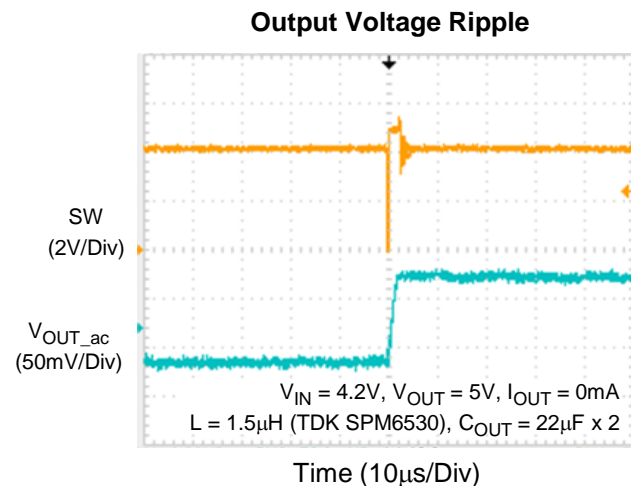
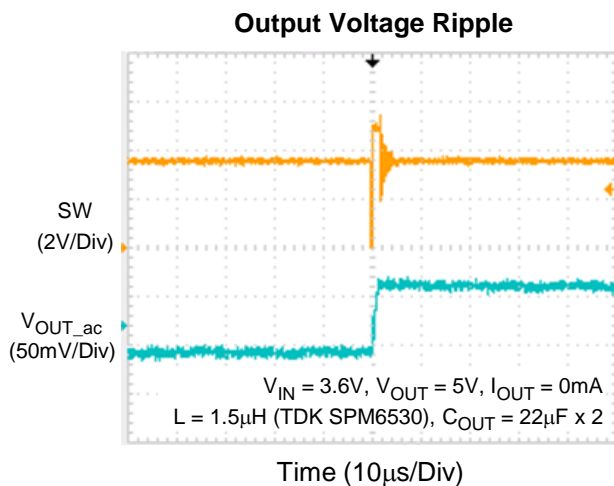
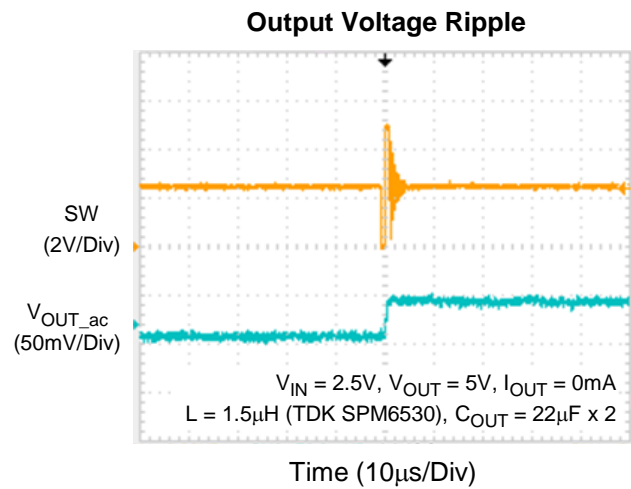
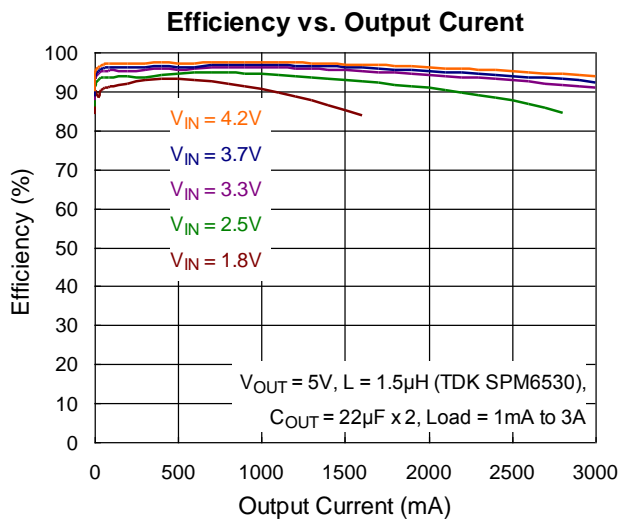
**Note 3.** Devices are ESD sensitive. Handling precaution is recommended.

**Note 4.** The device is not guaranteed to function outside its operating conditions.

## Typical Application Circuit

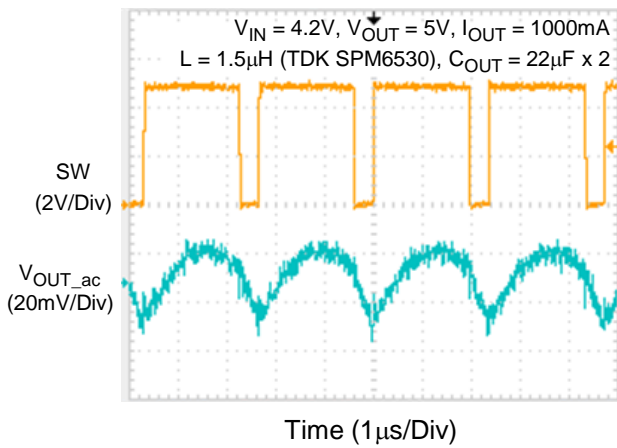


## Typical Operating Characteristics

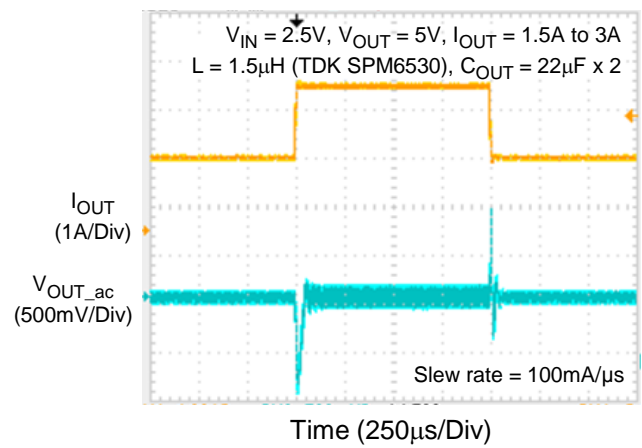




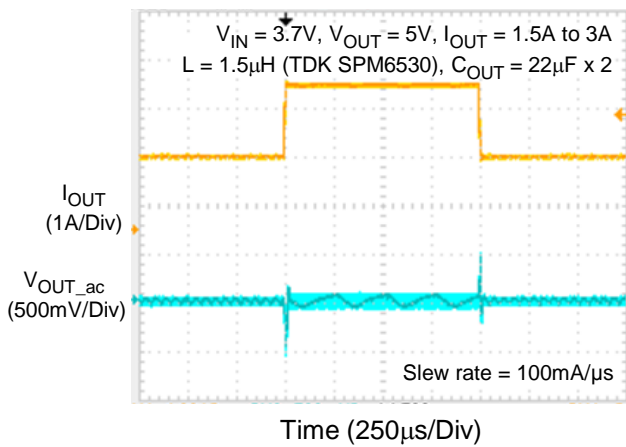
Output Voltage Ripple



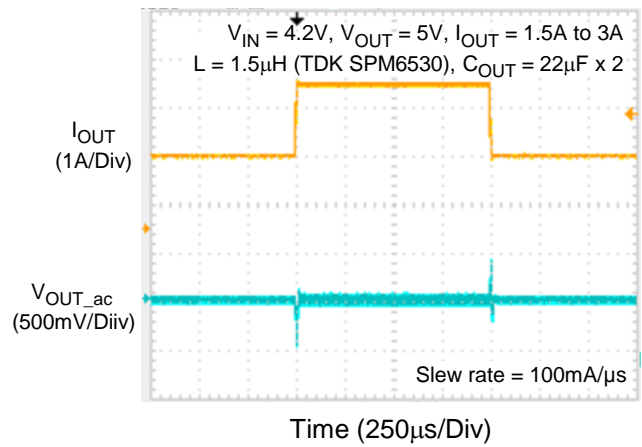
Load Transient Response



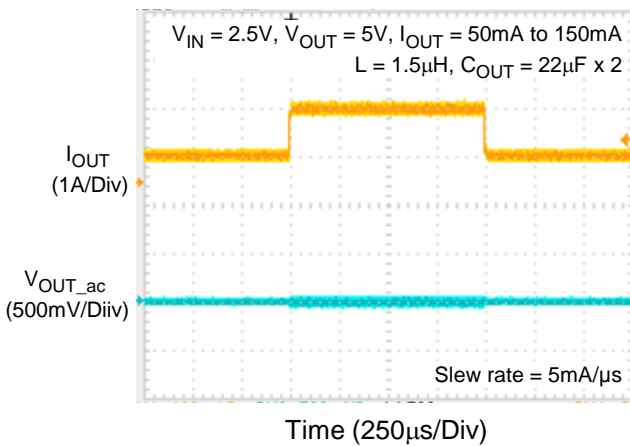
Load Transient Response



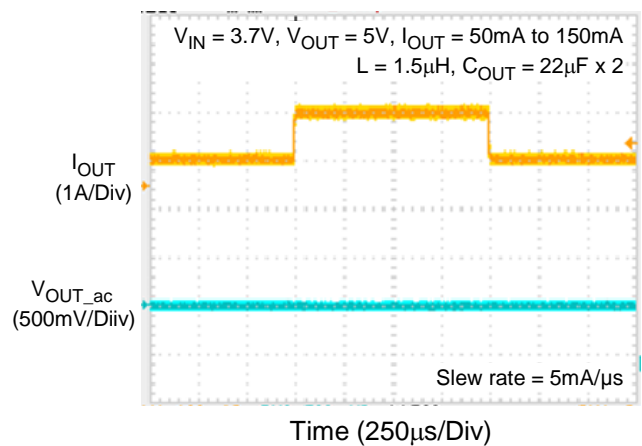
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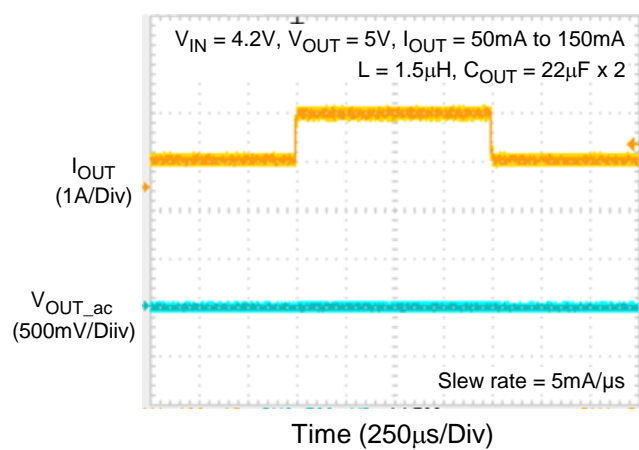
Load Transient Response



Load Transient Response



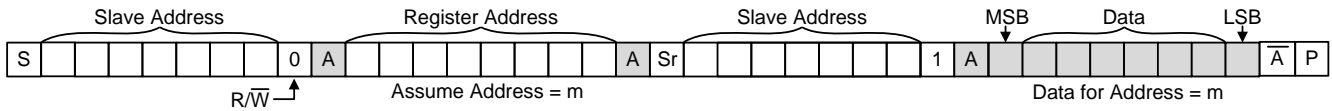
## Load Transient Response



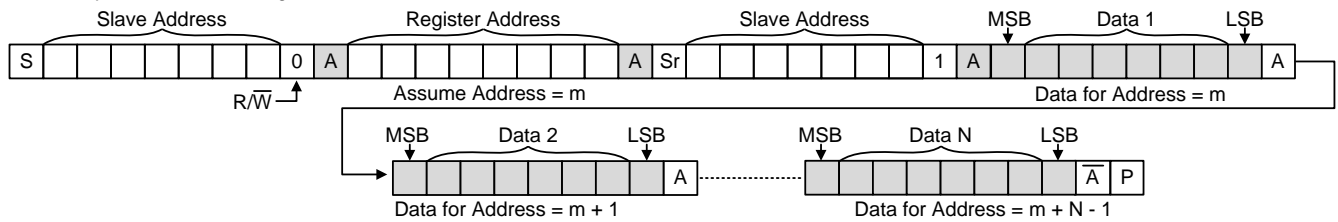
## I<sup>2</sup>C Interface

RT4813 I<sup>2</sup>C slave address = 0111001 (7 bits). I<sup>2</sup>C interface supports fast mode (bit rate up to 400kb/s). The write or read bit stream (N ≥ 1) is shown below :

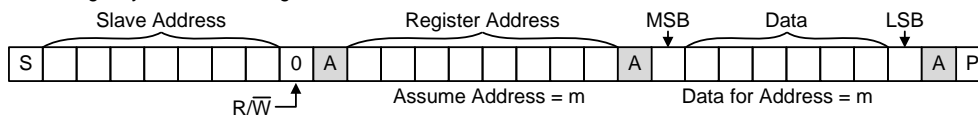
Read single byte of data from Register



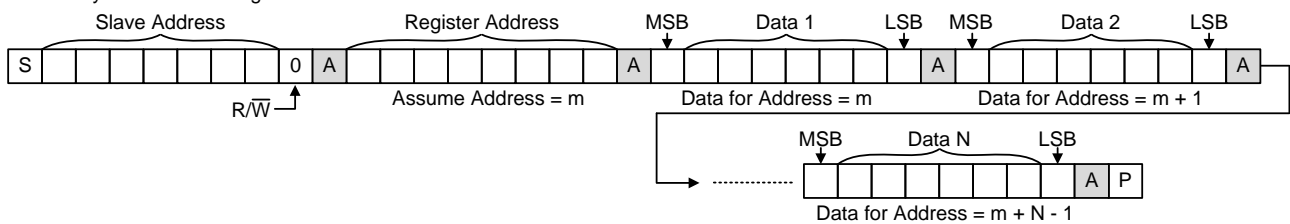
Read N bytes of data from Registers



Write single byte of data to Register

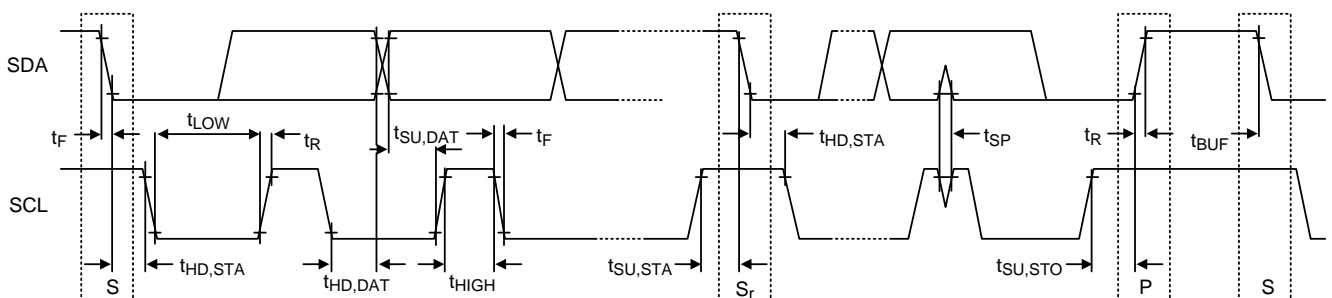


Write N bytes of data to Registers



□ Driven by Master, ■ Driven by Slave, [P] Stop, [S] Start, [Sr] Repeat Start

## I<sup>2</sup>C Waveform Information



I<sup>2</sup>C Register

Function	Register Address		b[7] (MSB)	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0] (LSB)
Config	0X01	Meaning	Reversed	ILIM_OFF	IPCHG		DRV_SEL<2:0>			SSFM
		Default	0	0	0	1	1	1	1	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ILIM_OFF			Boost valley current limit setting 0 : Boost current limit enable (default) 1 : Boost current limit disable							
IPCHG			Pre-charge current setting. 00 : 0.5A 01 : 1A (default) 10 : 1.5A 11 : 2A							
DRV_SEL<2:0>			LG driver driving capability 000 : Slowest : : 111 : Fastest (default)							
SSFM			Spread spectrum setting. 0 : Spread spectrum disable (default) 1 : Spread spectrum enable							

Function	Register Address		b[7] (MSB)	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0] (LSB)
Charger Control 3	0X03	Meaning	ILIM_SS<7:4>				ILIM_AVG<3:0>			
		Default	0	0	0	0	0	0	0	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ILIM_SS<7:4>			Soft-start period boost current limit setting. The default current and soft-start min boost current limit setting is 3000mA.							
			Code		Current		Code		Current	
			1001		3000mA (default)		1101		5000mA	
			1010		3500mA		1110		5500mA	
			1011		4000mA		1111		6000mA	
			1100		4500mA					
ILIM_AVG<3:0>			Average Output Current limit setting. The default current is 3100mA.							
			Code	Current	Code	Current	Code	Current	Code	Current
			0000	3100mA (Default)	0100	2420mA	1000	1740mA	1100	1060mA
			0001	2930mA	0101	2250mA	1001	1570mA	1101	890mA
			0010	2760mA	0110	2080mA	1010	1400mA	1110	720mA
			0011	2590mA	0111	1910mA	1011	1230mA	1111	550mA

Function	Register Address		b[7] (MSB)	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0] (LSB)
OPTION	0X04	Meaning	Reversed	Reversed	Reversed	Reversed	FSW		EN_IavgCL	EN_Discharge
		Default	0	0	0	0	1	1	1	1
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
FSW			Boost frequency setting. 00 : 2MHz 01 : Do not allowed 10 : 1MHz 11 : 500kHz (default)							
EN_IavgCL			Enable average output current limit 0 : Disable 1 : Enable (default)							
EN_Discharge			Enable discharge 0 : Disable 1 : Enable (default)							

## Application Information

### Enable

The device can be enabled or disabled by the EN pin. When the EN pin is higher than the threshold of logic-high, the device starts operating with soft-start. Once the EN pin is set at low, the device will be shut down. In shutdown mode, the converter stops switching, internal control circuitry is turned off, and the load is disconnected from the input. This also means that the output voltage can drop below the input voltage during shutdown.

### Soft-Start State

After the successful completion of the LIN state ( $V_{OUT} \geq V_{IN} - 300\text{mV}$ ), the regulator begins switching with boost valley-current limited value 3000mA.

During Soft-Start state,  $V_{OUT}$  is ramped up by Boost internal loop. If  $V_{OUT}$  fails to reach target value during the Soft-Start period for more than 2ms, a fault condition is declared.

### Output Voltage Setting

The output voltage is adjustable by an external resistive divider. The resistive divider must be connected between  $V_{OUT}$ , FB and GND. When the output voltage is regulated properly, the typical value of the voltage at the FB pin is 500mV. Output voltage can be calculated by equation as below :

$$R1 = R2 \times \left( \frac{V_{OUT}}{V_{FB}} - 1 \right)$$

### Power Save Mode

PSM is the way to improve efficiency at light load.

When the output voltage is lower than a set threshold voltage, the converter will operate in PSM.

It raises the output voltage with several pulses until the loop exits PSM.

### Under-Voltage Lockout

The under-voltage lockout circuit prevents the device from operating incorrectly at low input voltages. It prevents the converter from turning on the power switches under undefined conditions and prevents the battery from deep discharge.  $V_{IN}$  voltage must be greater than 1.65V to enable the converter. During operation, if  $V_{IN}$  voltage drops below 1.55V, the converter is disabled until the supply exceeds the UVLO rising threshold. The RT4813 automatically restarts if the input voltage recovers to the input voltage UVLO high level.

### Thermal Shutdown

The device has a built-in temperature sensor which monitors the internal junction temperature. If the temperature exceeds the threshold, the device stops operating. As soon as the IC temperature has decreased below the threshold with a hysteresis, it starts operating again. The built-in hysteresis is designed to avoid unstable operation at IC temperatures near the over temperature threshold.

### Inductor Selection

The recommended nominal inductance value is 1.5μH

It is recommended to use inductor with dc saturation current  $\geq 6000\text{mA}$

Table 1. List of Inductors

Manufacturer	Series	Dimensions (in mm)	Saturation Current (mA)
TDK	SPM6530T	7.1 x 6.5 x 3.0	11500
Taiyo Yuden	NRS5040T	5.15 x 5.15 x 4.2	6400

### Input Capacitor Selection

At least two capacitor and capacitance is 22μF with rating voltage is 16V for DC bias input capacitor is recommended to improve transient behavior of the regulator and EMI behavior of the total power supply circuit for SW. And at least a 1μF ceramic capacitor placed as close as possible to the VIN and GND pins of the IC is recommended.

### Output Capacitor Selection

At least 22μF x 2 capacitors is recommended to improve V<sub>OUT</sub> ripple.

Output voltage ripple is inversely proportional to C<sub>OUT</sub>.

Output capacitor is selected according to output ripple which is calculated as :

$$V_{\text{RIPPLE(P-P)}} = t_{\text{ON}} \times \frac{I_{\text{LOAD}}}{C_{\text{OUT}}}$$

and

$$t_{\text{ON}} = t_{\text{SW}} \times D = t_{\text{SW}} \times \left(1 - \frac{V_{\text{IN}}}{V_{\text{OUT}}}\right)$$

therefore :

$$C_{\text{OUT}} = t_{\text{SW}} \times \left(1 - \frac{V_{\text{IN}}}{V_{\text{OUT}}}\right) \times \frac{I_{\text{LOAD}}}{V_{\text{RIPPLE(P-P)}}$$

and

$$t_{\text{SW}} = \frac{1}{f_{\text{SW}}}$$

The maximum V<sub>RIPPLE</sub> occurs at minimum input voltage and maximum output load.

### Output Discharge Function

With the EN pin set to low, the V<sub>OUT</sub> pin is internally connected to GND for 10ms by an internal discharge N-MOSFET switch. After the 10ms, IC will be true-shut down.

This feature prevents residual charge voltages on capacitor connected to V<sub>OUT</sub> pins, which may impact proper power up of the system.

### Valley Current Limit

The RT4813 employs a valley-current limit detection scheme to sense inductor current during the off-time. When the loading current is increased such that the loading is above the valley current limit threshold, the off-time is increased until the current is decreased to valley-current threshold. Next on-time begins after current is decreased to valley-current threshold. On-time is decided by (V<sub>OUT</sub> – V<sub>IN</sub>) / V<sub>OUT</sub> ratio. The output voltage decreases when further loading current increase. The current limit function is implemented by the scheme, refer to Figure 2.

### Average Output Current Limit

The RT4813 features the average output current limit to protect the output terminal. When the load current is over the limit, output current will be clamped.

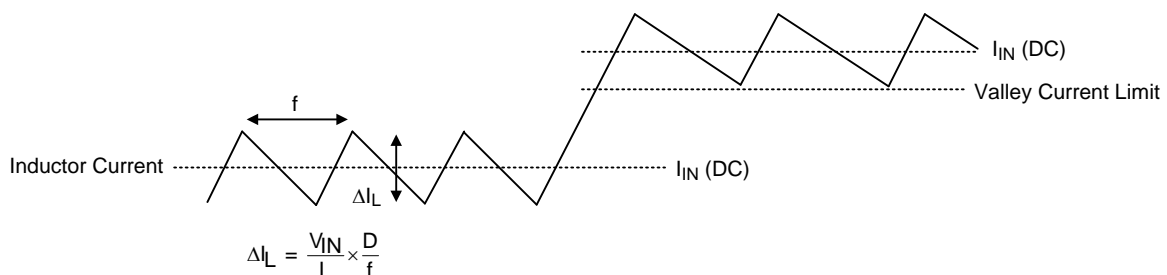


Figure 2. Inductor Currents In Current Limit Operation

### Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where  $T_{J(MAX)}$  is the maximum junction temperature,  $T_A$  is the ambient temperature, and  $\theta_{JA}$  is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance,  $\theta_{JA}$ , is layout dependent. For UQFN-9L 2x2 (FC) package, the thermal resistance,  $\theta_{JA}$ , is 111.5°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at  $T_A = 25^\circ\text{C}$  can be calculated by the following formula :

$$P_{D(MAX)} = (125^\circ\text{C} - 25^\circ\text{C}) / (111.5^\circ\text{C/W}) = 0.89\text{W for UQFN-9L 2x2 (FC) package}$$

The maximum power dissipation depends on the operating ambient temperature for fixed  $T_{J(MAX)}$  and thermal resistance,  $\theta_{JA}$ . The derating curve in Figure 3 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

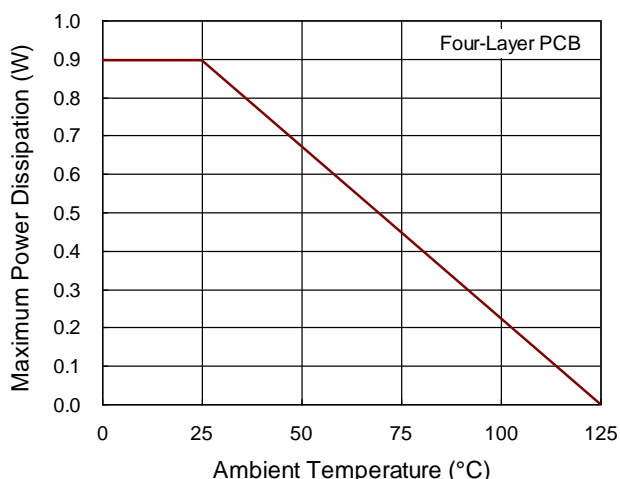


Figure 3. Derating Curve of Maximum Power Dissipation

### Layout Consideration

The PCB layout is an important step to maintain the high performance of the RT4813.

Both the high current and the fast switching nodes demand full attention to the PCB layout to save the robustness of the RT4813 through the PCB layout. Improper layout might show the symptoms of poor line or load regulation, ground and output voltage shifts, stability issues, unsatisfying EMI behavior or worsened efficiency. For the best performance of the RT4813, the following PCB layout guidelines must be strictly followed.

- ▶ Input/Output capacitors must be placed as close as possible to the Input/Output pins.
- ▶ SW should be connected to Inductor by wide and short trace, keep sensitive components away from this trace.
- ▶ The feedback divider should be placed as close as possible to the FB pin.

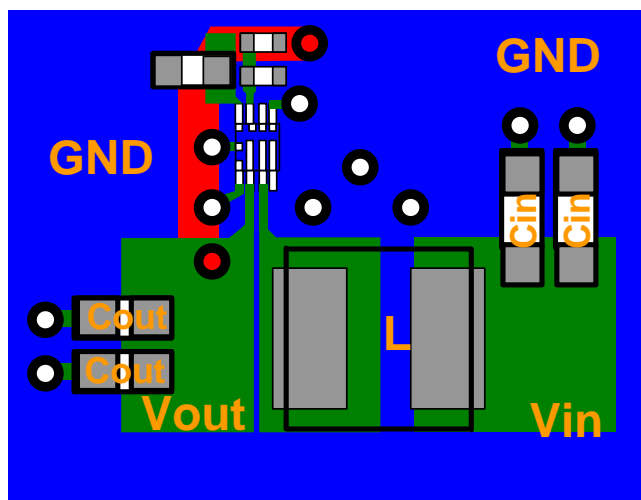
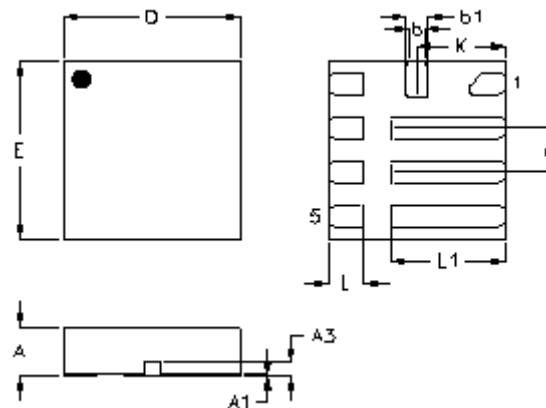


Figure 4. PCB Layout Guide



## Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.500	0.600	0.020	0.024
A1	0.000	0.050	0.000	0.002
A3	0.100	0.200	0.004	0.008
b	0.130	0.230	0.005	0.009
b1	0.200	0.300	0.008	0.012
D	1.950	2.050	0.077	0.081
E	1.950	2.050	0.077	0.081
e	0.500		0.020	
K	1.000		0.039	
L	0.350	0.450	0.014	0.018
L1	1.250	1.350	0.049	0.053

**U-Type 9L QFN 2x2 (FC) Package**

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