# Triple Channel PWM Controller with I²C Interface Control for IMVP9.2 CPU Core Power Supply

## General Description

The RT3634CJ is an IMVP9.2 compliant CPU power controller which includes three voltage rails: a 4-phase synchronous buck controller for VCCCORE VR, a 3-phase synchronous buck controller for VCCGT VR, and a 1-phase synchronous buck controller for VCCSA VR. The output of each rail can be configured to support the desired phase assignments up to a maximum phase count of 4 phases for VCCCORE, 3 phases for VCCGT and 1 phase for VCCSA. For example, the RT3634CJ supports output operations of 4+3+1, 4+2+1, 3+2+1, etc. The RT3634CJ adopts the Smart Phase Management (SPM) feature, to achieve maximum efficiency in all load range. Thresholds for automatic phase add/drop are user-programmable using I²C protocol interface. The RT3634CJ adopts G-NAVP™ (Green Native AVP), which is Richtek's proprietary topology derived from finite DC gain of EA amplifier with current mode control, making it easy to set the droop to meet all Intel CPU requirements of AVP (Adaptive Voltage Positioning). Based on the G-NAVP™ topology, the RT3634CJ features a new generation of quick response mechanism (Adaptive Quick Response, AQR) to optimize AVP performance during load transient and reduce output capacitors. The RT3634CJ supports mode transition function with various operating states. A serial VID (SVID) interface is built in to communicate with Intel IMVP9.2 compliant CPU. The RT3634CJ offers built-in non-volatile memory (NVM) for platform setting functions, such as ICCMAX, switching frequency or AQR trigger level. The RT3634CJ provides VR ready output signals. It also features complete fault protection functions including overvoltage (OV), overcurrent (OC), undervoltage (UV) and undervoltage lockout (UVLO). The RT3634CJ is available in the WQFN-60L 7x7 footprint package. The recommended junction temperature is –40°C to 125°C.

## Features

- **Intel IMVP9.2 Compliant**
- **4/3/2/1/0 Phase (VCCCORE VR) + 3/2/1/0 Phase (VCCGT VR) + 1/0 Phase (VCCSA VR) PWM Controller**
- **Support Multi-Source Dr.MOS**
- **Support Phase Doubler RT9637 for CORE Rail Up to 8-Phase Operation**
- **Support Application of SPS with Current Sensing by Either Current Type or Voltage Type**
- **Easy-Set G-NAVP™ (Green Native Adaptive Voltage Positioning) Control**
- **0.5% DAC Accuracy**
- **Differential Remote Voltage Sensing**
- **Internal Non-Volatile Memory (NVM) to Store Custom Configuration**
- **Accurate Current Balance**
- **Diode Emulation Mode at Light Load Condition**
- **Fast Transient Response-Adaptive Quick Response (AQR)**
- **VR Ready Indicator**
- **Output Current Monitor**
- **Protection Flag for OVP, OCP, UVP**
- **Support Fast V-Mode (FVM)**
- **Switching Frequency Setting**
- **Slew Rate Setting**
- **DVID Enhancement**
- **Audio Noise Suppress Function**
- **Zero Load-Line**
- **Smart Phase Management (SPM) Adjustment**
- **Standard I²C Protocol Interface**
  - **Thermal Balance Adjustment**

## Applications

- IMVP9.2 Intel Core Supply
- Notebook/Desktop Computer
- AVP Step-Down Converter

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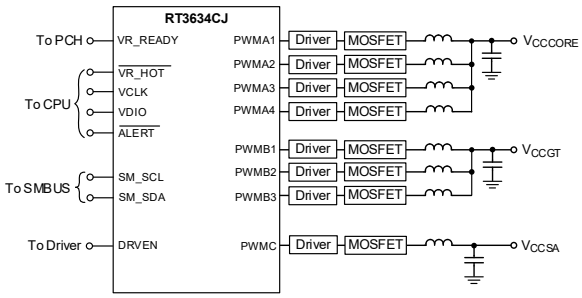
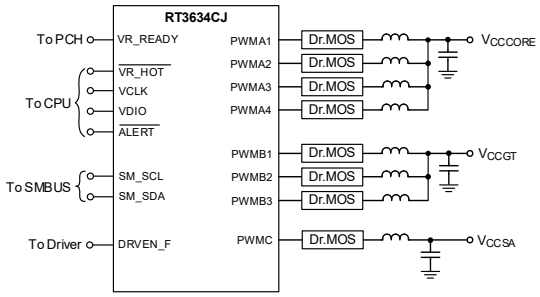
## Simplified Application Circuit




## Ordering Information

RT3634CJ□□-□

- The configuration code identifier for the register setting stored in the internal NVM
- Package Type
  QW: WQFN-60L 7x7 (W-Type)
- Lead Plating System
  G: Richtek Green Policy Compliant

Note:

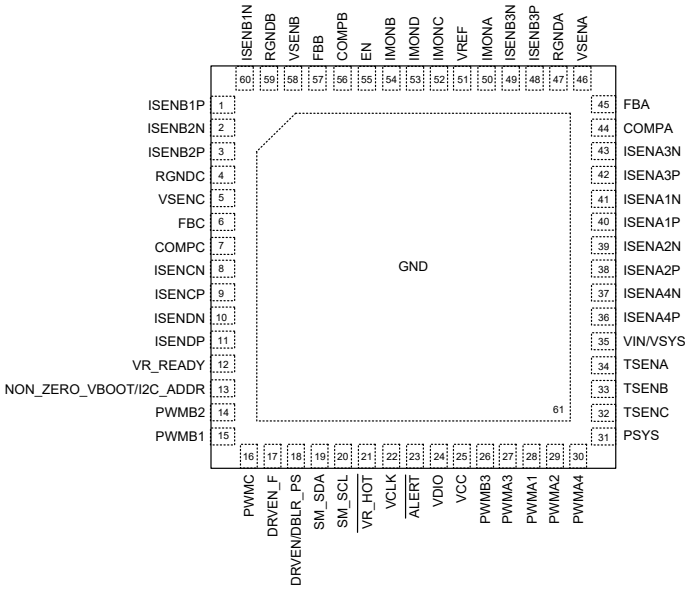
Richtek products are Richtek Green Policy compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.

## Marking Information

RT3634CJGQW: Product Code
YMDNN: Date Code

## Pin Configuration

(TOP VIEW)




WQFN-60L 7x7

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## Functional Pin Description

| Pin No | Pin Name | Pin Function |
|---|---|---|
| 1 | ISENB1P | Positive input of current-sense amplifier of phase 1 for Rail B. Connecting this pin to 5V disables Rail B. |
| 2 | ISENB2N | Negative input of current-sense amplifier of phase 2 for Rail B. |
| 3 | ISENB2P | Positive input of current-sense amplifier of phase 2 for Rail B. Connecting this pin to 5V disables phase 2 of Rail B. |
| 4 | RGNDC | Return ground for Rail C VR. This pin is the negative node of the differential remote voltage sensing. |
| 5 | VSENC | Rail C VR voltage sense input. This pin is connected to the terminal of Rail C VR output voltage. |
| 6 | FBC | Negative input of the error amplifier. This pin is for Rail C VR output voltage feedback to controller. |
| 7 | COMPC | Rail C VR compensation. This pin is an error amplifier output pin. |
| 8 | ISENCN | Negative input of current-sense amplifier for Rail C. |
| 9 | ISENCP | Positive input of current-sense amplifier for Rail C. Connecting this pin to 5V disables Rail C. |
| 10 | ISENDN | Negative input of current-sense amplifier for Rail D. |
| 11 | ISENDP | Positive input of current-sense amplifier for Rail D. |
| 12 | VR_READY | VR ready indicator. |
| 13 | NON_ZERO_VBOOT /I2C_ADDR | The NON_ZERO_VBOOT/I2C_ADDR pin can enable non-zero VBOOT function, in which the default voltage is set by the SD_GD_VID register.<br>Select the $I^2C$ slave address from 0x20 to 0x23 by connecting the resistor between this pin and GND.<br>To enable the non-zero VBOOT for soldering check, connect the NON_ZERO_VBOOT/I2C_ADDR pin to 5V and pull the EN high. If the soldering is good, rail outputs are non-zero VBOOT.<br>To select the $I^2C$ slave address, connect the resistor in range of 1kΩ, 20kΩ, 60.4kΩ and 121kΩ between this pin and GND for $I^2C$ slave address of 0x20, 0x21, 0x22 and 0x23 respectively. |
| 14 | PWMB2 | PWM output of phase 2 for Rail B. The PWM tri-state level can be set from 1.16V to 2.2V by the register of 0x24. |
| 15 | PWMB1 | PWM output of phase 1 for Rail B. The PWM tri-state level can be set from 1.16V to 2.2V by the register of 0x24. |
| 16 | PWMC | PWM output of Rail C. The PWM tri-state level can be set from 1.16V to 2.2V by the register of 0x24. |
| 17 | DRVEN_F | External driver mode control and the output high state is VCC. This pin will be high state when PS0~PS3 command is received and be floating state when PS4 command is received.<br>For discrete power MOSFET driver application, connecting 100kΩ resister to GND is required. |

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| Pin No | Pin Name | Pin Function |
|---|---|---|
| 18 | DRVEN/DBLR_PS | The DRVEN/DBLR_PS pin can be configured as driver enable pin (DRVEN) or phase doubler power state pin (DBLR_PS) by the configuration register.<br>As DRVEN pin for the external driver mode control, this pin will be high state when PS0 to PS3 command is received and be low state when PS4 command is received. The output high state is VCC.<br>As DBLR_PS, which is an external driver mode control when receiving PS4 command, this pin will be in high state. This pin can work with RT9637 on 1 PWM drive 2 power stage. As PS0 command is received, this pin will be in low state. As PS1 command is received, this pin will be in floating state. As PS2/3 command is received, this pin will be in high state. |
| 19 | SM_SDA | Data line for the $I^2C$ interface. If the $I^2C$ communication is not used, connect the SM_SDA and SM_SCL pins to higher than 3.3V to achieve power saving. |
| 20 | SM_SCL | Clock input for the $I^2C$ interface. If the $I^2C$ communication is not used, connect the SM_SDA and SM_SCL pins to higher than 3.3V to achieve power saving. |
| 21 | $\overline{\text{VR_HOT}}$ | Thermal monitor output. (Active low). |
| 22 | VCLK | Synchronous clock from the CPU. |
| 23 | $\overline{\text{ALERT}}$ | SVID alert. (Active low) |
| 24 | VDIO | VR and CPU data transmission interface. |
| 25 | VCC | Controller power supply. Connect this pin to 5V and place a RC filter, R = 1Ω and C = 4.7μF. The decoupling capacitor should be placed as close to PWM controller as possible. The recommended size of $R_{VCC}$ is 0603. |
| 26 | PWMB3 | PWM output of phase 3 for Rail B. The PWM tri-state level can be set from 1.16V to 2.2V by the register of 0x24. |
| 27 | PWMA3 | PWM output of phase 3 for Rail A. The PWM tri-state level can be set from 1.16V to 2.2V by the register of 0x24. |
| 28 | PWMA1 | PWM output of phase 1 for Rail A. The PWM tri-state level can be set from 1.16V to 2.2V by the register of 0x24. |
| 29 | PWMA2 | PWM output of phase 2 for Rail A. The PWM tri-state level can be set from 1.16V to 2.2V by the register of 0x24. |
| 30 | PWMA4 | PWM output of phase 4 for Rail A. The PWM tri-state level can be set from 1.16V to 2.2V by the register of 0x24. |
| 31 | PSYS | System input power monitor. Place the PSYS resistor as close to the IC as possible. The PSYS function can be disabled by pulling the voltage at the PSYS pin > (VCC – 0.5V). If the platform does not support PSYS function, it is recommended to connect PSYS pin to GND to avoid affecting system performance. |
| 32 | TSENC | Thermal sense input for Rail C. |
| 33 | TSENB | Thermal sense input for Rail B. |
| 34 | TSENA | Thermal sense input for Rail A. |
| 35 | VIN/VSYS | Input voltage pin. Connect a low pass filter of which time constant is at the switching frequency to this pin for setting on-time. |
| 36 | ISENA4P | Positive input of current-sense amplifier of phase 4 for Rail A. Connecting this pin to 5V can disable phase 4 of Rail A. |

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| Pin No | Pin Name | Pin Function |
|---|---|---|
| 37 | ISENA4N | Negative input of current-sense amplifier of phase 4 for Rail A. |
| 38 | ISENA2P | Positive input of current-sense amplifier of phase 2 for Rail A. Connecting this pin to 5V can disable phase 2 of Rail A. |
| 39 | ISENA2N | Negative input of current-sense amplifier of phase 2 for Rail A. |
| 40 | ISENA1P | Positive input of current-sense amplifier of phase 1 for Rail A. Connecting this pin to 5V disables Rail A. |
| 41 | ISENA1N | Negative input of current-sense amplifier of phase 1 for Rail A. |
| 42 | ISENA3P | Positive input of current-sense amplifier of phase 3 for Rail A. Connecting this pin to 5V can disable phase 3 of Rail A. |
| 43 | ISENA3N | Negative input of current-sense amplifier of phase 3 for Rail A. |
| 44 | COMPA | Rail A VR compensation. This pin is an error amplifier output pin. |
| 45 | FBA | Negative input of the error amplifier. This pin is for Rail A VR output voltage feedback to controller. |
| 46 | VSENA | Rail A VR voltage sense input. This pin is connected to the terminal of Rail A VR output voltage. |
| 47 | RGNDA | Return ground for Rail A VR. This pin is the negative node of the differential remote voltage sensing. |
| 48 | ISENB3P | Positive input of current-sense amplifier of phase 3 for Rail B. Connecting this pin to 5V can disable phase 3 of Rail B. |
| 49 | ISENB3N | Negative input of current-sense amplifier of phase 3 for Rail B. |
| 50 | IMONA | Rail A VR current monitor output for controller. This pin outputs a voltage proportional to the output current. |
| 51 | VREF | Fixed 0.6V output reference voltage. This voltage is used to offset the output voltage of all IMON pins. When the controller shuts down or sets all rails in PS4, voltage source shuts down. An exact 0.47μF decoupling capacitor and a 3.9Ω resistor must be placed between this pin and GND. |
| 52 | IMONC | Rail C VR current monitor output for controller. This pin outputs a voltage proportional to the output current. |
| 53 | IMOND | Rail D VR current monitor output for controller. This pin outputs a voltage proportional to the output current. |
| 54 | IMONB | Rail B VR current monitor output for controller. This pin outputs a voltage proportional to the output current. |
| 55 | EN | VR enable control input. |
| 56 | COMPB | Rail B VR compensation. This pin is an error amplifier output pin. |
| 57 | FBB | Negative input of the error amplifier. This pin is for Rail B VR output voltage feedback to controller. |
| 58 | VSENB | Rail B VR voltage sense input. This pin is connected to the terminal of Rail B VR output voltage. |
| 59 | RGNDB | Return ground for Rail B VR. This pin is the negative node of the differential remote voltage sensing. |
| 60 | ISENB1N | Negative input of current-sense amplifier of phase 1 for Rail B. |
| 61 (Exposed Pad) | GND | Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation. |

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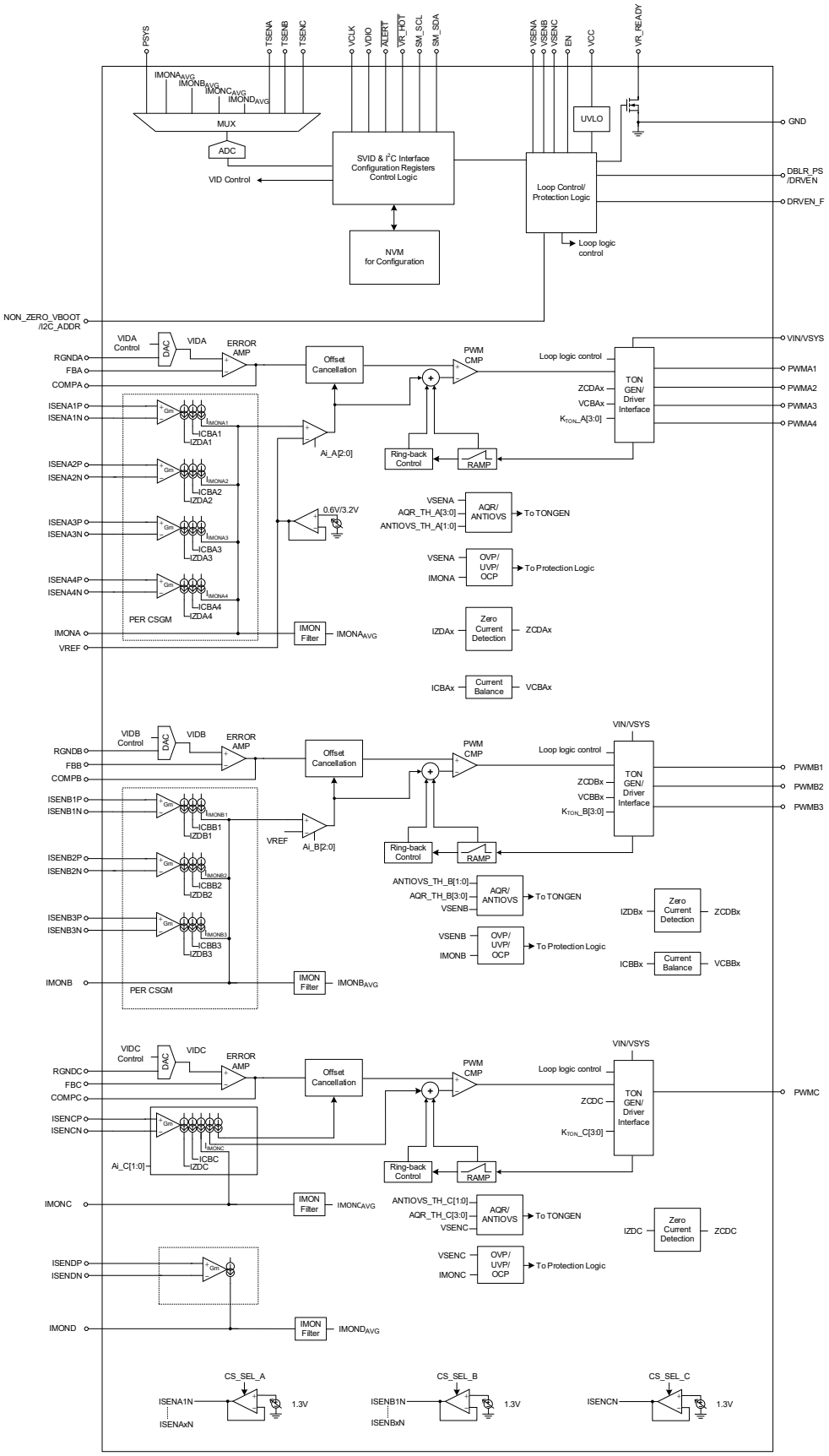
## Functional Block Diagram

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## Absolute Maximum Ratings (Note 1)

- VIN/VSYS to GND ----------–0.3V to 28V
- VCC to GND ----------–0.3V to 6.5V
- VDIO, VCLK, $\overline{\text{ALERT}}$ to GND
  DC ----------–0.3V to 6.8V
  < 10ns ----------–0.45V to 7.5V
- RGNDA/B/C to GND ----------–0.3V to 0.3V
- Other Pins----------–0.3V to 6.8V
- Lead Temperature (Soldering, 10 sec.)----------260°C
- Junction Temperature----------150°C
- Storage Temperature Range----------–65°C to 150°C

## ESD Rating (Note 2)

- HBM (Human Body Model) ----------2kV

## Recommended Operating Conditions (Note 3)

- VIN/VSYS to GND ----------4.5V to 24V
- Supply Input Voltage, VCC ----------4.5V to 5.5V
- Junction Temperature Range ----------–40°C to 125°C

## Thermal Information (Note 4)

- WQFN-60L 7x7, $\theta_{JA}$ ----------25.5°C/W
- WQFN-60L 7x7, $\theta_{JC(Top)}$ ----------13.5°C/W

## Electrical Characteristics

($V_{CC}$ = 5V, typical values are referenced to $T_J$ = 25°C, Min and Max values are referenced to $T_J$ from –10°C to 105°C, unless otherwise specified)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Supply Input** | | | | | | |
| Supply Voltage | $V_{CC}$ | | 4.5 | 5 | 5.5 | V |
| Supply Current | $I_{VCC}$ | EN = H, not switching | -- | 10.7 | -- | mA |
| Supply Current at PS2 DACOFF | $I_{VCC}$ | EN = H, not switching | -- | 4.3 | -- | mA |
| Supply Current at PS3 DACOFF | $I_{VCC}$ | EN = H, not switching | -- | 1.8 | -- | mA |
| Supply Current at PS4 | $I_{VCC_PS4}$ | EN = H, not switching | -- | 69 | -- | μA |
| Shutdown Current | $I_{SHDN}$ | EN = L | -- | 50 | -- | μA |
| **EA Amplifier** | | | | | | |
| DC Gain | $A_{DC}$ | $R_L$ = 47kΩ | 70 | -- | -- | dB |
| Gain-Bandwidth Product | $G_{BW}$ | $C_{LOAD}$ = 5pF | -- | 10 | -- | MHz |

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| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Slew Rate | $SR_{EA}$ | $C_{LOAD}$ = 10pF (Gain = –4, Rf = 47kΩ, $V_{OUT}$ = 0.5V to 3V) | -- | 5 | -- | V/μs |
| Output Voltage Range | $V_{COMP}$ | $R_L$ = 47kΩ | 0.3 | -- | 3.6 | V |
| Maximum Source/Sink Current | $I_{OUTEA}$ | $V_{COMP}$ = 2V | -- | 5 | -- | mA |
| **Current Sensing Amplifier (Rail A/B/C/D)** | | | | | | |
| Impedance at Positive Input | $R_{ISENxP}$ | | 1 | -- | -- | MΩ |
| CS Input Voltage | $V_{CSIN}$ | Differential voltage range of DCR sense. ($V_{CSIN}$ = Inductor current x DCR x DCR divider) | –10 | -- | 80 | mV |
| Current Sense Gain Error | $A_{MIRROR}$ | Internal current mirror gain of per phase current sense $I_{IMON}/I_{CS,PERx}$ | 1.2125 | 1.25 | 1.2875 | A/A |
| **TON Setting (Rail A/B/C)** | | | | | | |
| On-Time Setting | $t_{ON}$ | $V_{IN}$ = 19V, VID = 0.9V, $K_{TON}$ = 2 | -- | 93 | -- | ns |
| Minimum Off-Time | $t_{OFF}$ | VID = 1V under PS1 condition | -- | 130 | 300 | ns |
| Minimum On-Time | $t_{ON(MIN)}$ | | -- | 50 | -- | ns |
| **Protections** | | | | | | |
| Undervoltage Lockout Threshold | $V_{UVLO,rise}$ | Rising edge | 4.1 | -- | 4.45 | V |
| | $V_{UVLO}$ | Falling edge | 3.9 | -- | 4.2 | V |
| | $\Delta V_{UVLO}$ | Rising edge hysteresis | 100 | 170 | 250 | mV |
| Overvoltage Protection Threshold | $V_{ROVP}$ | Respect to VID voltage, VID > 1V | VID + 320 | VID + 350 | VID + 380 | mV |
| | $V_{AOVP}$ | VID ≤ 1V | 1.3 | 1.35 | 1.4 | V |
| Undervoltage Protection Threshold | $V_{UV}$ | Respect to VID voltage | –680 | –650 | –620 | mV |
| **VR Enable and VR_READY** | | | | | | |
| VR EN Threshold | Logic-High | $V_{IH_EN}$ | | 0.7 | -- | -- | V |
| | Logic-Low | $V_{IL_EN}$ | | -- | -- | 0.3 | |
| Leakage Current of EN | | $I_{LEAK_EN}$ | | –1 | -- | 1 | μA |
| VR_READY Pull Low Voltage | | $V_{VR_READY}$ | $I_{VR_READY}$ = 10mA | -- | -- | 0.13 | V |
| **Serial VID and $\overline{VR_HOT}$** | | | | | | |
| VCLK, VDIO Input Voltage | Logic-High | $V_{IH_SVID}$ | | 0.65 | -- | -- | V |
| | Logic-Low | $V_{IL_SVID}$ | | -- | -- | 0.45 | |
| Leakage Current of VCLK, VDIO, $\overline{ALERT}$ and $\overline{VR_HOT}$ | | $I_{LEAK_SVID}$ | | –1 | -- | 1 | μA |

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| Parameter | | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Output Voltage Low of VDIO / $\overline{\text{ALERT}}$ / $\overline{\text{VR_HOT}}$ | | $V_{OL_VDIO}$ | $I_{VDIO}$ = 10mA | -- | -- | 0.13 | V |
| | | $V_{OL_ALERT}$ | $I_{ALERT}$ = 10mA | -- | -- | 0.13 | |
| | | $V_{OL_VRHOT}$ | $I_{VRHOT}$ = 10mA | -- | -- | 0.13 | |
| **$I^2C$ Interface** | | | | | | | |
| SCL, SDA | Logic-High | $V_{IH_I2C}$ | | 1 | -- | -- | V |
| | Logic-Low | $V_{IL_I2C}$ | | -- | -- | 0.6 | |
| **Standard/Fast Mode** | | | | | | | |
| SCL Clock Rate | | $f_{SCL}$ | Standard mode | -- | -- | 100 | kHz |
| | | | Fast mode | -- | -- | 400 | |
| Hold Time (Repeated) Start Condition. After this period, the first clock pulse is generated. | | $t_{HD_STA}$ | | 0.6 | -- | -- | µs |
| Low Period Of the SCL Clock | | $t_{LOW}$ | | 1.3 | -- | -- | µs |
| High Period Of the SCL Clock | | $t_{HIGH}$ | | 0.6 | -- | -- | µs |
| Set-Up Time for a Repeated START Condition | | $t_{SU_STA}$ | | 0.6 | -- | -- | µs |
| Data Hold Time | | $t_{HD_DAT}$ | Standard mode | 0 | -- | -- | µs |
| | | | Fast mode | 0 | -- | 0.9 | |
| Data Set-Up Time | | $t_{SU_DAT}$ | Standard mode | 250 | -- | -- | ns |
| | | | Fast mode | 100 | -- | -- | |
| Set-Up Time for STOP Condition | | $t_{SU_STO}$ | | 0.6 | -- | -- | µs |
| Bus Free Time Between a STOP and START Condition | | $t_{BUF}$ | | 1.3 | -- | -- | µs |
| Rising Time of Both SDA and SCL Signals | | $t_R$ | Standard mode | -- | -- | 300 | ns |
| | | | Fast mode | 20 | -- | 300 | |
| Falling Time of Both SDA and SCL signals | | $t_F$ | Standard mode | -- | -- | 300 | ns |
| | | | Fast mode | 20 | -- | 300 | |
| SDA Output Low Sink Current | | $I_{OL}$ | SDA voltage = 0.4V | 2 | -- | -- | mA |
| **$V_{REF}$** | | | | | | | |
| VREF Voltage | | $V_{REF}$ | Normal operation | 0.59 | 0.6 | 0.61 | V |
| VREF SPS Voltage | | $V_{REF_SPS}$ | Normal operation (ISEN1N) | 1.2 | 1.3 | 1.4 | V |

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| Parameter | | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **ADC** | | | | | | | |
| Digital IMON Set | Rail A/B/C | $dV_{IMON_ICCMAX}$ | $V_{IMON} - V_{REF}$ = 0.8V @ ICCMAX ≥ 80A | -- | 255 | -- | Decimal |
| | | | $V_{IMON} - V_{REF}$ = 0.4V @ 40A ≤ ICCMAX < 80A | | | | |
| | | | $V_{IMON} - V_{REF}$ = 0.2V @ ICCMAX < 40A | | | | |
| | Rail D | $dV_{IMON_ICCMAX}$ | $V_{IMON}$-$V_{REF}$ = 1.6V | -- | 255 | -- | Decimal |
| PSYS Maximum Input Voltage | | PSYS | $V_{PSYS}$ = 1.6V | -- | 255 | -- | Decimal |
| VSYS Maximum Input Voltage | | VSYS | VIN/VSYS = 24V | -- | 255 | -- | Decimal |
| Average Period of IMON | | $t_{IMON}$ | | -- | 150 | -- | μs |
| Average Period of TSEN | | $t_{TSEN}$ | | -- | 600 | -- | μs |
| **Thermal Monitor** | | | | | | | |
| TSEN Voltage Threshold to Pull Low $\overline{VR_HOT}$ (Asserts $\overline{VR_HOT}$) | | $V_{TSEN}$ for negative temperature coefficient | Falling | 1.105 | 1.112 | 1.124 | V |
| TSEN Voltage Threshold to Pull High $\overline{VR_HOT}$ (De-Asserts $\overline{VR_HOT}$) | | | Rising | 1.147 | 1.154 | 1.166 | V |
| TSEN Rises (voltage down) to pull Low $\overline{ALERT}$ | | | $\overline{ALERT}$ = Low | 1.147 | 1.154 | 1.166 | V |
| TSEN Down (voltage up) to pull Low $\overline{ALERT}$ | | | $\overline{ALERT}$ = Low | 1.196 | 1.201 | 1.213 | V |
| TSEN Voltage Threshold to Pull Low $\overline{VR_HOT}$ (Asserts $\overline{VR_HOT}$) | | $V_{TSEN}$ for positive temperature coefficient | Falling | 1.366 | 1.376 | 1.39 | V |
| TSEN Voltage Threshold to Pull High $\overline{VR_HOT}$ (De-Asserts $\overline{VR_HOT}$) | | | Rising | 1.39 | 1.4 | 1.414 | V |
| TSEN Rises (Voltage Up) to Pull Low $\overline{ALERT}$ | | | $\overline{ALERT}$ = Low | 1.366 | 1.376 | 1.39 | V |
| TSEN Down (Voltage Down) to Pull Low $\overline{ALERT}$ | | | $\overline{ALERT}$ = Low | 1.342 | 1.352 | 1.366 | V |
| **ITSEN** | | | | | | | |
| TSEN Source Current | | $I_{TSEN}$ | $V_{TSEN}$ = 1.6V | 79.2 | 80 | 80.8 | μA |
| Input Power Domain Disable Voltage | | $V_{PSYS}$ | | VCC – 0.5 | -- | -- | V |
| **PWM Driving Capability** | | | | | | | |
| PWM Source Resistance | | $R_{PWM_SRC}$ | | -- | 25 | -- | Ω |

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| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| PWM Sink Resistance | $R_{PWM_SNK}$ | | -- | 10 | -- | Ω |
| **PWM Output** | | | | | | |
| PWMx Output High Level | | $I_{OUT}$ = 4mA | VCC – 0.16 | -- | -- | V |
| PWMx Output Low Level | | $I_{OUT}$ = 4mA | -- | -- | 0.08 | V |

**Note 1.** Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

**Note 2.** Devices are ESD sensitive. Handling precautions are recommended.

**Note 3.** The device is not guaranteed to function outside its operating conditions.

**Note 4.** For more information about thermal parameter, see the Application and Definition of Thermal Resistances report, AN061.

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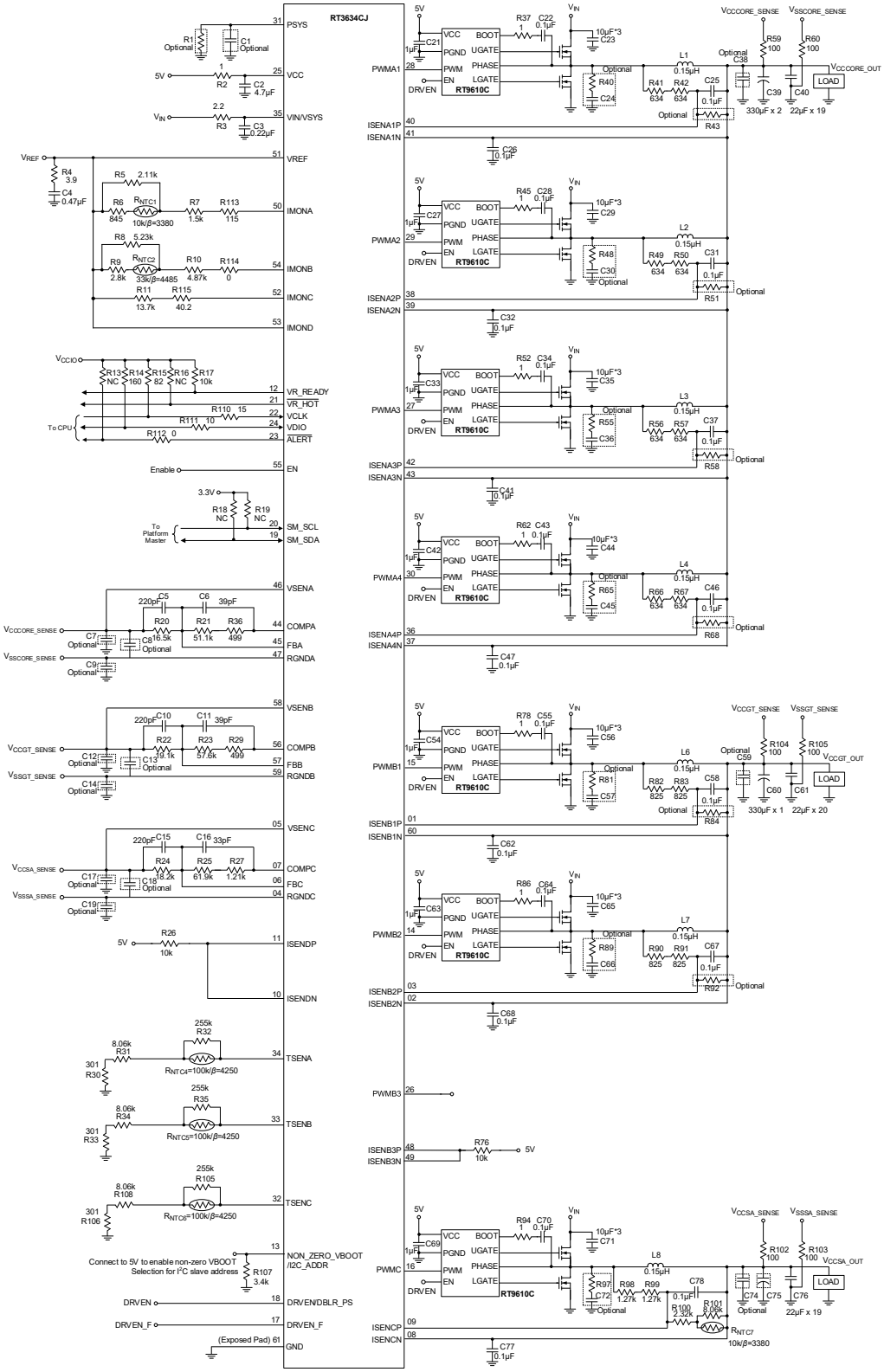
## Typical Application Circuit

### Platform : MTL-H45W Performance

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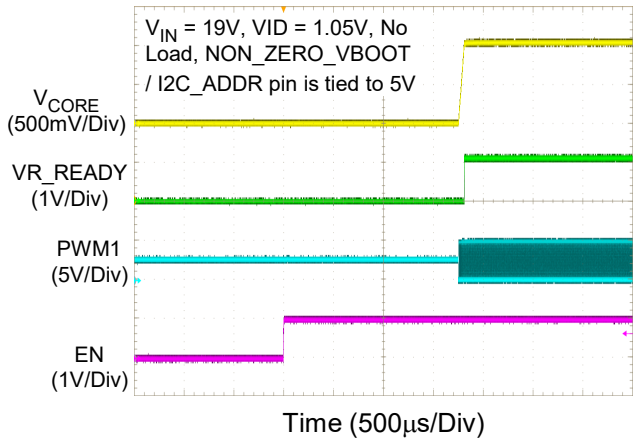
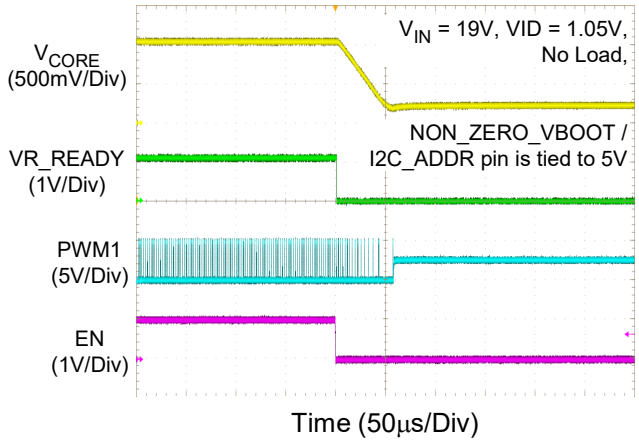
## Typical Operating Characteristics

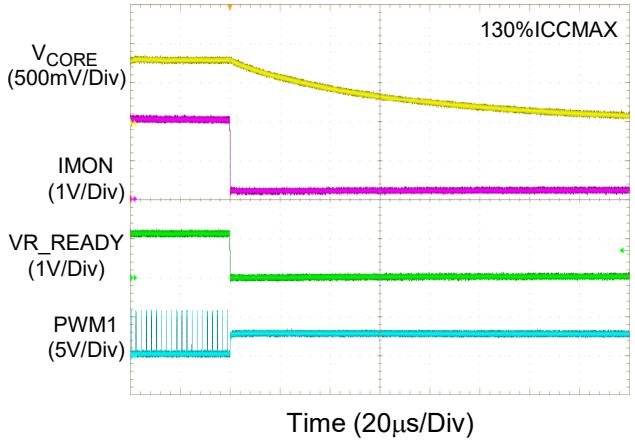
### CORE VR Power On from EN



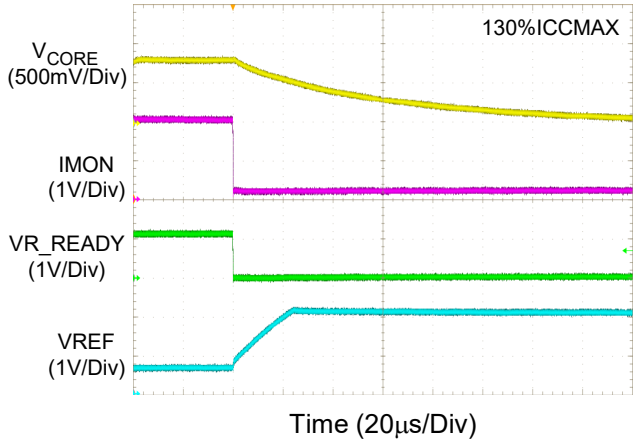

### CORE VR Power Off from EN



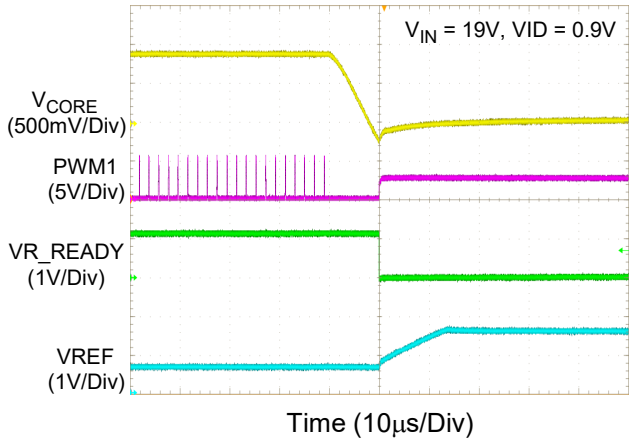

### CORE VR OCP



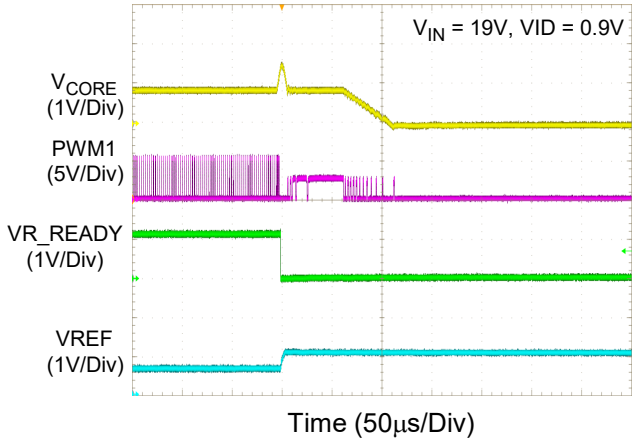

### CORE VR OCP




### CORE VR UVP




### CORE VR OVP

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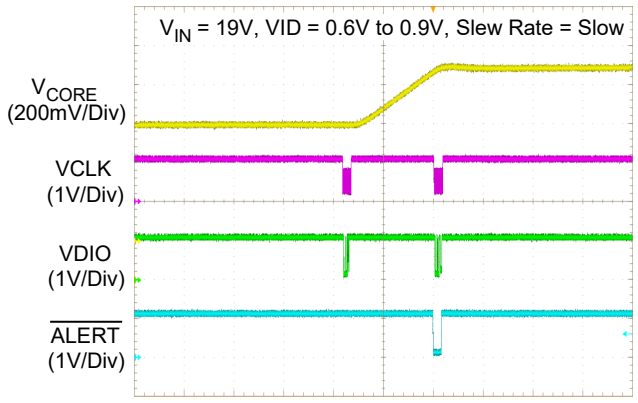
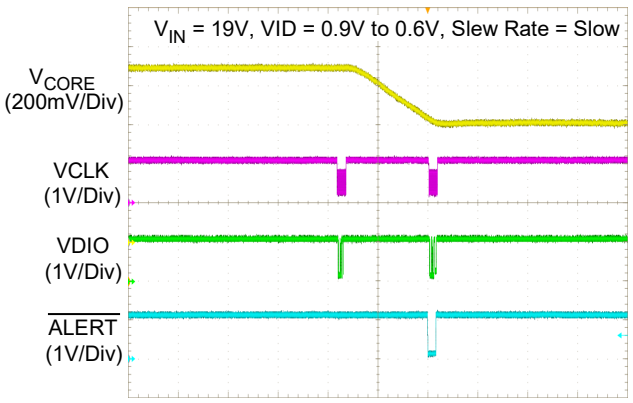
### CORE VR Dynamic VID Up



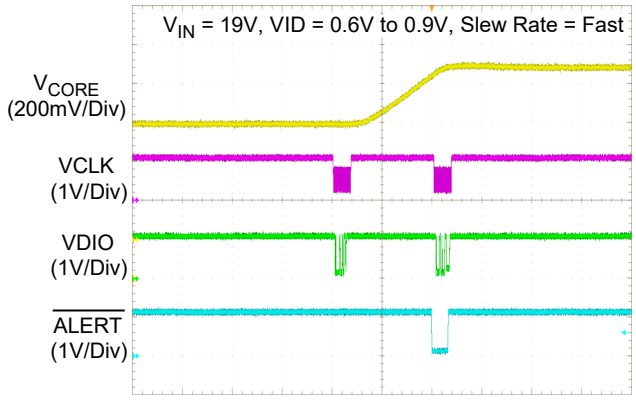

Time (10μs/Div)

### CORE VR Dynamic VID Down



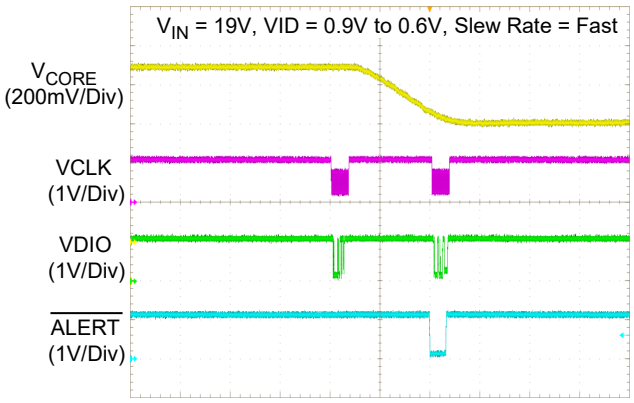

Time (10μs/Div)

### CORE VR Dynamic VID Up



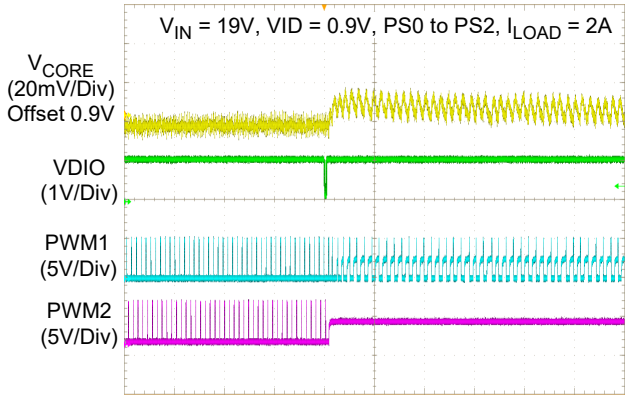

Time (5μs/Div)

### CORE VR Dynamic VID Down



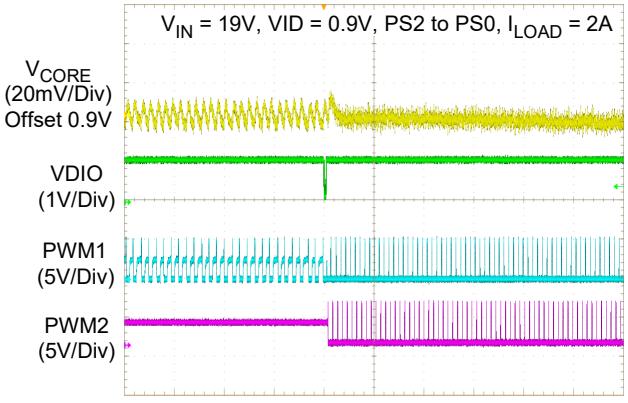

Time (5μs/Div)

### CORE VR Mode Transient




Time (20μs/Div)

### CORE VR Mode Transient




Time (20μs/Div)

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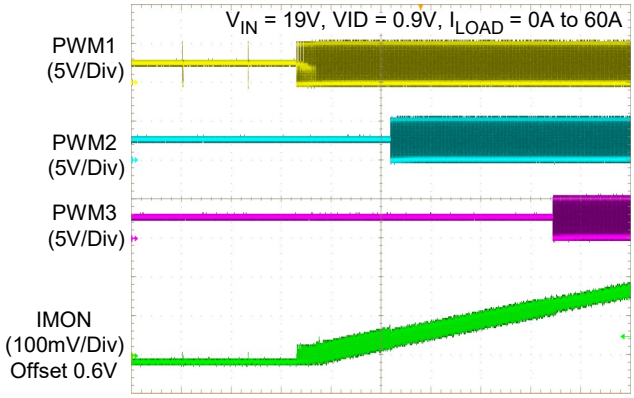
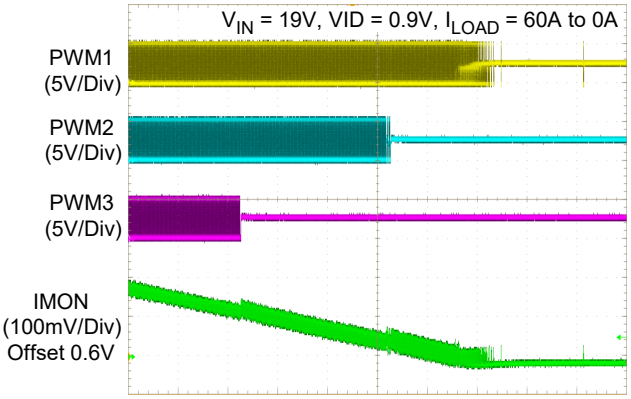
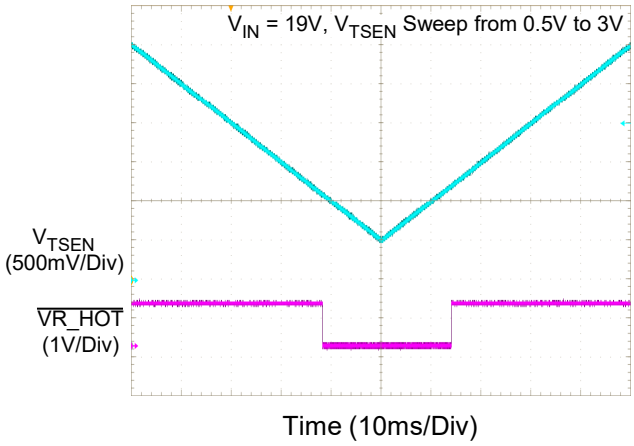
### CORE VR Smart Phase Management



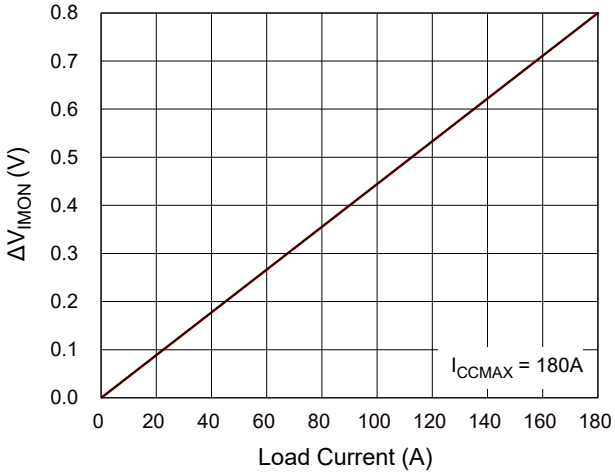

### CORE VR Smart Phase Management



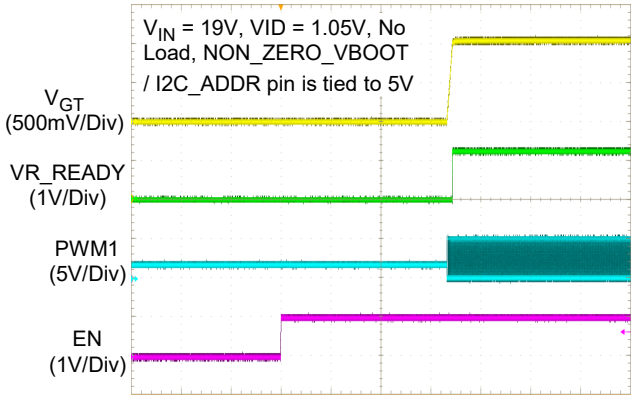

### CORE VR Thermal Monitioring



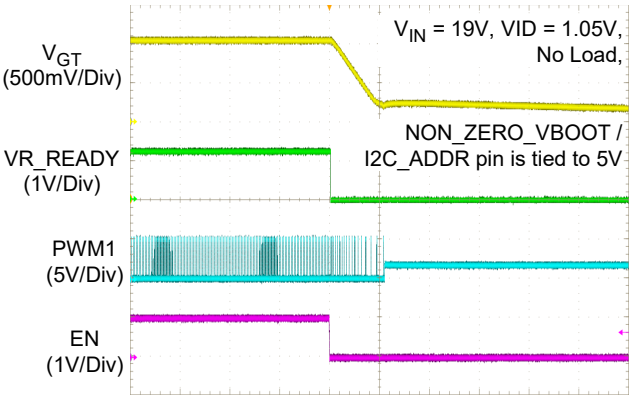

### $\Delta V_{IMON}$ vs. Load Current




### GT VR Power On from EN




### GT VR Power Off from EN

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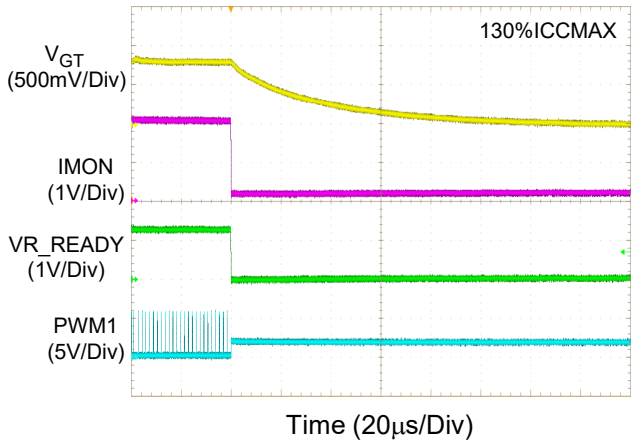
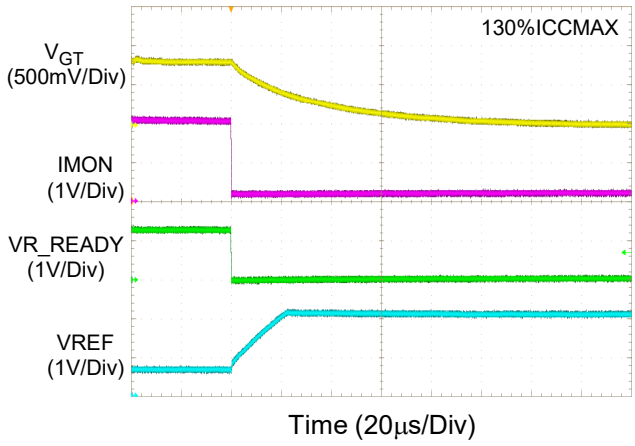
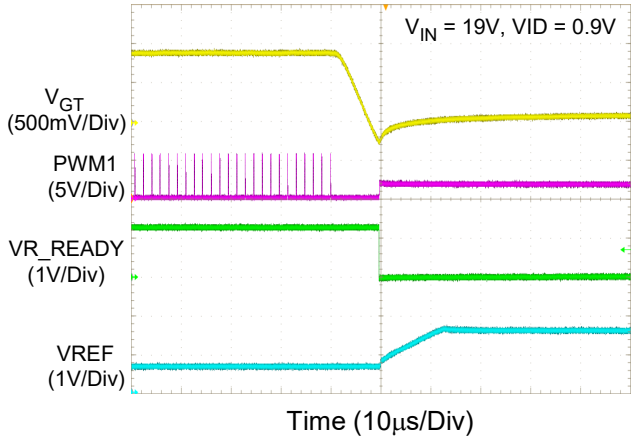
### GT VR OCP



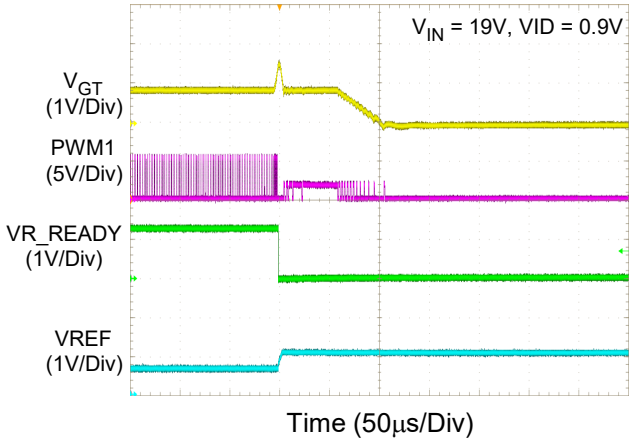

### GT VR OCP



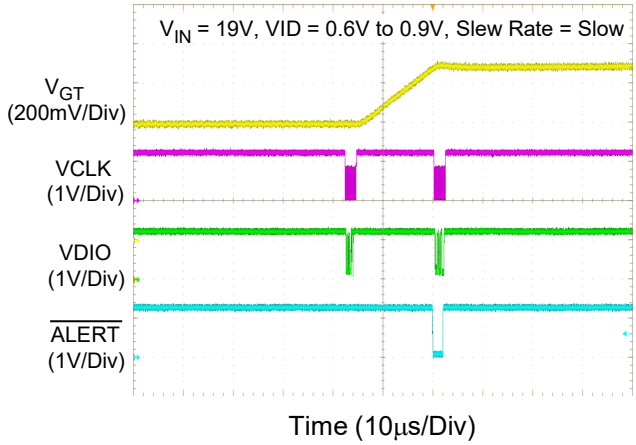

### GT VR UVP



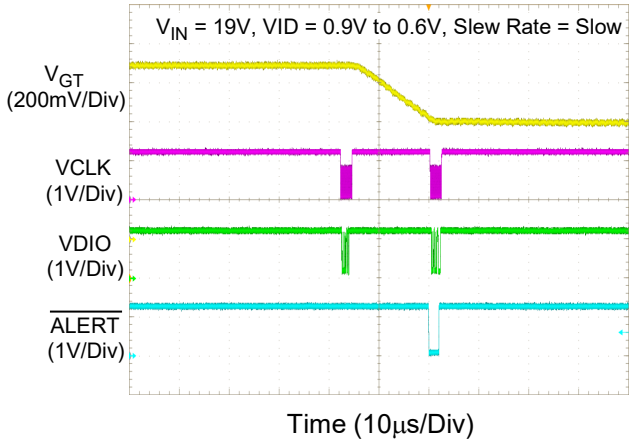

### GT VR OVP




### GT VR Dynamic VID Up




### GT VR Dynamic VID Down

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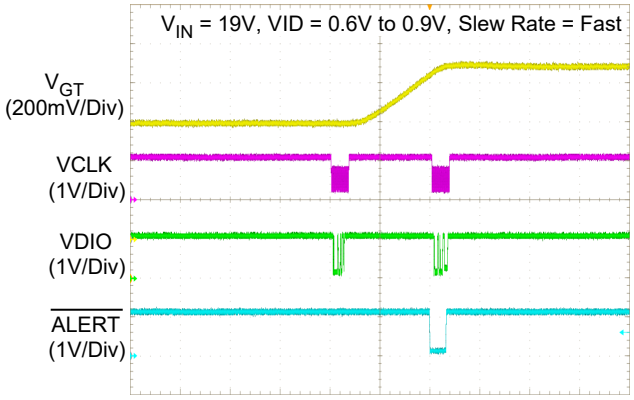
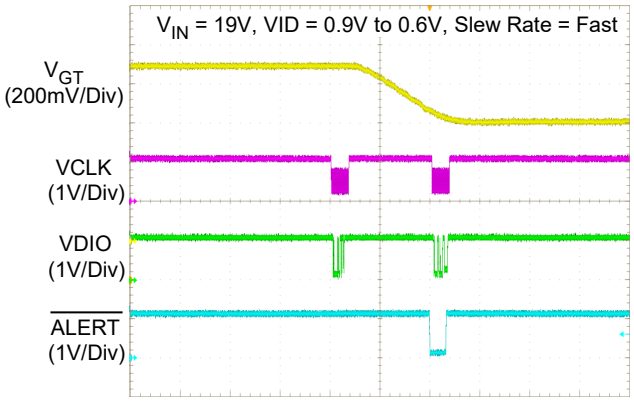
### GT VR Dynamic VID Up



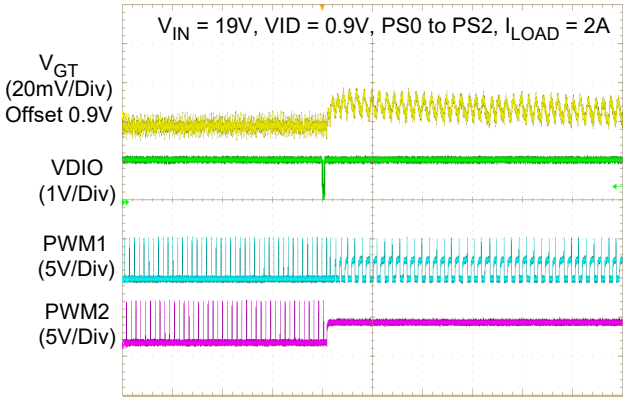

Time (5μs/Div)

### GT VR Dynamic VID Down



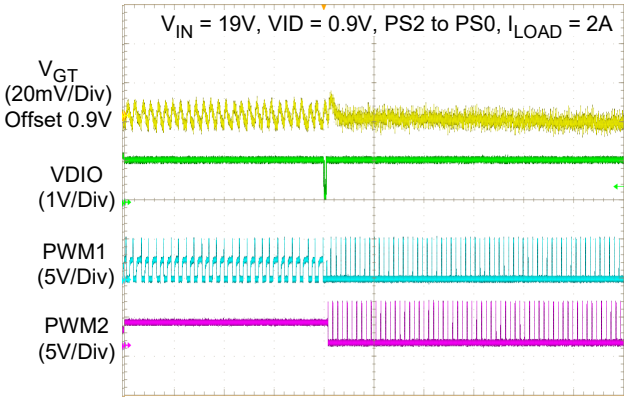

Time (5μs/Div)

### GT VR Mode Transient



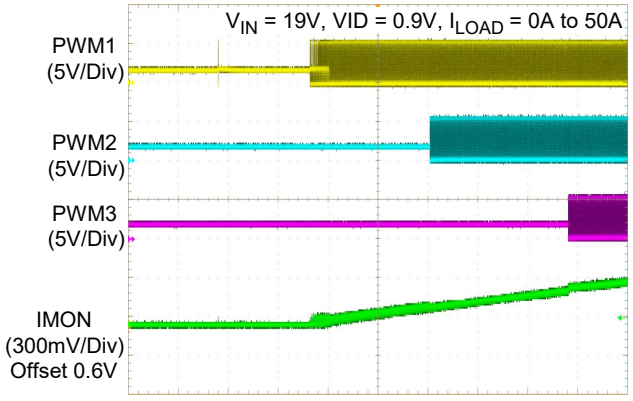

Time (20μs/Div)

### GT VR Mode Transient



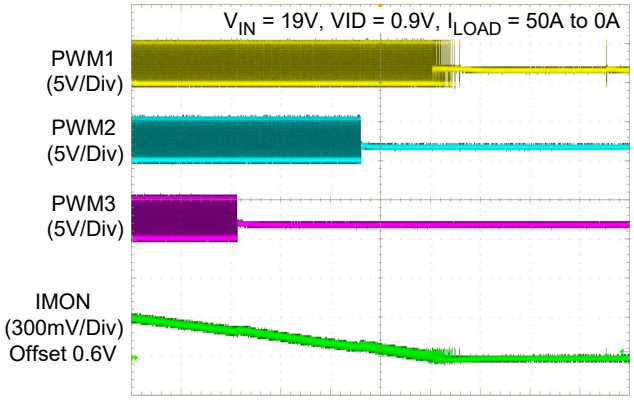

Time (20μs/Div)

### GT VR Smart Phase Management




Time (200μs/Div)

### GT VR Smart Phase Management




Time (200μs/Div)

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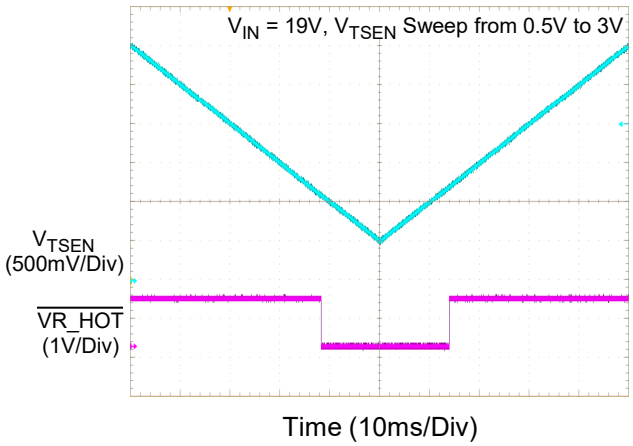
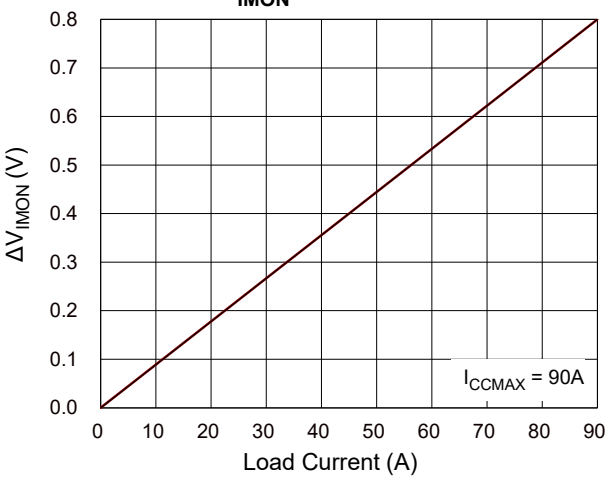
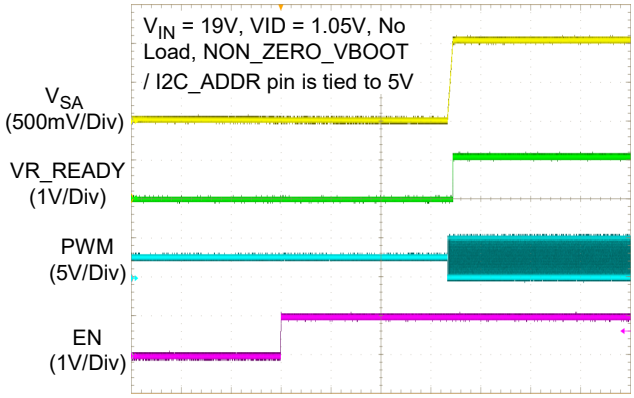
### GT VR Thermal Monitioring



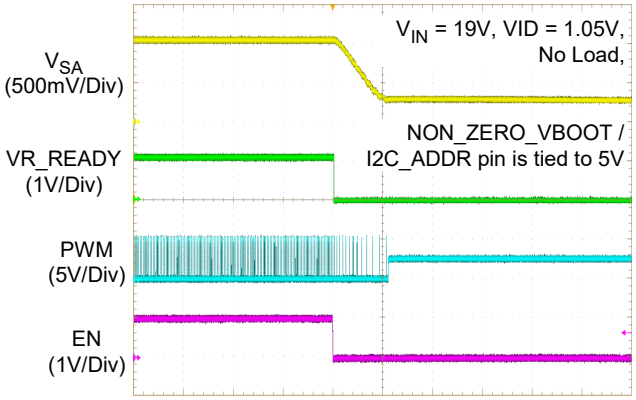

### ΔVIMON vs. Load Current



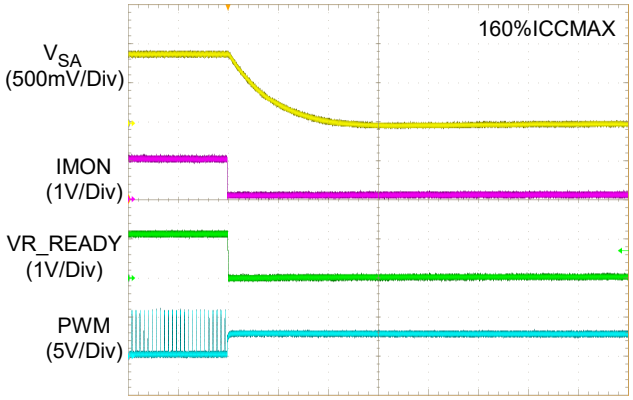

### SA VR Power On from EN



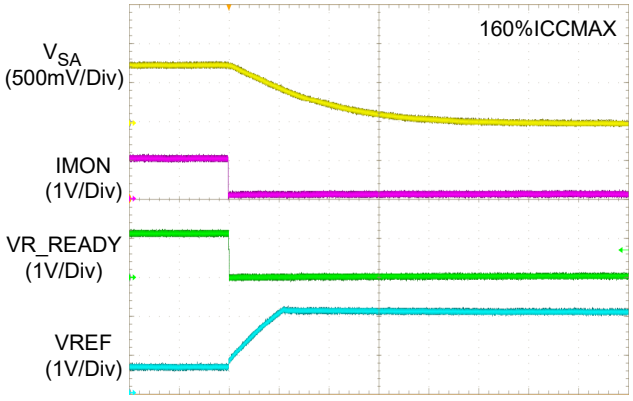

### SA VR Power Off from EN




### SA VR OCP




### SA VR OCP

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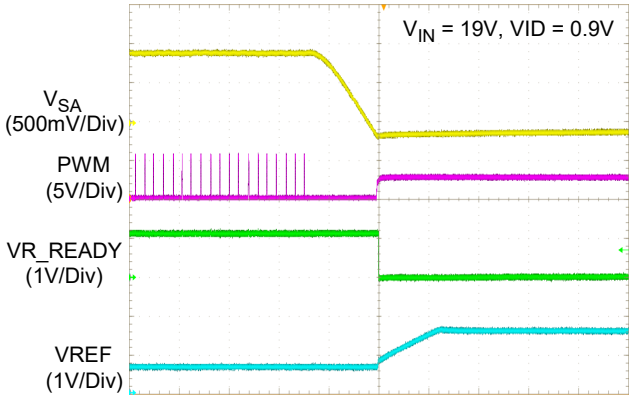
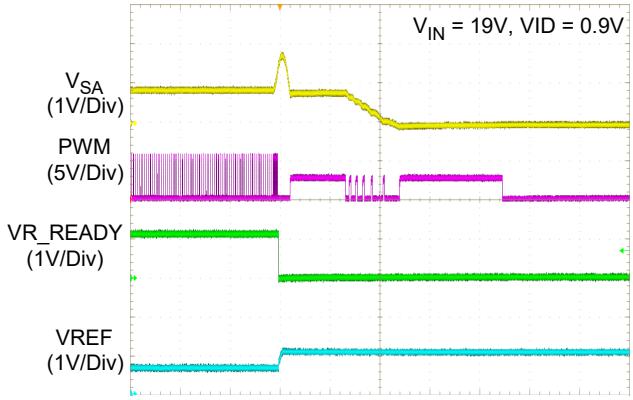
### SA VR UVP



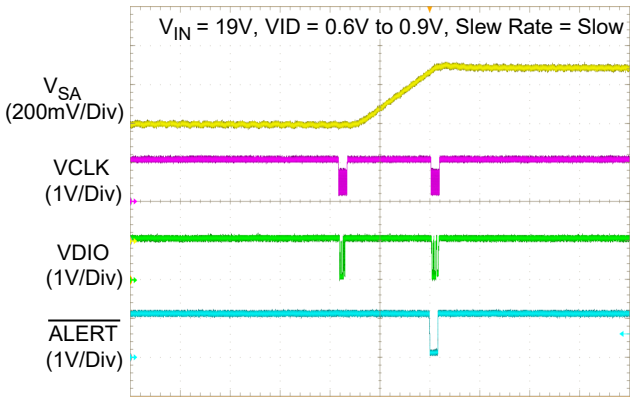

Time (10µs/Div)

### SA VR OVP



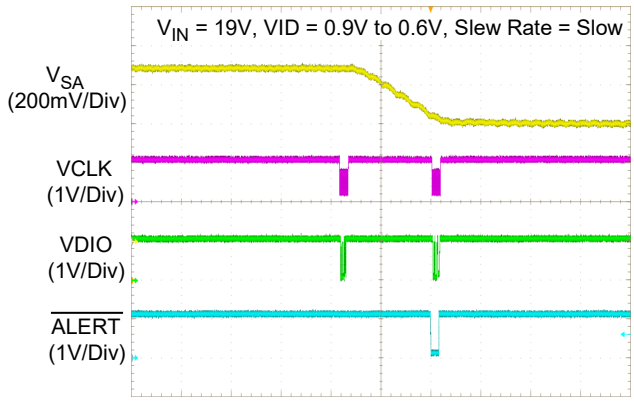

Time (50µs/Div)

### SA VR Dynamic VID Up



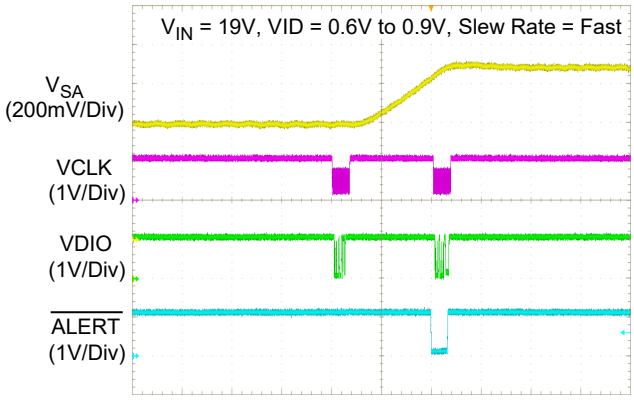

Time (10µs/Div)

### SA VR Dynamic VID Down



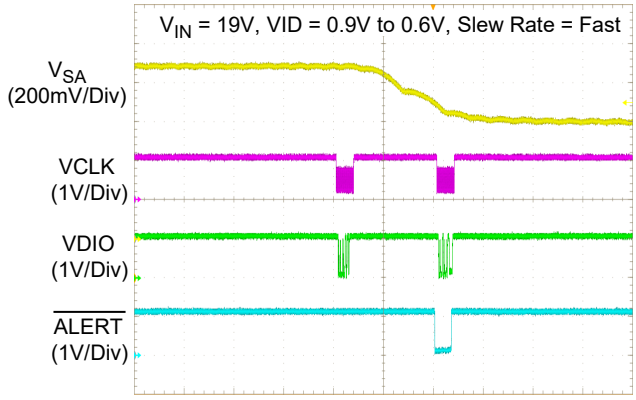

Time (10µs/Div)

### SA VR Dynamic VID Up




Time (5µs/Div)

### SA VR Dynamic VID Down




Time (5µs/Div)

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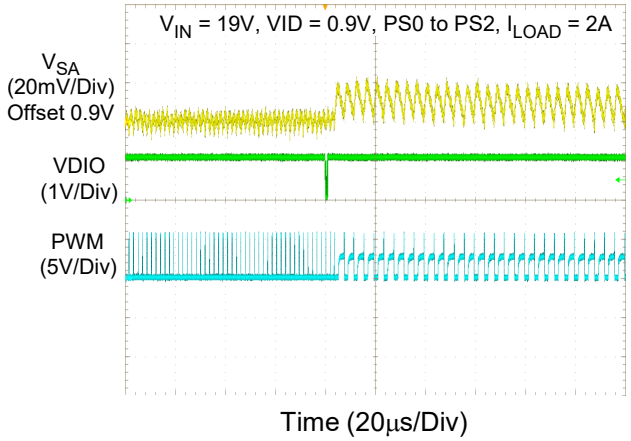
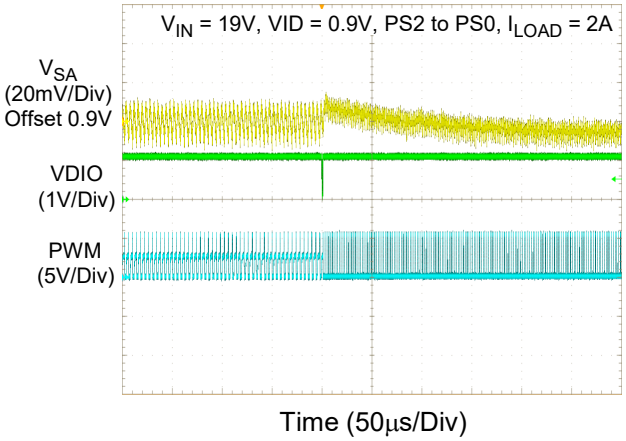
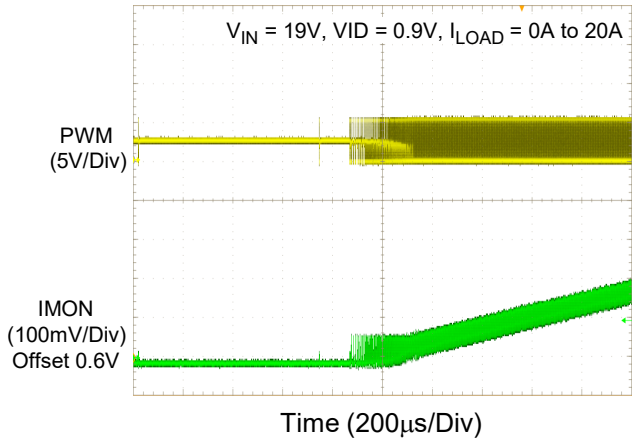
### SA VR Mode Transient



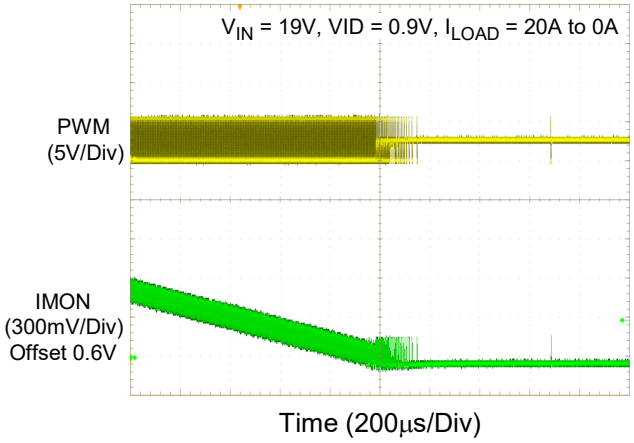

### SA VR Mode Transient



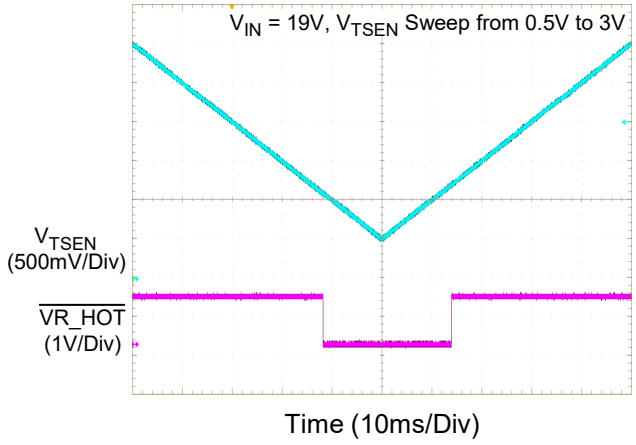

### SA VR Smart Phase Management



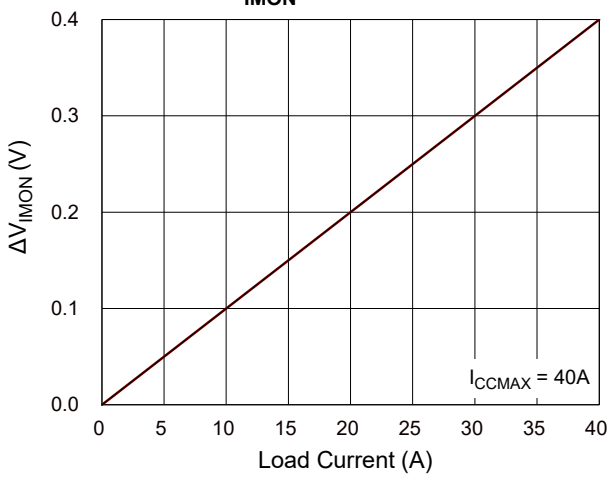

### SA VR Smart Phase Management




### SA VR Thermal Monitioring




### $\Delta V_{IMON}$ vs. Load Current

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## Operation

### G-NAVP™ Control Mode

The RT3634CJ adopts G-NAVP™ (Green Native AVP), which is Richtek's proprietary topology. It is derived from current mode constant on-time control with finite DC gain of error amplifier and DC offset cancellation. The topology can achieve easy loadline design and provide high DC accuracy and fast transient response. When sensed current signal reaches sensed voltage signal, the RT3634CJ generates a PWM pulse to achieve loop modulation. Figure 1 shows the basic G-NAVP™ behavior waveforms. The COMP signal is the sensed voltage that is inverted and amplified signal of output voltage. While current loading is increasing, referring to Figure 1, COMP rises due to output voltage droop. Then rising COMP forces PWM to turn on earlier and closely. While inductor current reaches loading current, COMP enters another steady state of higher voltage, and the corresponding output voltage is in the steady state of lower voltage. The loadline, output voltage drooping by an amount proportional to loading current, is achieved.

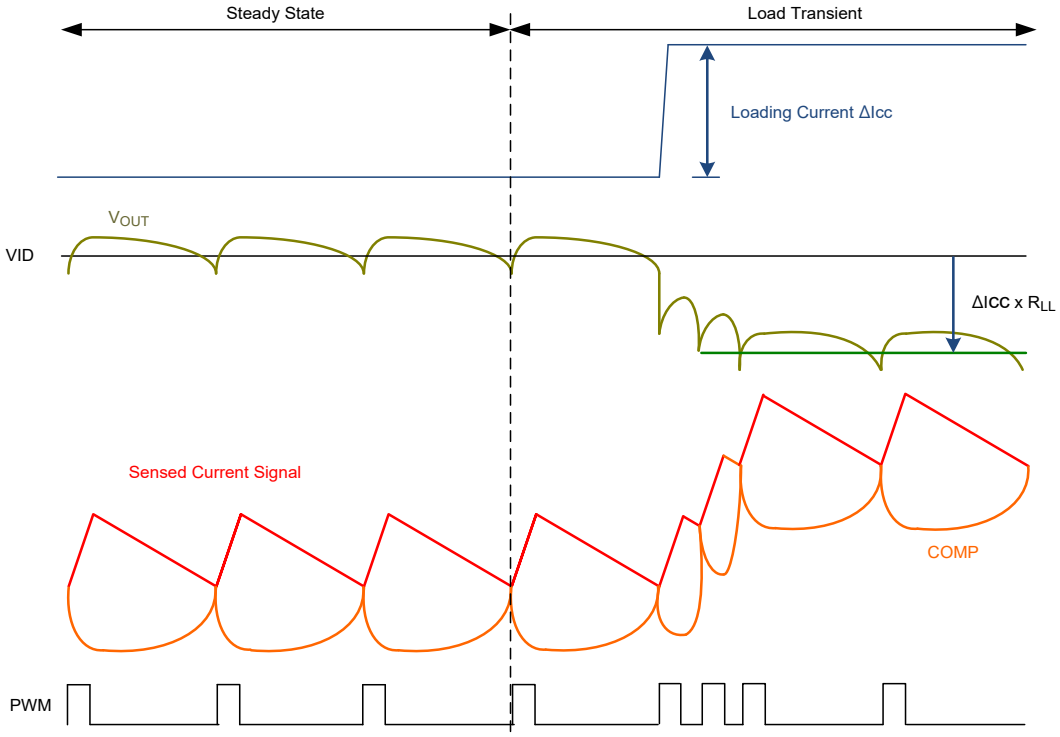


Figure 1. G-NAVP™ Behavior Waveform

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### SVID Interface, Control Logic and Configuration Registers

SVID Interface receives or transmits SVID signal from/to CPU. Control Logic executes command (Read/Write registers, SetVID, SetPS) and sends related signals to control VR. Configuration Registers include function setting registers and CPU required registers.

### IMON Filter

IMON Filter is used to average current signal by analog low-pass filter. It outputs $IMON_{AVG}$ to the MUX of ADC for current reporting.

### MUX and ADC

The MUX supports the inputs of, TSENA, TSENB, TSENC, PSYS, $IMONA_{AVG}$, $IMONB_{AVG}$, $IMONC_{AVG}$ and $IMOND_{AVG}$. The ADC converts these analog signals to digital codes for reporting or function settings.

### UVLO

The UVLO detects the VCC voltage. As VCC exceeds threshold, controller issues POR = high and waits EN. After both POR and EN are ready, then controller is enabled.

### Loop Control and Protection Logic

It controls power-on/off sequence, protections, power state transition, and PWM sequence.

### DAC

The DAC generates a reference VID voltage according to the VID code sent by Control Logic. According to SetVID command, Control Logic dynamically changes VID voltage to target with required slew rate.

### ERROR AMP

The ERROR AMP inverts and amplifies the difference between output voltage and VID with externally setting finite DC gain. The output signal is COMP for PWM trigger.

### PER CSGM

The PER CSGM senses per-phase inductor current. The outputs are used for loop response, Current Balance, Zero Current Detection, current reporting and overcurrent protection.

### SUM CSGM

The SUM CSGM senses total inductor current with RIMON gain adjustment. SUM CSGM output current ratio can also be selected by the configuration registers. It helps wider application range of DCR and load line. SUM CSGM output is used for PWM trigger.

### RAMP

The RAMP helps loop stability and transient response.

### PWM CMP

The PWM comparator compares COMP signal and sum current signal based on RAMP to trigger PWM.

### Offset Cancellation

The offset cancellation is based on VID, COMP voltage and current signal from SUM CSGM to control output voltage accuracy.

### Current Balance

Per-phase current sense signal is compared with sensed average current. The comparison result will adjust each phase PWM width to optimize current and thermal balance.

### Zero Current Detection

Detect whether each phase current crosses zero current. The result is used for DEM power saving and overshoot reduction (Anti-overshoot Function).

### AQR and ANTIOVS

The AQR is a new generation of quick response mechanism (Adaptive Quick Response, AQR) which detects loading rising edge and allows all PWM to turn on. The PWM pulse width triggered by AQR is adaptive to loading level. The AQR trigger level can be set by the configuration registers. ANTIOVS can help overshoot reduction which detects loading falling edge and forces all PWM in tri-state until the zero current is detected.

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### TONGEN and Driver Interface

The PWM comparator output signal will trigger TONGEN to generate PWM pulse. The PWM sequence is controlled by Loop Control. The PWM pulse width is determined by frequency setting, current balance output and Adaptive Quick Response (AQR) settings. Once AQR is triggered, VR will allow all PWMs to turn on at the same time. Driver Interface provides high/low/tri-state to drive external driver. In power saving mode, Driver Interface forces PWM in tri-state to turn off high-side and low-side power MOSFETs according to Zero Current Detection output. In addition, PWM state is controlled by Protection Logic. Different protections force required PWM state.

### OVP, UVP and OCP

Overvoltage protection/undervoltage protection/ overcurrent protection.

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## Application Information

***Richtek's component specification does not include the following information in the Application Information section. Thereby no warranty is given regarding its validity and accuracy. Customers should take responsibility to verify their own designs and reserve suitable design margin to ensure the functional suitability of their components and systems.***

The RT3634CJ includes three voltage rails: a 4-phase synchronous buck controller for VCCCORE VR, a 3-phase synchronous buck controller for VCCGT VR, and a 1-phase synchronous buck controller for VCCSA VR. The output of each rail can be configured to support the desired phase assignments up to a maximum phase count of 4 phases for VCCCORE, 3 phases for VCCGT and 1 phase for VCCSA. For example, output operation as a 4+3+1, 4+2+1, 3+2+1 etc, are supported. The RT3634CJ is designed to meet Intel IMVP9.2 compatible CPUs specification with a serial SVID control interface. The controller offers Multi-Time Programmable (MTP) built-in non-volatile memory (NVM) and $I^2C$ interface to store customized configuration. The RT3634CJ is used in notebook computers or desktop computers.

### Power-ON Sequence

In order to confirm sufficient power supply for proper operation, the VR triggers UVLO if VCC voltage drops below 4.2V (max). UVLO protection shuts down controller and forces high-side MOSFET and low-side MOSFET off. When VCC > 4.45V (max), RT3634CJ issues POR = high and waits for EN signal. After POR = high and EN > 0.7V, controller powers on (Chip Enable = H) and starts VR internal settings, which include internal circuit offset correction and loading the data from the NVM to the configuration registers. It is suggested that the EN signal must be pulled high after the VCC is ready. Users can set multi-functions through the configuration registers by $I^2C$ interface. Figure 2 shows the typical timing of controller power-on. Driver power (PVCC) is strongly suggested to be ready after VCC. This can prevent current from flowing back to VCC from PVCC through the PWMx pin or DRVEN/DRVEN_F pin.

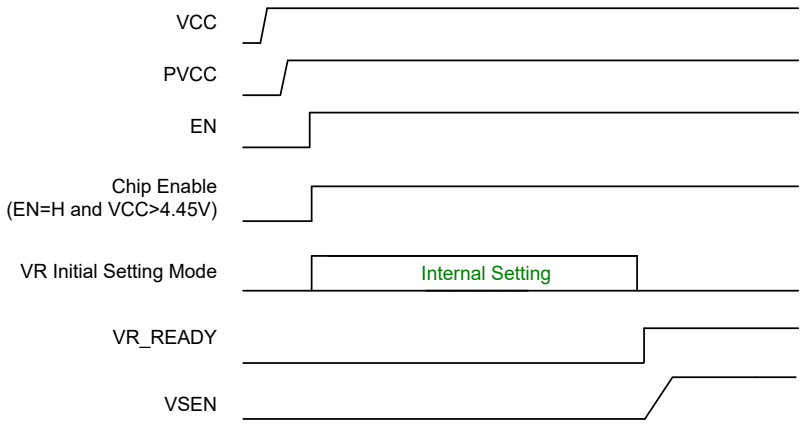


Figure 2. Typical Timing of Controller Power-ON

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### Maximum Active Phases Number Setting

The number of active phases is determined by ISENxP voltages. The detection is only active and latched at Chip Enable rising edge (EN = H and VCC > 4.45V). While voltage at ISENxP > (VCC − 0.5V), maximum active phase number is (x-1). For example, pulling ISEN4P to VCC programs a 3-phase operation, while pulling ISEN3P to VCC programs a 2-phase operation.

The unused ISENxN pins are recommended to be connect to VCC or be floating for the application with DCR current sensing. The unused PWMx pins are recommended to be floating. Figure 3 shows the example of the 3-phase operation in DCR current sense application. For the smart power stage (SPS) application, the unused ISENxN pins must be floating.

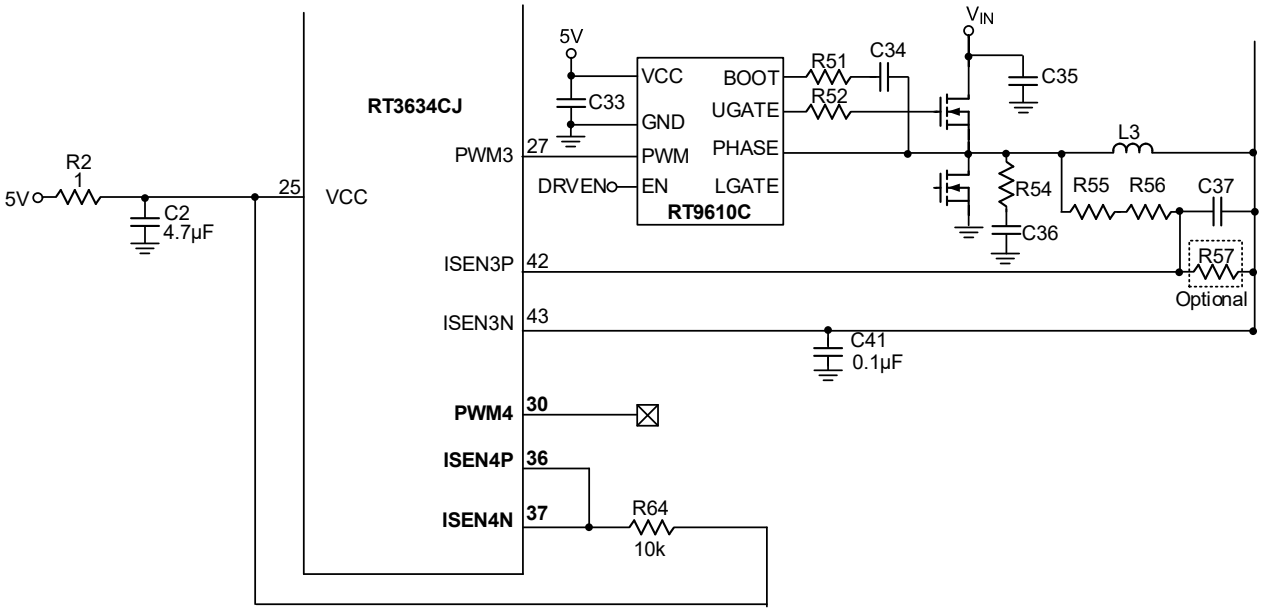


Figure 3. 3-Phase Operation Setting

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### Rail Disable

Pulling ISENA1P to VCC disables Rail A. It is recommended to connect the unused ISENAxN pins to VCC, and the unused PWMAx pins can be floating. Pulling ISENB1P to VCC disables Rail B. It is recommended to connect the unused ISENBxN pins to VCC, and the unused PWMBx pins can be floating. Pulling ISENCP to VCC disables Rail C. It is recommended to connect the unused ISENCN pin to VCC, and the unused PWMC pins can be floating. Pulling the PSYS pin to (VCC – 0.5V) disables input power domain rail D. RT3634CJ rejects any commands to the input power domain rail. It is recommended to connect the unused ISENDP pin and ISENDN pin to VCC.

### Acoustic Noise Suppression

The RT3634CJ supports acoustic noise suppression function for reducing acoustic noise induced by piezoelectric effect from MLCC. As output voltage transition occurs, especially in dynamic VID, the vibrating MLCC produces acoustic noise if the vibrating frequency falls into audible band and the noise level is related to the output voltage transition amplitude ΔV. Therefore, the RT3634CJ adopts acoustic noise suppression function which can be enabled through the configuration register by $I^2C$ protocol interface to reduce ΔV when SetVID down and SetVID Decay down in DEM mode.

### NVM Configuration Mechanism

The RT3634CJ provides multiple parameters for platform setting and BOM optimization. These parameters can be set through the configuration registers via $I^2C$. While POR = high and enable loading NVM command is received, the VR starts loading data from the NVM to the configuration registers and function settings. Once the loading process is done, user configuration and NVM programing are available. Keep EN = L when NVM is programing. When EN > 0.7V, the VR loads the data from NVM again. After loading, VR proceeds internal setting. Figure 4 shows the simplified VR initialization and programing timing diagram. Richtek provides a Microsoft Excel-based design tool for user configuration, including unlocking, page setting and programming, etc. All setting functions are summarized in the section of Functional Register Description.

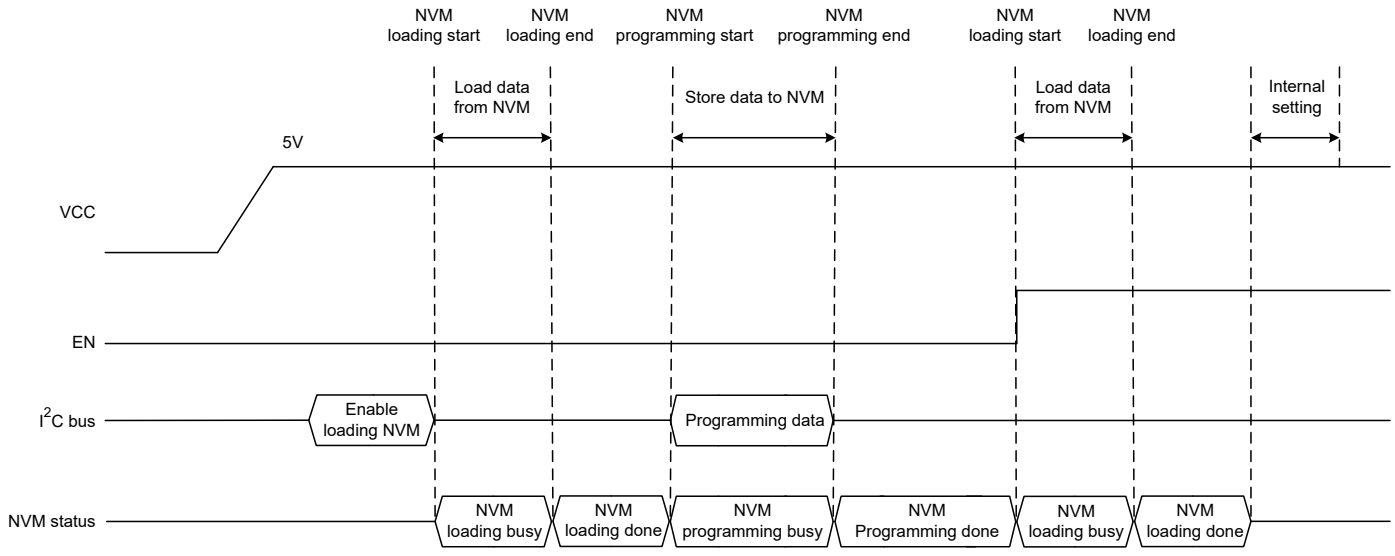


Figure 4. Simplified VR Initialization and Programing Timing Diagram

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### I²C Address Setting

The RT3634CJ provides multiple I²C address to support multiple devices used in I²C interface. Set the I²C address (7-bit and 8-bit format) by the 1% tolerance resistor connected from the pin of NON_ZERO_VBOOT/I2C_ADDR to ground. Resistor value is described in Table 1.

**Table 1. I²C Address Setting (7-bit and 8-bit format)**

| I²C Address (7-bit) | I²C Address (8-bit) | Resistance (kΩ) | | |
|---|---|---|---|---|
| | | Min | Typ | Max |
| 20 | 40 | 1 | 3.4 | 5.76 |
| 21 | 42 | 15.8 | 21 | 26.7 |
| 22 | 44 | 46.4 | 57.6 | 68.1 |
| 23 | 46 | 107 | 118 | 130 |

### Thermal Monitoring and Indicator

TSEN pin is available to process thermal monitoring by either NTC thermistor or temperature monitor (TMON) of the smart power stage (SPS).

When NTC thermistor is used as thermal monitoring, TSEN pin voltage = 80μA x (R1+R2) which is defined as Thermal Voltage where R2 is the NTC thermistor network to sense temperature as shown in Figure 5. The NTC thermistor is recommended to be placed at the hottest point of the VR, and route the feedback path to the controller in the differential pair. Higher temperature causes smaller R2 and lower Thermal Voltage. According to NTC thermistor temperature curve, design Thermal Voltage v.s Temperature with proper R2 network to meet Intel temperature zone. 100°C. Thermal Voltage = 80μA x (R1 + R2 (100°C) = 1.105V and 97°C. Thermal Voltage = 80μA x (R1 + R2 (97°C) = 1.147V must be required. Controller processes the TSEN pin voltage to report to temperature zone register. While the TSEN pin voltage is less than 1.105V, the $\overline{\text{VR_HOT}}$ is pulled low to indicate thermal alert. The signal is an open-drain signal. Thermal Register data is updated every 75μs and average interval is 600μs. The NTC thermistor of the TSEN network is recommend to be 100kΩ/β = 4250 with accuracy less than 1% error. The NTC thermistor of the NCP15WF104F03RC from Murata is suggested. Please refer to the design tool for the more detailed calculation.

When thermal monitoring is implemented by TMON of SPS with positive temperature coefficient, the registers of TSEN_SEL_A, TSEN_SEL_B and TSEN_SEL_C need to be selected as positive temperature coefficient for Rail A, Rail B and Rail C respectively and the TSEN pin operates as an input terminal to receive the TMON output from SPS. The RT3634CJ offers the thermal register of 0.6V at 0°C and 1.4 V at 100°C with 8 mV/°C typical slope.

$$\text{Temp.}(°C) = \frac{V_{TMON} - 0.6V}{8mV/°C}$$

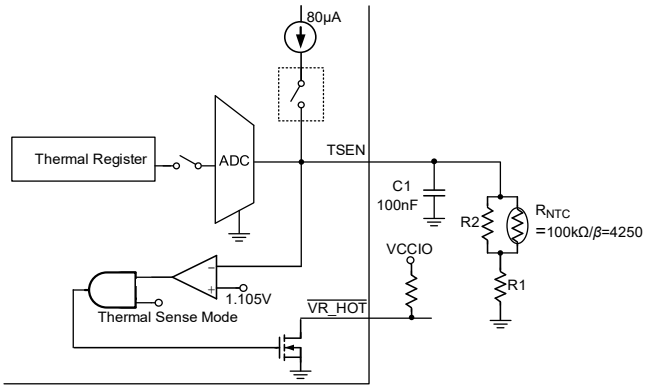


Figure 5. Thermal Monitoring by NTC Thermistor

### System Input Power Monitoring (PSYS)

The RT3634CJ provides PSYS function to monitor total platform system power and report to the CPU via SVID interface. The PSYS function is illustrated in Figure 6. PSYS meter measures system input current and outputs a proportional current signal IPSYS. RPSYS is designed for the PSYS voltage = 1.6V with maximum IPSYS for 100% system input power. The PSYS threshold can be set through SVID interface with 1.6V full-scale analog signal for FFh digitized code. If input power is higher than critical threshold, controller asserts $\overline{\text{VR_HOT}}$.

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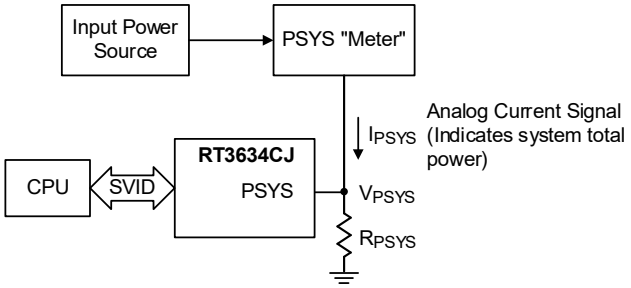


Figure 6. PSYS Function Block Diagram

### System Input Voltage Monitoring (VSYS)

The RT3634CJ provides optional VSYS function to monitor system input voltage. The VSYS threshold can be set through SVID interface and FFh digitized code indicates for 24V input voltage (24V/255 per code). If input voltage is lower than critical threshold, controller asserts $\overline{\text{VR_HOT}}$.

### Zero Load-line

The RT3634CJ can also support enable zero load-line function. When zero load-line function is enabled, the output voltage is determined only by VID and does not vary with the loading current like load-line system behavior. The RT3634CJ adopts AC-droop to effectively suppress load transient ring back and control overshoot for zero load-line application. Figure 7 shows the condition without AC-droop control. The output voltage without AC-droop control has extra ring back ΔV2 due to C area charge. Figure 8 shows the condition with AC-droop control. While loading occurs, controller changes VID target to short-term voltage target temporarily. Short-term voltage target is related to transient loading current $\Delta I_{CC}$ and can be represented as the following:

$$\text{Short_Term_Voltage_Target} = \text{VID} - \Delta I_{CC} \times R_{LL}$$

The setting method of $R_{LL}$ is the same as load-line system. The short-term voltage target reverts to VID target slowly after a period of time. The short-term voltage target can help inductor current not to exceed loading current too much and then the ring back ΔV2 can be suppressed. The overshoot amplitude is reduced to only ΔV3.

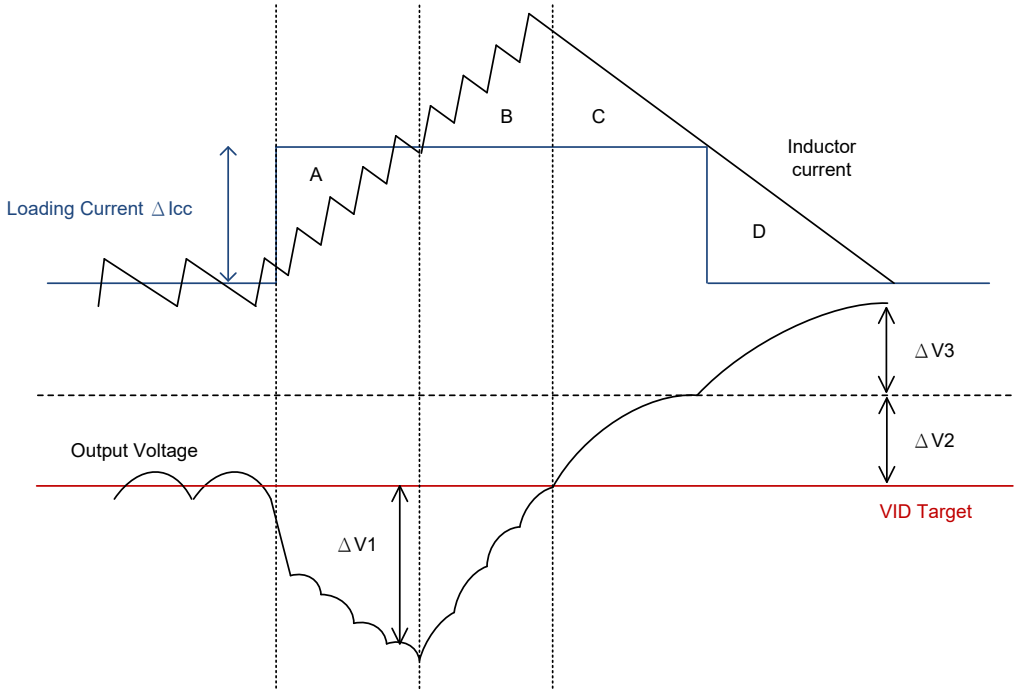


Figure 7. Zero Load-line without AC-droop Control

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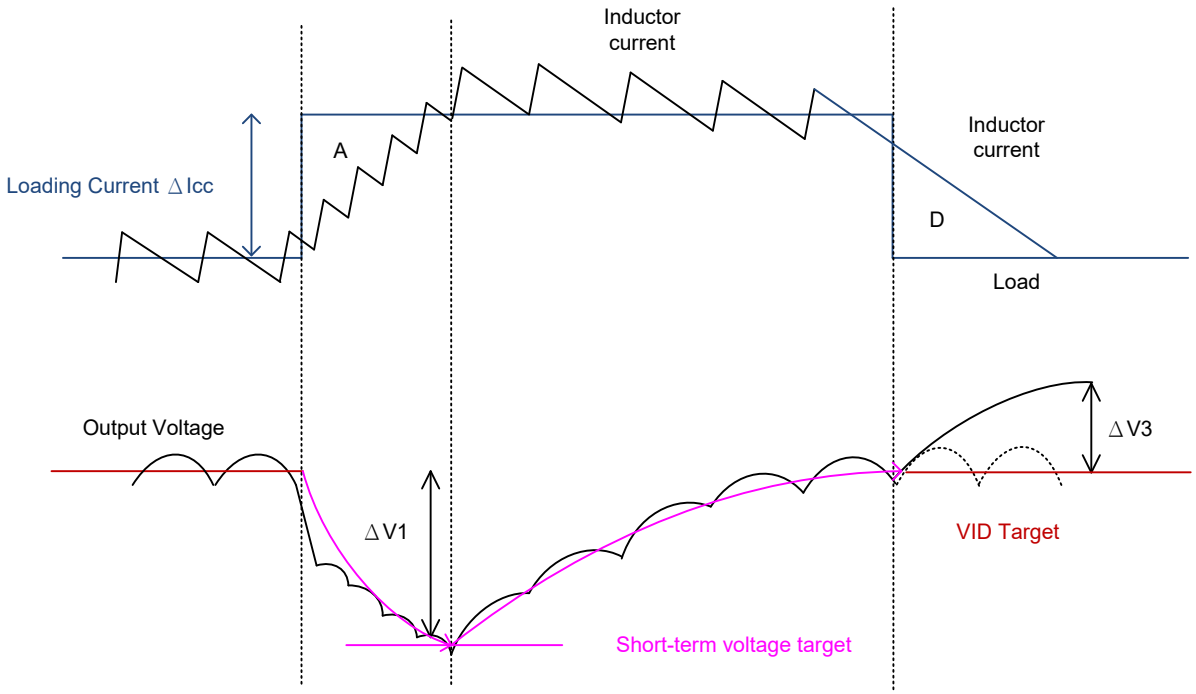


Figure 8. Zero Load-line with AC-droop Control

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### Current Sense

The RT3634CJ supports DCR current sensing report and Smart Power Stage (SPS) current sensing report.

### DCR Current Sense

To achieve higher efficiency, the RT3634CJ adopts inductor DCR current sensing to get each phase current signal, as illustrated in Figure 9. An external low-pass filter $R_{X1}$, $R_{X2}$ and $C_X$ reconstruct the current signal. The low-pass filter time constant ($R_{X1}$//$R_{X2}$) x $C_X$ should match time constant $\frac{L}{DCR}$ of inductance and DCR. It is necessary to fine tune $R_{X1}$, $R_{X2}$ and $C_X$ for transient performance and current reporting. If RC network time constant matches inductor time constant, an ideal load transient waveform can be designed. If RC network time constant is larger than inductor time constant, VSEN waveform has a sluggish droop during load transient. If RC network is smaller than inductor time constant, VSEN waveform sags to create an undershooting to fail the specification and mis-trigger overcurrent protections (sum OCP). Figure 10 shows the output waveforms according to the RC network time constant. The $R_{X1}$ is highly recommended as two 0603 size resistors in series to enhance the $I_{OUT}$ reporting accuracy. The $C_X$ is suggested to be 0.1μF X7R/0603 for low de-rating value at high frequency.

$$I_{CS,PERx} = \frac{V_{CSIN}}{R_{CS}} = \frac{I_{Lx} \times DCR}{R_{CS}}$$

The $R_{X2}$ is optional for prevent $V_{CSIN}$ exceeding current sense amplifier input range. The time constant of ($R_{X1}$//$R_{X2}$) x $C_X$ should match $\frac{L}{DCR}$.

$$I_{CS,PERx} = \frac{V_{CSIN}}{R_{CS}} = \frac{I_{LX} \times DCR}{R_{CS}} \times \frac{R_{X2}}{R_{X1}+R_{X2}}$$

The current signal $I_{CS,PERx}$ is mirrored for load-line control/current reporting, current balance and zero current. The mirrored current to IMON pin is 1.25 time of $I_{CS,PER}$,

$I_{IMONX}$ = $A_{MIRROR}$ x $I_{CS,PERx}$, $A_{MIRROR}$ = 1.25

The current sense lines must be routed as differential pair from the inductor to the controller on the same layer. Proper differential routing of current sense lines will provide accurate current telemetry for current balance, load-line regulation and OCP.

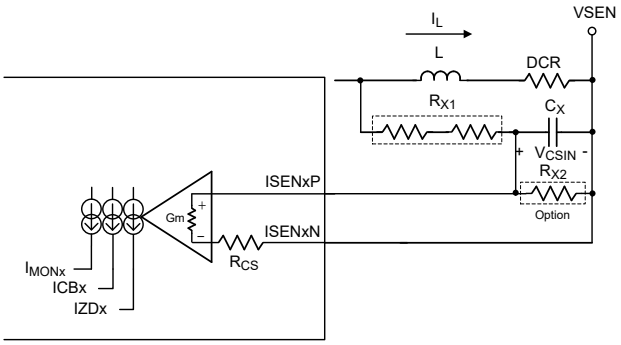


Figure 9. Inductor DCR Current Sensing Method

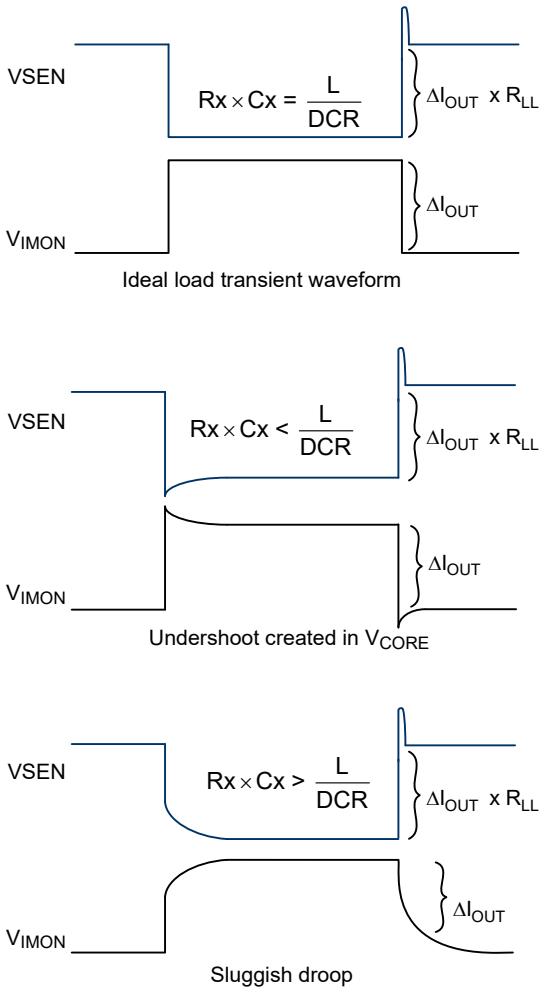


Figure 10. All Kinds of RC Network Time Constant

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All phase current signals are gathered to the IMON pin and converted to a voltage signal $V_{IMON}$ by $R_{IMON,EQ}$ based on the VREF pin. The VREF pin provides 0.6V voltage source (as presented as $V_{VREF}$) during normal operation. The relationship between $V_{IMON}$ and inductor current $I_{LX}$ is:

$$V_{IMON} - V_{VREF} = (I_{L1}+I_{L2}+...) \times \frac{DCR}{1k\Omega} \times A_{MIRROR} \times R_{IMON,EQ}$$

$V_{IMON}$ - $V_{VREF}$ is proportional to output current. $V_{IMON}$ - $V_{VREF}$ is used for output current reporting and load-line loop-control and sum overcurrent protection. For the reporting, $V_{IMON}$ - $V_{VREF}$ is averaged by analog low-pass filter and then coded by 8-bit ADC. The digitized reporting value is scaled as FFh = ICCMAX. The $R_{IMON,EQ}$ should be designed so that $V_{IMON}$ - $V_{VREF}$ = $V_{ICCMAX}$ while ($I_{L1}$+$I_{L2}$+...) = ICCMAX(A) = ICCMAX register value, where $V_{ICCMAX}$ setting for each rail is shown below:

For Rail A/B/C,

$V_{ICCMAX}$ = 0.8V, when ICCMAX ≥ 80A

$V_{ICCMAX}$ = 0.4V, when 80A > ICCMAX ≥ 40A

$V_{ICCMAX}$ = 0.2V, when 40A > ICCMAX

For Rail D,

$V_{ICCMAX}$ = 1.6V for all ICCMAX setting

For load-line loop control, $V_{IMON} - V_{VREF}$ is scaled by Ai, that can be selected by the registers of Ai_A, Ai_B and Ai_C for Rail A, Rail B and Rail C respectively. The detailed application is described in the load-line setting section.

**Smart Power Stage (SPS) Current Sensing Report**

As SPS current sensing report is used, the registers of CS_SEL_A, CS_SEL_B and CS_SEL_C need to be selected for Rail A, Rail B and Rail C respectively. When the register of CS_SEL_A/B/C is selected as SPS, the ISENxN of each phase will be connected internally and the ISEN1N operates as the output terminal which provides the reference voltage of 1.3V for the reference inputs of the SPS. A capacitor of 0.22μF to 1μF is suggested to be connected between ISEN1N and GND. Figure 12 shows the implementation of SPS current sensing report. The $V_{IMON}$ and current reporting from SPS can be calculated as:

$$V_{IMON} - V_{VREF} = (I_{OUT_SPS1} + I_{OUT_SPS2} + ...) \times \frac{R_{SENSE}}{1k\Omega} \times A_{MIRROR} \times R_{IMON}$$

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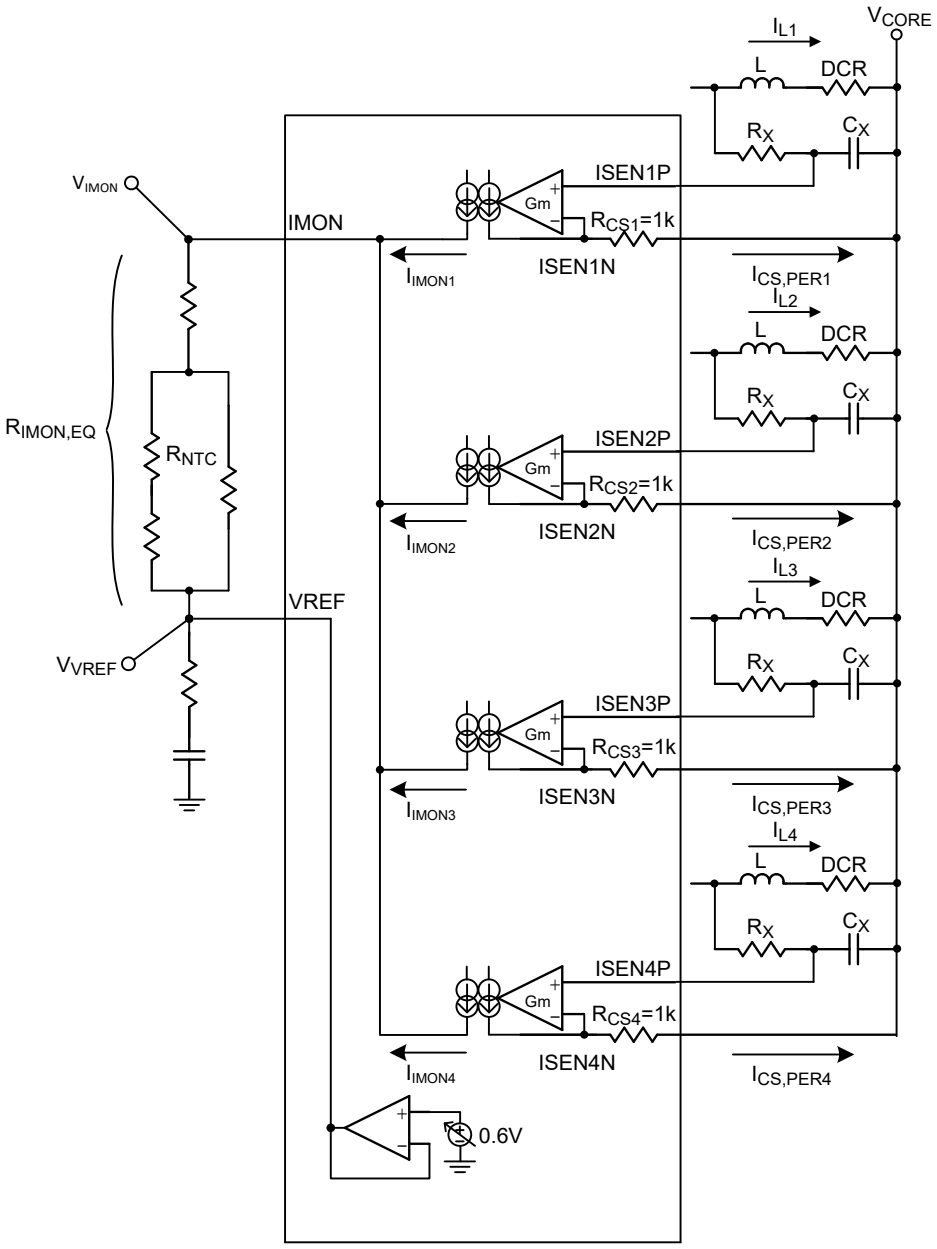


Figure 11. Total Current Sense Method

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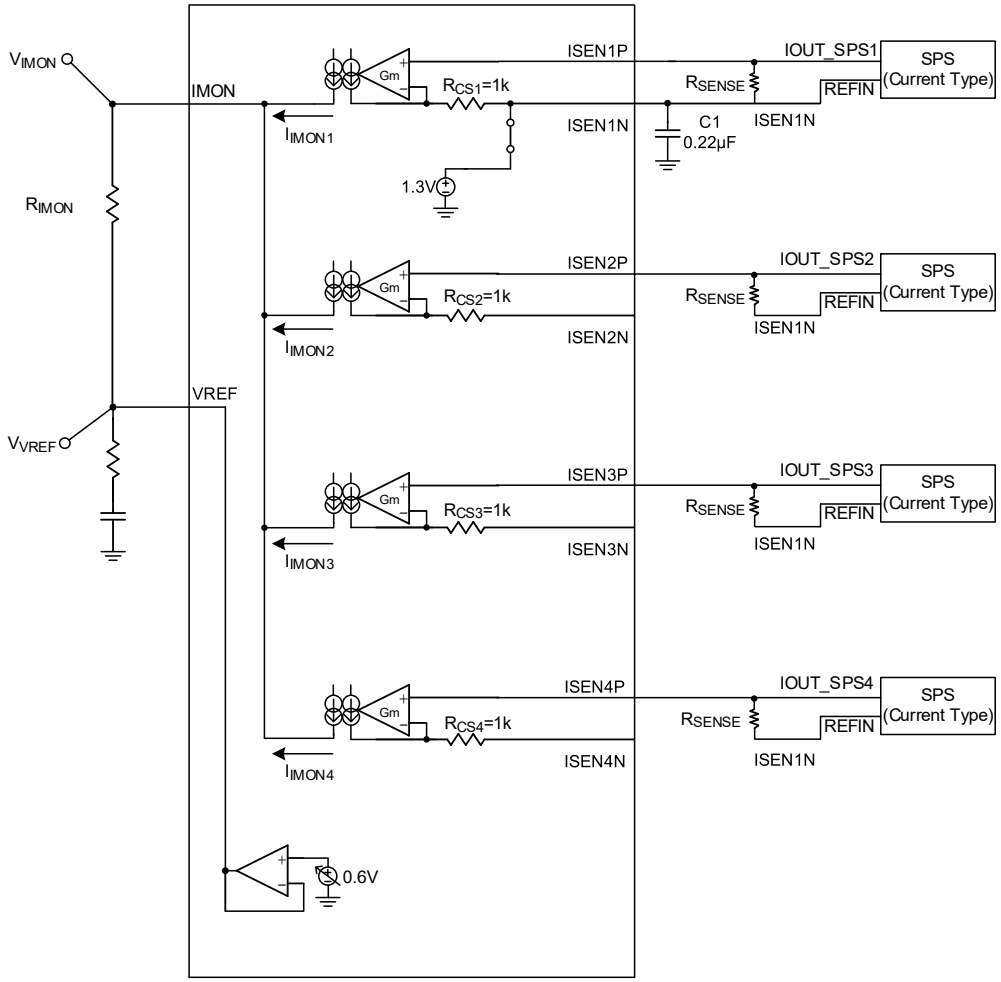


Figure 12. SPS Current Sensing Report

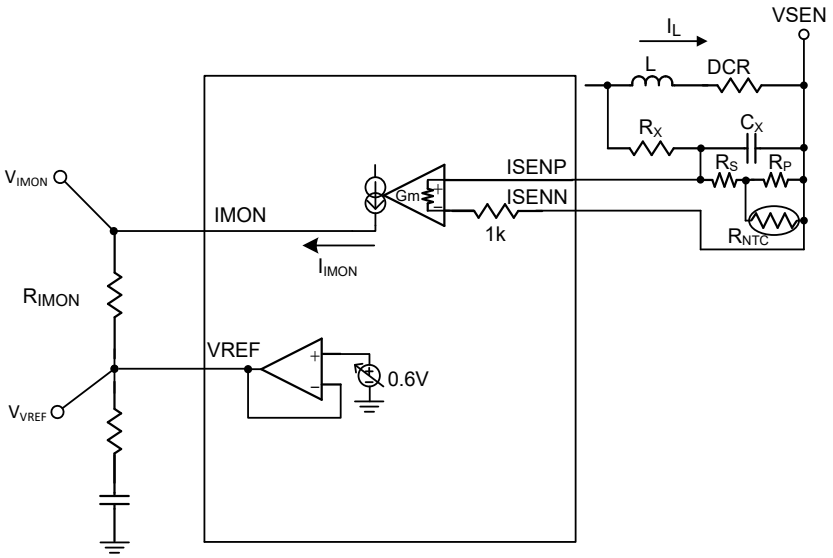


Figure 13. Thermal Compensation method for Single Phase

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### Thermal Compensation for Current Sense

Since the copper wire of inductor has a positive temperature coefficient, temperature compensation is necessary for the lossless inductor current sense. For single phase thermal compensation, Figure 13 shows a simple and effective way to compensate temperature variation for single-phase operation. An NTC thermistor is added in the current sensing network and is suggested to be placed near the inductor of power stage for compensating DCR variation due to temperature change.

The current sense network equation can be derived below:

$$V_{IMON} - V_{VREF} = I_L \times \frac{DCR}{1k\Omega} \times \frac{R_S + R_P // R_{NTC}}{R_X + (R_S + R_P // R_{NTC})} \times A_{MIRROR} \times R_{IMON}$$

Please refer to the design tool for the more detailed calculation.

Above thermal compensation method needs an NTC thermistor for each phase. In order to reduce the number of NTC for multi-phase application, the RT3634CJ adopts a patented total current sense method that requires only one NTC thermistor for thermal compensation. The NTC resistor is designed within $I_{MON}$ resistor network on IMON pin. It is suggested to be placed near the inductor of the first phase. Figure 11 shows the configuration.

$$V_{IMON} - V_{VREF} = (I_{L1} + I_{L2} + ...) \times \frac{DCR}{1k\Omega} \times A_{MIRROR} \times (R_{IMON1} + R_{IMON2} // (R_{NTC} + R_{IMON3}))$$

Please refer to the design tool for the more detailed calculation.

### Load-line Setting ($R_{LL}$)

An output voltage load-line (Adaptive Voltage Positioning) is specified in CPU VR for power saving and output capacitance reduction. The characteristic of load-line is that the output voltage decreases by an amount proportional to the increasing loading current. The slope between output voltage and loading current ($R_{LL}$) is shown in Figure 14. Figure 15 shows the voltage and current loop circuits of the RT3634CJ for the load-line control. The detailed equation is described as below

$$R_{LL} = \frac{\text{Current Loop Gain}}{\text{Voltage Loop Gain}} = \frac{DCR}{1k\Omega} \times A_{MIRROR} \times R_{IMON,EQ} \times \frac{A_i}{\frac{R_{EA2}}{R_{EA1}}} \times \frac{3}{2}$$

, where Ai is current gain and $\frac{R_{EA2}}{R_{EA1}}$ is ERROR AMP gain and suggested to be 1.5~4 for better transient response. $R_{LL}$ can be programmed by Ai which can be selected by the registers of Ai_A, Ai_B and Ai_C for Rail A, Rail B and Rail C respectively, which are all listed in the section of Functional Register Description.

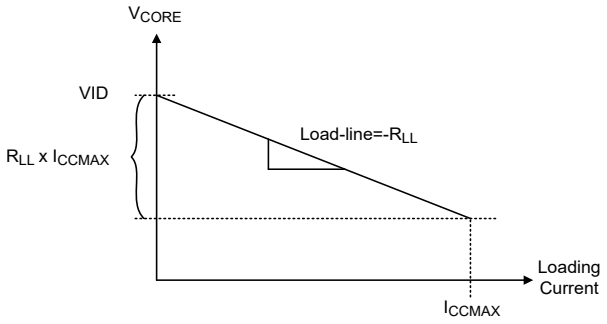


Figure 14. Load-line (Droop)

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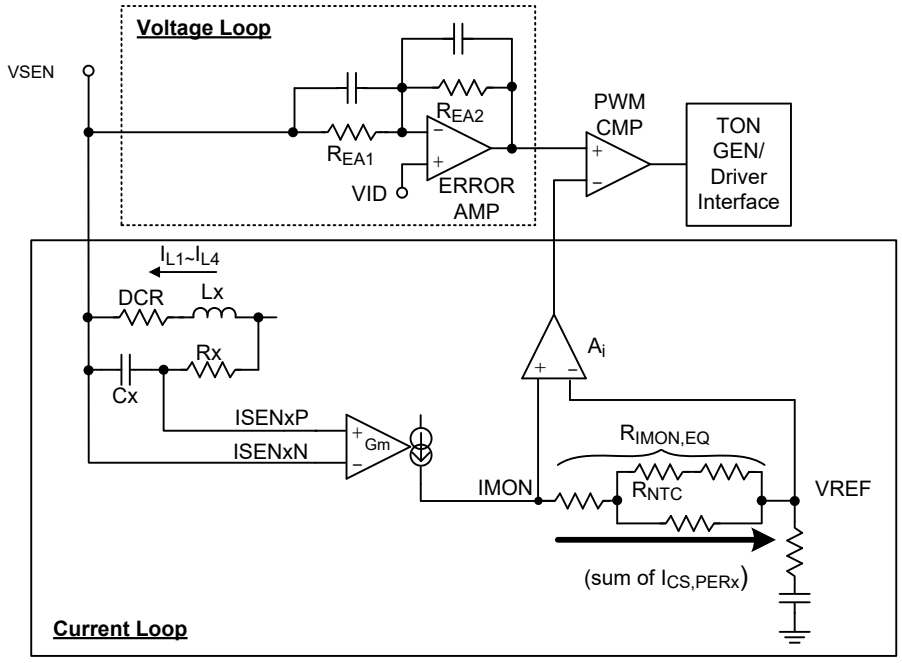


Figure 15. Voltage Loop and Current Loop for Load-line

### Dynamic VID (DVID) Compensation

During DVID up transition, an extra current is required to charge output capacitors for the increasing voltage. The charging current approximates to the product of the DVID slew rate and output capacitance. For droop system, the extra charging current induces extra voltage droop so that the output voltage cannot reach the target within the specified time. The extra voltage drop approximates to DVID Up Slew Rate x Output Capacitance x $R_{LL}$ ($R_{LL}$ is the load-line slope, mΩ). This phenomenon is called droop effect. How charging current affects loop is illustrated in Figure 16. The RT3634CJ provides the DVID up compensation function as shown in Figure 17. An internal current $I_{DVID_LIFT}$ sinks internally from FB pin to generate DVID up compensation, $I_{DVID_LIFT}$ x $R_{EA1}$. $I_{DVID_LIFT}$ for fast DVID up SR can be set from registers of DVID_LIFT_A, DVID_LIFT_B and DVID_LIFT_C for Rail A, Rail B and Rail C respectively. Compensating magnitude can also be adjusted by $R_{EA1}$. When DAC output reaches the target ($\overline{ALERT}$ issue timing), inductor current is still high and needs a time to settle down to the DC loading current. In the settling time, the falling down current keeps charging output capacitor (The magnitude is related with inductor, capacitance and VID). Thus, DVID compensation can be less than DVID Slew Rate x Output Capacitance (capacitance deration should be considered). While output capacitance is so large that DVID compensation cannot cover, adding a resistor and capacitor from FB to GND can also provide similar function. The ERROR AMP compensation (resistance and capacitance network among VSEN, FB and COMP) also affects DVID behavior. The final setting should be based on actual measurement.

As description above, an extra current required to discharge output capacitors for the decreasing voltage during the DVID down transition also affects the output voltage reaching the target within the specified time. How discharging current affects loop is illustrated in Figure 18. The RT3634CJ provides the DVID down compensation function as shown in Figure 19. An internal current $I_{DVID_PULL}$ sources internally to generate DVID down compensation, $I_{DVID_PULL}$ x $R_{EA1}$. $I_{DVID_PULL}$ for fast DVID down SR can be set from registers of DVIDDN_PULL_SEL_A, DVIDDN_PULL_SEL_B and DVIDDN_PULL_SEL_C for Rail A, Rail B and Rail C respectively.

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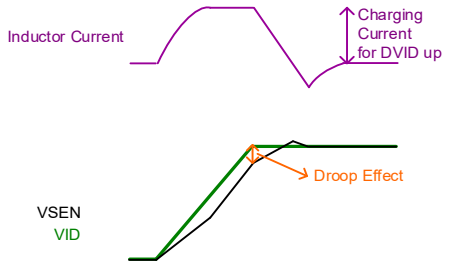


Figure 16. Droop Effect in DVID up Transition

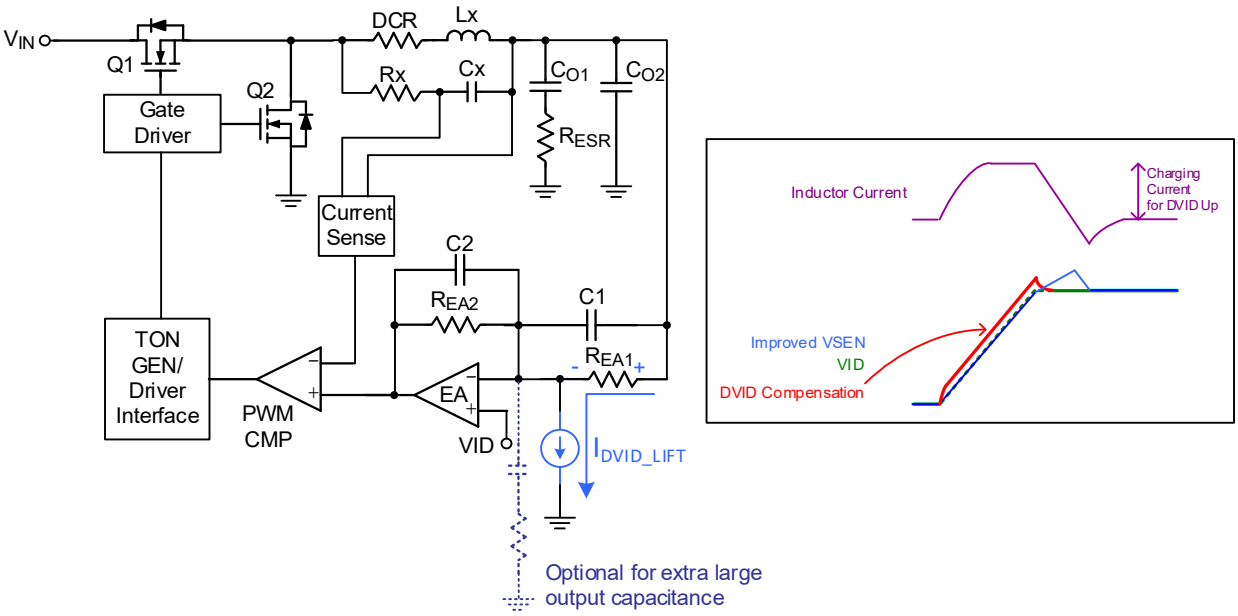


Figure 17. DVID Up Compensation

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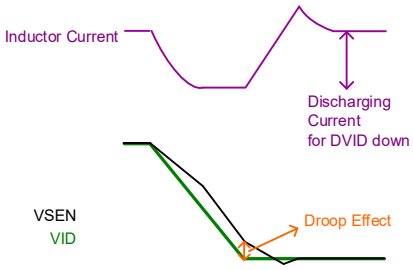


Figure 18. Droop Effect in DVID Down Transition

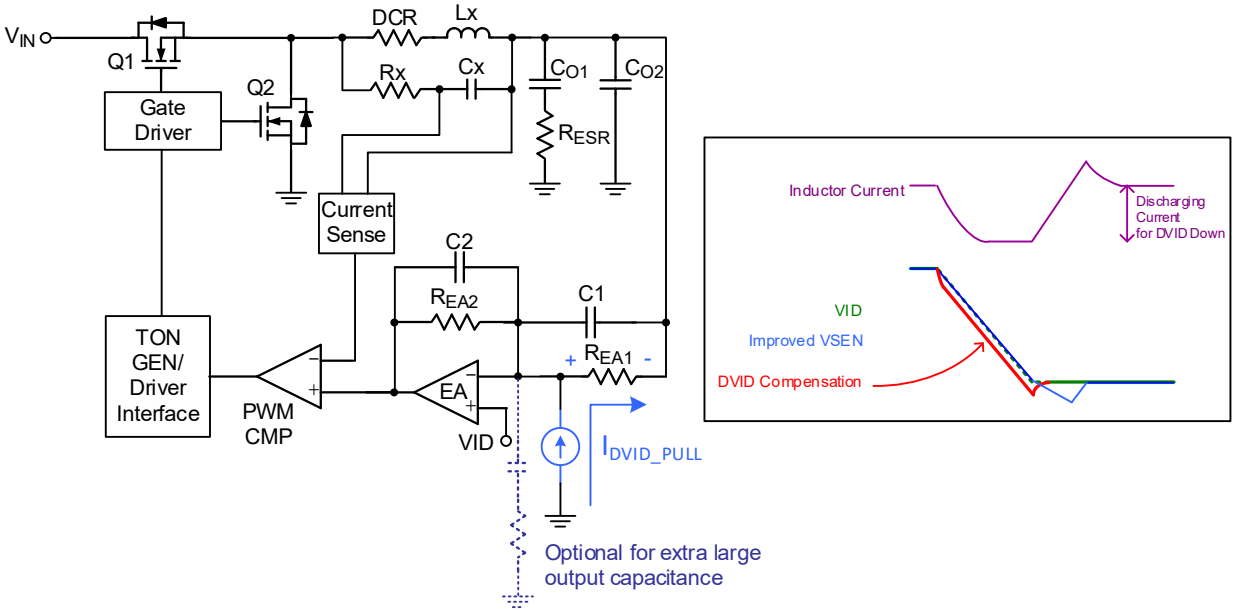


Figure 19. DVID Down Compensation

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### Ripple Compensation during DVID Transition

For better efficiency, the magnitude of output voltage ripple will be different in low VID and high VID condition due to the frequency control. The ripple difference may affect the output voltage reaching the tolerance band in time during DVID slew up and down caused by the DC offset cancellation mechanism, as shown in Figure 20. The RT3634CJ provides the ripple compensation during DVID transition to eliminate the influence of the ripple difference by adding auxiliary compensation current when VID = 0.3V to 0.9V, which is shown in Figure 21. The ripple compensation can be selected from the registers of

SET_RIPPLE_COMP_A,

RIPPLE_COMP_DOUBLE_A,

SET_RIPPLE_COMP_B,

RIPPLE_COMP_DOUBLE_B,

SET_RIPPLE_COMP_C,

RIPPLE_COMP_DOUBLE_C for Rail A, Rail B and Rail C respectively.

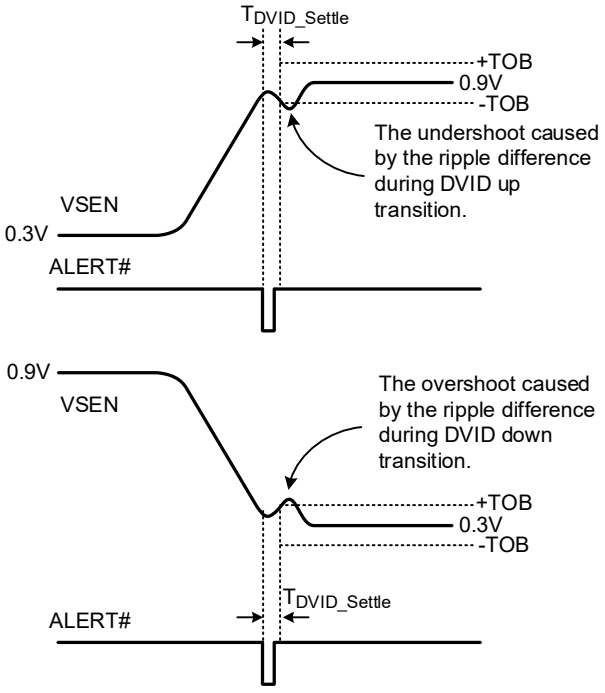


Figure 20. Ripple Difference Effect during DVID Up/Down Transition

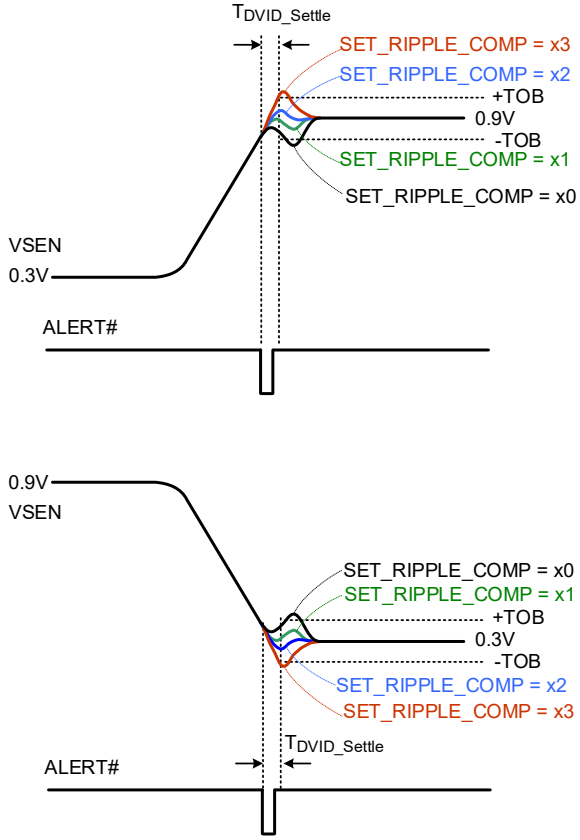


Figure 21. Ripple Compensation during DVID Up/Down Transition

### Compensator Design

The compensator of the RT3634CJ does not need a complex type II or type III compensator to optimize control loop performance. It can adopt a simple type I compensator (one pole, one zero) in the G-NAVP™ topology to fine tune ACLL performance. The one pole and one zero compensator is shown in Figure 22. For IMVP9.2 ACLL specification, it is recommended to adjust compensator according to load transient ring back level. Refer to the design tool for default compensator values.

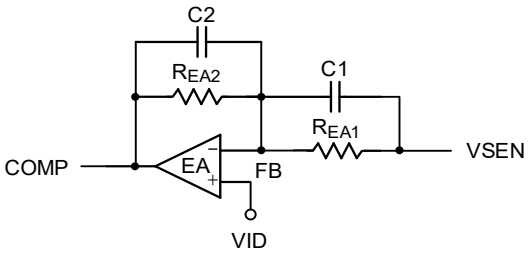


Figure 22. Type I Compensator

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### Differential Remote Sense Setting

The VR provides differential remote-sense inputs to eliminate the effects of voltage drops along the PC board traces, CPU internal power routes and socket contacts. The CPU contains on-die sense pins, $V_{CC_SENSE}$ and $V_{SS_SENSE}$. The related connection is shown in Figure 23. The VID voltage (DAC) is referenced to RGND to provide accurate voltage at remote CPU side. While CPU is not mounted on the system, two resistors of typical 100Ω are required to provide output voltage feedback.

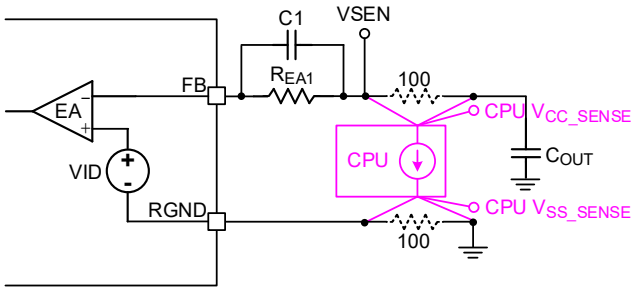


Figure 23. Remote Sensing Circuit

### Switching Frequency Setting

The RT3634CJ G-NAVP™ (Green Native AVP) topology is a current-mode constant on-time control. It generates an adaptive $t_{ON}$ (PWM) with input voltage (VIN) for better line regulation. The $t_{ON}$ is also adaptive to VID voltage to achieve constant frequency concept. The constant switching frequency operation makes the thermal estimation easy. The RT3634CJ provides a parameter setting of $K_{TON}$ to design $T_{ON}$ width. $K_{TON}$ is set by registers of KTON_A, KTON_B and KTON_C for Rail A, Rail B and Rail C respectively. The related setting table is listed in Table 2.

The equations of $t_{ON}$ are listed as below:

$$VID \geq 0.9V$$

$$t_{ON} = \frac{VID}{V_{IN} \times 300000 \times K_{TON}} + 14ns$$

$$VID < 0.9V$$

$$t_{ON} = \frac{0.9V}{V_{IN} \times 300000 \times K_{TON}} + 14ns$$

**Table 2. Function Setting of $K_{TON}$**

| Address / Value | 0x15 [7:4] | 0x15 [3:0] | 0x16 [7:4] |
|---|---|---|---|
| 0000 | KTON_A = 1 | KTON_B = 1 | KTON_C = 1 |
| 0001 | KTON_A = 1.25 | KTON_B = 1.25 | KTON_C = 1.25 |
| 0010 | KTON_A = 1.5 | KTON_B = 1.5 | KTON_C = 1.5 |
| 0011 | KTON_A = 1.75 | KTON_B = 1.75 | KTON_C = 1.75 |
| 0100 | KTON_A = 2 | KTON_B = 2 | KTON_C = 2 |
| 0101 | KTON_A = 2.25 | KTON_B = 2.25 | KTON_C = 2.25 |
| 0110 | KTON_A = 2.5 | KTON_B = 2.5 | KTON_C = 2.5 |
| 0111 | KTON_A = 2.875 | KTON_B = 2.875 | KTON_C = 2.875 |
| 1000 | Reserved | Reserved | Reserved |
| 1001 | Reserved | Reserved | Reserved |
| 1010 | KTON_A = 3 | KTON_B = 3 | KTON_C = 3 |
| 1011 | KTON_A = 3.5 | KTON_B = 3.5 | KTON_C = 3.5 |
| 1100 | KTON_A = 4.25 | KTON_B = 4.25 | KTON_C = 4.25 |
| 1101 | KTON_A = 5 | KTON_B = 5 | KTON_C = 5 |
| 1110 | KTON_A = 5.75 | KTON_B = 5.75 | KTON_C = 5.75 |
| 1111 | KTON_A = 6.75 | KTON_B = 6.75 | KTON_C = 6.75 |

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The switching frequency can be derived from $t_{ON}$ as shown below. The losses in the power stage and driver characteristics are considered.

$$Freq = \frac{VID + \frac{I_{CC}}{N} \times \left( DCR + \frac{R_{ONLS,max}}{n_{LS}} - N \times R_{LL} \right)}{\left[ V_{IN} + \frac{I_{CC}}{N} \times \left( \frac{R_{ONLS,max}}{n_{LS}} - \frac{R_{ONHS,max}}{n_{HS}} \right) \right] \times (t_{ON} - t_D + t_{ON,VAR}) + \frac{I_{CC}}{N} \times \frac{R_{ONLS,max}}{n_{LS}} \times t_D}$$

VID: VID voltage

$V_{IN}$: input voltage

$I_{CC}$: loading current

N: total phase number

$R_{ONHS,max}$: maximum equivalent of the high-side $R_{DS(ON)}$

$n_{HS}$: number of high-side MOSFETs

$R_{ONLS,max}$: maximum equivalent of the low-side $R_{DS(ON)}$

$n_{LS}$: number of low-side MOSFETs.

$t_D$: summation of the high-side MOSFET delay time and rising time

$t_{ONVAR}$: on-time variation value

DCR: the inductor DCR

$R_{LL}$: loadline setting ($\Omega$).

### Adaptive Quick Response (AQR)

The RT3634CJ adopts Adaptive Quick Response (AQR) to optimize transient response. The mechanism is illustrated in Figure 24. Controller detects output voltage drop slew rate. While the slew rate exceeds the AQR threshold, all PWMs turn on for 53.3% of $t_{ON}$. In multi-phase operation, the AQR threshold can be selected through registers of MULTI-PH_QR_A and MULTI-PH_QR_B for Rail A and Rail B. In single-phase operation, the AQR threshold can be selected through registers of 1-PH_QR_A and 1-PH_QR_B for Rail A and Rail B. The AQR threshold are listed in Table 3 and Table 4. The following equation can initially decide the AQR starting trigger threshold. Note that the threshold should be larger than steady-state output voltage ripple falling slew rate and also the overshoot falling slew rate to avoid the accidental trigger of AQR.

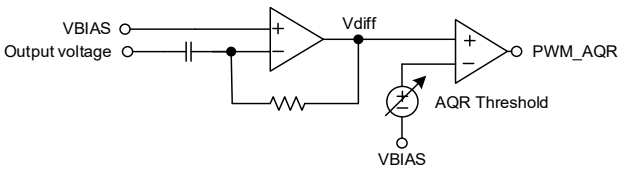


Figure 24. Adaptive Quick Response Mechanism

### Anti-overshoot (ANTI-OVS)

The RT3634CJ provides anti-overshoot function to suppress output voltage overshoot. Controller detects overshoot by signals related to output voltage. The overshoot trigger level can be adjusted by registers of ANTI-OVS_TH_A, ANTI-OVS_TH_B and ANTI-OVS_TH_C for Rail A, Rail B and Rail C rail respectively. The main detecting signal comes from COMP. However, COMP characteristic varies with compensation. Initial trigger level setting is based on the following equation:

$$\Delta COMP \times \frac{4}{3} = \Delta VSEN \times \frac{R_{EA2}}{R_{EA1}} \times \frac{4}{3} > \text{Anti-OVS threshold}$$

The final setting should be determined according to actual Error AMP compensator design and measurement.

While overshoot exceeds the set trigger level, all PWMs keep in tri-state until the zero current is detected or VSEN returns to normal level. Turning off LGs forces positive current flow through body diode to cause diode forward voltage drop. The extra forward voltage can speed up inductor current discharge and decrease overshoot.

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**Table 3. Function Setting of MULTI-PH_QR**

| Address / Value | 0x1B [7:4] | 0x1C [7:4] |
|---|---|---|
| 0000 | MULTI-PH_QR_A = 320 | MULTI-PH_QR_B = 320 |
| 0001 | MULTI-PH_QR_A = 480 | MULTI-PH_QR_B = 480 |
| 0010 | MULTI-PH_QR_A = 640 | MULTI-PH_QR_B = 640 |
| 0011 | MULTI-PH_QR_A = 800 | MULTI-PH_QR_B = 800 |
| 0100 | MULTI-PH_QR_A = 960 | MULTI-PH_QR_B = 960 |
| 0101 | MULTI-PH_QR_A = 1120 | MULTI-PH_QR_B = 1120 |
| 0110 | MULTI-PH_QR_A = 1280 | MULTI-PH_QR_B = 1280 |
| 0111 | Reserved | Reserved |
| 1000 | Reserved | Reserved |
| 1001 | Reserved | Reserved |
| 1010 | Reserved | Reserved |
| 1011 | Reserved | Reserved |
| 1100 | MULTI-PH_QR_A = 1440 | MULTI-PH_QR_B = 1440 |
| 1101 | MULTI-PH_QR_A = 1600 | MULTI-PH_QR_B = 1600 |
| 1110 | MULTI-PH_QR_A = 1760 | MULTI-PH_QR_B = 1760 |
| 1111 | MULTI-PH_QR_A = Disable | MULTI-PH_QR_B = Disable |

**Table 4. Function Setting of 1-PH_QR**

| Address / Value | 0x1B [3:0] | 0x1C [3:0] |
|---|---|---|
| 0000 | 1-PH_QR_ A = 320 | 1-PH_QR_B = 320 |
| 0001 | 1-PH_QR_A = 480 | 1-PH_QR_B = 480 |
| 0010 | 1-PH_QR_A = 640 | 1-PH_QR_B = 640 |
| 0011 | 1-PH_QR_A = 800 | 1-PH_QR_B = 800 |
| 0100 | 1-PH_QR_A = 960 | 1-PH_QR_B = 960 |
| 0101 | 1-PH_QR_A = 1120 | 1-PH_QR_B = 1120 |
| 0110 | 1-PH_QR_A = 1280 | 1-PH_QR_B = 1280 |
| 0111 | Reserved | Reserved |
| 1000 | Reserved | Reserved |
| 1001 | Reserved | Reserved |
| 1010 | Reserved | Reserved |
| 1011 | Reserved | Reserved |
| 1100 | 1-PH_QR_A = 1440 | 1-PH_QR_B = 1440 |
| 1101 | 1-PH_QR_A = 1600 | 1-PH_QR_B = 1600 |
| 1110 | 1-PH_QR_A = 1760 | 1-PH_QR_B = 1760 |
| 1111 | 1-PH_QR_A = Disable | 1-PH_QR_B = Disable |

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### ACLL Performance Enhancement

The RT3634CJ provides another optional function to improve undershoot by applying a positive offset at loading edge. Controller detects the COMP signal and compares it with steady state. While $V_{COMP}$ variation exceeds a threshold, an additional positive offset is added to the output voltage. The undershoot suppression (the adaptive ramp) threshold for multi-phase operation (PS0) can be set through registers of MULTI-PH_AR_TH_A and MULTI-PH_AR_TH_B for Rail A and B respectively. The undershoot suppression (the adaptive ramp) threshold for single-phase operation (PS1) can be set through registers of 1-PH_AR_TH_A, 1-PH_AR_TH_B and 1-PH_AR_TH_C for Rail A, B and C respectively. The smaller index indicates that the detection is triggered easily. The positive offset is related to the compensation.

The ACLL performance enhancement threshold can approximate to $60mV/\frac{V_{EA2}}{V_{EA1}}$. In PS0, the slew rate of $V_{RAMP}$ increases when the $V_{COMP}$ intersects the positive offset in order to send out another on-time earlier to improve undershoot. In PS1, except for the positive offset, an additional 10mV is applied to the DAC and one pulse of PWM is also forced to turn on while the function is triggered. The positive offset is released gradually in about hundred micro-second. Figure 25 and Figure 26 show undershoot suppression behavior in PS0 and PS1. For different platform, the optimized setting is different. The final setting must be based on actual measurement.

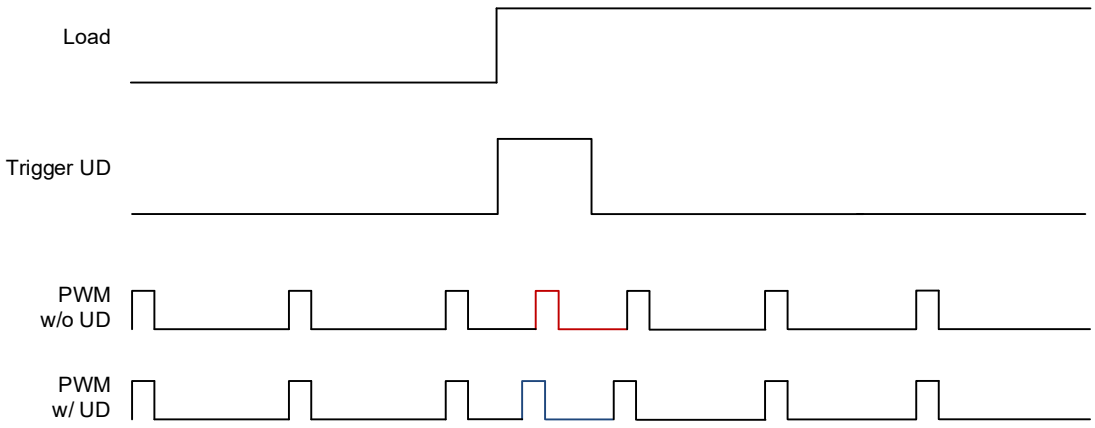


Figure 25. Undershoot Suppression Behavior in Multi-Phase

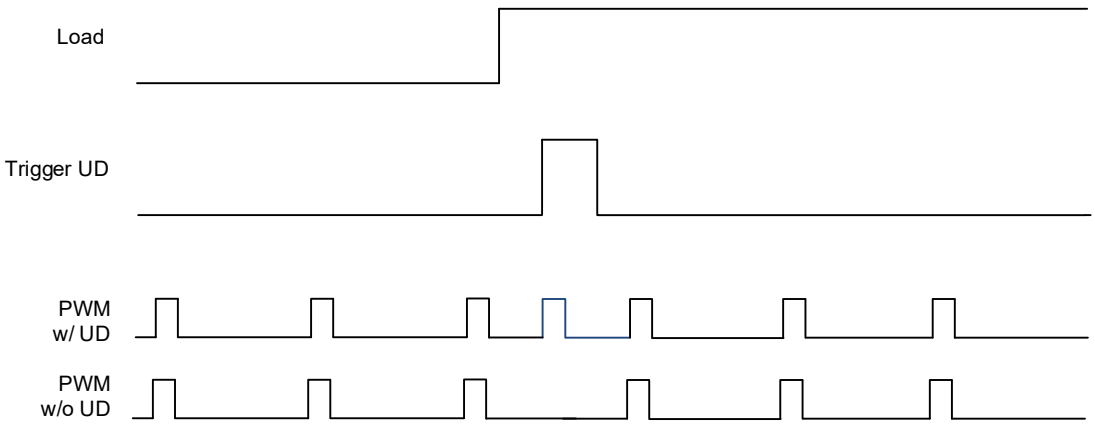


Figure 26. Undershoot Suppression Behavior in Single Phase

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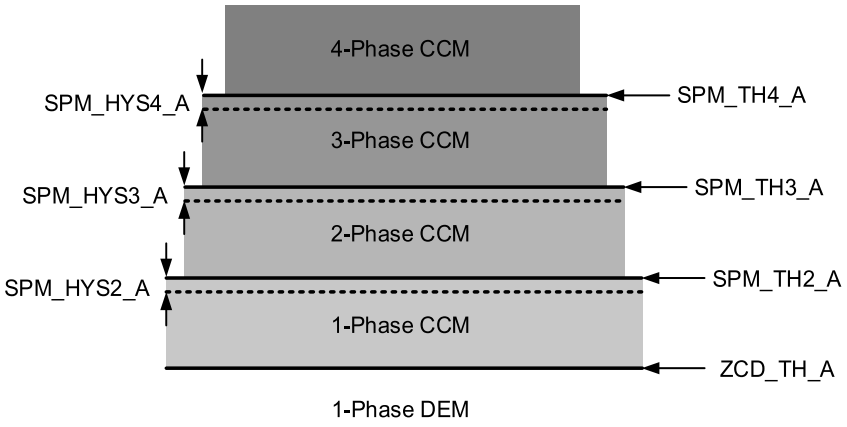
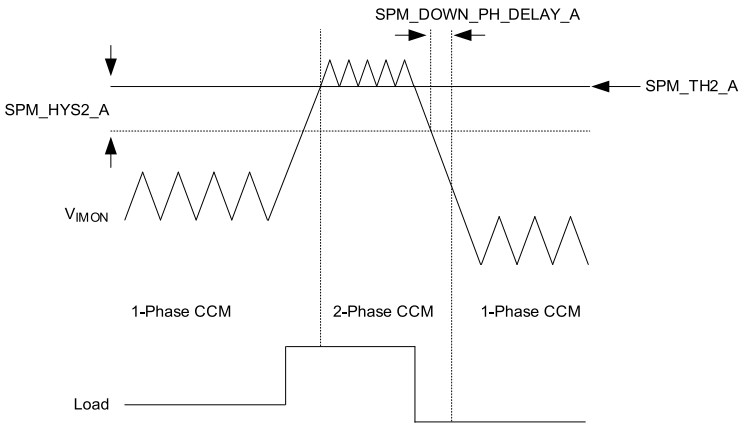
**Smart Phase Management (SPM)**

The RT3634CJ adopts the Smart Phase Management (SPM) to improve light load efficiency and provide the fast phase adding and phase shedding. The SPM function can be enabled and disabled through the NVM registers of EN_SPM_A, EN_SPM_B and EN_SPM_C for Rail A, Rail B and Rail C respectively. The controller compares IMON reporting with threshold and hysteresis of SPM to decide the number of phase adding and phase shedding. The threshold of SPM can be adjusted through the registers of SPM_THx_A (0x36, 0x37) and SPM_THx_B (0x3B) for Rail A and Rail B respectively. For example, set the SPM_TH4_A = 60% of ICCMAX_A to drive the 4-phase operation when the IMON reporting is higher than the 60% of ICCMAX of Rail A. The hysteresis of SPM can be adjusted through the registers of SPM_HYSx_A (0x38, 0x39) and SPM_HYSx_B (0x3C) for Rail A and Rail B respectively. For example, set the SPM_HYS4_A = 5% of ICCMAX_A with SPM_TH4_A = 60% of ICCMAX_A to drive the 3-phase operation when the IMON reporting is less than the 55% (SPM_TH4_A - SPM_HYS4_A) of ICCMAX of Rail A. The controller enters the diode emulation mode (DEM) automatically when the inductor current is lower than the zero current detection threshold (ZCD) when the SPM function is enabled. There is no delay time during phase adding from lower to higher phase number operation. The delay time during the phase shedding from higher to lower phase number operation can be set through the 0x3A[7:6] and 0x3D[7:6] for Rail A and Rail B respectively. In addition to the output current comparison, the RT3634CJ provides three events to operate in full phase immediately. One is DVID up, another is DVID down, the other is the AQR function be triggered during transient response. Figure 27 shows smart phase management mechanism.




(a) Phase Diagram of Smart Phase Management




(b) Phase Adding and Phase Shedding of Smart Phase Management

Figure 27. Smart Phase Management Mechanism

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### Soft-Start Overcurrent Protection (SSOCP)

The RT3634CJ provides soft-start overcurrent protection (SSOCP) during the period of the first-time output ramps up from 0V and 80μs after it is settled. Figure 28 illustrates the mechanism for SSOCP. When the inductor current exceeds the threshold of SSOCP, the controller will turn off both the high-side and low-side MOSFETs immediately, and de-assert VR_READY. The SSOCP threshold is defined as:

When ICCMAX < 40A

$$\Delta V_{SSOCP} = 200mV \cdot \frac{70}{ICCMAX} \cdot \text{phase number;}$$

When 40A ≤ ICCMAX < 80A

$$\Delta V_{SSOCP} = 400mV \cdot \frac{70}{ICCMAX} \cdot \text{phase number;}$$

When ICCMAX ≥ 80A

$$\Delta V_{SSOCP} = 800mV \cdot \frac{70}{ICCMAX} \cdot \text{phase number.}$$

After SSOCP event is removed, the controller can be restarted by toggling VCC power or EN pin.

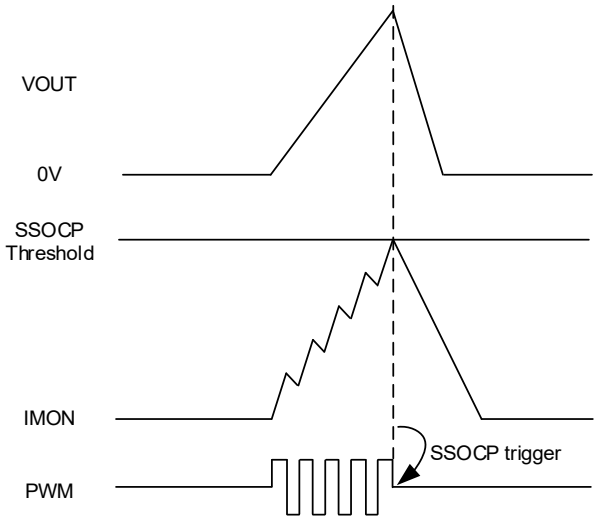


Figure 28. Soft-Start Overcurrent Protection Mechanism

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### Overcurrent Protection (OCP)

The RT3634CJ has sum OCP mechanisms and the threshold of sum OCP for PS0 is defined as:

$$I_{SUM_OC,PS0} = K_{SOCP} \times VIMON_{ICCMAX} \times \frac{1k\Omega}{DCR} \times \frac{1}{A_{MIRROR}} \times \frac{1}{R_{IMON,EQ}}$$

$$I_{SUM_OC,PS1,2,3} = K_{SOCP1} \times VIMON_{ICCMAX} \times \frac{1k\Omega}{DCR} \times \frac{1}{A_{MIRROR}} \times \frac{1}{R_{IMON,EQ}}$$

ICCMAX >= 40, $K_{SOCP} = 1.3$,

$$K_{SOCP1} = \frac{1.3}{\text{phase number}}$$

ICCMAX < 40, $K_{SOCP} = K_{SOCP1} = 1.6$

While $R_{IMON,EQ}$ is designed exactly to meet

$$VIMON_{ICCMAX} = \text{ICCMAX registe value} \times A_{MIRROR} \times \frac{DCR}{1k\Omega} \times R_{IMON,EQ}$$

ICCMAX register value = ICCMAX and $VIMON_{ICCMAX}$ = 0.2V, 0.4V or 0.8V according to ICCMAX.

Sum OCP threshold can be simplified as $I_{SUM_OC,PS0} = K_{SOCP}$ x ICCMAX and $I_{SUM_OC,PS1,2,3} = K_{SOCP1}$ x ICCMAX. Note that the modification of ICCMAX register value cannot change sum OCP threshold.

While inductor current above sum OCP threshold lasts 40µs, controller de-asserts VR_READY and latches PWM in tri-state to turn off high-side and low-side power MOSFETs. Sum OCP is masked during DVID period plus 80µs after VID settles. It is also masked when VID = 0V condition.

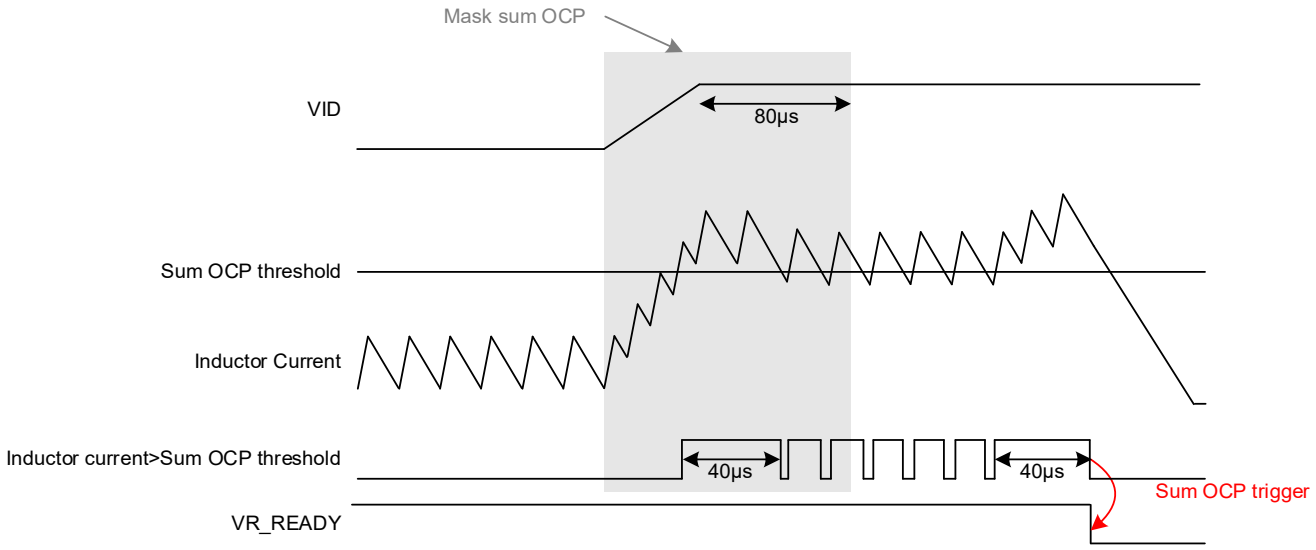


Figure 29. SUM OC Protection Mechanism

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### Overvoltage Protection (OVP)

The OVP threshold is linked with VID. The classification table is illustrated in Table 5. While VID = 0V, OVP is masked. When VID ramps up from VID = 0V till the first PWM after VID settles, OVP threshold is 2.45V to allow not-fully-discharged VSEN. Otherwise, the OVP threshold is relative to VID and equals to VID+350mV with minimum limit = 1.35V. While VID ≤ 1V, the OVP threshold is limited at 1.35V.

The OV protection mechanism is illustrated in Figure 30 and Figure 31. When OVP is triggered with 0.5μs filter time, controller de-asserts VR_READY and forces all PWMs low to turn on low-side power MOSFETs. PWM remains low until the output voltage is pulled down to below 2.1V for DVID up from 0V and below VID for other conditions. After 60μs from OVP trigger, VID starts to ramp down to 0V with slow slew rate. During the period, PWM is not allowed to turn on. Controller controls PWM to be low or tri-state to pull down the output voltage along with VID.

**Table 5. Summary of Overvoltage Protection**

| VID Condition | OVP Threshold | Example | Protection Flag | Protection Action | Protection Reset |
|---|---|---|---|---|---|
| VID = 0 | OVP is masked. | | VREF = 1V | | VCC/EN Toggle |
| DVID up period from 0V to 1st PWM pulse after VID settles | 2.45V | | | VR_READY latched low. The output voltage is pulled down to below 2.1V and then ramps down to 0V. | |
| DVID period from non-zero VID | VID+350mV if VID > 1.0V, 1.35V if VID ≤ 1.0V | VID = 1.2V, OVP threshold = 1.55V<br>VID = 0.9V, OVP threshold = 1.35V | | VR_READY latched low. The output voltage is pulled down to below VID and then ramps down to 0V. | |
| VID≠0 | VID+350mV if VID > 1.0V, 1.35V if VID ≤ 1.0V | VID = 1.2V, OVP threshold = 1.55V<br>VID = 0.9V, OVP threshold = 1.35V | | | |

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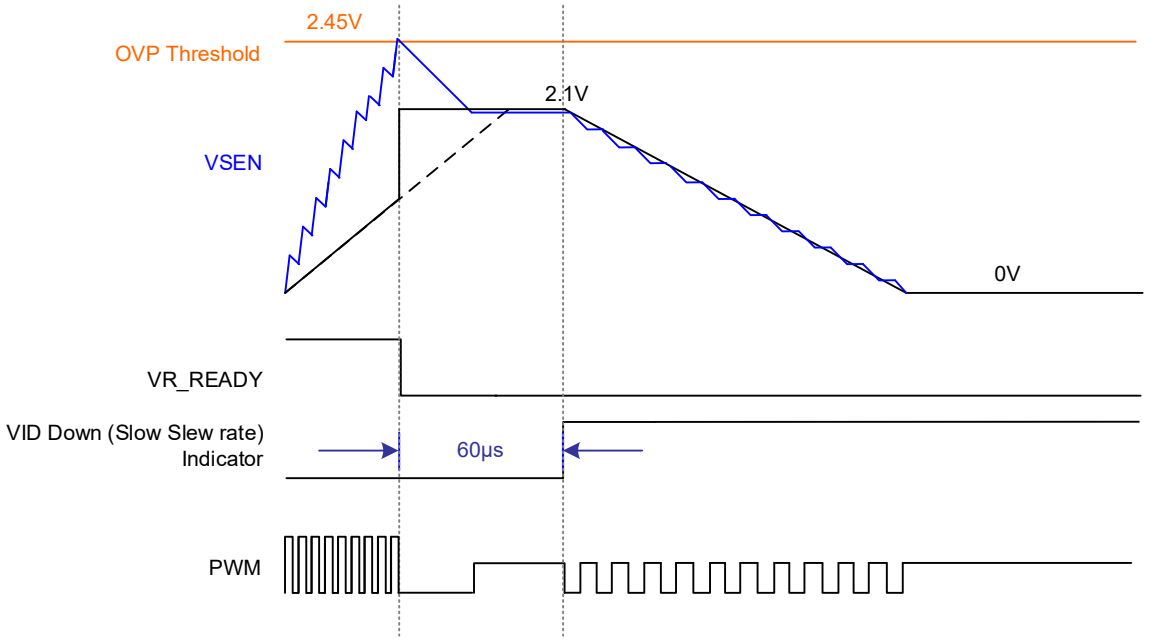


Figure 30. Overvoltage Protection Mechanism for DVID up from 0V

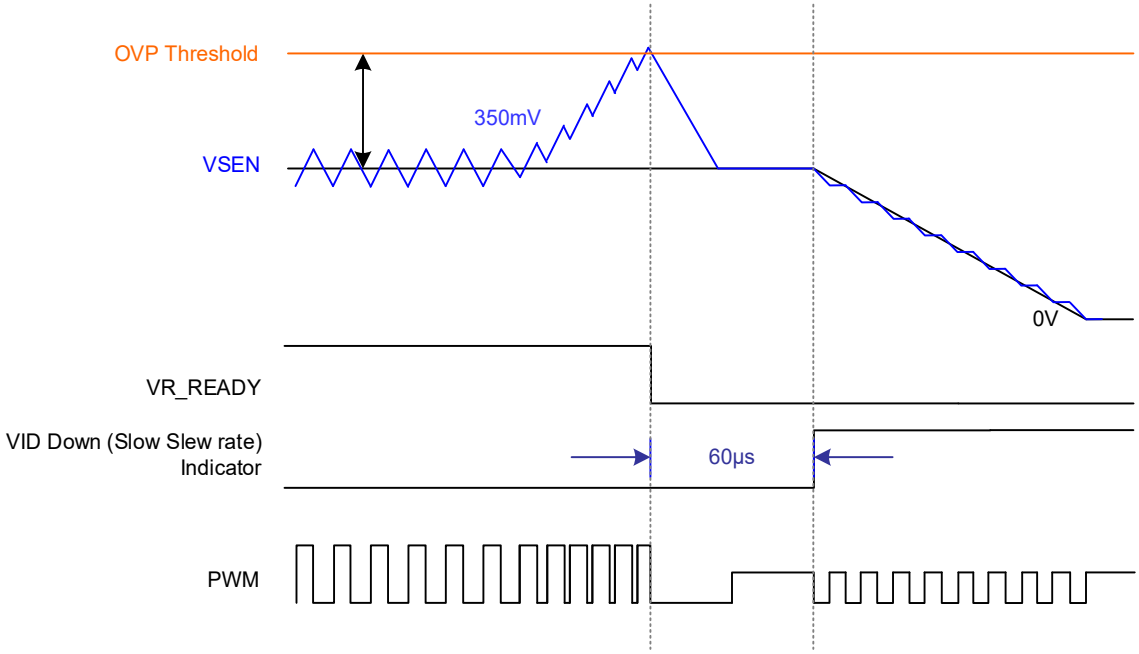


Figure 31. Overvoltage Protection Mechanism

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### Undervoltage Protection

When the output voltage is lower than VID-650mV with 3μs filter time, UVP is triggered and VR_READY is de-asserted and all PWMs are in tri-state to turn off high-side and low-side power MOSFETs. UVP is masked during DVID period and 80μs after VID settles. The mechanism is illustrated in Figure 32.

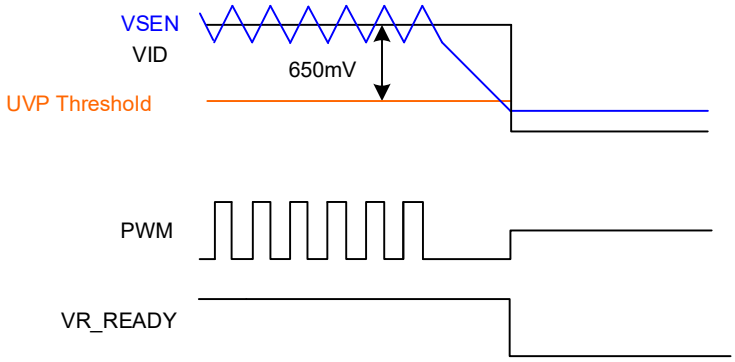


Figure 32. Undervoltage Protection Mechanism

All protections are reset only by VCC/EN toggle. UVP and OCP protections are listed in Table 6. Note that the real filter time also depends on the magnitude of detected signal. The signal magnitude affects analog comparator's overdrive voltage and output slew rate.

The RT3634CJ provides protection flag to promptly determine which kind of protections is triggered. As protection happens, VREF is forced to be 1V/1.5V/2V for OVP/UVP/SUM_OCP, respectively.

**Table 6. Summary of UVP and OCP Protection**

| Protection Type | Protection Threshold | Protection Flag | Protection Action | DVID Mask Time | Protection Reset |
|---|---|---|---|---|---|
| SSOCP | When ICCMAX< 40A<br>$\Delta V_{SSOCP} = 200mV \cdot \frac{70}{ICCMAX} \cdot$phase number;<br>When 40A ≤ ICCMAX < 80A<br>$\Delta V_{SSOCP} = 400mV \cdot \frac{70}{ICCMAX} \cdot$phase number;<br>When ICCMAX ≥ 80A<br>$\Delta V_{SSOCP} = 800mV \cdot \frac{70}{ICCMAX} \cdot$phase number. | VREF = 2V | PWM tri-state, VR_READY latched low | After the period of the first-time DVID up from 0V and 80μs after it is settled | VCC/EN Toggle |
| Sum OCP for PS0 | $I_{SUM_OC,PS0} = K_{SOCP} \times VIMON_{ICCMAX} \times \frac{R_{CSx}}{DCR} \times \frac{1}{R_{IMON,EQ}}$ | VREF = 2V | | DVID+80μs | |
| Sum OCP for non PS0 | $I_{SUM_OC,PS1,2,3} = K_{SOCP1} \times VIMON_{ICCMAX} \times \frac{R_{CSx}}{DCR} \times \frac{1}{R_{IMON,EQ}}$ | VREF = 2V | | | |
| UVP | VID-650mV | VREF = 1.5V | | | |

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### Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, $T_A$ is the ambient temperature, and $\theta_{JA}$ is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, $\theta_{JA}$, is highly package dependent. For a WQFN-60L 7x7 package, the thermal resistance, $\theta_{JA}$, is 25.5°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at $T_A$ = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C – 25°C)/(25.5°C/W) = 3.92W for a WQFN-60L 7x7 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, $\theta_{JA}$. The derating curves in Figure 33 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

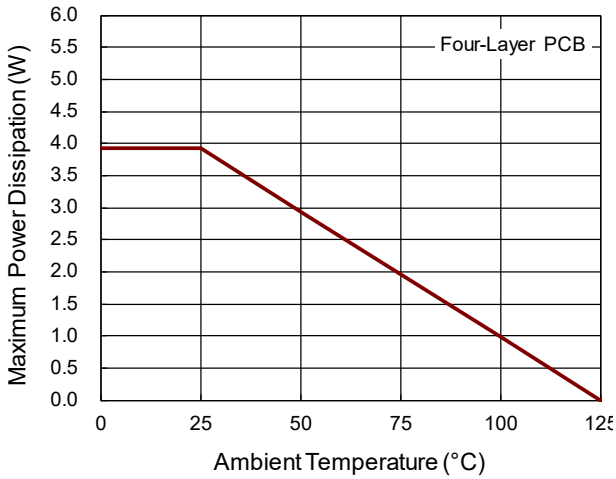


Figure 33. Derating Curve of Maximum Power Dissipation

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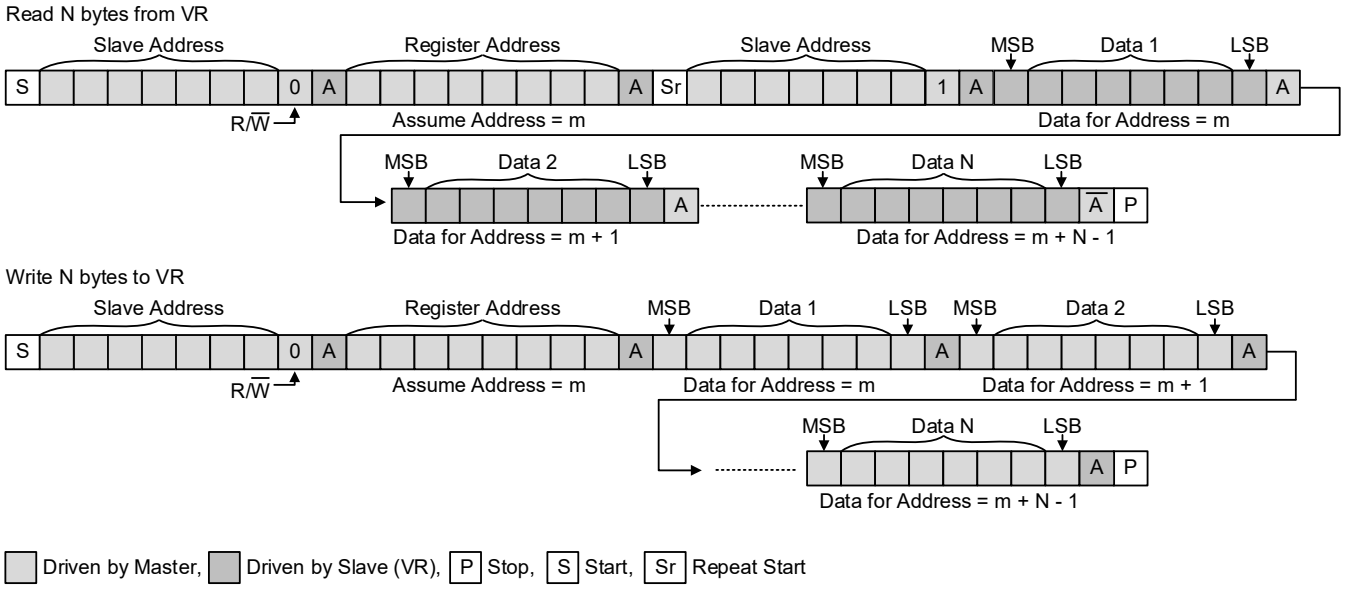
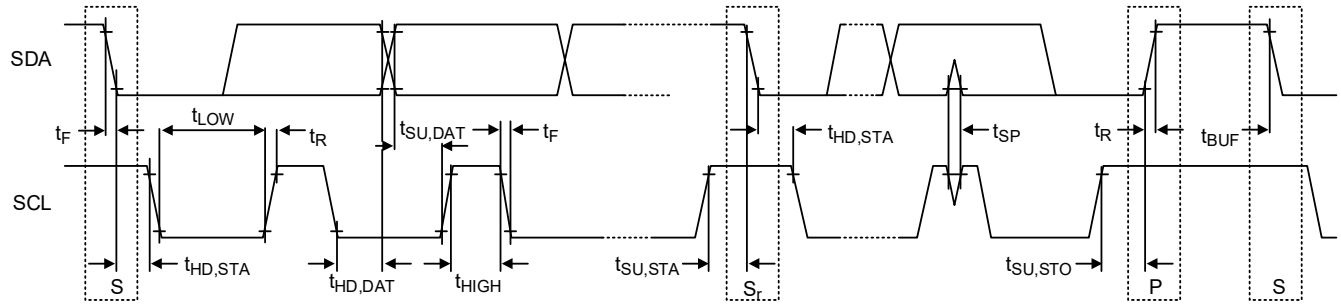
## Functional Register Description

The I$^2$C slave address = 0x20 to 0x23.

This I$^2$C does not have a stretch function.

The I$^2$C interface supports standard slave mode (100kbps), and fast mode (400kbps). The write or read bit stream (N > 1) is shown below:

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All reserved bit(s) must be kept at their default values.

**Table 7. Register List**

| Page | Address | Register Name | Default | Type | Paged | NVM |
|---|---|---|---|---|---|---|
| 0x82 | 0x00 | DVID_COMP_MT_A | 0x4C | RW | Yes | Yes |
| 0x82 | 0x01 | DVID_COMP_MT_B | 0xC4 | RW | Yes | Yes |
| 0x82 | 0x02 | DVID_COMP_MT_C | 0xC2 | RW | Yes | Yes |
| 0x82 | 0x03 | LGON_RIP_COMP_A | 0x80 | RW | Yes | Yes |
| 0x82 | 0x04 | LGON_RIP_COMP_B | 0x00 | RW | Yes | Yes |
| 0x82 | 0x05 | LGON_RIP_COMP_C | 0x80 | RW | Yes | Yes |
| 0x82 | 0x06 | MT_FVM_UVP | 0x21 | RW | Yes | Yes |
| 0x82 | 0x07 | TSEN_SEL | 0x10 | RW | Yes | Yes |
| 0x82 | 0x08 | FVM_NON_OVERLAP | 0x00 | RW | Yes | Yes |
| 0x82 | 0x09 | SPM_1PH_AR_AB_SLL_C | 0x27 | RW | Yes | Yes |
| 0x82 | 0x0A | MT_RIP_COMP_AB | 0x00 | RW | Yes | Yes |
| 0x82 | 0x10 | ICCMAX_A | 0xB0 | RW | Yes | Yes |
| 0x82 | 0x11 | ICCMAX_ADD_VBOOT_SR | 0x22 | RW | Yes | Yes |
| 0x82 | 0x12 | ICCMAX_B | 0x51 | RW | Yes | Yes |
| 0x82 | 0x13 | ICCMAX_C | 0x28 | RW | Yes | Yes |
| 0x82 | 0x14 | VIDT_0LL | 0x00 | RW | Yes | Yes |
| 0x82 | 0x15 | KTON_AB | 0x34 | RW | Yes | Yes |
| 0x82 | 0x16 | KTON_C_Ai_AB | 0x3F | RW | Yes | Yes |
| 0x82 | 0x17 | Ai_BC_EN_SPM | 0xAF | RW | Yes | Yes |
| 0x82 | 0x18 | DBLR_PH_CS_SEL | 0x00 | RW | Yes | Yes |
| 0x82 | 0x19 | ICCMAX_D | 0x20 | RW | Yes | Yes |
| 0x82 | 0x1A | ANTI_OVS_SLL_A | 0xC0 | RW | Yes | Yes |
| 0x82 | 0x1B | QR_TH_A | 0x21 | RW | Yes | Yes |
| 0x82 | 0x1C | QR_TH_B | 0x55 | RW | Yes | Yes |
| 0x82 | 0x1D | AR_TH_AB | 0xB6 | RW | Yes | Yes |
| 0x82 | 0x1E | AR_TH_C_ZCD_AB | 0xE0 | RW | Yes | Yes |
| 0x82 | 0x1F | ZCD_C_ICCMAX_ADD_D_SLL_B | 0x02 | RW | Yes | Yes |
| 0x82 | 0x20 | LPF_INITIAL_AB | 0x11 | RW | Yes | Yes |
| 0x82 | 0x21 | RT_SPS_DBLR_SPM_FVM_HLPF_LPF_INT_C | 0x3E | RW | Yes | Yes |
| 0x82 | 0x22 | DVID_LIFT_AB | 0x54 | RW | Yes | Yes |
| 0x82 | 0x23 | DVID_LIFT_C | 0x32 | RW | Yes | Yes |
| 0x82 | 0x24 | PSYS_PWM_TRI_0V_DVID | 0x05 | RW | Yes | Yes |
| 0x82 | 0x25 | ACLL_LPF_TSEN_POS_OFST_A | 0xE0 | RW | Yes | Yes |
| 0x82 | 0x26 | ACLL_LPF_TSEN_POS_OFST_B | 0x20 | RW | Yes | Yes |
| 0x82 | 0x27 | ACLL_LPF_TSEN_POS_OFST_C | 0x20 | RW | Yes | Yes |

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| Page | Address | Register Name | Default | Type | Paged | NVM |
|---|---|---|---|---|---|---|
| 0x82 | 0x28 | FVM_CTRL_AB | 0x44 | RW | Yes | Yes |
| 0x82 | 0x29 | RESERVED | 0xF8 | RW | Yes | Yes |
| 0x82 | 0x2A | ZCD_HYS_OFST_C | 0xC0 | RW | Yes | Yes |
| 0x82 | 0x2B | EN_RAIL_MAX_PH | 0x42 | RW | Yes | Yes |
| 0x82 | 0x2C | SVID_ADDR | 0x06 | RW | Yes | Yes |
| 0x82 | 0x2D | LPF_LIMIT_AB | 0x8E | RW | Yes | Yes |
| 0x82 | 0x2E | ZCD_HYS_OFST_A | 0x80 | RW | Yes | Yes |
| 0x82 | 0x2F | ZCD_HYS_OFST_B | 0x82 | RW | Yes | Yes |
| 0x82 | 0x30 | VBOOT_VID_A | 0xA1 | RW | Yes | Yes |
| 0x82 | 0x31 | SD_GD_VID_A | 0xA1 | RW | Yes | Yes |
| 0x82 | 0x32 | VBOOT_VID_B | 0xA1 | RW | Yes | Yes |
| 0x82 | 0x33 | SD_GD_VID_B | 0xA1 | RW | Yes | Yes |
| 0x82 | 0x34 | VBOOT_VID_C | 0xA1 | RW | Yes | Yes |
| 0x82 | 0x35 | SD_GD_VID_C | 0xA1 | RW | Yes | Yes |
| 0x82 | 0x36 | SPM_TH_A_1 | 0x79 | RW | Yes | Yes |
| 0x82 | 0x37 | SPM_TH_A_2 | 0xBD | RW | Yes | Yes |
| 0x82 | 0x38 | SPM_HYS_A_1 | 0x12 | RW | Yes | Yes |
| 0x82 | 0x39 | SPM_HYS_A_2 | 0x48 | RW | Yes | Yes |
| 0x82 | 0x3A | SPM_PH_CTRL_A | 0xC1 | RW | Yes | Yes |
| 0x82 | 0x3B | SPM_TH_B | 0x7A | RW | Yes | Yes |
| 0x82 | 0x3C | SPM_HYS_B | 0x24 | RW | Yes | Yes |
| 0x82 | 0x3D | SPM_PH_CTRL_B | 0xC7 | RW | Yes | Yes |
| 0x82 | 0x3E | ANS_EN_SPM_PSK_CTRL | 0x00 | RW | Yes | Yes |
| 0x82 | 0x3F | RESERVED | 0x00 | RW | Yes | Yes |
| 0x82 | 0x40 | RESERVED | 0x00 | RW | Yes | Yes |
| 0x82 | 0x41 | RESERVED | 0x00 | RW | Yes | Yes |
| 0x82 | 0x42 | RESERVED | 0x00 | RW | Yes | Yes |
| 0x82 | 0x43 | RESERVED | 0x00 | RW | Yes | Yes |
| 0x82 | 0x44 | RESERVED | 0x00 | RW | Yes | Yes |
| 0x82 | 0x45 | RESERVED | 0x00 | RW | Yes | Yes |
| 0x82 | 0x46 | RESERVED | 0x00 | RW | Yes | Yes |
| 0x82 | 0x47 | RESERVED | 0x00 | RW | Yes | Yes |
| 0x82 | 0x48 | RESERVED | 0x00 | RW | Yes | Yes |
| 0x82 | 0x49 | RESERVED | 0x00 | RW | Yes | Yes |
| 0x82 | 0x4A | RESERVED | 0x00 | RW | Yes | Yes |
| 0x82 | 0x4B | RESERVED | 0x00 | RW | Yes | Yes |
| 0x82 | 0x4C | RESERVED | 0x00 | RW | Yes | Yes |
| 0x82 | 0x4D | RESERVED | 0x00 | RW | Yes | Yes |

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| Page | Address | Register Name | Default | Type | Paged | NVM |
|---|---|---|---|---|---|---|
| 0x82 | 0x4E | RESERVED | 0x00 | RW | Yes | Yes |
| 0x82 | 0x4F | RESERVED | 0x00 | RW | Yes | Yes |
| 0x82 | 0x50 | RESERVED | 0x00 | RW | Yes | Yes |
| 0x82 | 0x51 | RESERVED | 0x00 | RW | Yes | Yes |
| 0x82 | 0x52 | RESERVED | 0x00 | RW | Yes | Yes |
| 0x82 | 0x53 | RESERVED | 0x00 | RW | Yes | Yes |
| 0x82 | 0x54 | RESERVED | 0x00 | RW | Yes | Yes |
| 0x82 | 0x55 | RESERVED | 0x00 | RW | Yes | Yes |
| 0x82 | 0x56 | RESERVED | 0x00 | RW | Yes | Yes |
| 0x82 | 0x57 | RESERVED | 0x00 | RW | Yes | Yes |
| 0x82 | 0x58 | RESERVED | 0x00 | RW | Yes | Yes |
| 0x82 | 0x59 | RESERVED | 0x00 | RW | Yes | Yes |
| 0x82 | 0x5A | RESERVED | 0x00 | RW | Yes | Yes |
| 0x82 | 0x60 | RESERVED | 0x00 | RW | Yes | Yes |
| 0x82 | 0x61 | RESERVED | 0x00 | RW | Yes | Yes |
| 0x82 | 0x62 | RESERVED | 0x00 | RW | Yes | Yes |
| 0x82 | 0x63 | RESERVED | 0x00 | RW | Yes | Yes |
| 0x82 | 0x64 | RESERVED | 0x00 | RW | Yes | Yes |
| 0x82 | 0x65 | RESERVED | 0x00 | RW | Yes | Yes |
| 0x82 | 0x66 | RESERVED | 0x00 | RW | Yes | Yes |
| 0x82 | 0x67 | RESERVED | 0x00 | RW | Yes | Yes |
| 0x82 | 0x68 | RESERVED | 0x00 | RW | Yes | Yes |
| 0x82 | 0x69 | RESERVED | 0x00 | RW | Yes | Yes |
| 0x82 | 0x6A | RESERVED | 0x00 | RW | Yes | Yes |
| 0x82 | 0x70 | SET_FW_VER_LSB | 0x01 | RW | Yes | Yes |
| 0x82 | 0x71 | SET_FW_VER_MSB | 0x00 | RW | Yes | Yes |
| 0x82 | 0x72 | RESERVED | 0x01 | RW | Yes | Yes |
| 0x82 | 0x73 | RESERVED | 0x34 | RW | Yes | Yes |
| 0x82 | 0x74 | MODEL_ID | 0x00 | RW | Yes | Yes |
| 0x82 | 0x75 | RESERVED | 0x00 | RW | Yes | Yes |
| 0x82 | 0x76 | RESERVED | 0x00 | RW | Yes | Yes |
| 0x82 | 0x77 | RESERVED | 0x00 | RW | Yes | Yes |
| 0x82 | 0x78 | RESERVED | 0x00 | RW | Yes | Yes |
| 0x82 | 0x79 | RESERVED | 0x00 | RW | Yes | Yes |
| 0x82 | 0x7A | RESERVED | 0x03 | RW | Yes | Yes |
| 0x82 | 0x7B | RESERVED | 0x40 | RW | Yes | Yes |
| 0x82 | 0x7C | RESERVED | 0x00 | RW | Yes | Yes |
| 0x82 | 0x7D | RESERVED | 0x01 | RW | Yes | Yes |

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| Page | Address | Register Name | Default | Type | Paged | NVM |
|---|---|---|---|---|---|---|
| 0x82 | 0x7E | CRC _PAGE_GROUP_1 | N/A | R | Yes | No |
| Global | 0x90 | CBG_A_1 | 0x92 | RW | No | No |
| Global | 0x91 | CBG_A_2 | 0x48 | RW | No | No |
| Global | 0x95 | REVISION_ID | 0x01 | RW | No | No |
| Global | 0x96 | GROUP_0_FW_VER | 0x01 | RW | No | No |
| Global | 0x97 | CBG_B_1 | 0x92 | RW | No | No |
| Global | 0x98 | CBG_B_2_PRODUCT_ID | 0x34 | RW | No | No |
| Global | 0x9D | RESERVED | 0x38 | RW | No | No |
| Global | 0x9E | RESERVED | 0x00 | RW | No | No |
| Global | 0xEC | NVM_PROGRAM_STATUS | N/A | R | No | No |
| Global | 0xED | STORE_RESTORE_CFG | N/A | W | No | No |
| Global | 0xEF | PAGE | 0x80 | RW | No | No |
| Global | 0xF1 | ENTER_CONF_MODE | N/A | W | No | No |
| Global | 0xFC | UNLOCK_NVM | N/A | W | No | No |

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**Table 8. DVID_COMP_MT_A**

| **Address:** 0x00 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | EN_DVIDDN_LIFT_15mV_A | DVIDDN_PULL_SEL_A | | | EXIT_PS1_LIFT_VID_A | EXIT_PS1_RESET_LPF_A | EN_AI_DOUBLE_A | RIPPLE_COMP_DOUBLE_A |
| Default | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| Type | RW | RW | | | RW | RW | RW | RW |

| Bit | Name | Description |
|---|---|---|
| 7 | EN_DVIDDN_LIFT_15mV_A | Enable/Disable DVID down with fixed lift 15mV to prevent the DVID down undershoot of Rail A.<br>0: Enable<br>1: Disable |
| 6:4 | DVIDDN_PULL_SEL_A | DVID compensation during DVID ramp down of Rail A corresponding to the register of DVID_LIFT_A (0x22 [7:4])<br>000: Disable<br>001: IDVID_LIFT_A x 0.25<br>010: IDVID_LIFT_A x 0.5<br>011: IDVID_LIFT_A x 0.75<br>100: IDVID_LIFT_A x 1<br>101: IDVID_LIFT_A x 1.25<br>110: IDVID_LIFT_A x 1.5<br>111: IDVID_LIFT_A x 1.75 |
| 3 | EXIT_PS1_LIFT_VID_A | Enable/Disable the VID lift when VR exits PS1 to avoid undershoot at mode transition for Rail A.<br>0: Disable<br>1: Enable |
| 2 | EXIT_PS1_RESET_LPF_A | Enable/Disable the LPF resetting when VR exits PS1 to avoid the undershoot at mode transition for Rail A.<br>0: Disable<br>1: Enable |
| 1 | EN_AI_DOUBLE_A | Enable/Disable current gain Ai_A x2 of Rail A corresponding to the register of Ai_A (0x16 [3:1])<br>0: Disable<br>1: Enable |
| 0 | RIPPLE_COMP_DOUBLE_A | Enable/Disable ripple compensation x2 of Rail A corresponding to the register of SET_RIPPLE_COMP_A (0x03 [2:0])<br>0: Disable<br>1: Enable |

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**Table 9. DVID_COMP_MT_B**

| **Address:** 0x01 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | EN_DVIDDN_LIFT_15mV_B | DVIDDN_PULL_SEL_B | | | EXIT_PS1_LIFT_VID_B | EXIT_PS1_RESET_LPF_B | EN_AI_DOUBLE_B | RIPPLE_COMP_DOUBLE_B |
| Default | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| Type | RW | RW | | | RW | RW | RW | RW |

| Bit | Name | Description |
|---|---|---|
| 7 | EN_DVIDDN_LIFT_15mV_B | Enable/Disable DVID down with fixed lift 15mV to prevent the DVID down undershoot of Rail B.<br>0: Enable<br>1: Disable |
| 6:4 | DVIDDN_PULL_SEL_B | DVID compensation during DVID ramp down of Rail B corresponding to the register of DVID_LIFT_B (0x22 [3:0])<br>000: Disable<br>001: IDVID_LIFT_B x 0.25<br>010: IDVID_LIFT_B x 0.5<br>011: IDVID_LIFT_B x 0.75<br>100: IDVID_LIFT_B x 1<br>101: IDVID_LIFT_B x 1.25<br>110: IDVID_LIFT_B x 1.5<br>111: IDVID_LIFT_B x 1.75 |
| 3 | EXIT_PS1_LIFT_VID_B | Enable/Disable the VID lift when VR exits PS1 to avoid undershoot at mode transition for Rail B.<br>0: Disable<br>1: Enable |
| 2 | EXIT_PS1_RESET_LPF_B | Enable/Disable the LPF resetting when VR exits PS1 to avoid the undershoot at mode transition for Rail B.<br>0: Disable<br>1: Enable |
| 1 | EN_AI_DOUBLE_B | Enable/Disable current gain of Ai_B x2 of Rail B corresponding to the register of Ai_B (0x16 [0]: 0x17 [7:6])<br>0: Disable<br>1: Enable |
| 0 | RIPPLE_COMP_DOUBLE_B | Enable/Disable ripple compensation x2 of Rail B corresponding to the register of SET_RIPPLE_COMP_B (0x04 [2:0])<br>0: Disable<br>1: Enable |

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**Table 10. DVID_COMP_MT_C**

| **Address:** 0x02 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | EN_DVIDDN_LIFT_15mV_C | DVIDDN_PULL_SEL_C | | | Reserved | | EN_AI_DOUBLE_C | RIPPLE_COMP_DOUBLE_C |
| Default | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| Type | RW | RW | | | RW | | RW | RW |

| Bit | Name | Description |
|---|---|---|
| 7 | EN_DVIDDN_LIFT_15mV_C | Enable/Disable DVID down with fixed lift 15mV to prevent the DVID down undershoot of Rail C.<br>0: Enable<br>1: Disable |
| 6:4 | DVIDDN_PULL_SEL_C | DVID compensation during DVID ramp down of Rail C corresponding to the register of DVID_LIFT_C (0x23 [7:4])<br>000: Disable<br>001: IDVID_LIFT_C x 0.25<br>010: IDVID_LIFT_C x 0.5<br>011: IDVID_LIFT_C x 0.75<br>100: IDVID_LIFT_C x 1<br>101: IDVID_LIFT_C x 1.25<br>110: IDVID_LIFT_C x 1.5<br>111: IDVID_LIFT_C x 1.75 |
| 3:2 | Reserved | Reserved bits |
| 1 | EN_AI_DOUBLE_C | Enable/Disable current gain of Ai_C x2 of Rail C corresponding to the register of Ai_C (0x17 [5:4])<br>0: Disable<br>1: Enable |
| 0 | RIPPLE_COMP_DOUBLE_C | Enable/Disable ripple compensation x2 of Rail C corresponding to the register of SET_RIPPLE_COMP_C (0x05 [2:0])<br>0: Disable<br>1: Enable |

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**Table 11. LGON_RIP_COMP_A**

| **Address:** 0x03 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | DECAY_END_LGON_A | Reserved | | | | SET_RIPPLE_COMP_A | | |
| Default | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Type | RW | RW | | | | RW | | |

| Bit | Name | Description |
|---|---|---|
| 7 | DECAY_END_LGON_A | Enable/Disable turning low-gate ON when reaching target VID at the end of decay down for Rail A.<br>0: Disable<br>1: Enable |
| 6:3 | Reserved | [6:3] = 0000. All other combinations are not defined. |
| 2:0 | SET_RIPPLE_COMP_A | Adding auxiliary compensation current to VEA for compensating frequency difference when VID = 0.3V ~ 0.9V of Rail A, which helps the output voltage to reach the target within the specified time during DVID transition.<br>Icomp = VID/1.13MΩ x SET_RIPPLE_COMP_A.<br>As 0x00 [0] = 0,<br>0x03 [2:0] =<br>000: x0<br>001: x1<br>010: x2<br>011: x3<br>100: x4<br>101: x5<br>110: x6<br>111: x7<br><br>As 0x00 [0] = 1,<br>0x03 [2:0] =<br>000: x0<br>001: x2<br>010: x4<br>011: x6<br>100: x8<br>101: x10<br>110: x12<br>111: x14 |

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**Table 12. LGON_RIP_COMP_B**

| **Address:** 0x04 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | DECAY_END_LGON_B | Reserved | | | | SET_RIPPLE_COMP_B | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Type | RW | RW | | | | RW | | |

| Bit | Name | Description |
|---|---|---|
| 7 | DECAY_END_LGON_B | Enable/Disable turning low-gate ON when reaching target VID at the end of decay down for Rail B.<br>0: Disable<br>1: Enable |
| 6:3 | Reserved | [6:3] = 0000. All other combinations are not defined. |
| 2:0 | SET_RIPPLE_COMP_B | Adding auxiliary compensation current to VEA for compensating frequency difference when VID = 0.3V ~ 0.9V of Rail B, which helps the output voltage to reach the target within the specified time during DVID transition.<br>Icomp = VID/1.13MΩ x SET_RIPPLE_COMP_B.<br>As 0x01 [0] = 0,<br>0x04 [2:0] =<br>000: x0<br>001: x1<br>010: x2<br>011: x3<br>100: x4<br>101: x5<br>110: x6<br>111: x7<br><br>As 0x01 [0] = 1,<br>0x04 [2:0] =<br>000: x0<br>001: x2<br>010: x4<br>011: x6<br>100: x8<br>101: x10<br>110: x12<br>111: x14 |

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Table 13. LGON_RIP_COMP_C

| **Address:** 0x05 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | DECAY_END_LGON_C | Reserved | | | | SET_RIPPLE_COMP_C | | |
| Default | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Type | RW | RW | | | | RW | | |

| Bit | Name | Description |
|---|---|---|
| 7 | DECAY_END_LGON_C | Enable/Disable turning low-gate ON when reaching target VID at the end of decay down for Rail C.<br>0: Disable<br>1: Enable |
| 6:3 | Reserved | [6:3] = 0000. All other combinations are not defined. |
| 2:0 | SET_RIPPLE_COMP_C | Adding auxiliary compensation current to VEA for compensating frequency difference when VID = 0.3V ~ 0.9V of Rail C, which helps the output voltage to reach the target within the specified time during DVID transition.<br>Icomp = VID/1.13MΩ x SET_RIPPLE_COMP_C.<br>As 0x02 [0] = 0,<br>0x05 [2:0] =<br>000: x0<br>001: x1<br>010: x2<br>011: x3<br>100: x4<br>101: x5<br>110: x6<br>111: x7<br><br>As 0x02 [0] = 1,<br>0x05 [2:0] =<br>000: x0<br>001: x2<br>010: x4<br>011: x6<br>100: x8<br>101: x10<br>110: x12<br>111: x14 |

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**Table 14. MT_FVM_UVP**

| **Address:** 0x06 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | Reserved | EXIT_PS2_PS3_TRIG_PWM_A | EXIT_PS2_PS3_TRIG_PWM_B | EXIT_PS2_PS3_TRIG_PWM_C | FVM_UVP_A | FVM_UVP_B | FVM_UVP_C | Reserved |
| Default | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| Type | RW | RW | RW | RW | RW | RW | RW | RW |

| Bit | Name | Description |
|---|---|---|
| 7 | Reserved | [7] = 0. All other combinations are not defined. |
| 6 | EXIT_PS2_PS3_TRIG_PWM_A | The forced PWM Ton will be triggered upon exiting PS2/PS3 to avoid the undershoot during the mode transition of Rail A.<br>0: Disable.<br>1: Enable. |
| 5 | EXIT_PS2_PS3_TRIG_PWM_B | The forced PWM Ton will be triggered upon exiting PS2/PS3 to avoid the undershoot during the mode transition of Rail B.<br>0: Disable.<br>1: Enable. |
| 4 | EXIT_PS2_PS3_TRIG_PWM_C | The forced PWM Ton will be triggered upon exiting PS2/PS3 to avoid the undershoot during the mode transition of Rail C.<br>0: Disable.<br>1: Enable. |
| 3 | FVM_UVP_A | Enable/Disable blocking the UVP function when Fast V-Mode is triggered of Rail A.<br>0: Enable, the UVP is not blocked when Fast V-Mode is triggered.<br>1: Disable, the UVP is blocked when Fast V-Mode is triggered. |
| 2 | FVM_UVP_B | Enable/Disable blocking the UVP function when Fast V-Mode is triggered of Rail B.<br>0: Enable, the UVP is not blocked when Fast V-Mode is triggered.<br>1: Disable, the UVP is blocked when Fast V-Mode is triggered. |
| 1 | FVM_UVP_C | Enable/Disable blocking the UVP function when Fast V-Mode is triggered of Rail C.<br>0: Enable, the UVP is not blocked when Fast V-Mode is triggered.<br>1: Disable, the UVP is blocked when Fast V-Mode is triggered. |
| 0 | Reserved | [0] = 1. All other combinations are not defined. |

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**Table 15. TSEN_SEL**

| **Address:** 0x07 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | TSEN_SEL_A | TSEN_SEL_B | TSEN_SEL_C | Reserved | | | | |
| Default | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| Type | RW | RW | RW | RW | | | | |

| Bit | Name | Description |
|---|---|---|
| 7 | TSEN_SEL_A | Selection of TSEN table with positive or negative temperature coefficient of Rail A.<br>0: Negative temperature coefficient.<br>1: Positive temperature coefficient. |
| 6 | TSEN_SEL_B | Selection of TSEN table with positive or negative temperature coefficient of Rail B.<br>0: Negative temperature coefficient.<br>1: Positive temperature coefficient. |
| 5 | TSEN_SEL_C | Selection of TSEN table with positive or negative temperature coefficient of Rail C.<br>0: Negative temperature coefficient.<br>1: Positive temperature coefficient. |
| 4:0 | Reserved | [3:0] = 0000. All other combinations are not defined. |

**Table 16. FVM_NON_OVERLAP**

| **Address:** 0x08 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | Reserved | | | | | | | EN_FVM_NON_OVERLAP |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Type | RW | | | | | | | RW |

| Bit | Name | Description |
|---|---|---|
| 7:1 | Reserved | [7:1] = 0000000. All other combinations are not defined. |
| 0 | EN_FVM_NON_OVERLAP | When Fast V-Mode is triggered, the PWMs overlapping is forbidden to enhance the accuracy of the current limit.<br>0: Disable, PWMs overlapping is allowed when Fast V-Mode is triggered.<br>1: Enable, PWMs overlapping is forbidden within 5μs when Fast V-Mode is triggered. |

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**Table 17. SPM_1PH_AR_AB_SLL_C**

| **Address:** 0x09 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | SPM_1PH_AR_A | SPM_1PH_AR_B | EN_SSOCP | SMALL_LL_C | | Reserved | | |
| Default | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 |
| Type | RW | RW | RW | RW | | RW | | |

| Bit | Name | Description |
|---|---|---|
| 7 | SPM_1PH_AR_A | Enable/Disable the adaptive ramp at 1-ph operation when SPM enables for Rail A.<br>0: Disable.<br>1: Enable. |
| 6 | SPM_1PH_AR_B | Enable/Disable the adaptive ramp at 1-ph operation when SPM enables for Rail B.<br>0: Disable.<br>1: Enable. |
| 5 | EN_SSOCP | Enable/Disable soft start OCP<br>0: Disable<br>1: Enable |
| 4:3 | SMALL_LL_C | Small LL of Rail C, which sets $R_{LL}$ to,<br>00: 100%.<br>01: 84%.<br>10: 76%.<br>11: 48%. |
| 2:0 | Reserved | [2:0] = 111. All other combinations are not defined. |

**Table 18. MT_RIP_COMP_AB**

| **Address:** 0x0A | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | Reserved | SET_MT_RIPPLE_COMP_A | | | Reserved | SET_MT_RIPPLE_COMP_B | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Type | RW | RW | | | RW | RW | | |

| Bit | Name | Description |
|---|---|---|
| 7 | Reserved | Reserved bit. |
| 6:4 | SET_MT_RIPPLE_COMP_A | Selection of the ripple compensation to avoid the voltage undershoot at mode transition for Rail A.<br>As increasing the compensation voltage, the more voltage lift at mode transition.<br>000: Disable<br>001: x1<br>010: x2<br>011: x3<br>100: x4<br>101: x5<br>110: x6<br>111: x7 |
| 3 | Reserved | Reserved bit. |

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| Bit | Name | Description |
|---|---|---|
| 2:0 | SET_MT_RIPPLE_COMP_B | Selection of the ripple compensation to avoid the voltage undershoot at mode transition for Rail B.<br>As increasing the compensation voltage, the more voltage lift at mode transition.<br>000: Disable<br>001: x1<br>010: x2<br>011: x3<br>100: x4<br>101: x5<br>110: x6<br>111: x7 |

**Table 19. ICCMAX_A**

| **Address:** 0x10 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | ICCMAX_A | | | | | | | |
| Default | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| Type | RW | | | | | | | |

| Bit | Name | Description |
|---|---|---|
| 7:0 | ICCMAX_A | ICCMAX of Rail A, which can be set from 00h to FFh representing 0A to 255A.<br>[e.g.]<br>01100100: ICCMAX_A = 100A.<br>11111111: ICCMAX_A = 255A. |

**Table 20. ICCMAX_ADD_VBOOT_SR**

| **Address:** 0x11 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | ICCMAX_A_ADD | ICCMAX_B_ADD | Reserved | EN_NON_0_VBOOT_A | EN_NON_0_VBOOT_B | EN_NON_0_VBOOT_C | DVID_FAST_SR | |
| Default | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| Type | RW | RW | RW | RW | RW | RW | RW | |

| Bit | Name | Description |
|---|---|---|
| 7 | ICCMAX_A_ADD | Additional ICCMAX of Rail A. The effective ICCMAX can be encoded at 2 Amps per bit by setting 0x11 [7].<br>0x11 [7] = 0: ICCMAX_A = ICCMAX_A [7:0].<br>0x11 [7] = 1: ICCMAX_A = ICCMAX_A [7:0] x 2.<br>[e.g.]<br>As 0x11 [7] = 1,<br>0x10 [7:0] = 01100100: ICCMAX_A = 200A.<br>0x10 [7:0] = 11111111: ICCMAX_A = 510A. |

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| Bit | Name | Description |
|---|---|---|
| 6 | ICCMAX_B_ADD | Additional ICCMAX of Rail B. The effective ICCMAX can be encoded at 2 Amps per bit by setting 0x11 [6].<br>0x11 [6] = 0: ICCMAX_B = ICCMAX_B [7:0].<br>0x11 [6] = 1: ICCMAX_B = ICCMAX_B [7:0] x 2.<br>[e.g.]<br>As 0x11 [6] = 1,<br>0x12 [7:0] = 01100100: ICCMAX_B = 200A.<br>0x12 [7:0] = 11111111: ICCMAX_B = 510A. |
| 5 | Reserved | [5] = 1. All other combinations are not defined. |
| 4 | EN_NON_0_VBOOT_A | Enable/Disable non-zero VBOOT of Rail A.<br>0: Disable, EN_NON_0_VBOOT_A = 0V.<br>1: Enable, EN_NON_0_VBOOT_A = Non-zero VBOOT which is set by the register of 0x30 [7:0] |
| 3 | EN_NON_0_VBOOT_B | Enable/Disable non-zero VBOOT of Rail B.<br>0: Disable, EN_NON_0_VBOOT_B = 0V.<br>1: Enable, EN_NON_0_VBOOT_B = Non-zero VBOOT which is set by the register of 0x32 [7:0] |
| 2 | EN_NON_0_VBOOT_C | Enable/Disable non-zero VBOOT of Rail C.<br>0: Disable, EN_NON_0_VBOOT_C = 0V.<br>1: Enable, EN_NON_0_VBOOT_C = Non-zero VBOOT which is set by the register of 0x34 [7:0] |
| 1:0 | DVID_FAST_SR | DVID Fast slew rate.<br>00: 10mV/μs.<br>01: 24mV/μs.<br>10: 36mV/μs.<br>11: 48mV/μs. |

**Table 21. ICCMAX_B**

| **Address:** 0x12 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | ICCMAX_B | | | | | | | |
| Default | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| Type | RW | | | | | | | |

| Bit | Name | Description |
|---|---|---|
| 7:0 | ICCMAX_B | ICCMAX of Rail B, which can be set from 00h to FFh representing 0A to 255A.<br>[e.g.]<br>01100100: ICCMAX_B = 100A.<br>11111111: ICCMAX_B = 255A. |

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**Table 22. ICCMAX_C**

| **Address:** 0x13 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | ICCMAX_C | | | | | | | |
| Default | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| Type | RW | | | | | | | |

| Bit | Name | Description |
|---|---|---|
| 7:0 | ICCMAX_C | ICCMAX of Rail C, which can be set from 00h to FFh representing 0A to 255A.<br>[e.g.]<br>01100100: ICCMAX_C = 100A.<br>11111111: ICCMAX_C = 255A. |

**Table 23. VIDT_0LL**

| **Address:** 0x14 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | VIDT_A | VIDT_B | VIDT_C | EN_0LL_A | EN_0LL_B | EN_0LL_C | Reserved | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Type | RW | RW | RW | RW | RW | RW | RW | |

| Bit | Name | Description |
|---|---|---|
| 7 | VIDT_A | VID step of Rail A.<br>0: 5mV VID step.<br>1: 10mV VID step. |
| 6 | VIDT_B | VID step of Rail B.<br>0: 5mV VID step.<br>1: 10mV VID step. |
| 5 | VIDT_C | VID step of Rail C.<br>0: 5mV VID step.<br>1: 10mV VID step. |
| 4 | EN_0LL_A | Enable zero load-line of Rail A.<br>0: Disable 0LL.<br>1: Enable 0LL. |
| 3 | EN_0LL_B | Enable zero load-line of Rail B.<br>0: Disable 0LL.<br>1: Enable 0LL. |
| 2 | EN_0LL_C | Enable zero load-line of Rail C.<br>0: Disable 0LL.<br>1: Enable 0LL. |
| 1:0 | Reserved | Reserved bits. |

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**Table 24. KTON_AB**

| **Address:** 0x15 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | KTON_A | | | | KTON_B | | | |
| Default | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| Type | RW | | | | RW | | | |

| Bit | Name | Description |
|---|---|---|
| 7:4 | KTON_A | According to required frequency of Rail A, select adaptive KTON_A parameter. Please refer to the section of Switching Frequency Setting for the detailed description. |
| 3:0 | KTON_B | According to required frequency of Rail B, select adaptive KTON_B parameter. Please refer to the section of Switching Frequency Setting for the detailed description. |

**Table 25. KTON_C_Ai_AB**

| **Address:** 0x16 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | KTON_C | | | | Ai_A | | | Ai_B_MSB |
| Default | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| Type | RW | | | | RW | | | RW |

| Bit | Name | Description |
|---|---|---|
| 7:4 | KTON_C | According to required frequency of Rail C, select adaptive KTON_C parameter. Please refer to the section of Switching Frequency Setting for the detailed description. |
| 3:1 | Ai_A | Current gain setting of Rail A.<br>When EN_AI_DOUBLE_A = Disable(0x00[1] = 0)<br>000: Ai_A = 0.25.<br>001: Ai_A = 0.5.<br>010: Ai_A = 0.75.<br>011: Ai_A = 1.<br>100: Ai_A = 0.125.<br>101: Ai_A = 0.375.<br>110: Ai_A = 0.625.<br>111: Ai_A = 0.875.<br><br>When EN_AI_DOUBLE_A = Enable(0x00[1] = 1)<br>000: Ai_A = 0.5.<br>001: Ai_A = 1.<br>010: Ai_A = 1.5.<br>011: Ai_A = 2.<br>100: Ai_A = 0.25.<br>101: Ai_A = 0.75.<br>110: Ai_A = 1.25.<br>111: Ai_A = 1.75. |

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| Bit | Name | Description |
|---|---|---|
| 0 | Ai_B_MSB | Current gain setting of Rail B<br>Ai_B = (Ai_B_MSB:Ai_B_LSB)<br>When EN_AI_DOUBLE_B = Disable(0x01[1] = 0)<br>(Ai_B_MSB: Ai_B_LSB) = 000: Ai_B = 0.25.<br>(Ai_B_MSB: Ai_B_LSB) = 001: Ai_B = 0.5.<br>(Ai_B_MSB: Ai_B_LSB) = 010: Ai_B = 0.75.<br>(Ai_B_MSB: Ai_B_LSB) = 011: Ai_B = 1.<br>(Ai_B_MSB: Ai_B_LSB) = 100: Ai_B = 0.125<br>(Ai_B_MSB: Ai_B_LSB) = 101: Ai_B = 0.375.<br>(Ai_B_MSB: Ai_B_LSB) = 110: Ai_B = 0.625.<br>(Ai_B_MSB: Ai_B_LSB) = 111: Ai_B = 0.875.<br><br>When EN_AI_DOUBLE_B = Enable(0x01[1] = 1)<br>(Ai_B_MSB: Ai_B_LSB) = 000: Ai_B = 0.5.<br>(Ai_B_MSB: Ai_B_LSB) = 001: Ai_B = 1.<br>(Ai_B_MSB: Ai_B_LSB) = 010: Ai_B = 1.5.<br>(Ai_B_MSB: Ai_B_LSB) = 011: Ai_B = 2.<br>(Ai_B_MSB: Ai_B_LSB) = 100: Ai_B = 0.25<br>(Ai_B_MSB: Ai_B_LSB) = 101: Ai_B = 0.75.<br>(Ai_B_MSB: Ai_B_LSB) = 110: Ai_B = 1.25.<br>(Ai_B_MSB: Ai_B_LSB) = 111: Ai_B = 1.75. |

**Table 26. Ai_BC_EN_SPM**

| **Address:** 0x17 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | Ai_B_LSB | | Ai_C | | Reserved | EN_SPM_A | EN_SPM_B | EN_SPM_C |
| Default | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| Type | RW | | RW | | RW | RW | RW | RW |

| Bit | Name | Description |
|---|---|---|
| 7:6 | Ai_B_LSB | Current gain setting of Rail B<br>Ai_B = (Ai_B_MSB: Ai_B_LSB)<br>When EN_AI_DOUBLE_B = Disable(0x01[1] = 0)<br>(Ai_B_MSB: Ai_B_LSB) = 000: Ai_B = 0.25.<br>(Ai_B_MSB: Ai_B_LSB) = 001: Ai_B = 0.5.<br>(Ai_B_MSB: Ai_B_LSB) = 010: Ai_B = 0.75.<br>(Ai_B_MSB: Ai_B_LSB) = 011: Ai_B = 1.<br>(Ai_B_MSB: Ai_B_LSB) = 100: Ai_B = 0.125<br>(Ai_B_MSB: Ai_B_LSB) = 101: Ai_B = 0.375.<br>(Ai_B_MSB: Ai_B_LSB) = 110: Ai_B = 0.625.<br>(Ai_B_MSB: Ai_B_LSB) = 111: Ai_B = 0.875.<br><br>When EN_AI_DOUBLE_B = Enable(0x01[1] = 1)<br>(Ai_B_MSB: Ai_B_LSB) = 000: Ai_B = 0.5.<br>(Ai_B_MSB: Ai_B_LSB) = 001: Ai_B = 1.<br>(Ai_B_MSB: Ai_B_LSB) = 010: Ai_B = 1.5.<br>(Ai_B_MSB: Ai_B_LSB) = 011: Ai_B = 2.<br>(Ai_B_MSB: Ai_B_LSB) = 100: Ai_B = 0.25<br>(Ai_B_MSB: Ai_B_LSB) = 101: Ai_B = 0.75.<br>(Ai_B_MSB: Ai_B_LSB) = 110: Ai_B = 1.25.<br>(Ai_B_MSB: Ai_B_LSB) = 111: Ai_B = 1.75. |

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| Bit | Name | Description |
|---|---|---|
| 5:4 | Ai_C | Current gain setting of Rail C.<br>When EN_Ai_DOUBLE_C = Disable(0x02[1] = 0)<br>00: Ai_C = 0.25.<br>01: Ai_C = 0.5.<br>10: Ai_C = 0.75.<br>11: Ai_C = 1.<br><br>When EN_Ai_DOUBLE_C = Enable(0x02[1] = 1)<br>00: Ai_C = 0.5.<br>01: Ai_C = 1.<br>10: Ai_C = 1.5.<br>11: Ai_C = 2. |
| 3 | Reserved | [3] = 1. All other combinations are not defined |
| 2 | EN_SPM_A | Enable/Disable smart phase management of Rail A.<br>0: Disable.<br>1: Enable. |
| 1 | EN_SPM_B | Enable/Disable smart phase management of Rail B.<br>0: Disable.<br>1: Enable. |
| 0 | EN_SPM_C | Enable/Disable smart phase management of Rail C.<br>0: Disable.<br>1: Enable. |

**Table 27. DBLR_PH_CS_SEL**

| **Address:** 0x18 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | EN_DBLR | SET_DBLR_PH | | Reserved | | CS_SEL_A | CS_SEL_B | CS_SEL_C |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Type | RW | RW | | RW | | RW | RW | RW |

| Bit | Name | Description |
|---|---|---|
| 7 | EN_DBLR | Enable phase double for Rail A.<br>0: Disable, maximum 4-phase operation, Pin 18 is set as DRVEN.<br>1: Enable, maximum 8-phase operation, Pin 18 is set as DBLR_PS. |
| 6:5 | SET_DBLR_PH | Phase number selection of Rail A when EN_DBLR is enable.<br>As 0x18 [7] = 1,<br>00: Maximum 8-phase operation.<br>01: 5-phase operation.<br>10: 6-phase operation.<br>11: 7-phase operation. |
| 4:3 | Reserved | Reserved bits. |
| 2 | CS_SEL_A | Selection of current sense type for Rail A. If the Smart Power Stage (SPS) modules are used for Rail A, set this bit as 1'b1, the ISENA1N provides a reference voltage of 1.3V for the reference input of the SPS modules.<br>0: DCR.<br>1: SPS. |
| 1 | CS_SEL_B | Selection of current sense type for Rail B. If the Smart Power Stage (SPS) modules are used for Rail B, set this bit as 1'b1, the ISENB1N provides a reference voltage of 1.3V for the reference input of the SPS modules.<br>0: DCR.<br>1: SPS. |

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| Bit | Name | Description |
|---|---|---|
| 0 | CS_SEL_C | Selection of current sense type for Rail C. If the Smart Power Stage (SPS) modules are used for Rail C, set this bit as 1'b1, the ISENCN provides a reference voltage of 1.3V for the reference input of the SPS modules.<br>0: DCR.<br>1: SPS. |

**Table 28. ICCMAX_D**

| **Address:** 0x19 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | ICCMAX_D | | | | | | | |
| Default | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| Type | RW | | | | | | | |

| Bit | Name | Description |
|---|---|---|
| 7:0 | ICCMAX_D | ICCMAX of Rail D which can be set from 00h to FFh representing 0A to 255A.<br>[e.g.]<br>01100100: ICCMAX_D = 100A.<br>11111111: ICCMAX_D = 255A. |

**Table 29. ANTI_OVS_SLL_A**

| **Address:** 0x1A | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | ANTI_OVS_TH_A | | ANTI_OVS_TH_B | | ANTI_OVS_TH_C | | SMALL_LL_A | |
| Default | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| Type | RW | | RW | | RW | | RW | |

| Bit | Name | Description |
|---|---|---|
| 7:6 | ANTI_OVS_TH_A | Selection of anti-overshoot threshold for Rail A.<br>00: 90mV.<br>01:150mV.<br>10: 210mV.<br>11: Disable. |
| 5:4 | ANTI_OVS_TH_B | Selection of anti-overshoot threshold for Rail B.<br>00: 90mV.<br>01:150mV.<br>10: 210mV.<br>11: Disable. |
| 3:2 | ANTI_OVS_TH_C | Selection of anti-overshoot threshold for Rail C.<br>00: 90mV.<br>01:150mV.<br>10: 210mV.<br>11: Disable. |
| 1:0 | SMALL_LL_A | Small LL of Rail A, which set $R_{LL}$ to,<br>00: 100%.<br>01: 50%.<br>10: 85%.<br>11: 75%. |

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**Table 30. QR_TH_A**

| **Address:** 0x1B | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | MULTI_PH_QR_A | | | | 1_PH_QR_A | | | |
| Default | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| Type | RW | | | | RW | | | |

| Bit | Name | Description |
|---|---|---|
| 7:4 | MULTI_PH_QR_A | Multiple-phase quick response for transient response speed-up of loading rising edge of Rail A. Please refer to the section of Adaptive Quick Response (AQR) for the detailed description. |
| 3:0 | 1_PH_QR_ A | Single-phase quick response for transient response speed-up of loading rising edge of Rail A. Please refer to the section of Adaptive Quick Response (AQR) for the detailed description. |

**Table 31. QR_TH_B**

| **Address:** 0x1C | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | MULTI_PH_QR_B | | | | 1_PH_QR_ B | | | |
| Default | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| Type | RW | | | | RW | | | |

| Bit | Name | Description |
|---|---|---|
| 7:4 | MULTI_PH_QR_B | Multiple-phase quick response for transient response speed-up of loading rising edge of Rail B. Please refer to the section of Adaptive Quick Response (AQR) for the detailed description. |
| 3:0 | 1_PH_QR_ B | Single-phase quick response for transient response speed-up of loading rising edge of Rail B. Please refer to the section of Adaptive Quick Response (AQR) for the detailed description. |

**Table 32. AR_TH_AB**

| **Address:** 0x1D | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | MULTI_PH_AR_TH_A | | 1_PH_AR_TH_A | | MULTI_PH_AR_TH_B | | 1_PH_AR_TH_B | |
| Default | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| Type | RW | | RW | | RW | | RW | |

| Bit | Name | Description |
|---|---|---|
| 7:6 | MULTI_PH_AR_TH_A | Multiple-phase adaptive ramp threshold of Rail A.<br>00: Disable.<br>01: 150mV.<br>10: 200mV.<br>11: 250mV. |
| 5:4 | 1_PH_AR_TH_A | Single-phase adaptive ramp threshold of Rail A.<br>00: Disable.<br>01: 125mV.<br>10: 150mV. |

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| Bit | Name | Description |
|---|---|---|
| | | 11: 175mV. |
| 3:2 | MULTI_PH_AR_TH_B | Multiple-phase adaptive ramp threshold of Rail B.<br>00: Disable.<br>01: 150mV.<br>10: 200mV.<br>11: 250mV. |
| 1:0 | 1_PH_AR_TH_B | Single-phase adaptive ramp threshold of Rail B.<br>00: Disable.<br>01: 125mV.<br>10: 150mV.<br>11: 175mV. |

**Table 33. AR_TH_C_ZCD_AB**

| **Address:** 0x1E | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | 1_PH_AR_TH_C | | ZCD_TH_A | | | ZCD_TH_B | | |
| Default | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| Type | RW | | RW | | | RW | | |

| Bit | Name | Description |
|---|---|---|
| 7:6 | 1_PH_AR_TH_C | Single-phase adaptive ramp threshold of Rail C.<br>00: Disable.<br>01: 125mV.<br>10: 150mV.<br>11: 175mV. |
| 5:3 | ZCD_TH_A | Detect whether each phase current crosses zero current for Rail A. Set trigger level. Please refer to the section of Zero-Crossing Detection (ZCD) for detailed description.<br>000: Disable<br>001: 0.1552mV/V.<br>010: 0.31mV/V.<br>011: 0.465mV/V.<br>100: 0.62mV/V.<br>101: 0.775mV/V.<br>110: 0.93mV/V.<br>111: 1.085mV/V. |
| 2:0 | ZCD_TH_B | Detect whether each phase current crosses zero current for Rail B. Set trigger level. Please refer to the section of Zero-Crossing Detection (ZCD) for detailed description.<br>000: Disable<br>001: 0.1552mV/V.<br>010: 0.31mV/V.<br>011: 0.465mV/V.<br>100: 0.62mV/V.<br>101: 0.775mV/V.<br>110: 0.93mV/V.<br>111: 1.085mV/V. |

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**Table 34. ZCD_C_ICCMAX_ADD_D_SLL_B**

| **Address:** 0x1F | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | ZCD_TH_C | | | Reserved | | ICCMAX_D_ADD | SMALL_LL_B | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| Type | RW | | | RW | | RW | RW | |

| Bit | Name | Description |
|---|---|---|
| 7:5 | ZCD_TH_C | Detect whether each phase current crosses zero current for Rail C. Set trigger level. Please refer to the section of Zero-Crossing Detection (ZCD) for detailed description.<br>000: Disable<br>001: 0.1552mV/V.<br>010: 0.31mV/V.<br>011: 0.465mV/V.<br>100: 0.62mV/V.<br>101: 0.775mV/V.<br>110: 0.93mV/V.<br>111: 1.085mV/V. |
| 4:3 | Reserved | Reserved bits. |
| 2 | ICCMAX_D_ADD | Additional ICCMAX of Rail D. The effective ICCMAX can be encoded at 2 Amps per bit by setting 0x1F [2].<br>0x1F [2] = 0: ICCMAX_D = ICCMAX_D [7:0].<br>0x1F [2] = 1: ICCMAX_D = ICCMAX_D [7:0] x 2.<br>[e.g.]<br>As 0x1F [2] = 1,<br>0x19 [7:0] = 01100100: ICCMAX_D = 200A.<br>0x19 [7:0] = 11111111: ICCMAX_D = 510A. |
| 1:0 | SMALL_LL_B | Small LL of Rail B, which sets $R_{LL}$ to,<br>00: 100%.<br>01: 50%.<br>10: 85%.<br>11: 75%. |

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Table 35. LPF_INITIAL_AB

| **Address:** 0x20 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | Reserved | LPF_INITIAL_A | | | Reserved | LPF_INITIAL_B | | |
| Default | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| Type | RW | RW | | | RW | RW | | |

| Bit | Name | Description |
|---|---|---|
| 7 | Reserved | Reserved bit. |
| 6:4 | LPF_INITIAL_A | Reduce overshoot of DVID up from PS4 by selecting initial state of LPF of Rail A.<br><br>000: LPF_INITIAL_A = −0.5μA.<br>001: LPF_INITIAL_A = 0μA.<br>010: LPF_INITIAL_A = 0.5μA.<br>011: LPF_INITIAL_A = 1μA.<br>100: LPF_INITIAL_A = −2μA.<br>101: LPF_INITIAL_A = −1.5μA.<br>110: LPF_INITIAL_A = −1μA.<br>All other combinations are not defined.<br><br>$V_{LPF_INITIAL_A}$ (V)<br>= LPF_INITIAL_A * 100kΩ * 0.3 * $R_{EA1(A)}/R_{EA2(A)}$ |
| 3 | Reserved | Reserved bit. |
| 2:0 | LPF_INITIAL_B | Reduce overshoot of DVID up from PS4 by selecting initial state of LPF of Rail B.<br><br>000: LPF_INITIAL_B = −0.5μA.<br>001: LPF_INITIAL_B = 0μA.<br>010: LPF_INITIAL_B = 0.5μA.<br>011: LPF_INITIAL_B = 1μA.<br>100: LPF_INITIAL_B = −2μA.<br>101: LPF_INITIAL_B = −1.5μA.<br>110: LPF_INITIAL_B = −1μA.<br>All other combinations are not defined.<br><br>$V_{LPF_INITIAL_B}$ (V)<br>= LPF_INITIAL_B * 100kΩ * 0.3 * $R_{EA1(B)}/R_{EA2(B)}$ |

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**Table 36. RT_SPS_DBLR_SPM_FVM_HLPF_LPF_INT_C**

| **Address:** 0x21 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | EN_RT_SPS | EN_DBLR_SPM_PH1_1PHCCM | EN_FVM_HOLD_LPF_A | EN_FVM_HOLD_LPF_B | EN_FVM_HOLD_LPF_C | LPF_INITIAL_C | | |
| Default | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| Type | RW | RW | RW | RW | RW | RW | | |

| Bit | Name | Description |
|---|---|---|
| 7 | EN_RT_SPS | Enable/Disable compatible DRVEN_F for the SPS from Richtek.<br>0: Disable, the DRVEN_F is compatible with Dr.MOS/SPS<br>1: Enable, the DRVEN_F is compatible to the SPS from Richtek. |
| 6 | EN_DBLR_SPM_PH1_1PHCCM | Enable/Disable 1 phase CCM operation when DBLR and SPM are enabled.<br>0: Disable, 2 phase CCM operation (Phase 1A, Phase 1B).<br>1: Enable, 1 phase CCM operation (Phase 1A). |
| 5 | EN_FVM_HOLD_LPF_A | Enable/disable the hold low pass filter function to reduce the voltage drop during FVM for Rail A.<br>0: Disable.<br>1: Enable. |
| 4 | EN_FVM_HOLD_LPF_B | Enable/disable the hold low pass filter function to reduce the voltage drop during FVM for Rail B.<br>0: Disable.<br>1: Enable. |
| 3 | EN_FVM_HOLD_LPF_C | Enable/disable the hold low pass filter function to reduce the voltage drop during FVM for Rail C.<br>0: Disable.<br>1: Enable. |
| 2:0 | LPF_INITIAL_C | Reduce overshoot of DVID up from PS4 by selecting initial state of LPF of Rail C.<br><br>000, LPF_INITIAL_C = −0.5μA.<br>001, LPF_INITIAL_C = 0μA.<br>010, LPF_INITIAL_C = 0.5μA.<br>011, LPF_INITIAL_C = 1μA.<br>100, LPF_INITIAL_C = −2μA.<br>101, LPF_INITIAL_C = −1.5μA.<br>110, LPF_INITIAL_C = −1μA.<br>All other combinations are not defined.<br><br>$V_{LPF_INITIAL_C}$ (V)<br>= LPF_INITIAL_C * 100kΩ * 0.3 * $R_{EA1(C)}/R_{EA2(C)}$ |

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**Table 37. DVID_LIFT_AB**

| **Address:** 0x22 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | DVID_LIFT_A | | | | DVID_LIFT_B | | | |
| Default | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| Type | RW | | | | RW | | | |

| Bit | Name | Description |
|---|---|---|
| 7:4 | DVID_LIFT_A | Dynamic VID compensation during DVID ramp up for Rail A.<br>0000: IDVID_LIFT_A = Disable.<br>0001: IDVID_LIFT_A = 1μA.<br>0010: IDVID_LIFT_A = 2μA.<br>0011: IDVID_LIFT_A = 3μA.<br>0100: IDVID_LIFT_A = 4μA.<br>0101: IDVID_LIFT_A = 5μA.<br>0110: IDVID_LIFT_A = 6μA.<br>0111: IDVID_LIFT_A = 7μA.<br>1000: IDVID_LIFT_A = 8μA.<br>1001: IDVID_LIFT_A = 9μA.<br>1010: IDVID_LIFT_A = 10μA.<br>1011: IDVID_LIFT_A = 12μA.<br>1100: IDVID_LIFT_A = 14μA.<br>1101: IDVID_LIFT_A = 16μA.<br>1110: IDVID_LIFT_A = 18μA.<br>1111: IDVID_LIFT_A = 20μA. |
| 3:0 | DVID_LIFT_B | Dynamic VID compensation during DVID ramp up for Rail B.<br>0000: IDVID_LIFT_B = Disable.<br>0001: IDVID_LIFT_B = 1μA.<br>0010: IDVID_LIFT_B = 2μA.<br>0011: IDVID_LIFT_B = 3μA.<br>0100: IDVID_LIFT_B = 4μA.<br>0101: IDVID_LIFT_B = 5μA.<br>0110: IDVID_LIFT_B = 6μA.<br>0111: IDVID_LIFT_B = 7μA.<br>1000: IDVID_LIFT_B = 8μA.<br>1001: IDVID_LIFT_B = 9μA.<br>1010: IDVID_LIFT_B = 10μA.<br>1011: IDVID_LIFT_B = 12μA.<br>1100: IDVID_LIFT_B = 14μA.<br>1101: IDVID_LIFT_B = 16μA.<br>1110: IDVID_LIFT_B = 18μA.<br>1111: IDVID_LIFT_B = 20μA. |

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**Table 38. DVID_LIFT_C**

| **Address:** 0x23 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | DVID_LIFT_C | | | | Reserved | | | |
| Default | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| Type | RW | | | | RW | | | |

| Bit | Name | Description |
|---|---|---|
| 7:4 | DVID_LIFT_C | Dynamic VID compensation during DVID ramp up for Rail C.<br>0000: IDVID_LIFT_C = Disable.<br>0001: IDVID_LIFT_C = 1μA.<br>0010: IDVID_LIFT_C = 2μA.<br>0011: IDVID_LIFT_C = 3μA.<br>0100: IDVID_LIFT_C = 4μA.<br>0101: IDVID_LIFT_C = 5μA.<br>0110: IDVID_LIFT_C = 6μA.<br>0111: IDVID_LIFT_C = 7μA.<br>1000: IDVID_LIFT_C = 8μA.<br>1001: IDVID_LIFT_C = 9μA.<br>1010: IDVID_LIFT_C = 10μA.<br>1011: IDVID_LIFT_C = 12μA.<br>1100: IDVID_LIFT_C = 14μA.<br>1101: IDVID_LIFT_C = 16μA.<br>1110: IDVID_LIFT_C = 18μA.<br>1111: IDVID_LIFT_C = 20μA. |
| 3:0 | Reserved | [3:0] = 0010. All other combinations are not defined. |

**Table 39. PSYS_PWM_TRI_0V_DVID**

| **Address:** 0x24 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | ADJ_PSYS_LEVEL | PWM_TRI_LEVEL | | Reserved | | | EN_0V_DVID_UP_SMT | Reserved |
| Default | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| Type | RW | RW | | RW | | | RW | RW |

| Bit | Name | Description |
|---|---|---|
| 7 | ADJ_PSYS_LEVEL | Adjust the full-scale voltage level of PSYS.<br>0: PSYS = 1.6V<br>1: PSYS = 3.2V |
| 6:5 | PWM_TRI_LEVEL | Selection of PWM tri-state level<br>00: PWM_TRI_LEVEL = 1.6V to 2.2V.<br>01: PWM_TRI_LEVEL = 1.34V to 1.88V.<br>10: PWM_TRI_LEVEL = 1.4V to 2V.<br>11; PWM_TRI_LEVEL = 1.16V to 1.65V. |
| 4:2 | Reserved | [4:2] = 001. All other combinations are not defined. |
| 1 | EN_0V_DVID_UP_SMT | Enable/Disable the function to smooth the voltage ramp by adjusting the $t_{ON}$ width of the PWM signals when slewing up from 0V.<br>0: Disable.<br>1: Enable. |
| 0 | Reserved | [0] = 1. All other combinations are not defined. |

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**Table 40. ACLL_LPF_TSEN_POS_OFST_A**

| **Address:** 0x25 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | ACLL_LPF_LIFT_SEL_A | | TSEN_POS_OFFSET_A | | | | | |
| Default | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| Type | RW | | RW | | | | | |

| Bit | Name | Description |
|---|---|---|
| 7:6 | ACLL_LPF_LIFT_SEL_A | Selection of the voltage lifting when adaptive ramp is triggered in ACLL for Rail A.<br>00: 1x<br>01: 1.5x<br>10: 2x<br>11: 2.5x |
| 5:0 | TSEN_POS_OFFSET_A | Adjust the positive thermal coefficient offset for fine-tuning of Rail A. When the 0x25[5:0] = 6'd32, the VTSEN_A = 1.4V represents 100°C.<br>The equation of the positive thermal coefficient is described as below,<br>VTSEN_A = 1.5V - TSEN_POS_OFFSET_A x 3.125mV at 100°C |

**Table 41. ACLL_LPF_TSEN_POS_OFST_B**

| **Address:** 0x26 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | ACLL_LPF_LIFT_SEL_B | | TSEN_POS_OFFSET_B | | | | | |
| Default | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| Type | RW | | RW | | | | | |

| Bit | Name | Description |
|---|---|---|
| 7:6 | ACLL_LPF_LIFT_SEL_B | Selection of the voltage lifting when adaptive ramp is triggered in ACLL for Rail B.<br>00: 1x<br>01: 1.5x<br>10: 2x<br>11: 2.5x |
| 5:0 | TSEN_POS_OFFSET_B | Adjust the positive thermal coefficient offset for fine-tuning of Rail B. When the 0x26[5:0] = 6'd32, the VTSEN_B = 1.4V represents 100°C.<br>The equation of the positive thermal coefficient is described as below,<br>VTSEN_B = 1.5V - TSEN_POS_OFFSET_B x 3.125mV at 100°C |

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**Table 42. ACLL_LPF_TSEN_POS_OFST_C**

| **Address:** 0x27 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | ACLL_LPF_LIFT_SEL_C | | TSEN_POS_OFFSET_C | | | | | |
| Default | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| Type | RW | | RW | | | | | |

| Bit | Name | Description |
|---|---|---|
| 7:6 | ACLL_LPF_LIFT_SEL_C | Selection of the voltage lifting when adaptive ramp is triggered in ACLL for Rail C.<br>00: 1x<br>01: 1.5x<br>10: 2x<br>11: 2.5x |
| 5:0 | TSEN_POS_OFFSET_C | Adjust the positive thermal coefficient offset for fine-tuning of Rail C. When the 0x27[5:0] = 6'd32, the VTSEN_C = 1.4V represents 100°C.<br>The equation of the positive thermal coefficient is described as below,<br>VTSEN_C = 1.5V - TSEN_POS_OFFSET_C x 3.125mV at 100°C |

**Table 43. FVM_CTRL_AB**

| **Address:** 0x28 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | EN_FREQ_CTRL_FVM_A | EN_VEA_CLAMP_FVM_A | FVM_EXTEND_T_SEL_A | | EN_FREQ_CTRL_FVM_B | EN_VEA_CLAMP_FVM_B | FVM_EXTEND_T_SEL_B | |
| Default | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| Type | RW | RW | RW | | RW | RW | RW | |

| Bit | Name | Description |
|---|---|---|
| 7 | EN_FREQ_CTRL_FVM_A | Enable/Disable the frequency control of Rail A to avoid the multiple pulse when the FVM is triggered.<br>0: Disable.<br>1: Enable. |
| 6 | EN_VEA_CLAMP_FVM_A | Enable/Disable the error amplifier clamping of Rail A to enhance the accuracy of the current limit when the FVM is triggered.<br>0: Disable.<br>1: Enable. |
| 5:4 | FVM_EXTEND_T_SEL_A | Selection of the extended time for the non-overlap PWM Ton and VEA clamping for Rail A.<br>00: 0.625μs.<br>01: 1.25μs.<br>10: 1.875μs.<br>11: 2.5μs. |
| 3 | EN_FREQ_CTRL_FVM_B | Enable/Disable the frequency control of Rail B to avoid the multiple pulse when the FVM is triggered.<br>0: Disable.<br>1: Enable. |

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| Bit | Name | Description |
|---|---|---|
| 2 | EN_VEA_CLAMP_FVM_B | Enable/Disable the error amplifier clamping of Rail B to enhance the accuracy of the current limit when the FVM is triggered.<br>0: Disable.<br>1: Enable. |
| 1:0 | FVM_EXTEND_T_SEL_B | Selection of the extended time for the non-overlap PWM Ton and VEA clamping for Rail B.<br>00: 0.625μs.<br>01: 1.25μs.<br>10: 1.875μs.<br>11: 2.5μs. |

**Table 44. RESERVED**

| **Address:** 0x29 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | Reserved | | | | | | | |
| Default | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| Type | RW | | | | | | | |

| Bit | Name | Description |
|---|---|---|
| 7:0 | Reserved | [7:0] = 11111000. All other combinations are not defined. |

**Table 45. ZCD_HYS_OFST_C**

| **Address:** 0x2A | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | ZCD_HYS_C | | ZCD_OFFSET_C | | | | | |
| Default | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| Type | RW | | RW | | | | | |

| Bit | Name | Description |
|---|---|---|
| 7:6 | ZCD_HYS_C | Selection of ZCD hysteresis for Rail C.<br>ZCD_HYS = 0.208mV/step<br>[00]: 0mV<br>[01]: 0.208mV<br>[10]: 0.417mV<br>[11]: 0.625mV |
| 5:0 | ZCD_OFFSET_C | Selection of the additional ZCD offset for Rail C.<br>The additional ZCD offset is set as multiple by ZCD_OFFSET_C in decimal.<br>[5]: sign bit, 0 is positive<br>ZCD_OFFSET = 0.104mV/step<br>[000001]: 0.104mV<br>[001100]: 1.25mV<br>[100001]: –0.104mV<br>[101100]: –1.25mV |

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**Table 46. EN_RAIL_MAX_PH**

| **Address:** 0x2B | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | EN_RAIL_A | MAX_PH_A | | | EN_RAIL_C | EN_RAIL_B | MAX_PH_B | |
| Default | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| Type | | | | | | | | |

| Bit | Name | Description |
|---|---|---|
| 7 | EN_RAIL_A | Enable/Disable Rail A.<br>0: Enable Rail A.<br>1: Disable Rail A. |
| 6:4 | MAX_PH_A | Selection of maximum phases operation of Rail A.<br>100, 4-PH<br>101, 3-PH<br>110, 2-PH<br>111, 1-PH<br>Any other value is not available for 0x2B [6:4]. |
| 3 | EN_RAIL_C | Enable/Disable Rail C.<br>0: Enable Rail C.<br>1: Disable Rail C. |
| 2 | EN_RAIL_B | Enable/Disable Rail B.<br>0: Enable Rail B.<br>1: Disable Rail B. |
| 1:0 | MAX_PH_B | Selection of maximum phases operation of Rail B.<br>01, 3-PH<br>10, 2-PH<br>11, 1-PH<br>Any other value is not available for 0x2B [1:0]. |

**Table 47. SVID_ADDR**

| **Address:** 0x2C | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | Reserved | | SVID_ADDR_RAIL_A | | SVID_ADDR_RAIL_B | | SVID_ADDR_RAIL_C | |
| Default | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| Type | RW | | RW | | RW | | RW | |

| Bit | Name | Description |
|---|---|---|
| 7:6 | Reserved | [7:6] = 00. All other combinations are not defined. |
| 5:4 | SVID_ADDR_RAIL_A | SVID domain address setting for Rail A,<br>00: SVID domain address of Rail A is 00h.<br>01: SVID domain address of Rail A is 01h.<br>10: SVID domain address of Rail A is 02h.<br>11: SVID domain address of Rail A is 03h.<br>Duplicated SVID domain address of Rail A, Rail B and Rail C must be avoided. |
| 3:2 | SVID_ADDR_RAIL_B | SVID domain address setting for Rail B,<br>00: SVID domain address of Rail B is 00h.<br>01: SVID domain address of Rail B is 01h.<br>10: SVID domain address of Rail B is 02h.<br>11: SVID domain address of Rail B is 03h.<br>Duplicated SVID domain address of Rail A, Rail B and Rail C must be avoided. |

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| Bit | Name | Description |
|---|---|---|
| 1:0 | SVID_ADDR_RAIL_C | SVID domain address setting for Rail C,<br>00: SVID domain address of Rail C is 00h.<br>01: SVID domain address of Rail C is 01h.<br>10: SVID domain address of Rail C is 02h.<br>11: SVID domain address of Rail C is 03h.<br>Duplicated SVID domain address of Rail A, Rail B and Rail C must be avoided. |

**Table 48. LPF_LIMIT_AB**

| **Address:** 0x2D | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | 1_PH_LPF_LIMIT_A | | MULTI_PH _LPF_LIMIT_A | | 1_PH_LPF_LIMIT_B | | MULTI_PH _LPF_LIMIT_B | |
| Default | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| Type | RW | | RW | | RW | | RW | |

| Bit | Name | Description |
|---|---|---|
| 7:6 | 1_PH_LPF_LIMIT_A | Selection of LPF threshold to avoid voltage drop in the range of high frequency for 1-phase operation of Rail A.<br>00: 60mV.<br>01: 80mV.<br>10: 100mV.<br>11: Disable. |
| 5:4 | MULTI_PH _LPF_LIMIT_A | Selection of LPF threshold to avoid voltage drop in the range of high frequency for multi-phase operation of Rail A.<br>00: Disable.<br>01: 200mV.<br>10: 300mV.<br>11: 400mV. |
| 3:2 | 1_PH_LPF_LIMIT_B | Selection of LPF threshold to avoid voltage drop in the range of high frequency for 1-phase operation of Rail B.<br>00: 60mV.<br>01: 80mV.<br>10: 100mV.<br>11: Disable. |
| 1:0 | MULTI_PH _LPF_LIMIT_B | Selection of LPF threshold to avoid voltage drop in the range of high frequency for multi-phase operation of Rail B.<br>00: Disable.<br>01: 200mV.<br>10: 300mV.<br>11: 400mV. |

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**Table 49. ZCD_HYS_OFST_A**

| **Address:** 0x2E | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | ZCD_HYS_A | | ZCD_OFFSET_A | | | | | |
| Default | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Type | RW | | RW | | | | | |

| Bit | Name | Description |
|---|---|---|
| 7:6 | ZCD_HYS_A | Selection of ZCD hysteresis for Rail A.<br>ZCD_HYS = 0.208mV/step<br>[00]: 0mV<br>[01]: 0.208mV<br>[10]: 0.417mV<br>[11]: 0.625mV |
| 5:0 | ZCD_OFFSET_A | Selection of the additional ZCD offset for Rail A.<br>The additional ZCD offset is set as multiple by ZCD_OFFSET_A in decimal.<br>[5]: sign bit, 0 is positive<br>ZCD_OFFSET = 0.104mV/step<br>[000001]: 0.104mV<br>[001100]: 1.25mV<br>[100001]: –0.104mV<br>[101100]: –1.25mV |

**Table 50. ZCD_HYS_OFST_B**

| **Address:** 0x2F | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | ZCD_HYS_B | | ZCD_OFFSET_B | | | | | |
| Default | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| Type | RW | | RW | | | | | |

| Bit | Name | Description |
|---|---|---|
| 7:6 | ZCD_HYS_B | Selection of ZCD hysteresis for Rail B.<br>ZCD_HYS = 0.208mV/step<br>[00]: 0mV<br>[01]: 0.208mV<br>[10]: 0.417mV<br>[11]: 0.625mV |
| 5:0 | ZCD_OFFSET_B | Selection of the additional ZCD offset for Rail B.<br>The additional ZCD offset is set as multiple by ZCD_OFFSET_B in decimal.<br>[5]: sign bit, 0 is positive<br>ZCD_OFFSET = 0.104mV/step<br>[000001]: 0.104mV<br>[001100]: 1.25mV<br>[100001]: –0.104mV<br>[101100]: –1.25mV |

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**Table 51. VBOOT_VID_A**

| **Address:** 0x30 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | VBOOT_VID_A | | | | | | | |
| Default | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| Type | RW | | | | | | | |

| Bit | Name | Description |
|---|---|---|
| 7:0 | VBOOT_VID_A | Selection the non-zero VBOOT voltage for Rail A.<br><br>As 0x14 [7] = 0 (5mV VID step),<br>The non-zero VBOOT can be selected from 0.25V~1.52V corresponding to hexadecimal 0x01 to 0xFF via the equation below.<br>Non-zero VBOOT(V) = 0.245+0.005*(VBOOT_VID_A in decimal).<br><br>As 0x14 [7] = 1 (10mV VID step),<br>The non-zero VBOOT can be selected from 0.2V~2.2V corresponding to hexadecimal 0x01 to 0xC9 via the equation below.<br>Non-zero VBOOT(V) = 0.190+0.010*(VBOOT_VID_A in decimal).<br><br>Note that the VBOOT_VID_A = 0x00 is unacceptable. |

**Table 52. SD_GD_VID_A**

| **Address:** 0x31 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | SD_GD_VID_A | | | | | | | |
| Default | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| Type | RW | | | | | | | |

| Bit | Name | Description |
|---|---|---|
| 7:0 | SD_GD_VID_A | Selection the soldering good voltage for Rail A.<br><br>As 0x14 [7] = 0 (5mV VID step),<br>The soldering good voltage can be selected from 0.25V~1.52V corresponding to hexadecimal 0x01 to 0xFF via the equation below.<br>Soldering good voltage(V) = 0.245+0.005*(SD_GD_VID_A in decimal).<br><br>As 0x14 [7] = 1 (10mV VID step),<br>The soldering good voltage can be selected from 0.2V~2.2V corresponding to hexadecimal 0x01 to 0xC9 via the equation below.<br>Soldering good voltage (V) = 0.190+0.010*(SD_GD_VID_A in decimal).<br><br>Note that the SD_GD_VID_A = 0x00 is unacceptable. |

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**Table 53. VBOOT_VID_B**

| **Address:** 0x32 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | VBOOT_VID_B | | | | | | | |
| Default | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| Type | RW | | | | | | | |

| Bit | Name | Description |
|---|---|---|
| 7:0 | VBOOT_VID_B | Selection the non-zero VBOOT voltage for Rail B.<br><br>As 0x14 [6] = 0 (5mV VID step),<br>The non-zero VBOOT can be selected from 0.25V~1.52V corresponding to hexadecimal 0x01 to 0xFF via the equation below.<br>Non-zero VBOOT(V) = 0.245+0.005*(VBOOT_VID_B in decimal).<br><br>As 0x14 [6] = 1 (10mV VID step),<br>The non-zero VBOOT can be selected from 0.2V~2.2V corresponding to hexadecimal 0x01 to 0xC9 via the equation below.<br>Non-zero VBOOT(V) = 0.190+0.010*(VBOOT_VID_B in decimal).<br><br>Note that the VBOOT_VID_B = 0x00 is unacceptable. |

**Table 54. SD_GD_VID_B**

| **Address:** 0x33 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | SD_GD_VID_B | | | | | | | |
| Default | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| Type | RW | | | | | | | |

| Bit | Name | Description |
|---|---|---|
| 7:0 | SD_GD_VID_B | Selection the soldering good voltage for Rail B.<br><br>As 0x14 [6] = 0 (5mV VID step),<br>The soldering good voltage can be selected from 0.25V~1.52V corresponding to hexadecimal 0x01 to 0xFF via the equation below.<br>Soldering good voltage(V) = 0.245+0.005*(SD_GD_VID_B in decimal).<br><br>As 0x14 [6] = 1 (10mV VID step),<br>The soldering good voltage can be selected from 0.2V~2.2V corresponding to hexadecimal 0x01 to 0xC9 via the equation below.<br>Soldering good voltage (V) = 0.190+0.010*(SD_GD_VID_B in decimal).<br><br>Note that the SD_GD_VID_B = 0x00 is unacceptable. |

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**Table 55. VBOOT_VID_C**

| **Address:** 0x34 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | VBOOT_VID_C | | | | | | | |
| Default | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| Type | RW | | | | | | | |

| Bit | Name | Description |
|---|---|---|
| 7:0 | VBOOT_VID_C | Selection the non-zero VBOOT voltage for Rail C.<br><br>As 0x14 [5] = 0 (5mV VID step),<br>The non-zero VBOOT can be selected from 0.25V~1.52V corresponding to hexadecimal 0x01 to 0xFF via the equation below.<br>Non-zero VBOOT(V) = 0.245+0.005*(VBOOT_VID_C in decimal).<br><br>As 0x14 [5] = 1 (10mV VID step),<br>The non-zero VBOOT can be selected from 0.2V~2.2V corresponding to hexadecimal 0x01 to 0xC9 via the equation below.<br>Non-zero VBOOT(V) = 0.190+0.010*(VBOOT_VID_C in decimal).<br><br>Note that the VBOOT_VID_C = 0x00 is unacceptable. |

**Table 56. SD_GD_VID_C**

| **Address:** 0x35 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | SD_GD_VID_C | | | | | | | |
| Default | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| Type | RW | | | | | | | |

| Bit | Name | Description |
|---|---|---|
| 7:0 | SD_GD_VID_C | Selection the soldering good voltage for Rail C.<br><br>As 0x14 [5] = 0 (5mV VID step),<br>The soldering good voltage can be selected from 0.25V~1.52V corresponding to hexadecimal 0x01 to 0xFF via the equation below.<br>Soldering good voltage(V) = 0.245+0.005*(SD_GD_VID_C in decimal).<br><br>As 0x14 [5] = 1 (10mV VID step),<br>The soldering good voltage can be selected from 0.2V~2.2V corresponding to hexadecimal 0x01 to 0xC9 via the equation below.<br>Soldering good voltage (V) = 0.190+0.010*(SD_GD_VID_C in decimal).<br><br>Note that the SD_GD_VID_C = 0x00 is unacceptable. |

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**Table 57. SPM_TH_A_1**

**Address:** 0x36
**Description:** Adjust smart phase management of Rail A for 3-phase to 4-phase operation.

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | Reserved | | | | SPM_TH4_A | | | |
| Default | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| Type | RW | | | | RW | | | |

| Bit | Name | Description |
|---|---|---|
| 7:4 | Reserved | Reserved bits. |
| 3:0 | SPM_TH4_A | Adjust SPM threshold for 3-phase to 4-phase of Rail A.<br>0000: SPM_TH4_A = 100% of ICCMAX_A,<br>0001: SPM_TH4_A = 90% of ICCMAX_A,<br>0010: SPM_TH4_A = 80% of ICCMAX_A,<br>0011: SPM_TH4_A = 70% of ICCMAX_A,<br>0100: SPM_TH4_A = 60% of ICCMAX_A,<br>0101: SPM_TH4_A = 50% of ICCMAX_A,<br>0110: SPM_TH4_A = 45% of ICCMAX_A,<br>0111: SPM_TH4_A = 40% of ICCMAX_A,<br>1000: SPM_TH4_A = 35% of ICCMAX_A,<br>1001: SPM_TH4_A = 30% of ICCMAX_A,<br>1010: SPM_TH4_A = 25% of ICCMAX_A,<br>1011: SPM_TH4_A = 20% of ICCMAX_A,<br>1100: SPM_TH4_A = 15% of ICCMAX_A,<br>1101: SPM_TH4_A = 10% of ICCMAX_A,<br>1110: SPM_TH4_A = 5% of ICCMAX_A,<br>1111: SPM_TH4_A = 2.5% of ICCMAX_A. |

**Table 58. SPM_TH_A_2**

**Address:** 0x37
**Description:** Adjust smart phase management of Rail A for 2-phase to 3-phase and 1-phase to 2-phase operation.

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | SPM_TH3_A | | | | SPM_TH2_A | | | |
| Default | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 |
| Type | RW | | | | RW | | | |

| Bit | Name | Description |
|---|---|---|
| 7:4 | SPM_TH3_A | Adjust SPM threshold for 2-phase to 3-phase of Rail A.<br>0000: SPM_TH3_A = 100% of ICCMAX_A,<br>0001: SPM_TH3_A = 90% of ICCMAX_A,<br>0010: SPM_TH3_A = 80% of ICCMAX_A,<br>0011: SPM_TH3_A = 70% of ICCMAX_A,<br>0100: SPM_TH3_A = 60% of ICCMAX_A,<br>0101: SPM_TH3_A = 50% of ICCMAX_A,<br>0110: SPM_TH3_A = 45% of ICCMAX_A,<br>0111: SPM_TH3_A = 40% of ICCMAX_A,<br>1000: SPM_TH3_A = 35% of ICCMAX_A,<br>1001: SPM_TH3_A = 30% of ICCMAX_A,<br>1010: SPM_TH3_A = 25% of ICCMAX_A,<br>1011: SPM_TH3_A = 20% of ICCMAX_A,<br>1100: SPM_TH3_A = 15% of ICCMAX_A, |

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| Bit | Name | Description |
|---|---|---|
| | | 1101: SPM_TH3_A = 10% of ICCMAX_A,<br>1110: SPM_TH3_A = 5% of ICCMAX_A,<br>1111: SPM_TH3_A = 2.5% of ICCMAX_A. |
| 3:0 | SPM_TH2_A | Adjust SPM threshold for 1-phase to 2-phase of Rail A.<br>0000: SPM_TH2_A = 100% of ICCMAX_A,<br>0001: SPM_TH2_A = 90% of ICCMAX_A,<br>0010: SPM_TH2_A = 80% of ICCMAX_A,<br>0011: SPM_TH2_A = 70% of ICCMAX_A,<br>0100: SPM_TH2_A = 60% of ICCMAX_A,<br>0101: SPM_TH2_A = 50% of ICCMAX_A,<br>0110: SPM_TH2_A = 45% of ICCMAX_A,<br>0111: SPM_TH2_A = 40% of ICCMAX_A,<br>1000: SPM_TH2_A = 35% of ICCMAX_A,<br>1001: SPM_TH2_A = 30% of ICCMAX_A,<br>1010: SPM_TH2_A = 25% of ICCMAX_A,<br>1011: SPM_TH2_A = 20% of ICCMAX_A,<br>1100: SPM_TH2_A = 15% of ICCMAX_A,<br>1101: SPM_TH2_A = 10% of ICCMAX_A,<br>1110: SPM_TH2_A = 5% of ICCMAX_A,<br>1111: SPM_TH2_A = 2.5% of ICCMAX_A. |

**Table 59. SPM_HYS_A_1**

**Address:** 0x38
**Description:** Adjust smart phase management hysteresis threshold of Rail A for 4-phase to 3-phase operation.

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | EN_SPM_HYS_DOUBLE_A | Reserved | | | | SPM_HYS4_A | | |
| Default | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| Type | RW | RW | | | | RW | | |

| Bit | Name | Description |
|---|---|---|
| 7 | EN_SPM_HYS_DOUBLE_A | Enable SPM hysteresis threshold x2 of Rail A.<br>0: Disable.<br>1: Enable. |
| 6:3 | Reserved | Reserved bits |
| 2:0 | SPM_HYS4_A | Adjust SPM hysteresis threshold for 4-phase to 3-phase operation of Rail A.<br><br>As EN_SPM_HYS_DOUBLE_A = 0<br>000: SPM_HYS4_A = 0% of ICCMAX_A<br>001: SPM_HYS4_A = 2.5% of ICCMAX_A<br>010: SPM_HYS4_A = 5% of ICCMAX_A<br>011: SPM_HYS4_A = 7.5% of ICCMAX_A<br>100: SPM_HYS4_A = 10% of ICCMAX_A<br>101: SPM_HYS4_A = 12.5% of ICCMAX_A<br>110: SPM_HYS4_A = 15% of ICCMAX_A<br>111: SPM_HYS4_A = 17.5% of ICCMAX_A<br><br>As EN_SPM_HYS_DOUBLE_A = 1<br>000: SPM_HYS4_A = 0% of ICCMAX_A<br>001: SPM_HYS4_A = 5% of ICCMAX_A |

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| Bit | Name | Description |
|---|---|---|
| | | 010: SPM_HYS4_A = 10% of ICCMAX_A<br>011: SPM_HYS4_A = 15% of ICCMAX_A<br>100: SPM_HYS4_A = 20% of ICCMAX_A<br>101: SPM_HYS4_A = 25% of ICCMAX_A<br>110: SPM_HYS4_A = 30% of ICCMAX_A<br>111: SPM_HYS4_A = 35% of ICCMAX_A |

**Table 60. SPM_HYS_A_2_REV_ID**

**Address:** 0x39
**Description:** Adjust smart phase management hysteresis threshold of Rail A for 3-phase to 2-phase and 2-phase to 1-phase operation.

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | SPM_HYS3_A | | | SPM_HYS2_A | | | Reserved | |
| Default | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| Type | RW | | | RW | | | RW | |

| Bit | Name | Description |
|---|---|---|
| 7:5 | SPM_HYS3_A | Adjust SPM hysteresis threshold for 3-phase to 2-phase operation of Rail A.<br><br>As EN_SPM_HYS_DOUBLE_A = 0<br>000: SPM_HYS3_A = 0% of ICCMAX_A<br>001: SPM_HYS3_A = 2.5% of ICCMAX_A<br>010: SPM_HYS3_A = 5% of ICCMAX_A<br>011: SPM_HYS3_A = 7.5% of ICCMAX_A<br>100: SPM_HYS3_A = 10% of ICCMAX_A<br>101: SPM_HYS3_A = 12.5% of ICCMAX_A<br>110: SPM_HYS3_A = 15% of ICCMAX_A<br>111: SPM_HYS3_A = 17.5% of ICCMAX_A<br><br>As EN_SPM_HYS_DOUBLE_A = 1<br>000: SPM_HYS3_A = 0% of ICCMAX_A<br>001: SPM_HYS3_A = 5% of ICCMAX_A<br>010: SPM_HYS3_A = 10% of ICCMAX_A<br>011: SPM_HYS3_A = 15% of ICCMAX_A<br>100: SPM_HYS3_A = 20% of ICCMAX_A<br>101: SPM_HYS3_A = 25% of ICCMAX_A<br>110: SPM_HYS3_A = 30% of ICCMAX_A<br>111: SPM_HYS3_A = 35% of ICCMAX_A |

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| Bit | Name | Description |
|---|---|---|
| 4:2 | SPM_HYS2_A | Adjust SPM hysteresis threshold for 2-phase to 1-phase operation of Rail A.<br><br>As EN_SPM_HYS_DOUBLE_A = 0<br>000: SPM_HYS2_A = 0% of ICCMAX_A<br>001: SPM_HYS2_A = 2.5% of ICCMAX_A<br>010: SPM_HYS2_A = 5% of ICCMAX_A<br>011: SPM_HYS2_A = 7.5% of ICCMAX_A<br>100: SPM_HYS2_A = 10% of ICCMAX_A<br>101: SPM_HYS2_A = 12.5% of ICCMAX_A<br>110: SPM_HYS2_A = 15% of ICCMAX_A<br>111: SPM_HYS2_A = 17.5% of ICCMAX_A<br><br>As EN_SPM_HYS_DOUBLE_A = 1<br>000: SPM_HYS2_A = 0% of ICCMAX_A<br>001: SPM_HYS2_A = 5% of ICCMAX_A<br>010: SPM_HYS2_A = 10% of ICCMAX_A<br>011: SPM_HYS2_A = 15% of ICCMAX_A<br>100: SPM_HYS2_A = 20% of ICCMAX_A<br>101: SPM_HYS2_A = 25% of ICCMAX_A<br>110: SPM_HYS2_A = 30% of ICCMAX_A<br>111: SPM_HYS2_A = 35% of ICCMAX_A |
| 1:0 | Reserved | Reserved bits |

**Table 61. SPM_PH_CTRL_A**

**Address:** 0x3A
**Description:** The sequence adjustment and the timing control for phase shedding and phase adding of Rail A.

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | SPM_DOWN_PH_DELAY_A | | EN_SPM_STEP_DN_PH_A | EN_SPM_QR_FULL_PH_A | Reserved | | | |
| Default | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| Type | RW | | RW | RW | RW | | | |

| Bit | Name | Description |
|---|---|---|
| 7:6 | SPM_DOWN_PH_DELAY_A | The delay time setting for each phase shedding of Rail A.<br>00: 6μs<br>01: 4.5μs<br>10: 3μs<br>11: 1.5μs |
| 5 | EN_SPM_STEP_DN_PH_A | Enable/Disable SPM phase down to target phase by step for Rail A.<br>0: SPM phase down to target phase directly.<br>e.g. 4PH→2PH.<br><br>1: SPM phase down to target phase by step.<br>e.g. 4PH→3PH→2PH. |
| 4 | EN_SPM_QR_FULL_PH_A | Enable/Disable full-phase operation as quick response is triggered for Rail A.<br>0: Keep current phase number as quick response is triggered.<br>1: Turn all phases on as quick response is triggered. |
| 3:0 | Reserved | Reserved bits |

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**Table 62. SPM_TH_B**

**Address:** 0x3B
**Description:** Adjust smart phase management of Rail B for 2-phase to 3-phase and 1-phase to 2-phase operation.

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | SPM_TH3_B | | | | SPM_TH2_B | | | |
| Default | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 |
| Type | RW | | | | RW | | | |

| Bit | Name | Description |
|---|---|---|
| 7:4 | SPM_TH3_B | Adjust SPM threshold for 2-phase to 3-phase of Rail B.<br>0000: SPM_TH3_B = 100% of ICCMAX_B,<br>0001: SPM_TH3_B = 90% of ICCMAX_B,<br>0010: SPM_TH3_B = 80% of ICCMAX_B,<br>0011: SPM_TH3_B = 70% of ICCMAX_B,<br>0100: SPM_TH3_B = 60% of ICCMAX_B,<br>0101: SPM_TH3_B = 50% of ICCMAX_B,<br>0110: SPM_TH3_B = 45% of ICCMAX_B,<br>0111: SPM_TH3_B = 40% of ICCMAX_B,<br>1000: SPM_TH3_B = 35% of ICCMAX_B,<br>1001: SPM_TH3_B = 30% of ICCMAX_B,<br>1010: SPM_TH3_B = 25% of ICCMAX_B,<br>1011: SPM_TH3_B = 20% of ICCMAX_B,<br>1100: SPM_TH3_B = 15% of ICCMAX_B,<br>1101: SPM_TH3_B = 10% of ICCMAX_B,<br>1110: SPM_TH3_B = 5% of ICCMAX_B,<br>1111: SPM_TH3_B = 2.5% of ICCMAX_B. |
| 3:0 | SPM_TH2_B | Adjust SPM threshold for 1-phase to 2-phase of Rail B.<br>0000: SPM_TH2_B = 100% of ICCMAX_B,<br>0001: SPM_TH2_B = 90% of ICCMAX_B,<br>0010: SPM_TH2_B = 80% of ICCMAX_B,<br>0011: SPM_TH2_B = 70% of ICCMAX_B,<br>0100: SPM_TH2_B = 60% of ICCMAX_B,<br>0101: SPM_TH2_B = 50% of ICCMAX_B,<br>0110: SPM_TH2_B = 45% of ICCMAX_B,<br>0111: SPM_TH2_B = 40% of ICCMAX_B,<br>1000: SPM_TH2_B = 35% of ICCMAX_B,<br>1001: SPM_TH2_B = 30% of ICCMAX_B,<br>1010: SPM_TH2_B = 25% of ICCMAX_B,<br>1011: SPM_TH2_B = 20% of ICCMAX_B,<br>1100: SPM_TH2_B = 15% of ICCMAX_B,<br>1101: SPM_TH2_B = 10% of ICCMAX_B,<br>1110: SPM_TH2_B = 5% of ICCMAX_B,<br>1111: SPM_TH2_B = 2.5% of ICCMAX_B. |

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**Table 63. SPM_HYS_B**

**Address:** 0x3C
**Description:** Adjust smart phase management hysteresis threshold of Rail B for 3-phase to 2-phase and 2-phase to 1-phase operation.

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | EN_SPM_HYS_DOUBLE_B | Reserved | SPM_HYS3_B | | | SPM_HYS2_B | | |
| Default | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| Type | RW | RW | RW | | | RW | | |

| Bit | Name | Description |
|---|---|---|
| 7 | EN_SPM_HYS_DOUBLE_B | Enable SPM hysteresis threshold x2 of Rail B.<br>0: Disable.<br>1: Enable. |
| 6 | Reserved | Reserved bit. |
| 5:3 | SPM_HYS3_B | Adjust SPM hysteresis threshold for 3-phase to 2-phase operation of Rail B.<br><br>As EN_SPM_HYS_DOUBLE_B = 0<br>000: SPM_HYS3_B = 0% of ICCMAX_B<br>001: SPM_HYS3_B = 2.5% of ICCMAX_B<br>010: SPM_HYS3_B = 5% of ICCMAX_B<br>011: SPM_HYS3_B = 7.5% of ICCMAX_B<br>100: SPM_HYS3_B = 10% of ICCMAX_B<br>101: SPM_HYS3_B = 12.5% of ICCMAX_B<br>110: SPM_HYS3_B = 15% of ICCMAX_B<br>111: SPM_HYS3_B = 17.5% of ICCMAX_B<br><br>As EN_SPM_HYS_DOUBLE_B = 1<br>000: SPM_HYS3_B = 0% of ICCMAX_B<br>001: SPM_HYS3_B = 5% of ICCMAX_B<br>010: SPM_HYS3_B = 10% of ICCMAX_B<br>011: SPM_HYS3_B = 15% of ICCMAX_B<br>100: SPM_HYS3_B = 20% of ICCMAX_B<br>101: SPM_HYS3_B = 25% of ICCMAX_B<br>110: SPM_HYS3_B = 30% of ICCMAX_B<br>111: SPM_HYS3_B = 35% of ICCMAX_B |
| 2:0 | SPM_HYS2_B | Adjust SPM hysteresis threshold for 2-phase to 1-phase operation of Rail B.<br><br>As EN_SPM_HYS_DOUBLE_B = 0<br>000: SPM_HYS2_B = 0% of ICCMAX_B<br>001: SPM_HYS2_B = 2.5% of ICCMAX_B<br>010: SPM_HYS2_B = 5% of ICCMAX_B<br>011: SPM_HYS2_B = 7.5% of ICCMAX_B<br>100: SPM_HYS2_B = 10% of ICCMAX_B<br>101: SPM_HYS2_B = 12.5% of ICCMAX_B<br>110: SPM_HYS2_B = 15% of ICCMAX_B<br>111: SPM_HYS2_B = 17.5% of ICCMAX_B<br><br>As EN_SPM_HYS_DOUBLE_B = 1<br>000: SPM_HYS2_B = 0% of ICCMAX_B<br>001: SPM_HYS2_B = 5% of ICCMAX_B<br>010: SPM_HYS2_B = 10% of ICCMAX_B<br>011: SPM_HYS2_B = 15% of ICCMAX_B<br>100: SPM_HYS2_B = 20% of ICCMAX_B<br>101: SPM_HYS2_B = 25% of ICCMAX_B<br>110: SPM_HYS2_B = 30% of ICCMAX_B<br>111: SPM_HYS2_B = 35% of ICCMAX_B |

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**Table 64. SPM_PH_CTRL_B**

**Address:** 0x3D
**Description:** The sequence adjustment and the timing control for phase shedding and phase adding of Rail B.

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | SPM_DOWN_PH_DELAY_B | | EN_SPM_STEP_DN_PH_B | EN_SPM_QR_FULL_PH_B | Reserved | | | |
| Default | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 |
| Type | RW | | RW | RW | RW | | | |

| Bit | Name | Description |
|---|---|---|
| 7:6 | SPM_DOWN_PH_DELAY_B | The delay time setting for each phase shedding of Rail B.<br>00: 6μs<br>01: 4.5μs<br>10: 3μs<br>11: 1.5μs |
| 5 | EN_SPM_STEP_DN_PH_B | Enable/Disable SPM phase down to target phase by step for Rail B.<br>0: SPM phase down to target phase directly.<br>e.g. 3PH→1PH.<br><br>1: SPM phase down to target phase by step.<br>e.g. 3PH→2PH→1PH. |
| 4 | EN_SPM_QR_FULL_PH_B | Enable/Disable full-phase operation as quick response is triggered for Rail B.<br>0: Keep current phase number as quick response is triggered.<br>1: Turn all phases on as quick response is triggered. |
| 3:0 | Reserved | [3:0] = 0000. All other combinations are not defined. |

**Table 65. ANS_EN_SPM_PSK_CTRL**

**Address:** 0x3E
**Description:** Enable/Disable decay slow down function (acoustic noise suppression, ANS_EN). DCM control in SPM.

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | Reserved | EN_SPM_PS2_EXIT_RST_LPF_A | EN_SPM_PS2_EXIT_RST_LPF_B | EN_SPM_PS2_EXIT_RST_LPF_C | Reserved | SPM_ENTER_TON_SEL_A | SPM_ENTER_TON_SEL_B | SPM_ENTER_TON_SEL_C |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Type | RW | RW | RW | RW | RW | RW | RW | RW |

| Bit | Name | Description |
|---|---|---|
| 7 | Reserved | Reserved bit |
| 6 | EN_SPM_PS2_EXIT_RST_LPF_A | Enable/Disable the resetting of LPF at exiting PS2 to avoid undershoot in SPM operation for Rail A.<br>0: Disable.<br>1: Enable. |
| 5 | EN_SPM_PS2_EXIT_RST_LPF_B | Enable/Disable the resetting of LPF at exiting PS2 to avoid undershoot in SPM operation for Rail B.<br>0: Disable.<br>1: Enable. |

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| Bit | Name | Description |
|---|---|---|
| 4 | EN_SPM_PS2_EXIT_RST_LPF_C | Enable/Disable the resetting of LPF at exiting PS2 to avoid undershoot in SPM operation for Rail C.<br>0: Disable.<br>1: Enable. |
| 3 | Reserved | Reserved bit. |
| 2 | SPM_ENTER_TON_SEL_A | Enable/Disable the fast entering of DCM in SPM operation for Rail A.<br>0: Disable, entering DCM from CCM after 2x PWM Ton have been counted.<br>1: Enable, entering DCM from CCM after 4x PWM Ton have been counted. |
| 1 | SPM_ENTER_TON_SEL_B | Enable/Disable the fast entering of DCM in SPM operation for Rail B.<br>0: Disable, entering DCM from CCM after 2x PWM Ton have been counted.<br>1: Enable, entering DCM from CCM after 4x PWM Ton have been counted. |
| 0 | SPM_ENTER_TON_SEL_C | Enable/Disable the fast entering of DCM in SPM operation for Rail C.<br>0: Disable, entering DCM from CCM after 2x PWM Ton have been counted.<br>1: Enable, entering DCM from CCM after 4x PWM Ton have been counted. |

**Table 66. Reserved**

| **Address:** 0x3F<br>**Description:** Registers of 0x3F is reserved. | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | Reserved | | | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Type | RW | | | | | | | |

| Bit | Name | Description |
|---|---|---|
| 7:0 | Reserved | Reserved bits. |

**Table 67. SET_FW_VER_LSB**

| **Address:** 0x70 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | GROUP_1_FW_VER_LSB | | | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Type | RW | | | | | | | |

| Bit | Name | Description |
|---|---|---|
| 7:0 | GROUP_1_FW_VER_LSB | The least significant bits of the FW version of the Set Page (GROUP_1) (0x00~0x7E). |

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**Table 68. SET_FW_VER_MSB**

| **Address:** 0x71 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | GROUP_1_FW_VER_MSB | | | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Type | RW | | | | | | | |

| Bit | Name | Description |
|---|---|---|
| 7:0 | GROUP_1_FW_VER_MSB | The most significant bits of the FW version of the Set Page (GROUP_1) (0x00~0x7E). |

**Table 69. Reserved**

| **Address:** 0x72 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | Reserved | | | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Type | RW | | | | | | | |

| Bit | Name | Description |
|---|---|---|
| 7:0 | Reserved | Reserved bits. |

**Table 70. Reserved**

| **Address:** 0x73 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | Reserved | | | | | | | |
| Default | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| Type | RW | | | | | | | |

| Bit | Name | Description |
|---|---|---|
| 7:0 | Reserved | [7:0] = 00110100. All other combinations are not defined. |

**Table 71. MODEL_ID**

| **Address:** 0x74 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | MODEL_ID | | | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Type | RW | | | | | | | |

| Bit | Name | Description |
|---|---|---|
| 7:0 | MODEL_ID | Model ID. |

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**Table 72. Reserved**

| **Address:** 0x7A | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | Reserved | | | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| Type | RW | | | | | | | |

| Bit | Name | Description |
|---|---|---|
| 7:0 | Reserved | [2:0] = 011. All other combinations are not defined. |

**Table 73. Reserved**

| **Address:** 0x7B | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | Reserved | | | | | | | |
| Default | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| Type | RW | | | | | | | |

| Bit | Name | Description |
|---|---|---|
| 7:0 | Reserved | [7:0] = 01000000. All other combinations are not defined. |

**Table 74. Reserved**

| **Address:** 0x7C | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | Reserved | | | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Type | RW | | | | | | | |

| Bit | Name | Description |
|---|---|---|
| 7:0 | Reserved | [7:0] = 00000000. All other combinations are not defined. |

**Table 75. Reserved**

| **Address:** 0x7D | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | Reserved | | | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Type | RW | | | | | | | |

| Bit | Name | Description |
|---|---|---|
| 7:0 | Reserved | Reserved bits. |

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**Table 76. CRC _PAGE_GROUP_1**

| **Address:** 0x7E | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | CRC _PAGE_GROUP_1 | | | | | | | |
| Default | N/A | | | | | | | |
| Type | R | | | | | | | |

| Bit | Name | Description |
|---|---|---|
| 7:0 | CRC_PAGE_GROUP_1 | The cyclic redundancy code (CRC) of the data in the user configurable Set Page (GROUP_1). |

**Table 77. CBG_A_1**

| **Address:** 0x90<br>**Description:** Adjust phase 1, phase 2 and phase 3 current balance gain of Rail A. | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | CBG1_A | | | CBG2_A | | | CBG3_A_MSB | |
| Default | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| Type | RW | | | RW | | | RW | |

| Bit | Name | Description |
|---|---|---|
| 7:5 | CBG1_A | Adjust phase 1 current balance gain of Rail A<br>000: 69.2%,<br>001: 76.9%,<br>010: 84.6%,<br>011: 92.3%,<br>100: 100% (default),<br>101: 107.69%,<br>110: 115.38%,<br>111: 123.08%. |
| 4:2 | CBG2_A | Adjust phase 2 current balance gain of Rail A<br>000: 69.2%,<br>001: 76.9%,<br>010: 84.6%,<br>011: 92.3%,<br>100: 100% (default),<br>101: 107.69%,<br>110: 115.38%,<br>111: 123.08%. |
| 1:0 | CBG3_A_MSB | Adjust phase 3 current balance gain of Rail A,<br>CBG3_A<br>= (CBG3_A_MSB: CBG3_A_LSB)<br>(0x90[1:0]: 0x91[7]) = 000: 69.2%,<br>(0x90[1:0]: 0x91[7]) = 001: 76.9%,<br>(0x90[1:0]: 0x91[7]) = 010: 84.6%,<br>(0x90[1:0]: 0x91[7]) = 011: 92.3%,<br>(0x90[1:0]: 0x91[7]) = 100: 100% (default),<br>(0x90[1:0]: 0x91[7]) = 101: 107.69%,<br>(0x90[1:0]: 0x91[7]) = 110: 115.38%,<br>(0x90[1:0]: 0x91[7]) = 111: 123.08%. |

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**Table 78. CBG_A_2**

| **Address:** 0x91<br>**Description:** Adjust phase 3 and phase 4 current balance gain of Rail A. | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | CBG3_A_LSB | CBG4_A | | | Reserved | | | |
| Default | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| Type | RW | RW | | | RW | | | |

| Bit | Name | Description |
|---|---|---|
| 7 | CBG3_A_LSB | Adjust phase 3 current balance gain of Rail A,<br>CBG3_A<br>= (CBG3_A_MSB: CBG3_A_LSB)<br>(0x90[1:0]: 0x91[7]) = 000: 69.2%,<br>(0x90[1:0]: 0x91[7]) = 001: 76.9%,<br>(0x90[1:0]: 0x91[7]) = 010: 84.6%,<br>(0x90[1:0]: 0x91[7]) = 011: 92.3%,<br>(0x90[1:0]: 0x91[7]) = 100: 100% (default),<br>(0x90[1:0]: 0x91[7]) = 101: 107.69%,<br>(0x90[1:0]: 0x91[7]) = 110: 115.38%,<br>(0x90[1:0]: 0x91[7]) = 111: 123.08%. |
| 6:4 | CBG4_A | Adjust phase 4 current balance gain of Rail A<br>000: 69.2%,<br>001: 76.9%,<br>010: 84.6%,<br>011: 92.3%,<br>100: 100% (default),<br>101: 107.69%,<br>110: 115.38%,<br>111: 123.08%. |
| 3:0 | Reserved | Reserved bits. |

**Table 79. REV_ID**

| **Address:** 0x95<br>**Description:** Revision ID. | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | Reserved | | | Reserved | | | REVISION_ID | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Type | RW | | | RW | | | RW | |

| Bit | Name | Description |
|---|---|---|
| 7:5 | Reserved | Reserved bits |
| 4:2 | Reserved | Reserved bits |
| 1:0 | REVISION_ID | Revision ID. |

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**Table 80. GROUP_0_FW_VER**

**Address:** 0x96
**Description:** FW version of GROUP_0.

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | Reserved | | Reserved | Reserved | GROUP_0_FW_VER | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Type | RW | | RW | RW | RW | | | |

| Bit | Name | Description |
|---|---|---|
| 7:6 | Reserved | Reserved bits |
| 5 | Reserved | Reserved bits |
| 4 | Reserved | Reserved bits |
| 3:0 | GROUP_0_FW_VER | The FW version of the Page GROUP_0(0x90~0x9E). |

**Table 81. CBG_B_1**

**Address:** 0x97
**Description:** Adjust phase 1, phase 2 and phase 3 current balance gain of Rail B.

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | CBG1_B | | | CBG2_B | | | CBG3_B_MSB | |
| Default | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| Type | RW | | | RW | | | RW | |

| Bit | Name | Description |
|---|---|---|
| 7:5 | CBG1_B | Adjust phase 1 current balance gain of Rail B.<br>000: 69.2%,<br>001: 76.9%,<br>010: 84.6%,<br>011: 92.3%,<br>100: 100% (default),<br>101: 107.69%,<br>110: 115.38%,<br>111: 123.08%. |
| 4:2 | CBG2_B | Adjust phase 2 current balance gain of Rail B.<br>000: 69.2%,<br>001: 76.9%,<br>010: 84.6%,<br>011: 92.3%,<br>100: 100% (default),<br>101: 107.69%,<br>110: 115.38%,<br>111: 123.08%. |
| 1:0 | CBG3_B_MSB | Adjust phase 3 current balance gain of Rail B,<br>CBG3_B = (CBG3_B_MSB: CBG3_B_LSB )<br>(0x97[1:0]: 0x98[7]) = 000: 69.2%,<br>(0x97[1:0]: 0x98[7]) = 001: 76.9%,<br>(0x97[1:0]: 0x98[7]) = 010: 84.6%,<br>(0x97[1:0]: 0x98[7]) = 011: 92.3%,<br>(0x97[1:0]: 0x98[7]) = 100: 100% (default),<br>(0x97[1:0]: 0x98[7]) = 101: 107.69%,<br>(0x97[1:0]: 0x98[7]) = 110: 115.38%,<br>(0x97[1:0]: 0x98[7]) = 111: 123.08% |

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**Table 82. CBG_B_2_PRODUCT_ID**

| **Address:** 0x98<br>**Description:** Adjust phase 3 current balance gain of Rail B; Product ID. | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | CBG3_B_LSB | PRODUCT_ID | | | | | | |
| Default | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| Type | RW | RW | | | | | | |

| Bit | Name | Description |
|---|---|---|
| 7 | CBG3_B_LSB | Adjust phase 3 current balance gain of Rail B,<br>CBG3_B = (CBG3_B_MSB: CBG3_B_LSB )<br>(0x97[1:0]: 0x98[7]) = 000: 69.2%,<br>(0x97[1:0]: 0x98[7]) = 001: 76.9%,<br>(0x97[1:0]: 0x98[7]) = 010: 84.6%,<br>(0x97[1:0]: 0x98[7]) = 011: 92.3%,<br>(0x97[1:0]: 0x98[7]) = 100: 100% (default),<br>(0x97[1:0]: 0x98[7]) = 101: 107.69%,<br>(0x97[1:0]: 0x98[7]) = 110: 115.38%,<br>(0x97[1:0]: 0x98[7]) = 111: 123.08% |
| 6:0 | PRODUCT_ID | Product ID.<br>[6:0] = 0110100. ALL other combinations not defined |

**Table 83. Reserved**

| **Address:** 0x9D | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | Reserved | | | | | | | |
| Default | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| Type | RW | | | | | | | |

| Bit | Name | Description |
|---|---|---|
| 7:0 | Reserved | [7:0] = 00111000. All other combinations are not defined. |

**Table 84. Reserved**

| **Address:** 0x9E | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | Reserved | | | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Type | RW | | | | | | | |

| Bit | Name | Description |
|---|---|---|
| 7:0 | Reserved | [7:0] = 00000000. All other combinations are not defined. |

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**Table 85. NVM_PROGRAM_STATUS**

**Address:** 0xEC
**Description:** NVM status indicator.

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | RESTORE_FLAG | STORE_FLAG | STORE_ALLOW | RESTORE_BUSY | STORE_BUSY | CRC_GROUP_1 | CRC_GROUP_0 | CRC_GP0_GP1 |
| Default | N/A | | | | | | | |
| Type | R | R | R | R | R | R | R | R |

| Bit | Name | Description |
|---|---|---|
| 7 | RESTORE_FLAG | 1: NVM restoring is done.<br>0: NVM restoring is not done. |
| 6 | STORE_FLAG | 1: NVM storing is done.<br>0: NVM storing is not done. |
| 5 | STORE_ALLOW | 1: NVM is allowed to be store.<br>0: NVM is not allowed to be store. |
| 4 | RESTORE_BUSY | 1: NVM restoring is busy.<br>0: NVM restoring is not busy. |
| 3 | STORE_BUSY | 1: NVM storing is busy.<br>0: NVM storing is not busy. |
| 2 | CRC_GROUP_1 | 1: GROUP_1 (0x00~0x7E) check is failed.<br>0: GROUP_1 (0x00~0x7E) check is passed. |
| 1 | CRC_GROUP_0 | 1: GROUP_0 (0x90~0x9E) check is failed.<br>0: GROUP_0 (0x90~0x9E) check is passed. |
| 0 | CRC_GP0_GP1 | 1: GROUP_0 or GROUP_1 check is failed.<br>0: GROUP_0 and GROUP_1 check are passed. |

**Table 86. STORE_RESTORE_CFG**

**Address:** 0xED
**Description:** Store command instructs the device to copy the entire contents of the Operating Memory to the matching locations in the non-volatile User Store memory. Restore command instructs the device to copy the entire contents of the non-volatile User Store memory to the matching locations in the Operating Memory. This command must be used only while all outputs are disabled.

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | STORE_RESTORE_CFG | | | | | | | |
| Default | N/A | | | | | | | |
| Type | W | | | | | | | |

| Bit | Name | Description |
|---|---|---|
| 7:0 | STORE_RESTORE_CFG | 0x66: Restore all storable register settings from NVM.<br><br>0xAA: Store all current storable register settings of GROUP_1 (0x00~0x7D) into NVM as new defaults.<br><br>All other combinations are not defined. |

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**Table 87. PAGE**

| **Address:** 0xEF<br>**Description:** Selects the register groups to receive the commands. Do not select page during the VR is operating in non-zero VID. | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | PAGE | | | | | | | |
| Default | 0x80 | | | | | | | |
| Type | RW | | | | | | | |

| Bit | Name | Description |
|---|---|---|
| 7:0 | PAGE | 0x80:<br>Functions of GROUP_0 (0x90~0x9E) are available.<br>Functions of GROUP_1 (0x00~0x7E) are not available.<br>Functions of SVID commands are available.<br><br>0x82:<br>Functions of GROUP_0 (0x90~0x9E) are available.<br>Functions of GROUP_1 (0x00~0x7E) are available.<br>Functions of SVID commands are not available.<br><br>All other combinations are not defined. |

**Table 88. ENTER_CONF_MODE**

| **Address:** 0xF1<br>**Description:** Command to enter the user configuration mode. | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | ENTER_CONF_MODE | | | | | | | |
| Default | N/A | | | | | | | |
| Type | W | | | | | | | |

| Bit | Name | Description |
|---|---|---|
| 7:0 | ENTER_CONF_MODE | 0x62 is not available.<br>Please contact Richtek to receive the password for the user configuration mode. |

**Table 89. UNLOCK_NVM**

| **Address:** 0xFC<br>**Description:** Unlock command for the NVM configuration settings. | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | UNLOCK_NVM | | | | | | | |
| Default | N/A | | | | | | | |
| Type | W | | | | | | | |

| Bit | Name | Description |
|---|---|---|
| 7:0 | UNLOCK_NVM | Unlock the NVM configuration settings.<br>Please contact Richtek to receive the unlock command for the NVM configuration setting. |

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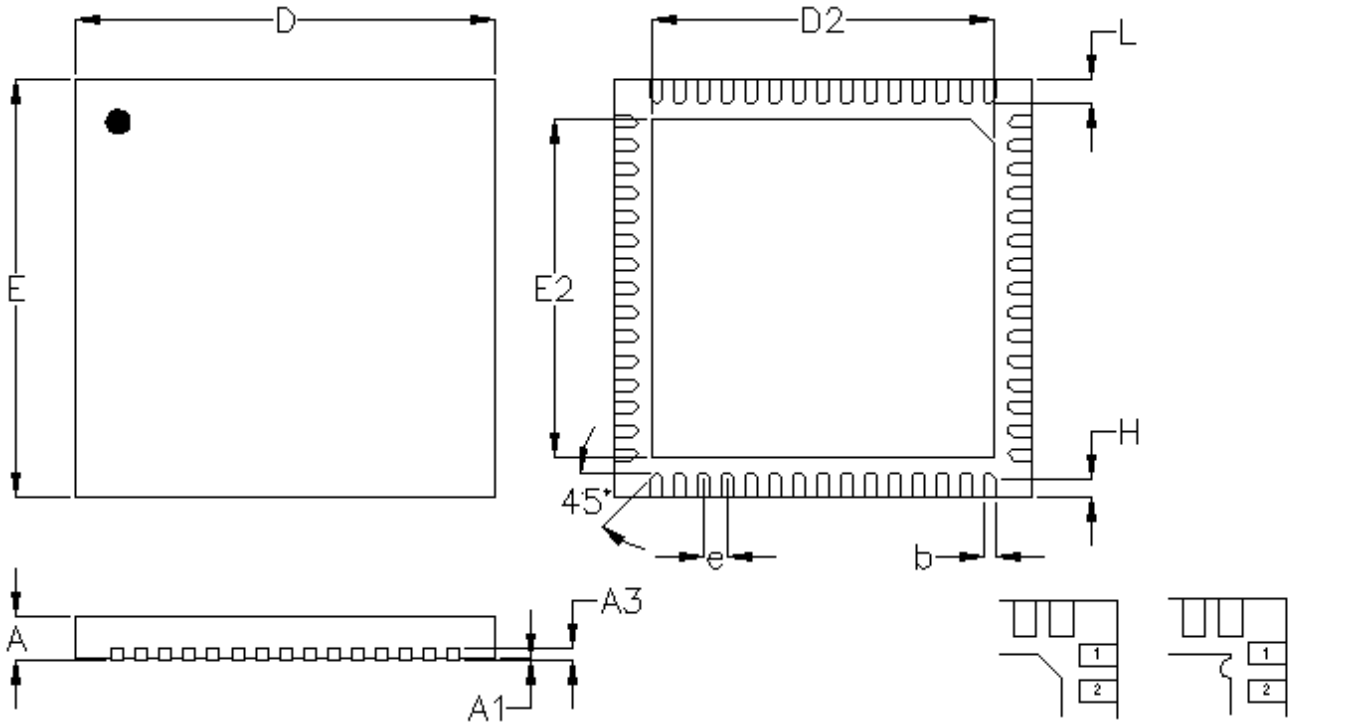
## Outline Dimension




**DETAIL A**

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min. | Max. | Min. | Max. |
| A | 0.700 | 0.800 | 0.028 | 0.031 |
| A1 | 0.000 | 0.050 | 0.000 | 0.002 |
| A3 | 0.175 | 0.250 | 0.007 | 0.010 |
| b | 0.150 | 0.250 | 0.006 | 0.010 |
| D | 6.900 | 7.100 | 0.272 | 0.280 |
| D2 | 5.650 | 5.750 | 0.222 | 0.226 |
| E | 6.900 | 7.100 | 0.272 | 0.280 |
| E2 | 5.650 | 5.750 | 0.222 | 0.226 |
| e | 0.400 | | 0.016 | |
| L | 0.350 | 0.450 | 0.014 | 0.018 |
| H | 0.250 | 0.350 | 0.010 | 0.014 |

**W-Type 60L QFN 7x7 Package**

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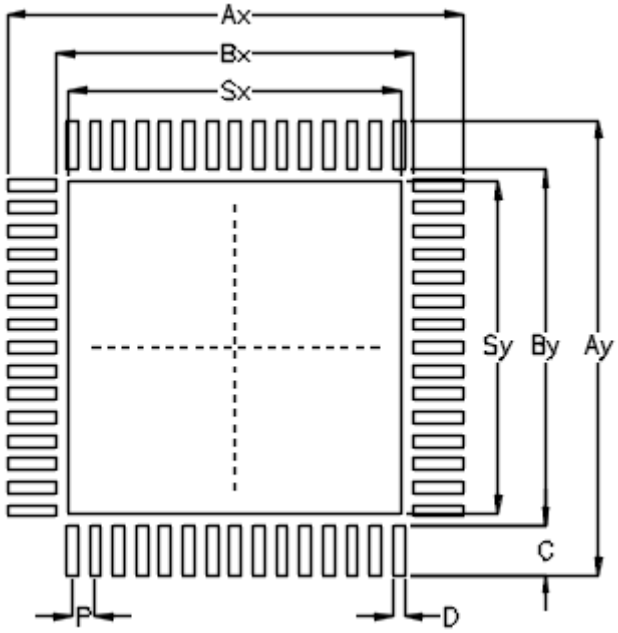
## Footprint Information




| Package | Number of Pin | Footprint Dimension (mm) | | | | | | | | | Tolerance |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | P | Ax | Ay | Bx | By | C | D | Sx | Sy | |
| V/W/U/XQFN7*7-60 | 60 | 0.40 | 7.80 | 7.80 | 6.10 | 6.10 | 0.85 | 0.20 | 5.70 | 5.70 | ±0.05 |

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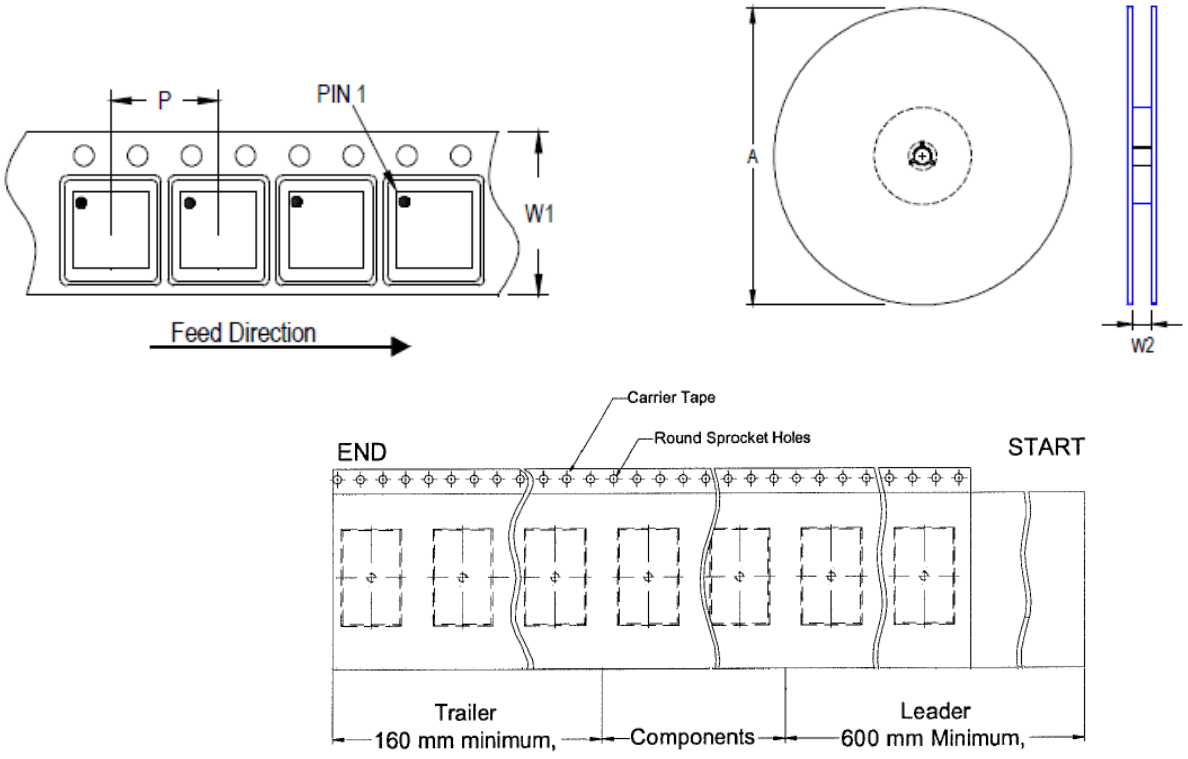
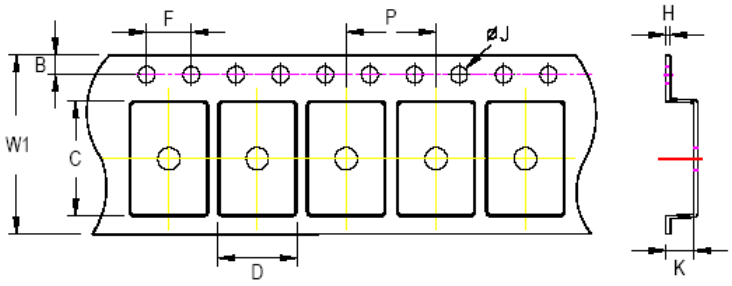
## Packing Information

### Tape and Reel Data




| Package Type | Tape Size (W1) (mm) | Pocket Pitch (P) (mm) | Reel Size (A) | | Units per Reel | Trailer (mm) | Leader (mm) | Reel Width (W2) Min./Max. (mm) |
|---|---|---|---|---|---|---|---|---|
| | | | (mm) | (in) | | | | |
| QFN/DFN 7x7 | 16 | 12 | 330 | 13 | 2,500 | 160 | 600 | 16.4/18.4 |




**C, D and K are determined by component size. The clearance between the components and the cavity is as follows:**

**- For 16mm carrier tape: 1.0mm max.**

| Tape Size | W1 | P | | B | | F | | ØJ | | H |
|---|---|---|---|---|---|---|---|---|---|---|
| | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Max. |
| 16mm | 16.3mm | 11.9mm | 12.1mm | 1.65mm | 1.85mm | 3.9mm | 4.1mm | 1.5mm | 1.6mm | 0.6mm |

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## Tape and Reel Packing

| Step | Photo/Description | Step | Photo/Description |
|---|---|---|---|
| 1 | Reel 13” | 4 | 1 reel per inner box **Box G** |
| 2 | HIC & Desiccant (2 Unit) inside | 5 | 6 inner boxes per outer box |
| 3 | Caution label is on backside of Al bag | 6 | Outer box **Carton A** |

| Container / Package | Reel | | Box | | | Carton | | |
|---|---|---|---|---|---|---|---|---|
| | Size | Units | Item | Reels | Units | Item | Boxes | Units |
| QFN and DFN 7x7 | 13” | 2,500 | Box G | 1 | 2,500 | Carton A | 6 | 15,000 |

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**Packing Material Anti-ESD Property**

| Surface Resistance | Aluminum Bag | Reel | Cover tape | Carrier tape | Tube | Protection Band |
|---|---|---|---|---|---|---|
| $\Omega/cm^2$ | **$10^4$ to $10^{11}$** | **$10^4$ to $10^{11}$** | **$10^4$ to $10^{11}$** | **$10^4$ to $10^{11}$** | **$10^4$ to $10^{11}$** | **$10^4$ to $10^{11}$** |

**Richtek Technology Corporation**
14F, No. 8, Tai Yuen 1st Street, Chupei City
Hsinchu, Taiwan, R.O.C.
Tel: (8863)5526789

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## Datasheet Revision History

| Version | Date | Description | Item |
|---|---|---|---|
| 00 | 2023/9/13 | Final | General Description on P1<br>Features on P1<br>Functional Pin Description on P3<br>Functional Register Description on P83 |
| 01 | 2023/11/8 | Modify | Functional Pin Description on P4<br>Typical Application Circuit on P12<br>Functional Register Description on P78, 79, 80, 83 |

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