

1A, 6V, Ultra-Low Dropout Linear Regulator

General Description

The RT2517B is a high performance positive voltage regulator designed for use in applications requiring ultra-low input voltage and ultra-low dropout voltage at up to 1A. The feature of ultra-low dropout voltage is ideal for the application where output voltage is very close to input voltage. The input voltage can be as low as 2.2V and the output voltage is adjustable by an external resistive divider. The RT2517B provides an excellent output voltage regulation over variations in line, load and temperature. Current limit and thermal shutdown protection functions are provided. Additionally, an enable pin is designed to further reduce power consumption while shutdown and the shutdown current is as low as 1.5 μ A.

The RT2517B is available in the SOP-8 (Exposed Pad) package.

Ordering Information

RT2517B	□□
	Package Type
SP	: SOP-8 (Exposed Pad-Option 2)
	Lead Plating System
G	: Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- ▶ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▶ Suitable for use in SnPb or Pb-free soldering processes.

Features

- AEC-Q100 Grade3 Certification
- Input Voltage Range : 2.2V to 6V
- V_{OUT} Range from 1.2V to $V_{IN} - V_{DROP}$
- Reference Voltage : 1.2V $\pm$ 2% over -40°C to 105°C
- Ultra-Low Dropout Voltage : 200mV at 1A over -40°C to 105°C
- Low Quiescent 1.5 μ A in Shutdown Mode
- Soft Discharge Functionality
- Thermal Shutdown and Current Limit
- RoHS Compliant and Halogen Free

Applications

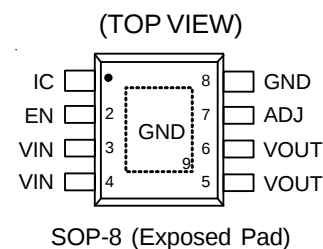
- Automotive Audio, Navigation, & Info systems
- Industrial Grade General Purpose Point of Load
- Digital Set top Boxes
- Vehicle Electronics

Marking Information

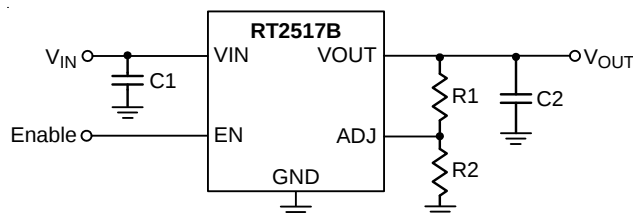
RT2517B
GSPYMDNN
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RT2517BGSP : Product Number
YMDNN : Date Code

Pin Configurations



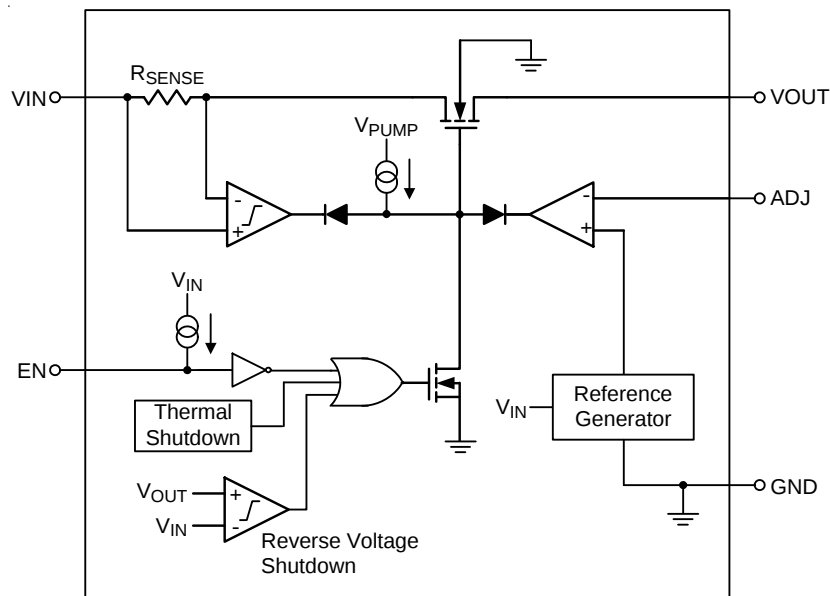
Simplified Application Circuit



Functional Pin Description

Pin No.	Pin Name	Pin Function
1	IC	Internal Connection. Leave floating and do not make connection to this pin.
2	EN	Chip Enable (Active High). This pin will be pulled up by internal circuit if this pin is open.
3,4	VIN	Supply Voltage Input. Connect a minimum 10 μ F ceramic capacitor at this pin.
5,6	VOUT	Output Voltage. A minimum 10 μ F capacitor should be placed directly at this pin.
7	ADJ	Feedback Voltage Input. Connect an external resistor divider to this pin for output voltage setting. If this pin is connected to the VOUT pin, the output voltage will be set at 1.2V.
8, 9 (Exposed pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum the power dissipation.

Function Block Diagram



Operation

The RT2517B is a linear regulator designed specially for ultra-low dropout voltage. The input voltage range is from 2.2V to 6V.

Output Transistor

The RT2517B builds in a MOSFET output transistor which provides a low switch-on resistance for low dropout voltage applications.

Error Amplifier

The Error Amplifier compares the internal reference voltage with the output feedback voltage from the internal divider, and controls the Gate voltage of MOSFET to support good line regulation and load regulation at output voltage.

Current Limit

The RT2517B provides current limit function to prevent the device from damages during over-load or short-circuit condition. This current is detected by an internal sensing device

Reference Generator

The RT2517B provides a reference voltage by internal reference generator circuit. The reference voltage can be used to determine the output voltage.

Thermal Shutdown

The thermal shutdown function will turn off the MOSFET when the junction temperature exceeds 160°C (typ.). Once the junction temperature cools down by approximately 10°C, the regulator will automatically resume operation.

Absolute Maximum Ratings (Note 1)

- Supply Voltage, V_{IN} ----- -0.3V to 7V
- Other Pins ----- -0.3V to 6V
- Power Dissipation, P_D @ $T_A = 25^\circ\text{C}$
 SOP-8 (Exposed Pad) ----- 2.041W
- Package Thermal Resistance (Note 2)
 SOP-8 (Exposed Pad), θ_{JA} ----- 49°C/W
 SOP-8 (Exposed Pad), θ_{JC} ----- 8°C/W
- Lead Temperature (Soldering, 10 sec.) ----- 260°C
- Junction Temperature ----- 150°C
- Storage Temperature Range ----- -65°C to 150°C
- ESD Susceptibility (Note 3)
 HBM (Human Body Model) ----- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, V_{IN} ----- 2.2V to 6V
- Junction Temperature Range ----- -40°C to 125°C

Electrical Characteristics

($V_{IN} = 2.2\text{V}$ to 6V , $I_{OUT} = 10\mu\text{A}$ to 1A , $V_{ADJ} = V_{OUT}$, $-40^\circ\text{C} \leq T_A \leq 105^\circ\text{C}$, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Shutdown Supply Current		I_{SHDN}	$V_{IN} = 3.3\text{V}$, $V_{EN} = 0\text{V}$	--	1	10	μA
Quiescent Current		I_Q	$V_{IN} = 3.3\text{V}$, $I_{OUT} = 0\text{A}$	--	0.7	1.5	mA
Line Regulation		ΔV_{LINE}	$I_{OUT} = 10\text{mA}$	--	--	0.4	%/V
Load Regulation		ΔV_{LOAD}	$I_{OUT} = 10\text{mA}$ to 1A	--	--	1	%
Current Limit		I_{LIM}	$V_{IN} = 3.3\text{V}$	1.05	--	2.8	A
Current Foldback Threshold		V_{Fold}	$V_{IN} = 3.3\text{V}$	0.3	--	0.5	V
Dropout Voltage		V_{DROP}	$I_{OUT} = 1\text{A}$,	--	--	400	mV
ADJ Reference Voltage		V_{ADJ}	$V_{IN} = 3.3\text{V}$, $V_{ADJ} = V_{OUT}$, $I_{OUT} = 10\text{mA}$	1.176	1.2	1.224	V
ADJ Pin Current		I_{ADJ}	$V_{IN} = 3.3\text{V}$	--	--	400	nA
EN Input Voltage	Logic-High	V_{IH}	$V_{IN} = 3.3\text{V}$	1.6	--	--	V
	Logic-Low	V_{IL}	$V_{IN} = 3.3\text{V}$	--	--	0.4	
Enable Pin Current		I_{EN}	$V_{IN} = 6\text{V}$, $V_{EN} = 0\text{V}$	--	--	1	μA
Thermal Shutdown Temperature		T_{SD}		--	160	--	$^\circ\text{C}$
Thermal Shutdown Hysteresis		ΔT_{SD}		--	10	--	$^\circ\text{C}$

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at $T_A = 25^\circ\text{C}$ on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package. The PCB copper area with exposed pad is 70mm^2 .

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit

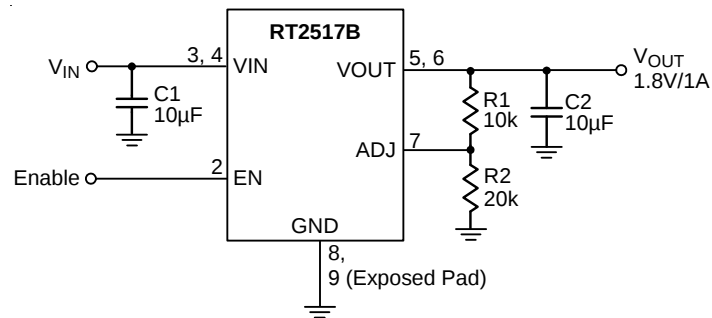
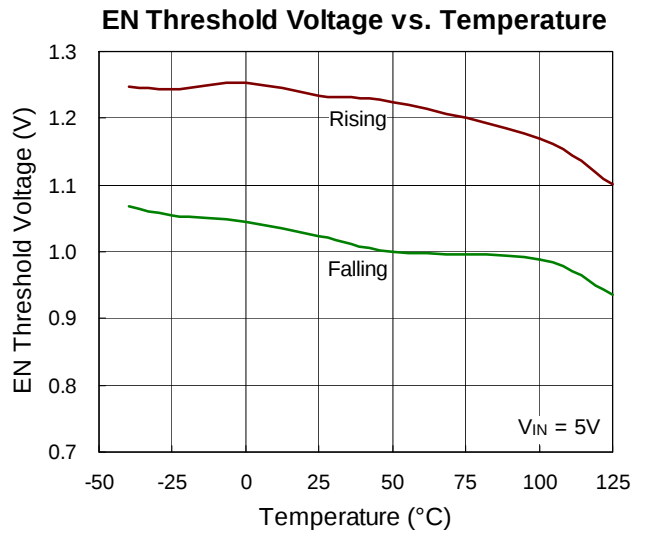
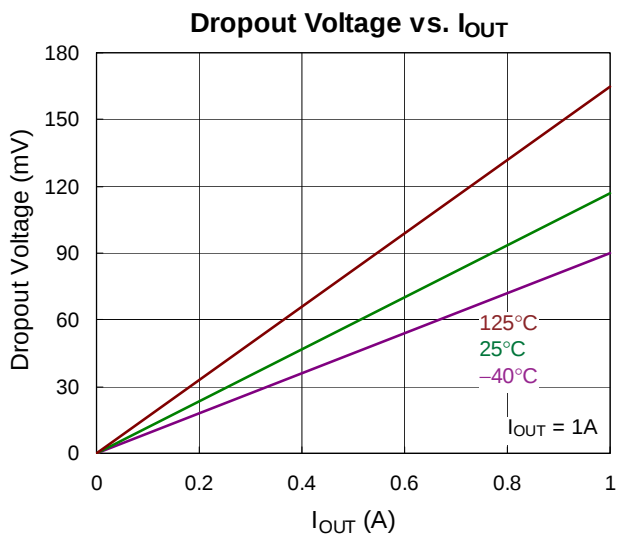
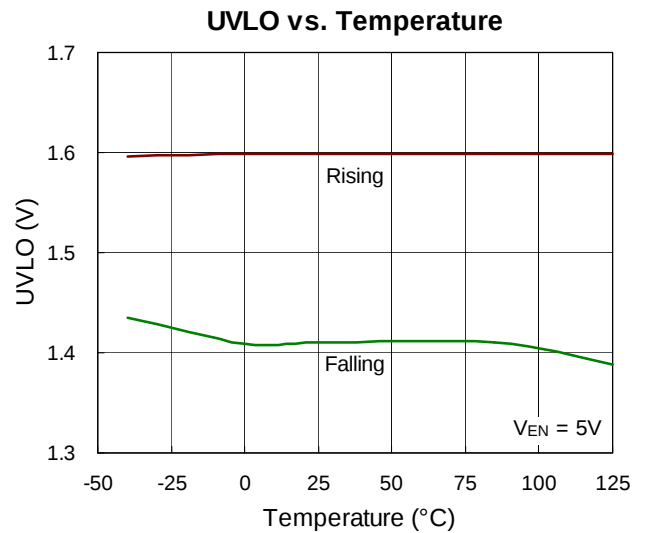
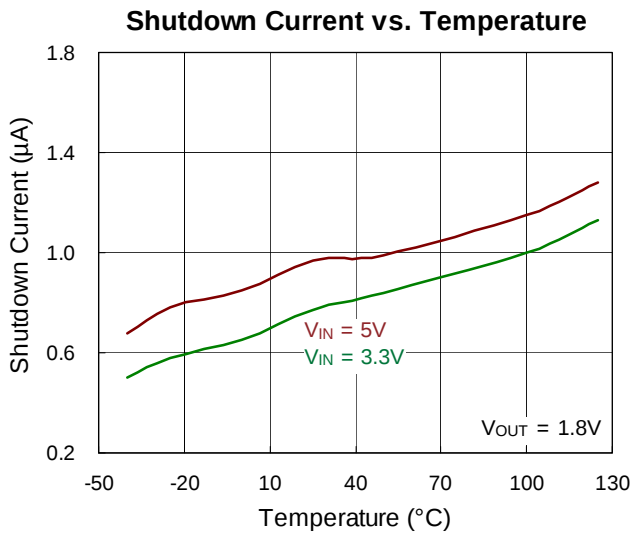
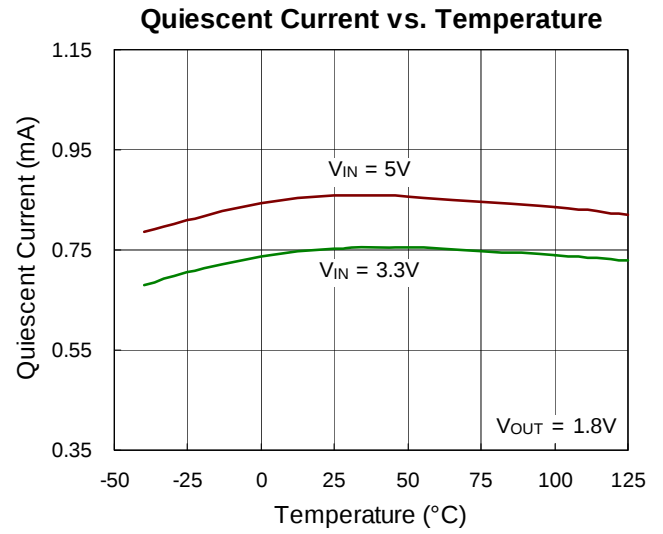
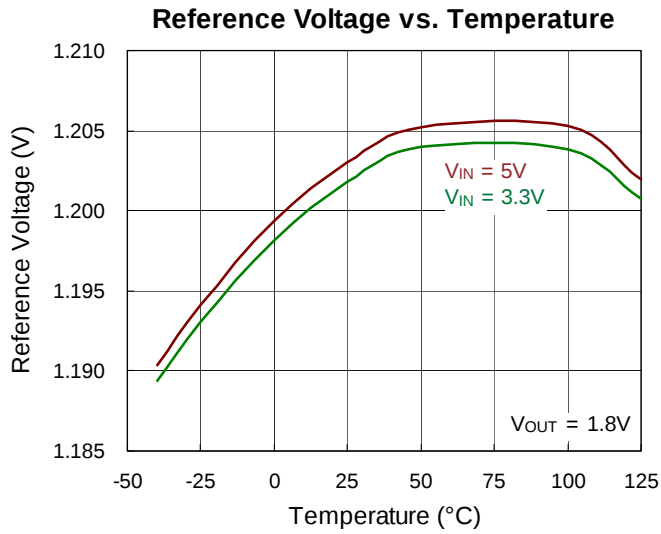
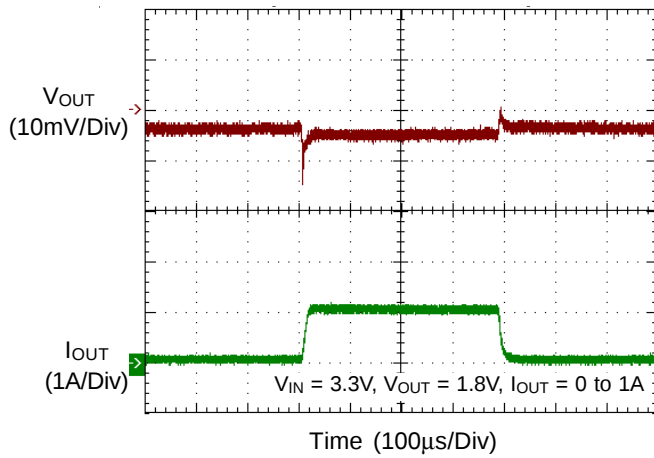


Figure 1. 1.8V Output Voltage Operation Circuit

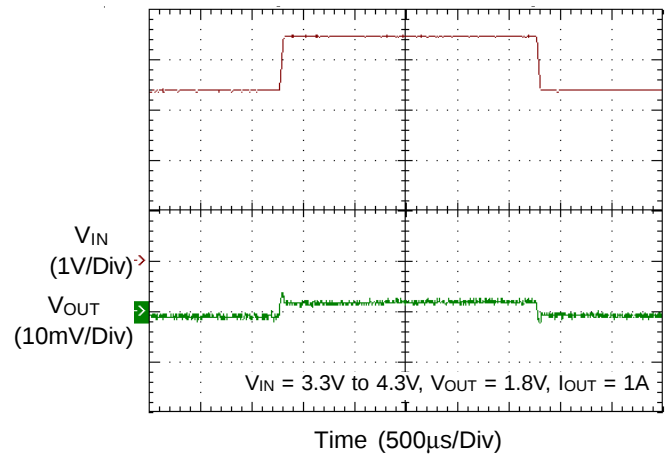
Typical Operating Characteristics



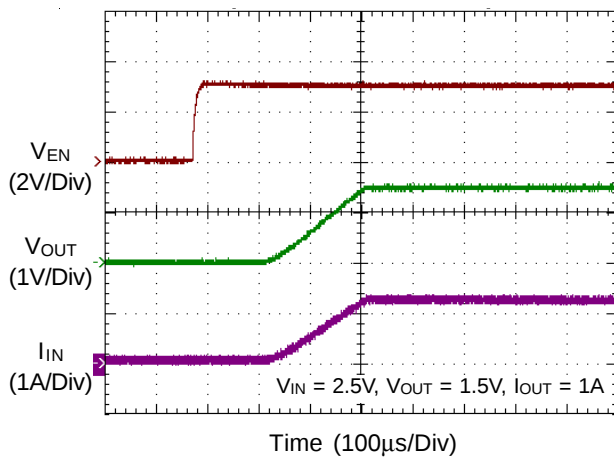
Load Transient Response



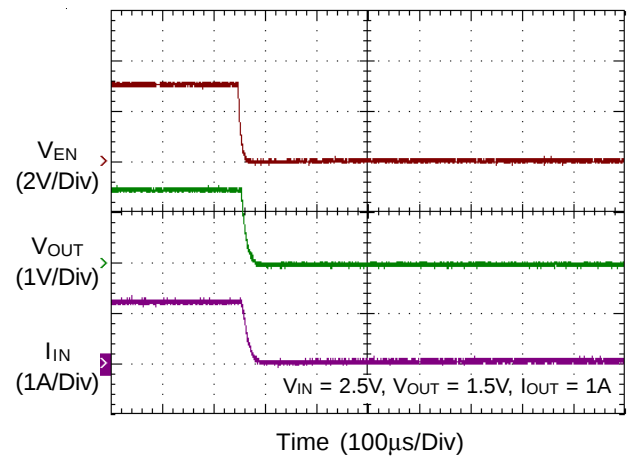
Line Transient Response



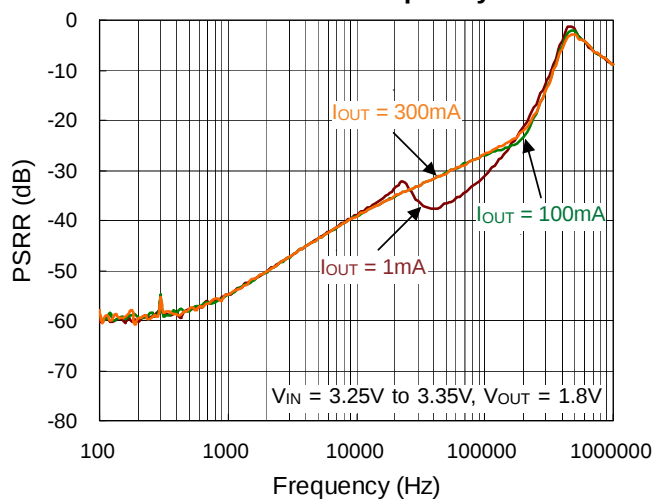
Power On from EN



Power Off from EN



PSRR vs. Frequency



Application Information

The RT2517B is a low voltage, low dropout linear regulator with an external bias supply input capable of supporting an input voltage range from 2.2V to 6V with a fixed output voltage from 1V to 2V in 0.1V increments.

Output Voltage Setting

The RT2517B output voltage is adjustable from 2.2V to 6V via the external resistive voltage divider. The voltage divider resistors can have values of up to 800kΩ because of the very high impedance and low bias current of the sense comparator. The output voltage is set according to the following equation :

$$V_{OUT} = V_{ADJ} \times \left(1 + \frac{R1}{R2}\right)$$

where V_{ADJ} is the reference voltage with a typical value of 1.2V.

Chip Enable Operation

The RT2517B goes into sleep mode when the EN pin is in a logic low condition. In this condition, the pass transistor, error amplifier, and band gap are all turned off, reducing the supply current to only 10μA (max.). The EN pin can be directly tied to VIN to keep the part on.

UVLO Protection

The RT2517B provides an input Under Voltage Lockout protection (UVLO). When the input voltage exceeds the UVLO rising threshold voltage (1.2V typ.), the device resets the internal circuit and prepares for operation. If the input voltage falls below the UVLO falling threshold voltage during normal operation, the device will be shut down. A hysteresis (140mV typ.) between the UVLO rising and falling threshold voltage is designed to avoid noise.

Current Limit

The RT2517B contains an independent current limit circuitry, which controls the pass transistor's gate voltage, limiting the output current to 1A (typ.).

C_{IN} and C_{OUT} Selection

Like any low dropout regulator, the external capacitors of the RT2517B must be carefully selected for regulator stability and performance. Using a capacitor of at least 10μF is suitable. The input capacitor must be located at a distance of not more than 0.5 inch from the input pin of the IC. Any good quality ceramic capacitor can be used. However, a capacitor with larger value and lower ESR (Equivalent Series Resistance) is recommended since it will provide better PSRR and line transient response.

The RT2517B is designed specifically to work with low ESR ceramic output capacitor for space saving and performance consideration. Using a ceramic capacitor with capacitance of at least 10μF and ESR larger than 1mΩ on the RT2517B output ensures stability. Nevertheless, the RT2517B can still work well with other types of output capacitors due to its wide range of stable ESR. Figure 2 shows the allowable ESR range as a function of load current for various output capacitance. Output capacitors with larger capacitance can reduce noise and improve load transient response, stability, and PSRR. The output capacitor should be located at a distance of not more than 0.5 inch from the output pin of the RT2517B.

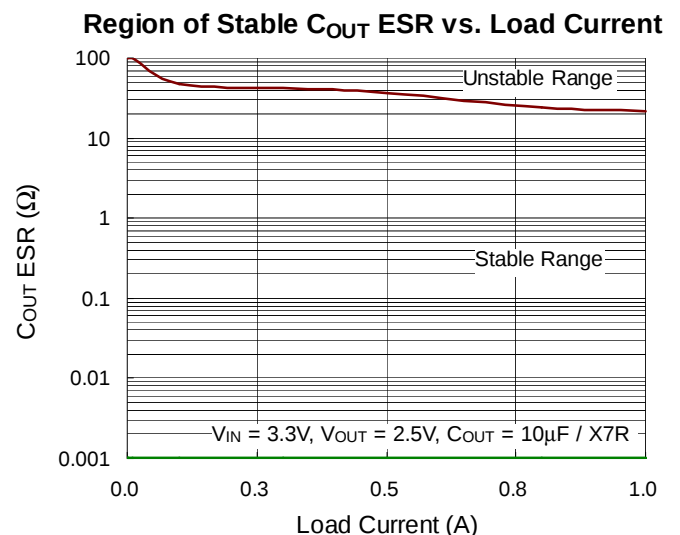


Figure 2

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA} , is layout dependent. For SOP-8 (Exposed Pad) package, the thermal resistance, θ_{JA} , is 49°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at $T_A = 25^\circ\text{C}$ can be calculated by the following formula :

$$P_{D(MAX)} = (125^\circ\text{C} - 25^\circ\text{C}) / (49^\circ\text{C/W}) = 2.041\text{W for SOP-8 (Exposed Pad) package}$$

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA} . The derating curve in Figure 3 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

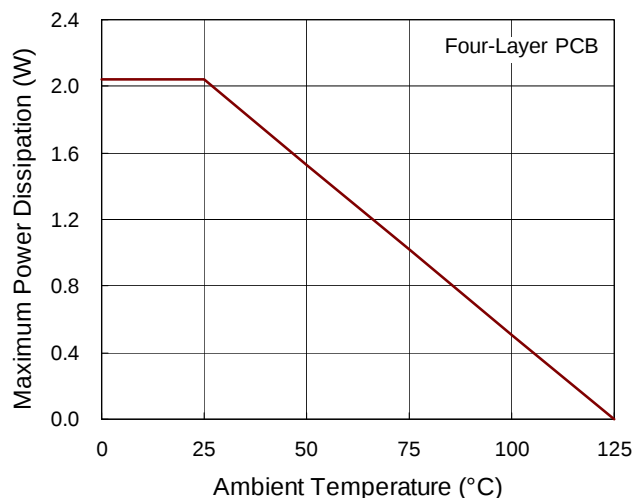
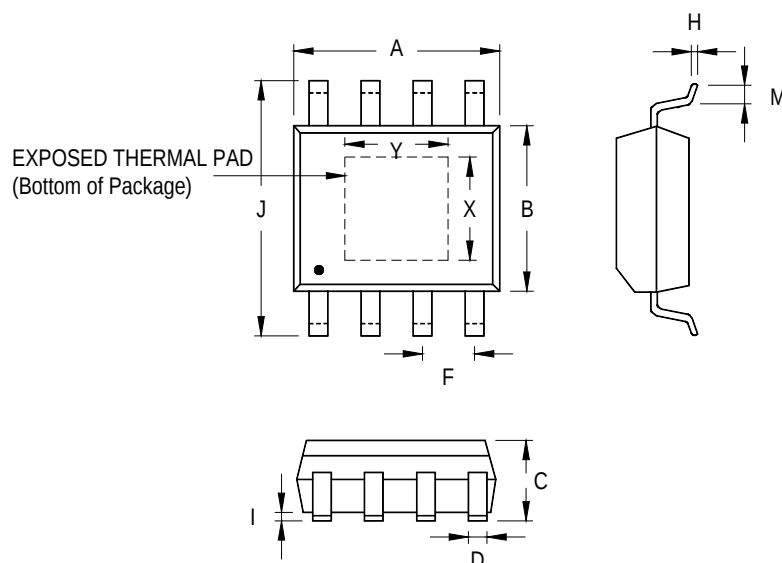


Figure 3. Derating Curve of Maximum Power Dissipation

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	4.801	5.004	0.189	0.197
B	3.810	4.000	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.510	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.170	0.254	0.007	0.010
I	0.000	0.152	0.000	0.006
J	5.791	6.200	0.228	0.244
M	0.406	1.270	0.016	0.050
Option 1	X	2.000	0.079	0.091
	Y	2.000	0.079	0.091
Option 2	X	2.100	0.083	0.098
	Y	3.000	0.118	0.138

8-Lead SOP (Exposed Pad) Plastic Package

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