

RSY160P05

Silicon P-channel MOSFET

- 1) Low On-resistance.
- 2) Built-in G-S Protection Diode.
- 3) Same land pattern as CPT3 (D-PAK).

Switching

Type	Package	Taping
	Code	TL
	Basic ordering unit (pieces)	2500
RSY160P05		○

Technical drawing of the TCPT connector showing front, side, and detail views with dimensions:

- Front View:**
 - Overall width: 6.6
 - Inner width: 5.0
 - Overall height: 9.5
 - Inner height: 8.3
 - Bottom mounting holes: (1) and (3)
 - Top mounting hole: (2)
 - Bottom hole spacing: 2.3 (from center to hole center)
 - Top hole offset: 0.72
- Side View:**
 - Overall depth: 2.0
 - Bottom flange thickness: 0.8
 - Bottom flange width: 0.5

*1 ESD PROTECTION DIODE
*2 BODY DIODE

(1) Gate
(2) Drain
(3) Source

Parameter		Symbol	Limits	Unit
Drain-source voltage		V_{DSS}	-45	V
Gate-source voltage		V_{GSS}	± 20	V
Drain current	Continuous	I_D	± 16	A
	Pulsed	I_{DP}^{*1}	± 32	A
Source current (Body diode)	Continuous	I_S	-16	A
	Pulsed	I_{SP}^{*1}	-32	A
Total power dissipation		P_D^{*2}	20	W
Channel temperature		T_{ch}	150	$^{\circ}\text{C}$
Range of Storage temperature		T_{stg}	-55 to +150	$^{\circ}\text{C}$

*1 $P_w \leq 10 \mu s$, Duty cycle $\leq 1\%$

*2 $T_c=25^{\circ}\text{C}$

Parameter	Symbol	Limits	Unit
Channel to ambient	Rth (ch-c) *	6.25	°C / W

* T_c=25°C

Transistors

●Electrical characteristics (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 20V, V_{DS} = 0V$
Drain-source breakdown voltage	$V_{(BR) DSS}$	−45	—	—	V	$I_D = -1mA, V_{GS} = 0V$
Zero gate voltage drain current	I_{DSS}	—	—	−1	μA	$V_{DS} = -45V, V_{GS} = 0V$
Gate threshold voltage	$V_{GS(th)}$	−1.0	—	−2.5	V	$V_{DS} = -10V, I_D = -1mA$
Static drain-source on-state resistance	$R_{DS(on)}$ *	—	35	50	m Ω	$I_D = -16A, V_{GS} = -10V$
		—	45	63	m Ω	$I_D = -8A, V_{GS} = -4.5V$
		—	50	70	m Ω	$I_D = -8A, V_{GS} = -4.0V$
Forward transfer admittance	$ Y_{fs} $ *	8.5	—	—	S	$V_{DS} = -10V, I_D = -8A$
Input capacitance	C_{iss}	—	2150	—	pF	$V_{DS} = -10V$
Output capacitance	C_{oss}	—	250	—	pF	$V_{GS} = 0V$
Reverse transfer capacitance	C_{rss}	—	150	—	pF	$f = 1MHz$
Turn-on delay time	$t_{d(on)}$ *	—	13	—	ns	$I_D = -10A$
Rise time	t_r *	—	30	—	ns	$V_{DD} = -25V$
Turn-off delay time	$t_{d(off)}$ *	—	90	—	ns	$V_{GS} = -10V$
Fall time	t_f *	—	105	—	ns	$R_L = 2.5\Omega$
Total gate charge	Q_g *	—	17.0	25.5	nC	$V_{DD} = -25V, I_D = -10A$
Gate-source charge	Q_{gs} *	—	5.2	—	nC	$V_{GS} = -5V$
Gate-drain charge	Q_{gd} *	—	5.5	—	nC	$R_L = 2.5\Omega, R_G = 10\Omega$

*Pulsed

●Body diode characteristics (Source-drain) (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V_{SD} *	—	—	−1.2	V	$I_S = -16A, V_{GS} = 0V$

*Pulsed

Transistors

●Electrical characteristic curves

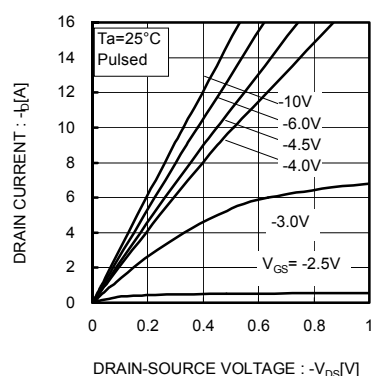


Fig.1 Typical Output Characteristics (I)

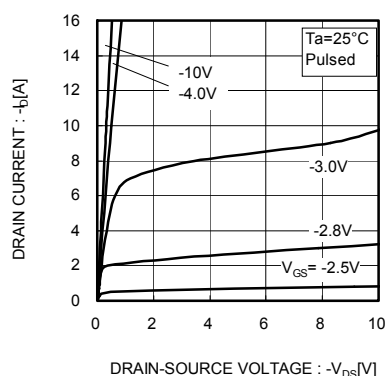


Fig.2 Typical Output Characteristics (II)

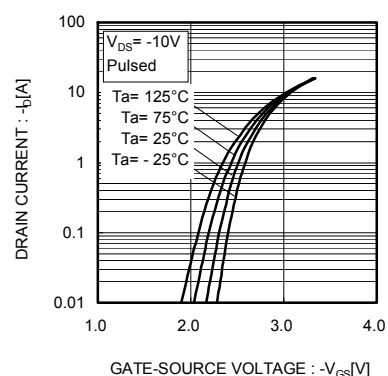


Fig.3 Typical Transfer Characteristics

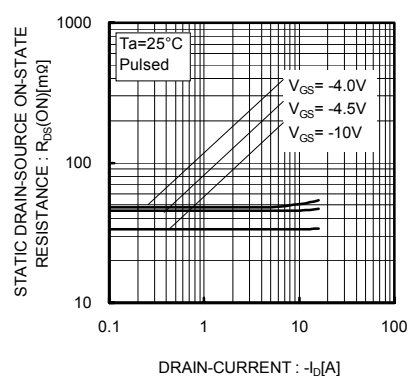


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current(I)

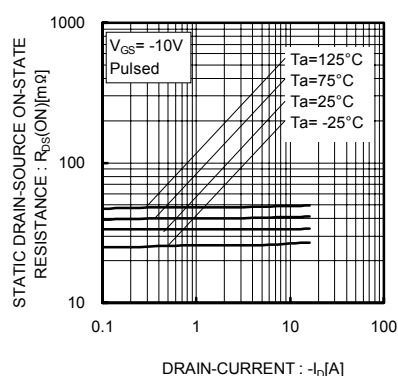


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current(II)

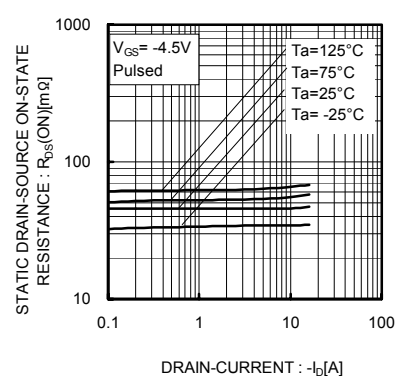


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current(III)

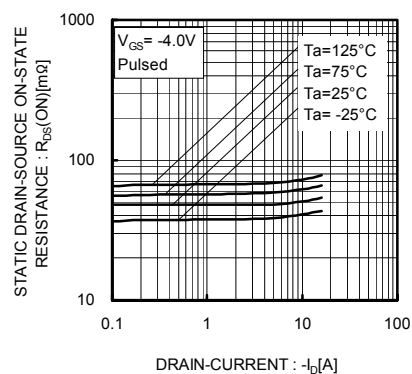


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current(IV)

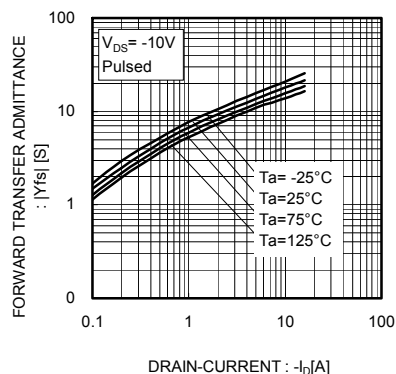


Fig.8 Forward Transfer Admittance vs. Drain Current

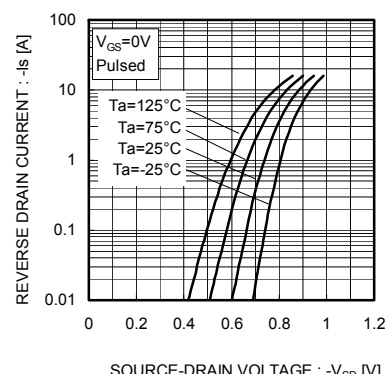


Fig.9 Reverse Drain Current vs. Source-Drain Voltage

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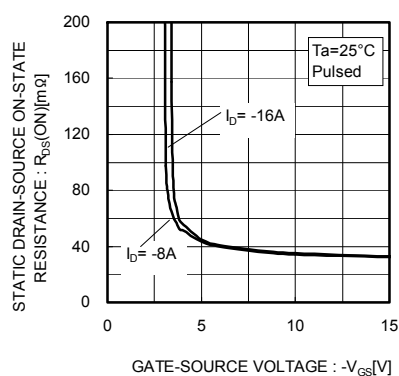


Fig. 10 Static Drain-Source On-State Resistance vs. Gate Source

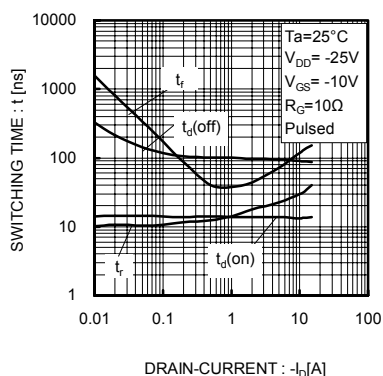


Fig. 11 Switching Characteristics

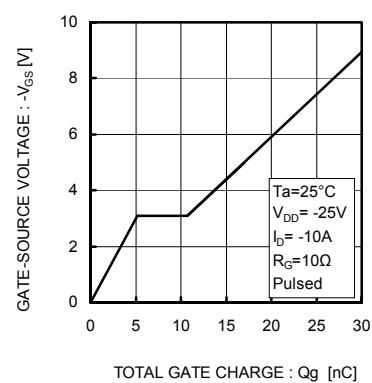


Fig. 12 Dynamic Input Characteristics

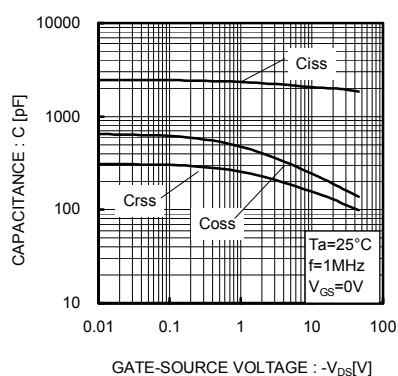


Fig. 13 Typical Capacitance vs. Drain-Source Voltage

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●Measurement circuits

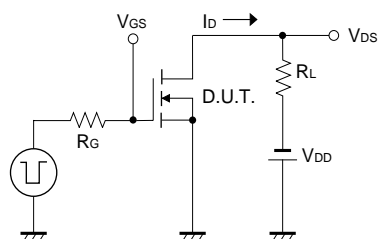


Fig.14 Switching Time Test Circuit

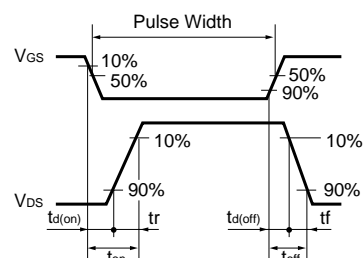


Fig.15 Switching Time Waveforms

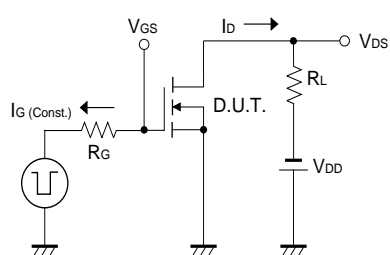


Fig.16 Gate Charge Test Circuit

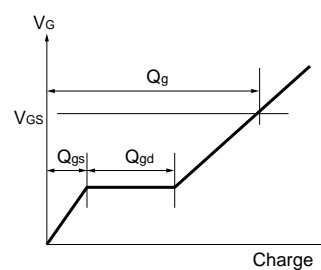


Fig.17 Gate Charge Waveform

Notes

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