PRELIMINARY

150mA Dual LDO REGULATOR

NO.EA-200-20090311

OUTLINE

The RP152/153x Series are CMOS-based voltage regulator ICs with high output voltage accuracy, low supply current, low dropout, and high ripple rejection. Each of these voltage regulator ICs consists of a voltage reference unit, an error amplifier, resistors for setting Output Voltage, a current limit circuit, and a chip enable circuit. Moreover, in C Version of RP152, the start-up sequence circuit is built-in.

These ICs perform with low dropout voltage due to built-in transistor with low ON resistance, and a chip enable function prolongs the battery life of each system. The line transient response and load transient response of the RP152/153x Series are excellent, thus these ICs are very suitable for the power supply for hand-held communication equipment.

The output voltage of these ICs is internally fixed with high accuracy. Since the packages for these ICs are SOT-23-6 and DFN1212-6 for RP152, and DFN1216-8 for RP153, dual LDO regulators are included in each package are high density mounting of the ICs on boards is possible.

In RP153, the power supply of each circuit can be individually supplied. The transient response characteristic of D and E Version is improved. (The supply current: Typ. 85μA).

FEATURES

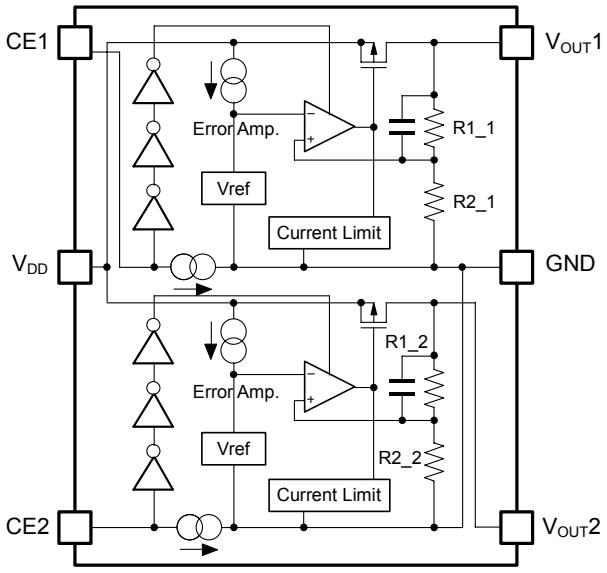
- Supply Current ····· Typ. 40μA (VR1, VR2)
- Supply Current (RP153xxxxD/E) ····· Typ. 85μA (VR1, VR2)
- Standby Mode ····· Typ. 0.1μA (VR1, VR2)
- Low Dropout Voltage ····· Typ. 0.22V(I_{OUT}=150mA, V_{OUT}=2.8V)
- High Ripple Rejection ····· TYP. 70dB (f=1kHz)
  TYP. 65dB (f=10kHz)
- High Output Voltage Accuracy ····· ±1.0%
- Low Temperature-Drift Coefficient of Output Voltage ····· Typ. ±80ppm/°C
- Excellent Line Regulation ····· Typ. 0.02%/V
- Small Packages ····· RP152: DFN1212-6, SOT-23-6,
  RP153: DFN1216-8
- Built-in Fold Back Protection Circuit ····· Typ. 40mA (Current at short mode)
- Ceramic capacitors are recommended to be used with this IC ····· 0.22μF or more

APPLICATIONS

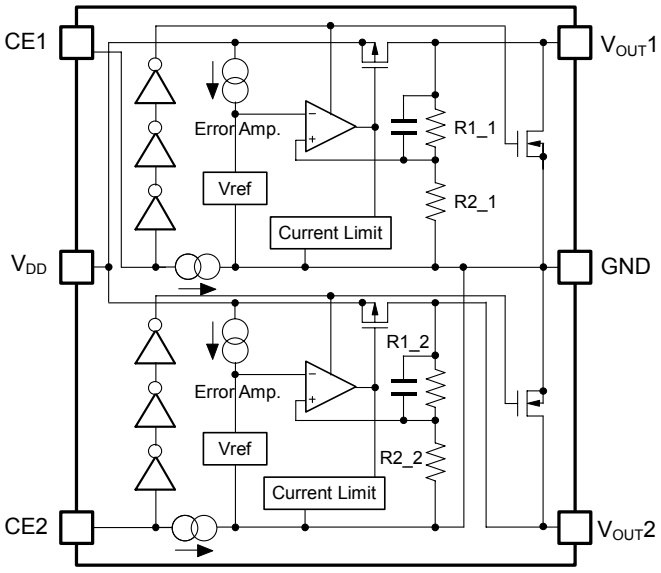
Power source for electrical applications such as cameras, VCRs and camcorders
Power source for battery-powered equipment
Power source for portable communication equipment

BLOCK DIAGRAMS (RP152xxxxA/B/C)

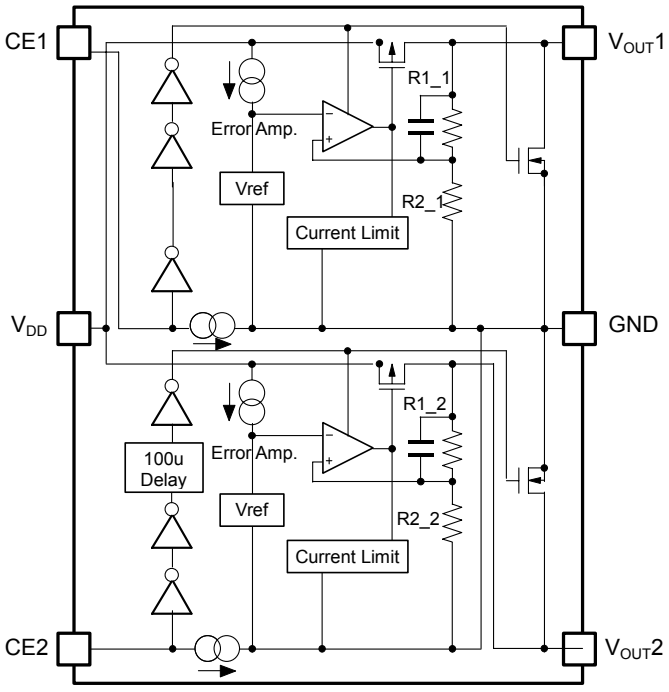
RP152xxxxA



RP152xxxxB

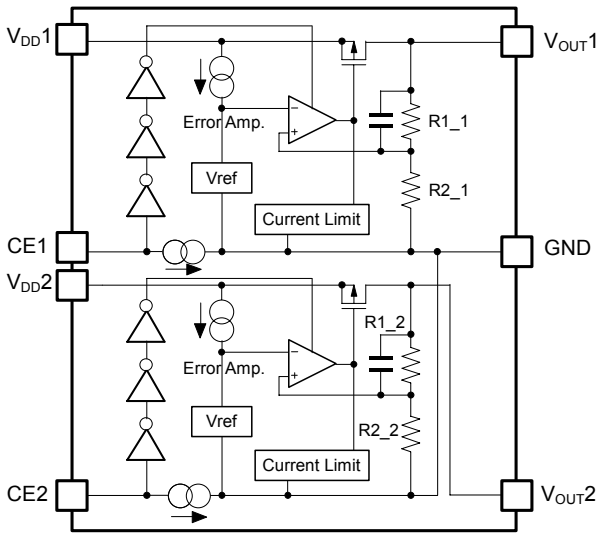


RP152xxxxC

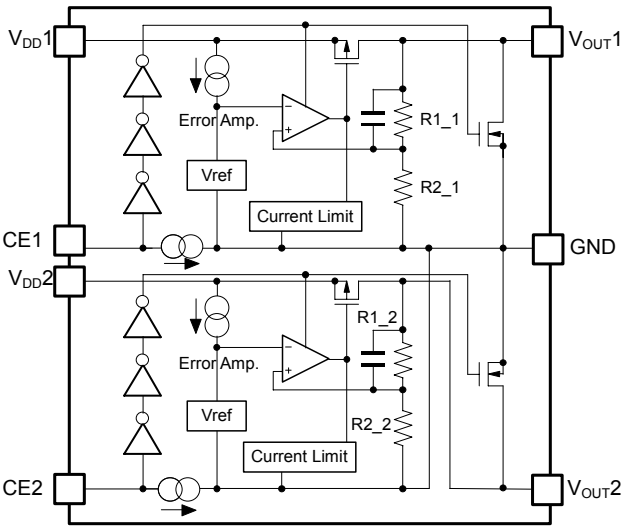


BLOCK DIAGRAMS (RP153xxxxA/B/D/E)

RP153LxxxA/D



RP153LxxxB/E



SELECTION GUIDE

The output voltage, version, and the taping type for the ICs can be selected at the user's request.

The selection can be made with designating the part number as shown below;

RP152x xxx x-xx-x ←Part Number
↑ ↑ ↑ ↑ ↑
a b c d e

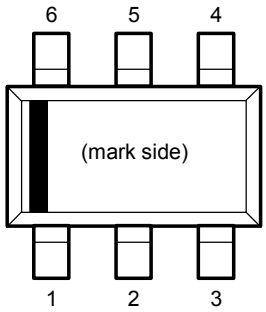
RP153x xxx x-xx-x ←Part Number
↑ ↑ ↑ ↑ ↑
a b c d e

Code	Contents
a	Designation of Package Type: RP152Nxxxx-xx-x: SOT-23-6 RP152Lxxxx-xx-x: DFN1212-6 RP153Lxxxx-xx-x: DFN1216-8
b	Setting combination of 2ch Output Voltage (V_{OUT}): Serial Number for Voltage Setting, Stepwise setting with a step of 0.1V in the range of 0.8V to 3.6V is possible for each channel.
c	Designation of Active Type RP152 A: without auto-discharge function* B: with auto-discharge function* C: The start-up sequence function with auto-discharge* RP153 A: without auto-discharge function* B: with auto-discharge function* D: without auto-discharge function*, (the transient response improved type) E: with auto-discharge function*, (the transient response improved type)
d	Designation of Taping Type (refer to Taping Specifications) Ex.TR : SOT-23-6, DFN1212-6 Ex.E2 : DFN1216-8
e	Designation of composition of plating: -F: Lead free plating (SOT-23-6) None: Au plating (DFN1212-6, DFN1216-8)

* When the mode is into standby with CE signal, auto-discharge transistor turns on, and it makes the turn-off speed faster than normal type.

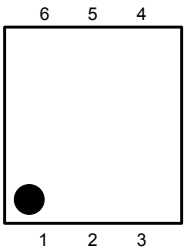
PIN CONFIGURATION

RP152N (SOT-23-6)

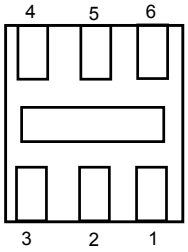


RP152L (DFN1212-6)

Top View

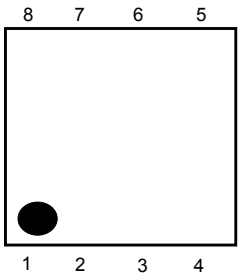


Bottom View

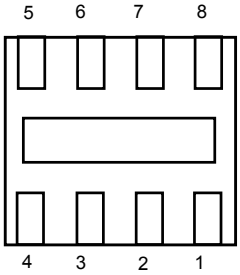


RP153L (DFN1216-8)

Top View



Bottom View



PIN DESCRIPTIONS

RP152

RP152N: SOT-23-6

Pin No.	Symbol	Description
1	CE1	Chip Enable Pin 1 (“H” Active)
2	V_{DD}	Input Pin
3	CE2	Chip Enable Pin 2 (“H” Active)
4	$V_{OUT}2$	Output Pin 2
5	GND	Ground Pin
6	$V_{OUT}1$	Output Pin 1

RP152L: DFN1212-6

Pin No.	Symbol	Description
1	$V_{OUT}1$	Output Pin 1
2	$V_{OUT}2$	Output Pin 2
3	GND	Ground Pin
4	CE2	Chip Enable Pin 2 (“H” Active)
5	V_{DD}	Input Pin
6	CE1	Chip Enable Pin 1 (“H” Active)

RP153

RP153L: DFN1216-8

Pin No.	Symbol	Description
1	GND	Ground Pin
2	$V_{OUT}1$	Output Pin 1
3	$V_{OUT}2$	Output Pin 2
4	GND	Ground Pin
5	CE2	Chip Enable Pin 2 (“H” Active)
6	$V_{DD}2$	Input Pin 2
7	$V_{DD}1$	Input Pin 1
8	CE1	Chip Enable Pin 1 (“H” Active)

ABSOLUTE MAXMUM RATINGS

Symbol	Items	Ratings		Unit
V_{IN}	Input Voltage	6.0		V
V_{CE}	Input Voltage (CE Pin)	-0.3~6.0		V
V_{OUT}	Output Voltage	-0.3~V_{IN}+0.3		V
$I_{OUT}1$	Output Current 1	180		mA
$I_{OUT}2$	Output Current 2	180		
P_D	Power Dissipation*	SOT-23-6 (RP152N)	420	mW
		DFN1212-6 (RP152L)	600	
		DFN1216-8 (RP153L)	625	
Ta	Ambient Temperature Range	-40~85		°C
Tstg	Storage Temperature Range	-55~125		°C

*For Power Dissipation, please refer to PACKAGE INFORMATION (p.14~) to be described

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause the permanent damages and may degrade the life time and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings is not assured.

ELECTRICAL CHARACTERISTICS

RP152/153xxxxx

V_{IN}=Set V_{OUT}+1.0V for V_{OUT} options greater than 1.5V, V_{IN}=2.5V for $V_{OUT} \leqq$ 1.5V
I_{OUT}=1mA, C_{IN}=C_{OUT}=0.22μF unless otherwise noted. Values surrounded by [ ] indicate the values under all temperature range, or -40°C ≦ Ta ≦ 85°C.

VR1/VR2 Ta=25°C

Symbol	Item	Conditions		Min.	Typ.	Max.	Unit
V_{OUT}	Output Voltage	Ta=25°C	V_{OUT}>2.0V	x 0.99		x 1.01	V
			$V_{OUT} \leqq$ 2.0V	-20		20	mV
		-40°C ≦ Ta ≦ 85°C	V_{OUT}>2.0V	[x 0.97]		[x 1.03]	V
			$V_{OUT} \leqq$ 2.0V	[-60]		[60]	mV
I_{OUT}	Output Current			[150]			mA
ΔV_{OUT} /ΔI_{OUT}	Load Regulation	1mA ≦ I_{OUT} ≦ 150mA	0.8V ≦ V_{OUT}<1.1V		10	[40]	mV
			1.1V ≦ V_{OUT}<1.6V		15	[50]	
			1.6V ≦ V_{OUT}<2.0V		15	[55]	
			2.0V ≦ $V_{OUT} \leqq$ 3.6V		15	[60]	
V_{DIF}	Dropout Voltage	Please see the table on next page (p.9)					
I_{SS}	Supply Current	I_{OUT}=0mA	RP153xxxxD/E Ver.		85	[120]	μA
			Others		40	[60]	
Istandby	Supply Current (Standby)	V_{CE}=0V			0.1	1.0	μA
ΔV_{OUT} /ΔV_{IN}	Line Regulation	Set V_{OUT}+0.5V ≦ V_{IN} ≦ 5.0V			0.02	[0.10]	%/V
RR	Ripple Rejection	f=1kHz, Ripple 0.2Vp-p V_{IN}=Set V_{OUT}+1.0V, I_{OUT}=30mA (In case $V_{OUT} \leqq$ 2.0V, V_{IN}=3.0V)			70		dB
V_{IN}	Input Voltage *1			[1.4]		[5.25]	V
ΔV_{OUT} /ΔTa	Output Voltage Temperature Coefficient	-40°C ≦ Ta ≦ 85°C			±80		ppm
I_{LIM}	Short Current	V_{OUT}=0V			40		mA
I_{PD}	CE Pull-down Current				0.3		μA
V_{CEH}	CE Input Voltage "H"			[1.0]			V
V_{CEL}	CE Input Voltage "L"					[0.4]	V
en	Output Noise	BW=10Hz~100kHz			60		μVrms
R_{LOW}	Nch ON Resistance for Auto Discharge (B/C/E Version Only)	V_{IN}=4.0V V_{CE}=0V	C Ver. (VR2)		10		Ω
			Others		50		

The specification in [ ] is checked and guaranteed by design engineering.
All of unit are tested and specified under load conditions such that Tj ≈ Ta=25°C except for Output Noise, Ripple Rejection and Output Voltage Temperature Coefficient items.

*1) The maximum Input Voltage of the ELECTRICAL CHARACTERISTICS is 5.25V. In case of exceeding this specification, the IC must be operated on condition that the Input Voltage is up to 5.5V and the total operating time is within 500hrs

Dropout Voltage

(Ta=25°)

V_{OUT} (V)	Dropout Voltage (V)		
	Condition	Typ.	Max.
V_{OUT} = 0.8	I_{OUT} = 150mA	0.63	0.87
V_{OUT} = 0.9		0.55	0.80
1.0 ≦ V_{OUT}<1.2		0.50	0.72
1.2 ≦ V_{OUT}<1.4		0.42	0.62
1.4 ≦ V_{OUT}<1.7		0.37	0.55
1.7 ≦ V_{OUT}<2.1		0.30	0.46
2.1 ≦ V_{OUT}<2.5		0.25	0.39
2.5 ≦ V_{OUT}<3.0		0.23	0.35
3.0 ≦ V_{OUT} ≦ 3.6		0.21	0.32

RECOMMENDED OPERATING CONDITIONS (ELECTRICAL CHARACTERISTICS)

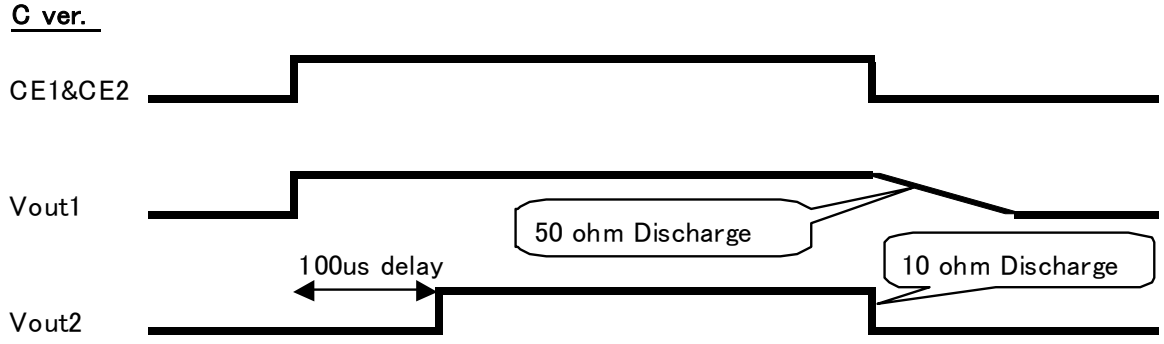
All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if when they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

THE START-UP SEQUENSE CIRCUIT

The Start-up sequence circuit is applied in C Version.

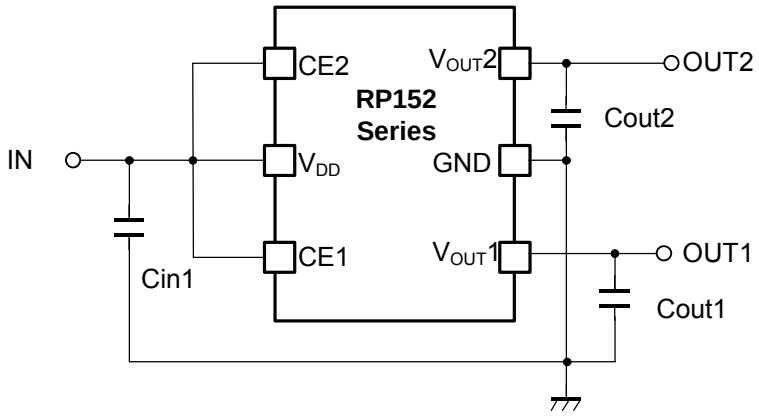
When the CE of VR1 and VR2 started-up at the same time, VR2 stands-up in 100us delay after VR1 stands up simultaneously with CE. Moreover, to disabling is depending upon the setting output voltage and the external capacitors. VR1 reduces the output voltage by the Nch driver of about 50Ω, and VR2 reduces the output voltage by the Nch driver of about 10Ω.

The Timing Chart of the Start-up Sequence



TYPICAL APPLICATION

RP152xxxxA/B/C



Cin1=Cout1=Cout2=Ceramic 0.22μF

TECHNICAL NOTES

When using these ICs, consider the following points:

Phase Compensation

In these ICs, phase compensation is made for securing stable operation even if the load current is varied. For this purpose, use capacitors (0.22μF or more) for $C_{OUT}1$ and $C_{OUT}2$ with good frequency characteristics and ESR (Equivalent Series Resistance).

(Note: If additional ceramic capacitors are connected with parallel to the output pin with an output capacitor for phase compensation, the operation might be unstable. Because of this, test these ICs with as same external components as ones to be used on the PCB.)

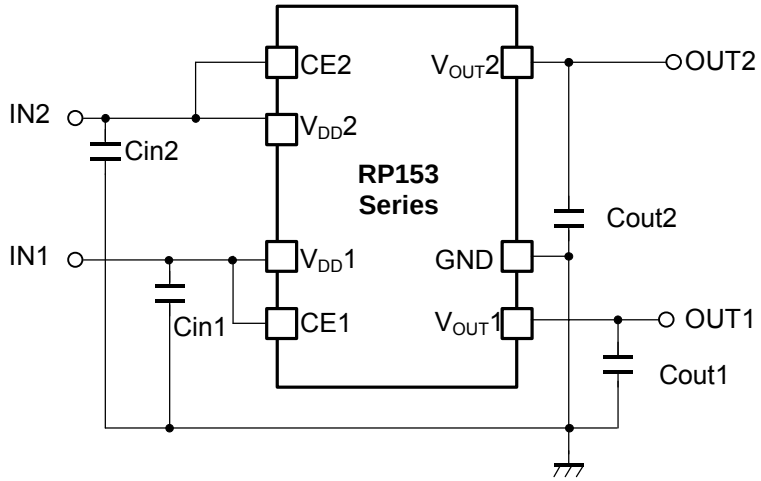
PCB Layout

Make V_{DD} and GND lines sufficient. If their impedance is high, noise pickup or unstable operation may result. Connect capacitors with a capacitance value as much as 0.22μF or more between V_{DD} and GND pin, and as close as possible to the pins (Cin1).

Set external components, especially the output capacitors, as close as possible to the ICs, and make wiring as short as possible (Cout1 / Cout2).

TYPICAL APPLICATION

RP153xxxxA/B/D/E



Cin1=Cin2=Cout1=Cout2=Ceramic 0.22μF

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PCB Layout

Make V_{DD} and GND lines sufficient. If their impedance is high, noise pickup or unstable operation may result. Connect capacitors with a capacitance value as much as 0.22μF or more between V_{DD} and GND pin, and as close as possible to the pins (Cin1 / Cin2).

Set external components, especially the output capacitors, as close as possible to the ICs, and make wiring as short as possible (Cout1 / Cout2).

TEST CIRCUITS (RP152xxxxA/B/C)

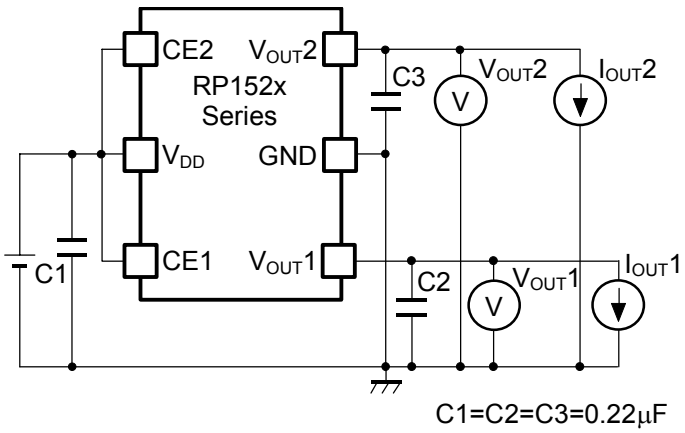


Fig.1 Basic Test Circuit

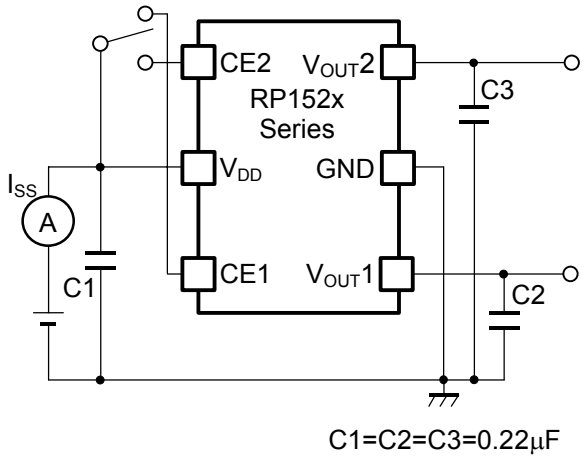


Fig.2 Test Circuit for Supply Current

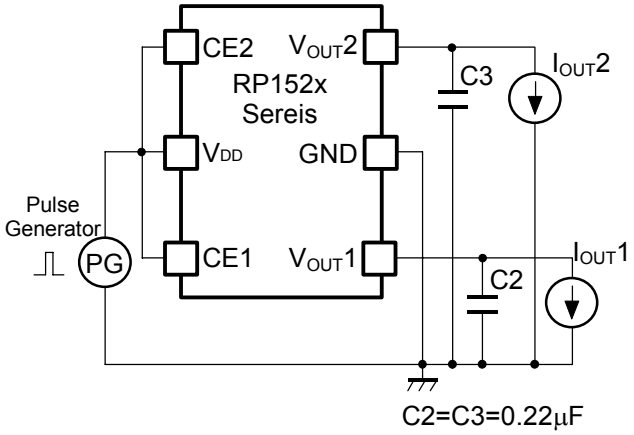


Fig. 3 Test Circuit for Ripple Rejection & Line Transient Response

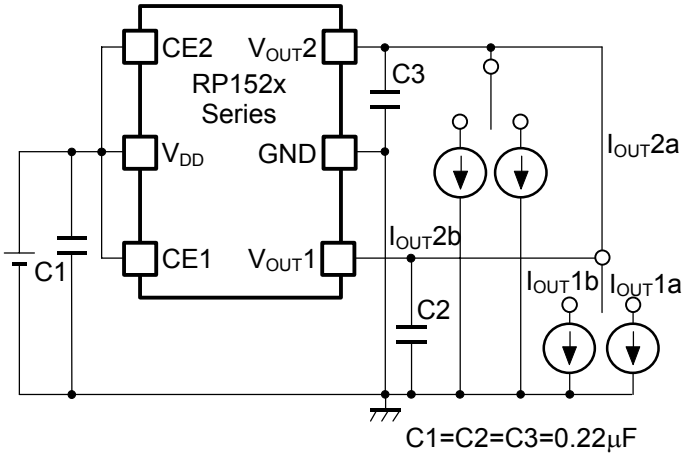


Fig.4 Test Circuits for Load Transient Response

TEST CIRCUITS (RP153xxxxA/B/D/E)

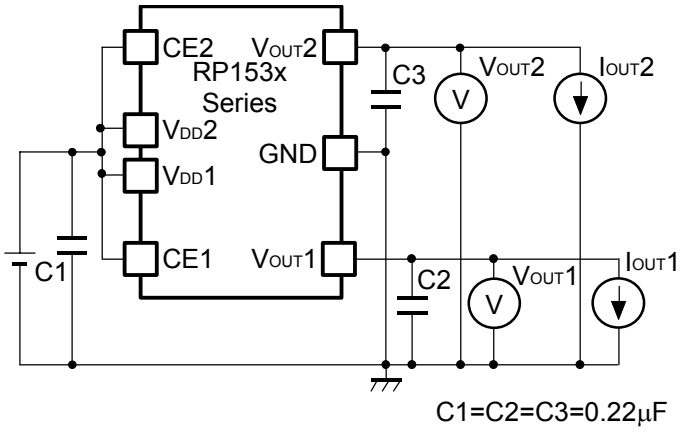


Fig.1 Basic Test Circuit

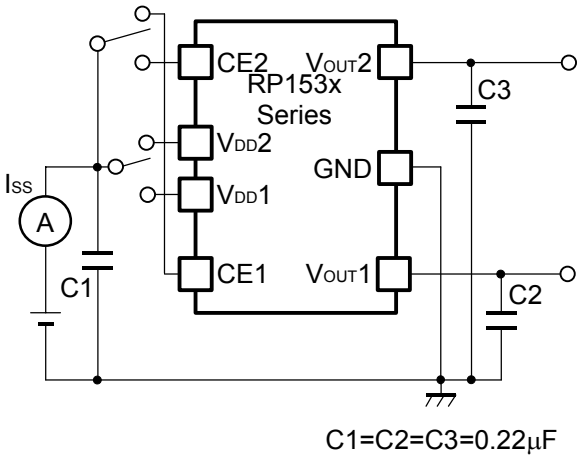


Fig.2 Test Circuit for Supply Current

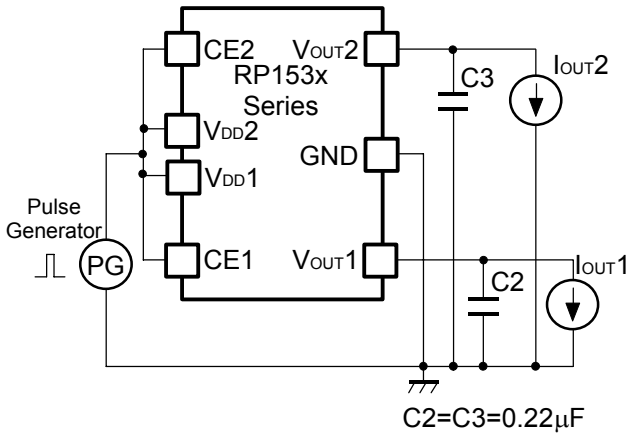


Fig. 3 Test Circuit for Ripple Rejection & Line Transient Response

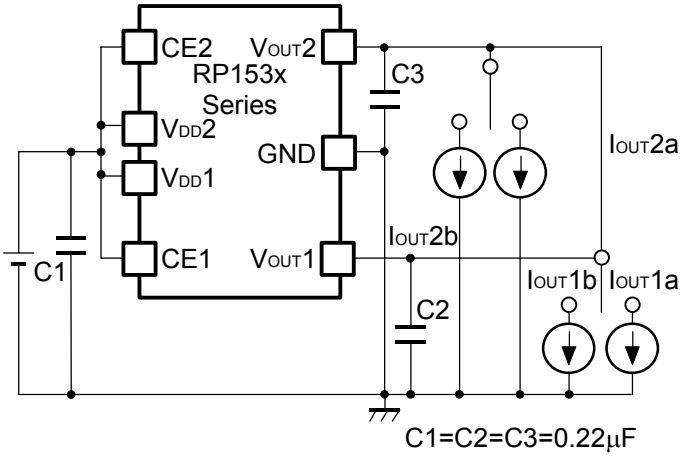
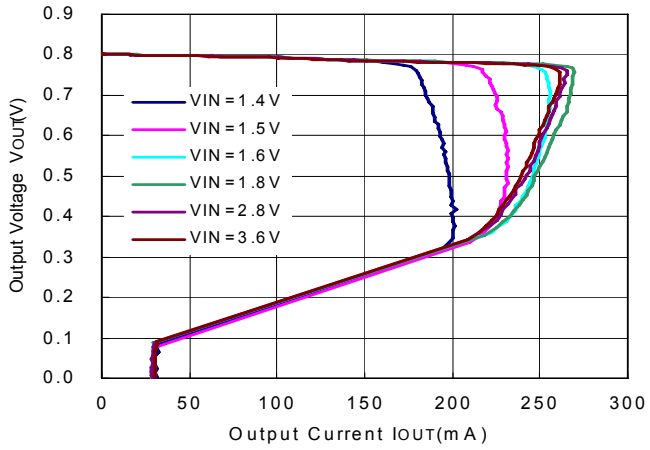


Fig.4 Test Circuits for Load Transient Response

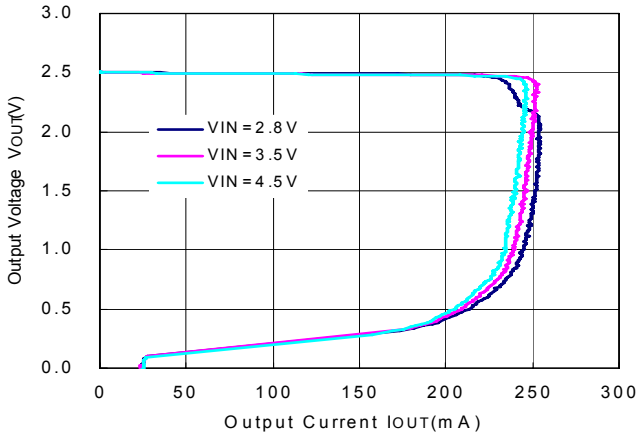
TYPICAL CHARACTERISTICS

1) Output Voltage vs. Output Current (Ta=25°C)

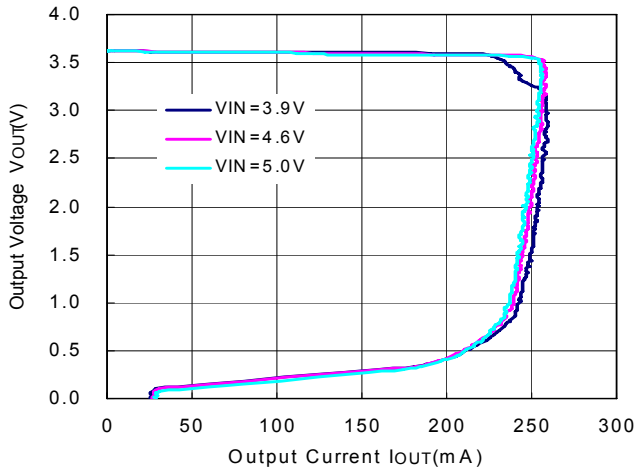
0.8V(VR1/VR2)



2.5V(VR1/VR2)

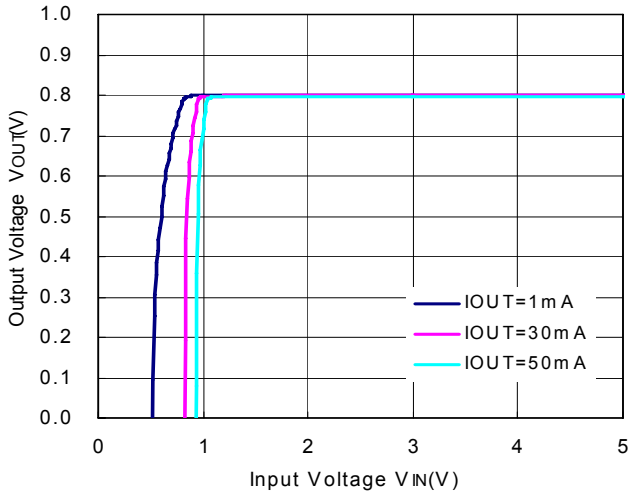


3.6V(VR1/VR2)

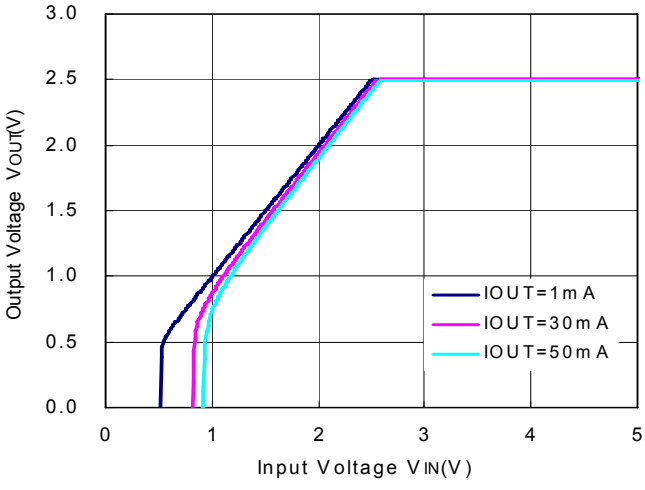


2) Input Voltage vs. Output Voltage (Ta=25°C)

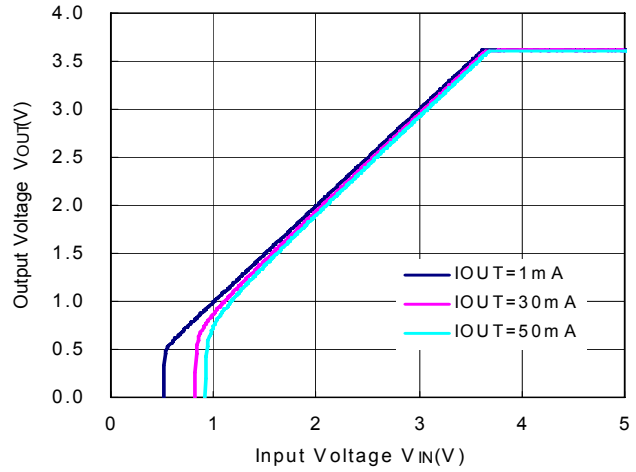
0.8V (VR1/VR2)



2.5V (VR1/VR2)

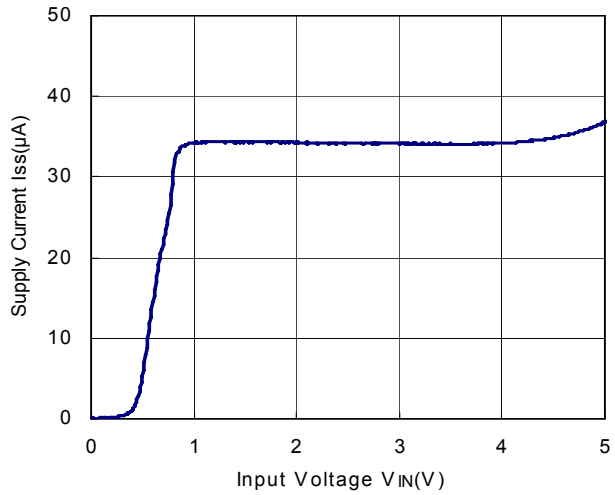


3.6V(VR1/VR2)

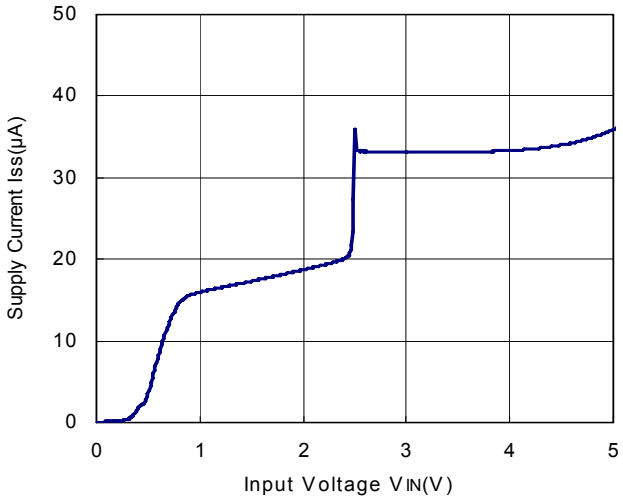


3) Supply Current vs. Input Voltage

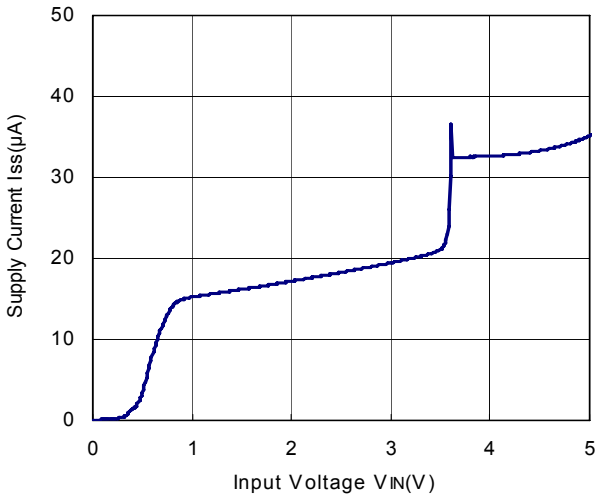
0.8V(VR1/VR2)



2.5V(VR1/VR2)

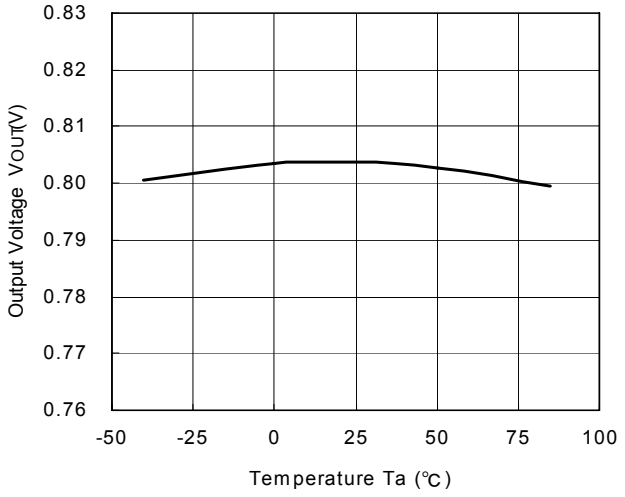


3.6V(VR1/VR2)

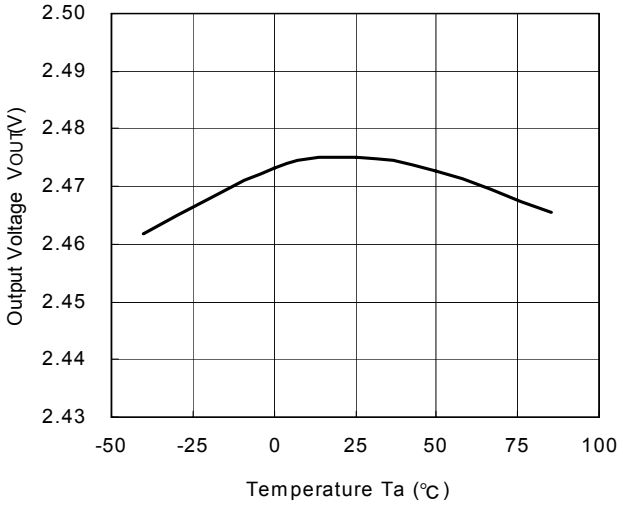


4) Output Voltage vs. Temperature

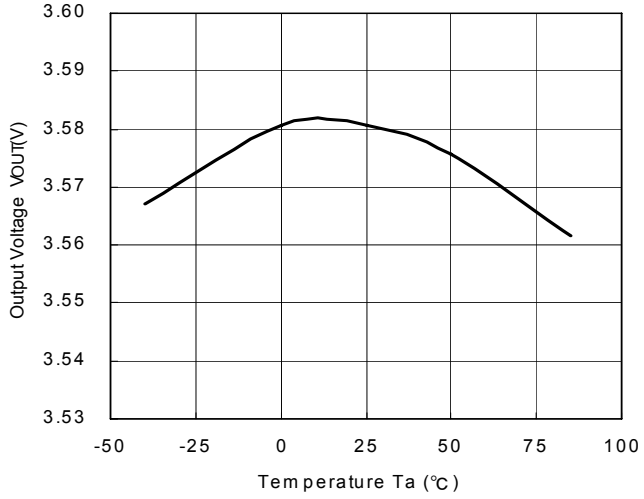
0.8V(VR1/VR2)



2.5V(VR1/VR2)

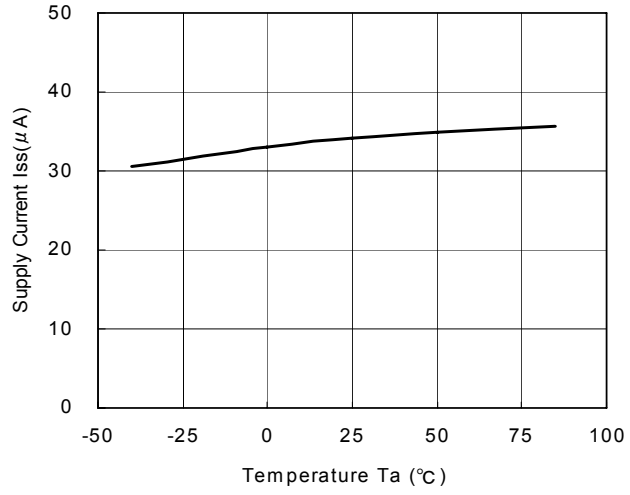


3.6V(VR1/VR2)

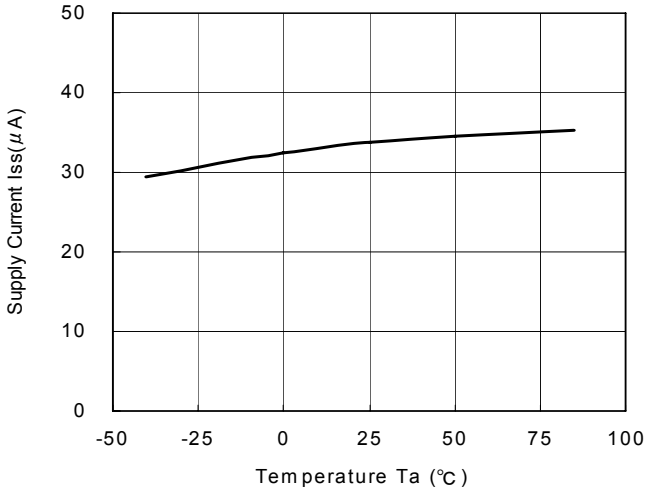


5) Supply Current vs. Temperature

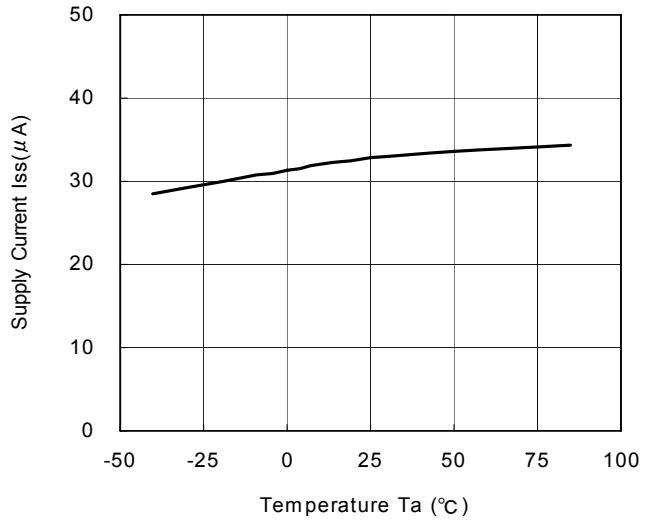
0.8V(VR1/VR2)



2.5V(VR1/VR2)

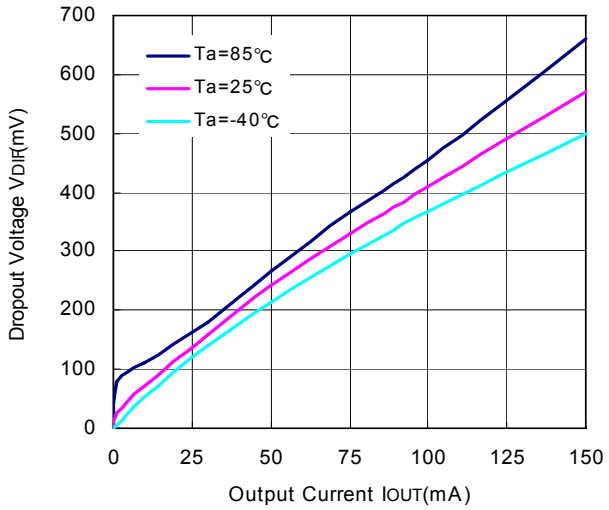


3.6V(VR1/VR2)

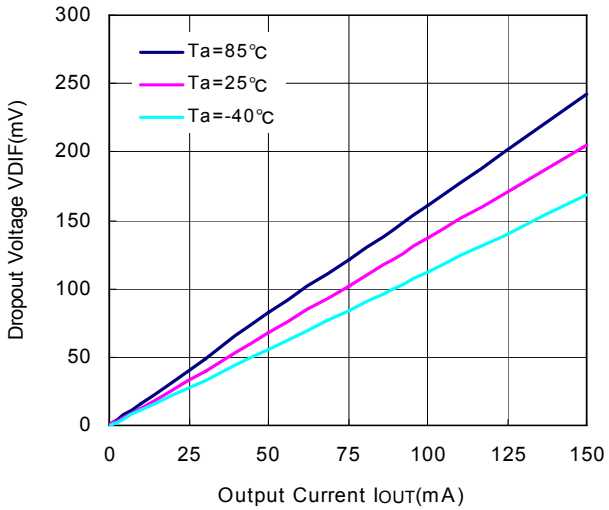


6) Dropout Voltage vs. Output Current

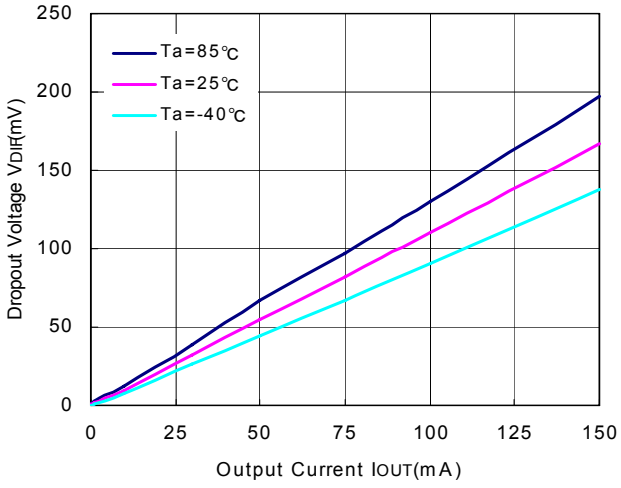
0.8V(VR1/VR2)



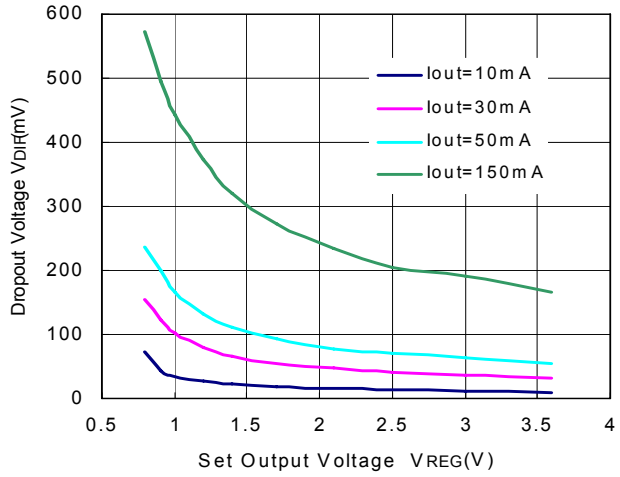
2.5V(VR1/VR2)



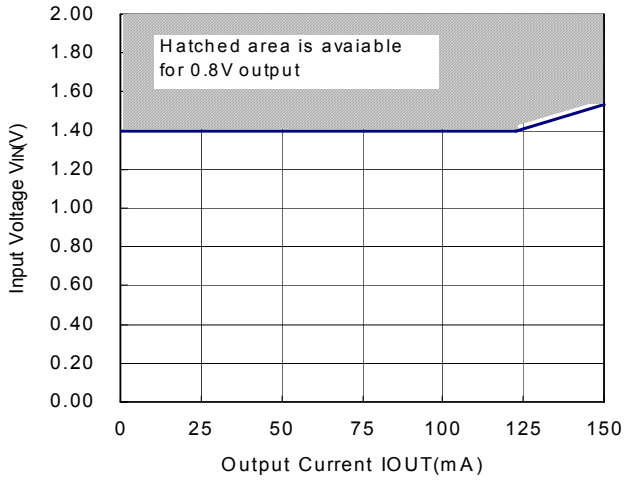
3.6V(VR1/VR2)



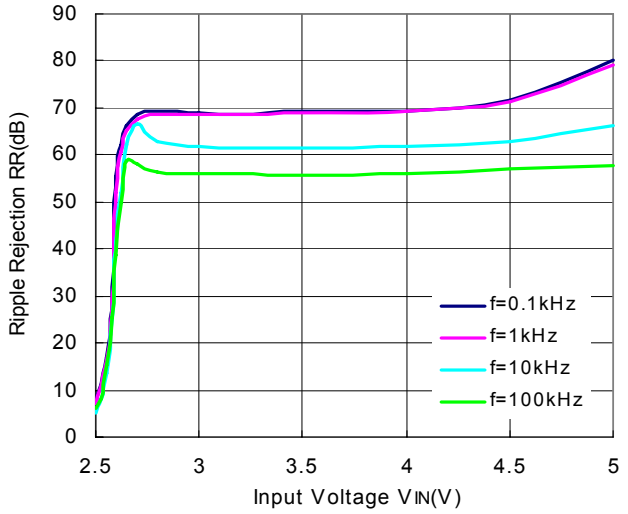
7) Dropout Voltage vs. Set Output Voltage



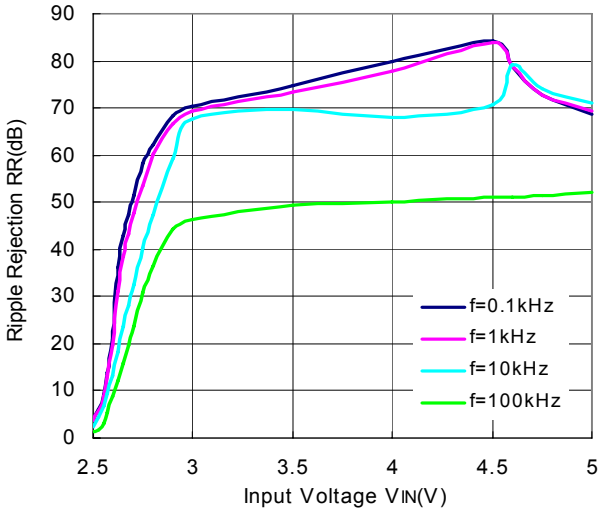
8) Minimum Operating Voltage
0.8V(VR1/VR2)



9) Ripple Rejection vs Input Voltage (Ta=25°C, Ripple 0.2Vp-p, CIN=none, COUT=Ceramic 0.22µF)
2.5V(VR1/VR2) IOUT=1mA

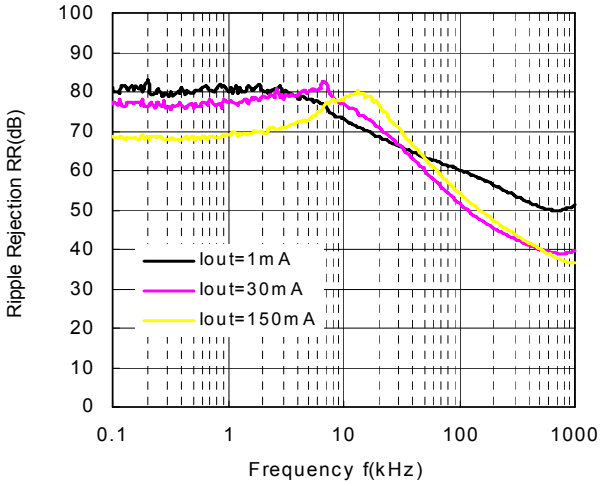


2.5V(VR1/VR2) IOUT=30mA

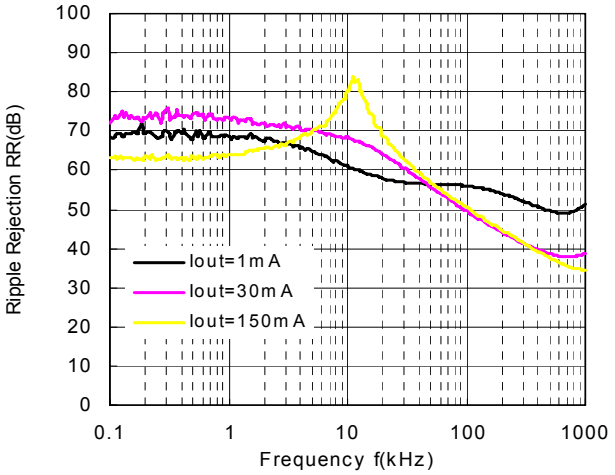


10) Ripple Rejection vs. Temperature (Ta=25°C, CIN=none, COUT=Ceramic 0.22µF)

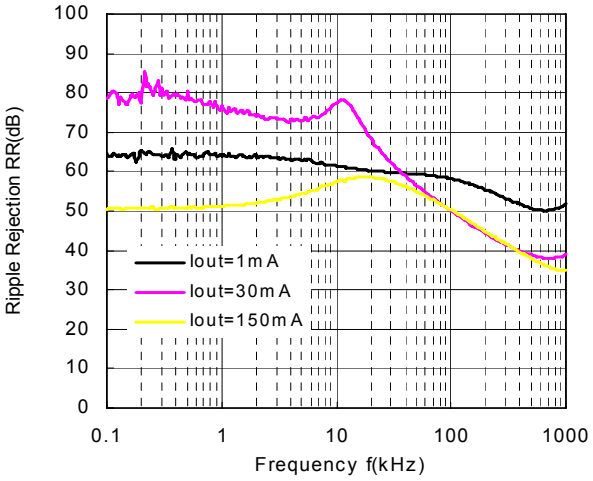
0.8V(VR1/VR2) VIN=3.0VDC+0.2Vp-p



2.5V(VR1/VR2) VIN=3.5VDC+0.2Vp-p

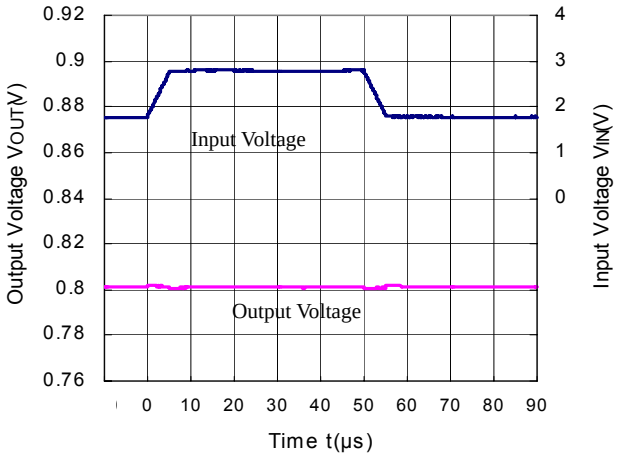


3.6V(VR1/VR2) VIN=4.6VDC+0.2Vp-p

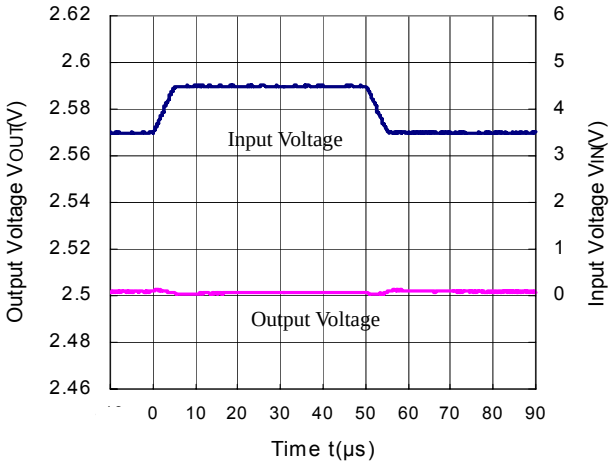


11) Input Transient Response (IOUT=30mA, tr=tf=5µs, CIN=none, COUT=0.22µF, Ta=25°C)

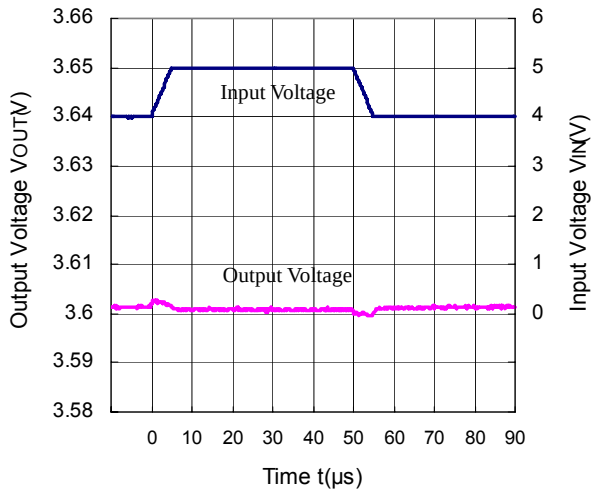
0.8V(VR1/VR2)



2.5V(VR1/VR2)

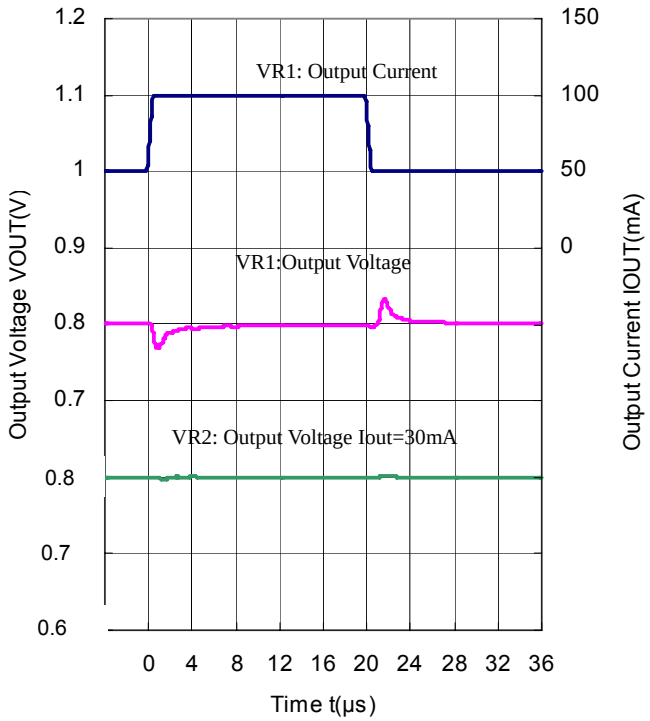


3.6V (VR1/VR2)

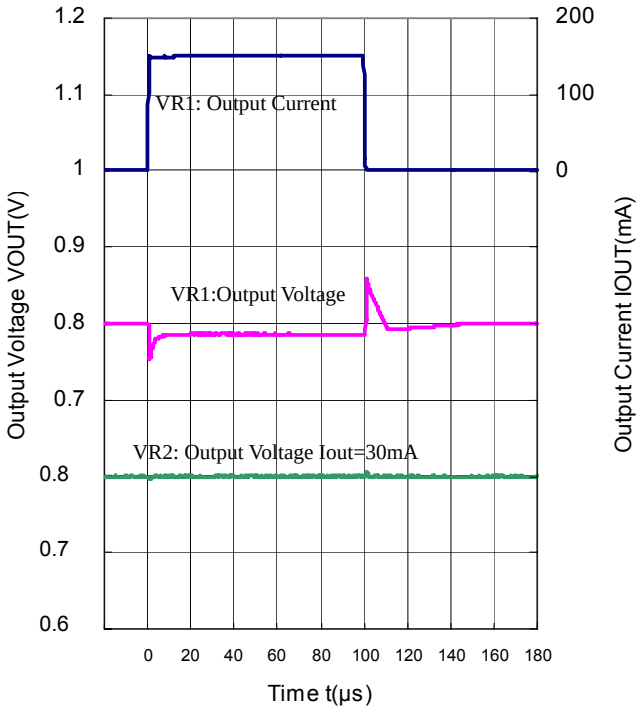


12) Load Transient Response (tr=tf=0.5µs, CIN=COUT=0.22µF, Ta=25°C)

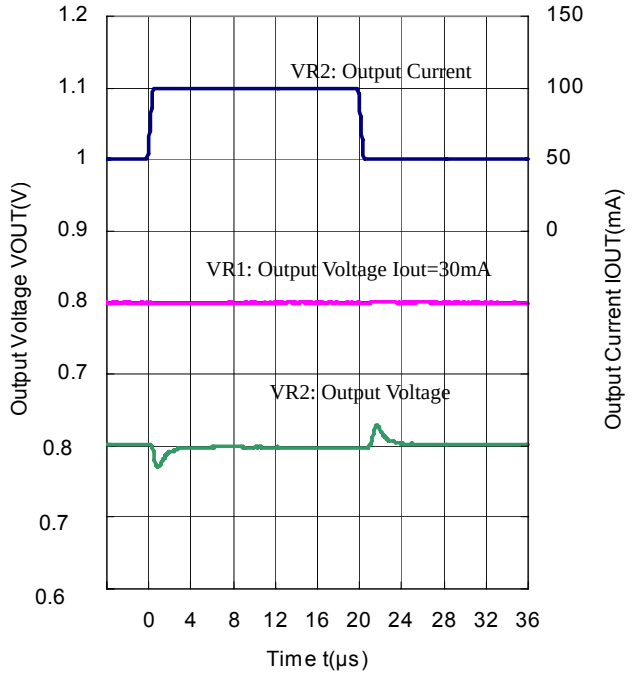
0.8V(VR1/VR2) VIN=1.8V



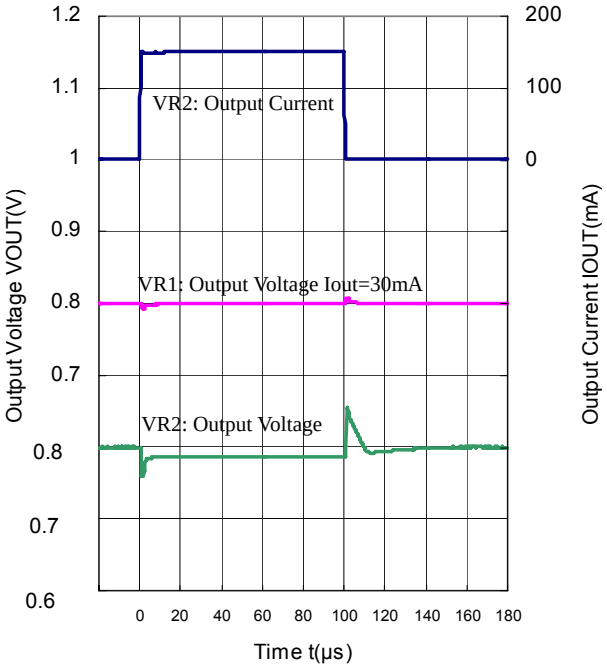
0.8V(VR1/VR2) VIN=1.8V



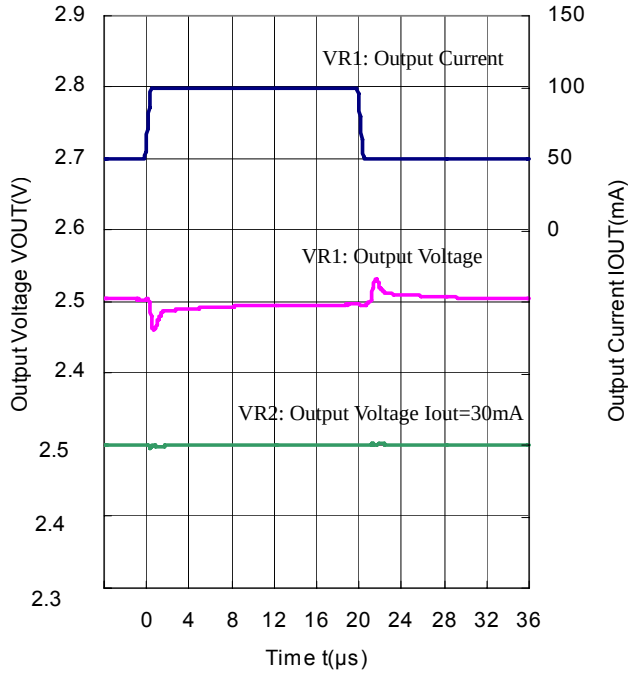
0.8V(VR1/VR2) VIN=1.8V



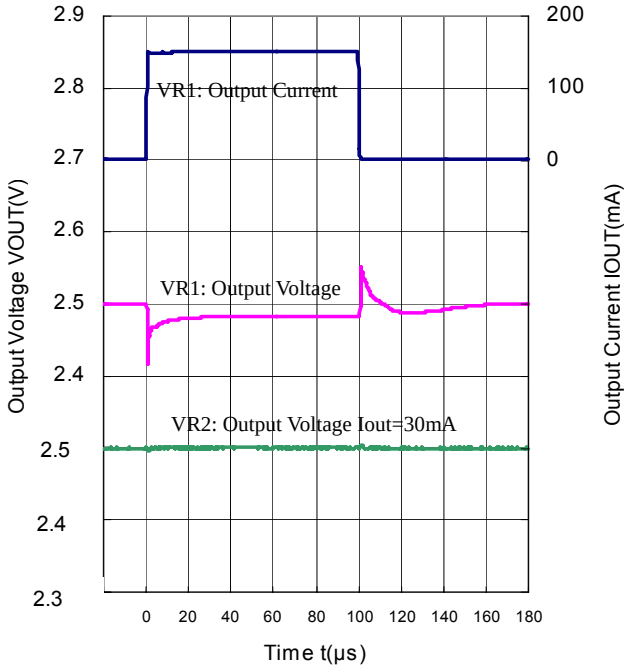
0.8V(VR1/VR2) VIN=1.8V



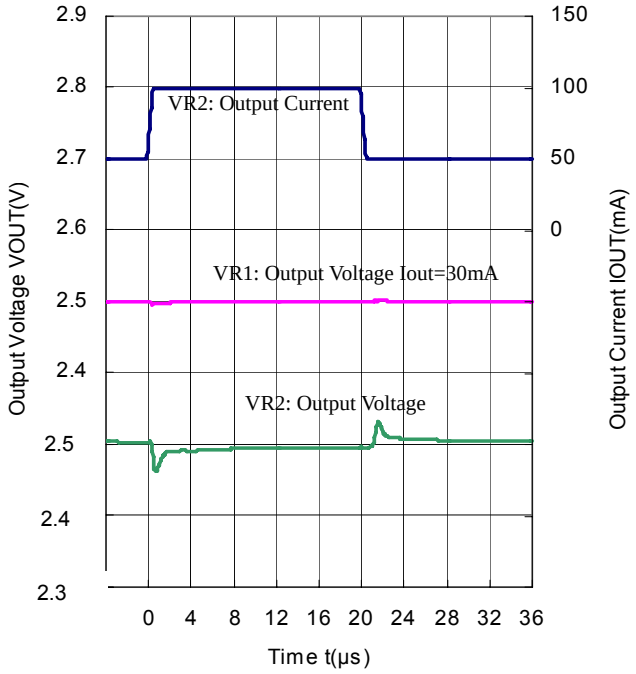
2.5V(VR1/VR2) VIN=3.5V



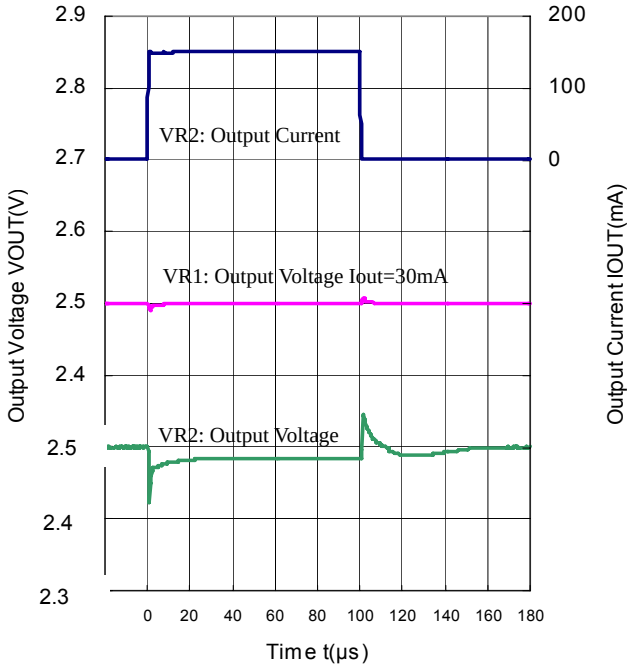
2.5V(VR1/VR2) VIN=3.5V



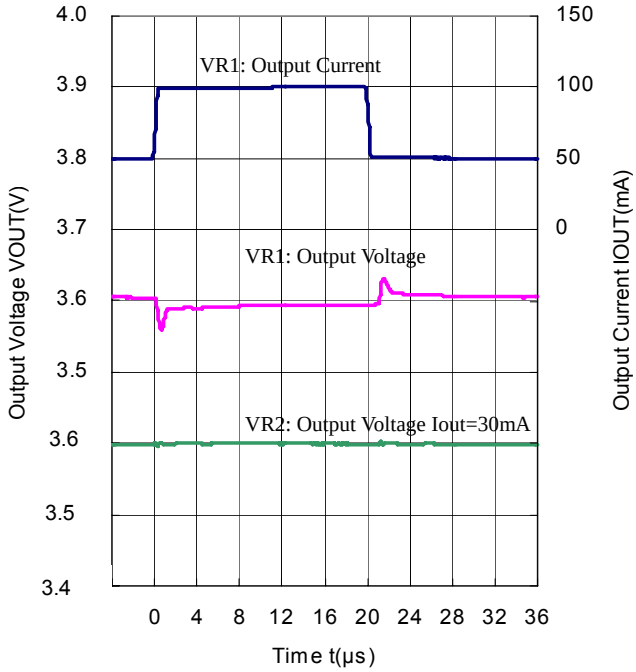
2.5V(VR1/VR2) VIN=3.5V



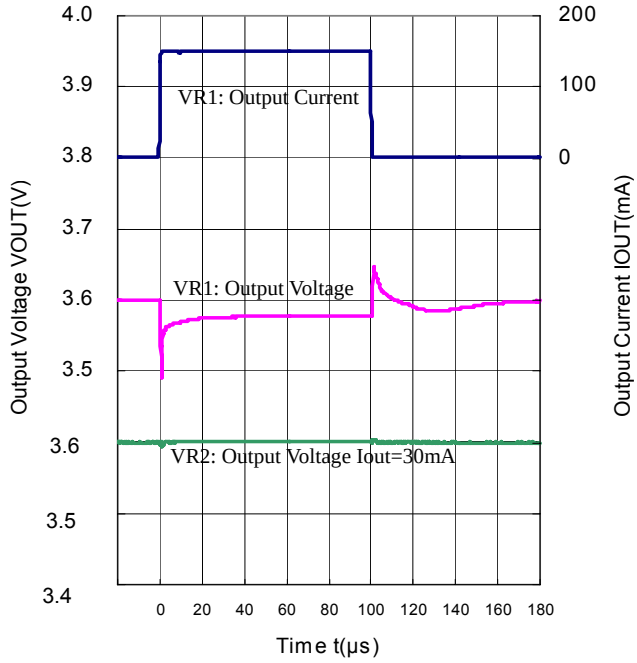
2.5V(VR1/VR2) VIN=3.5V



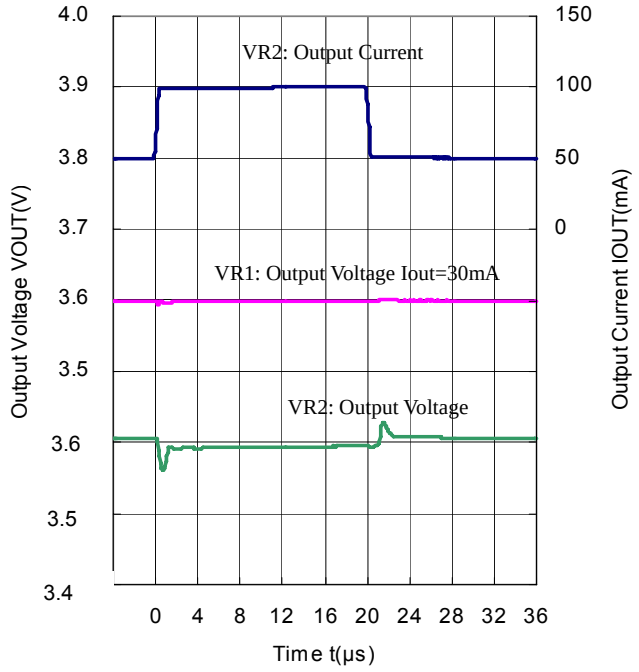
3.6V(VR1/VR2) VIN=4.6V



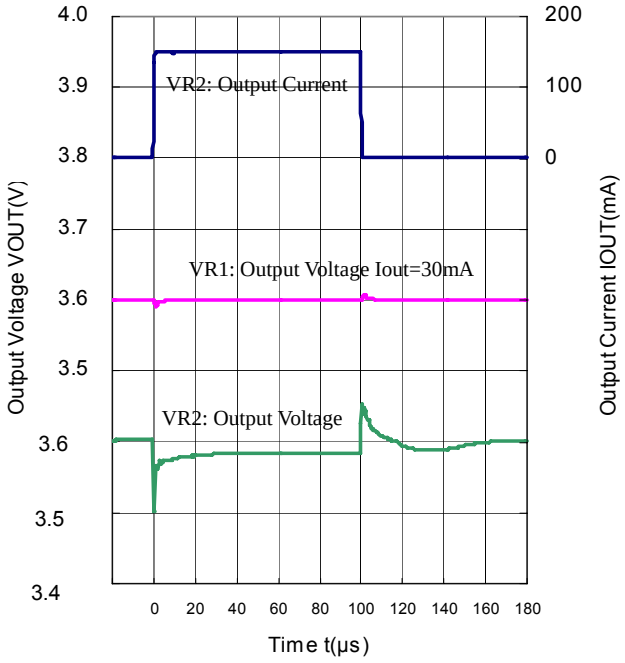
3.6V(VR1/VR2) VIN=4.6V



3.6V(VR1/VR2) VIN=4.6V

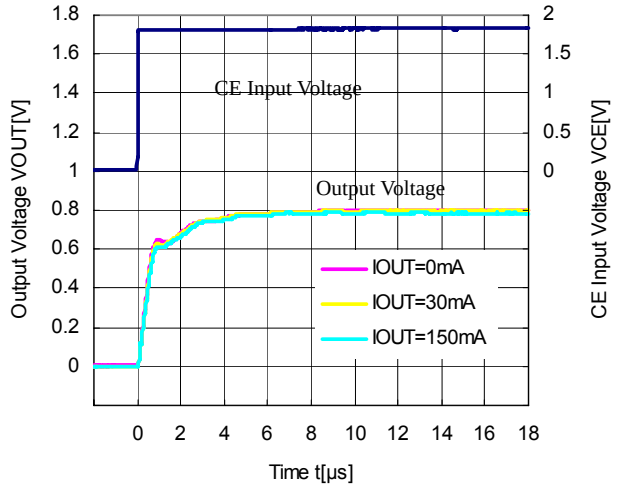


3.6V(VR1/VR2) VIN=4.6V

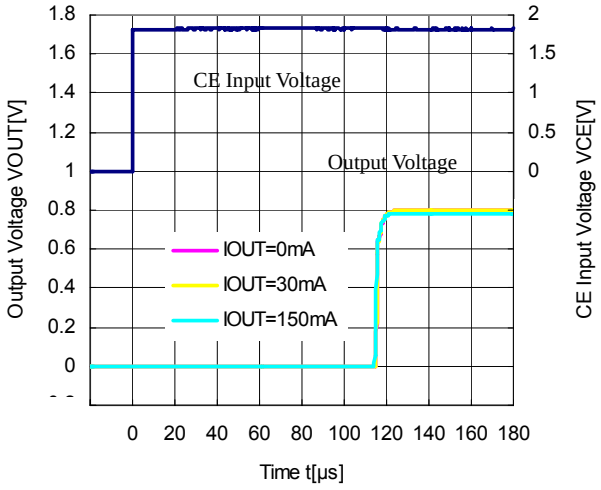


13) Turn on waveform with CE signal (Cin=Cout=0.22µF, Ta=25°C)

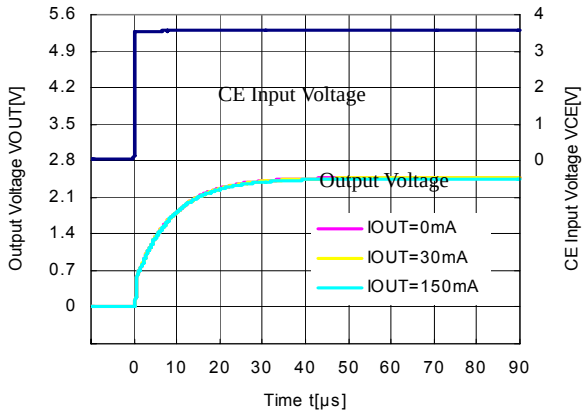
0.8V(VR1/2) version A/B, VR1 (version C)



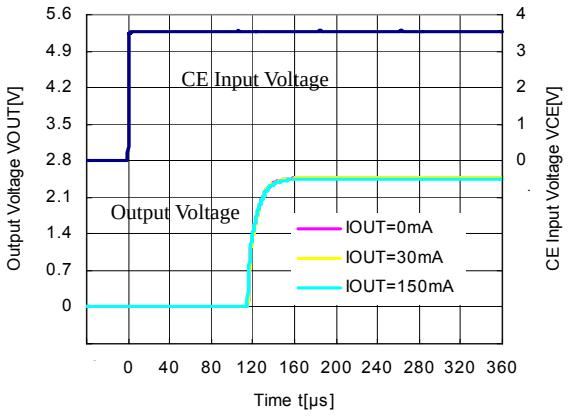
0.8V(VR2) version C VIN=1.8V



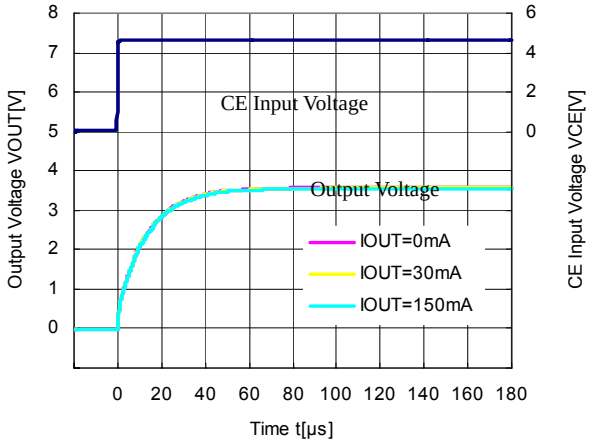
2.5V(VR1/2) version A/B, VR1 (version C)



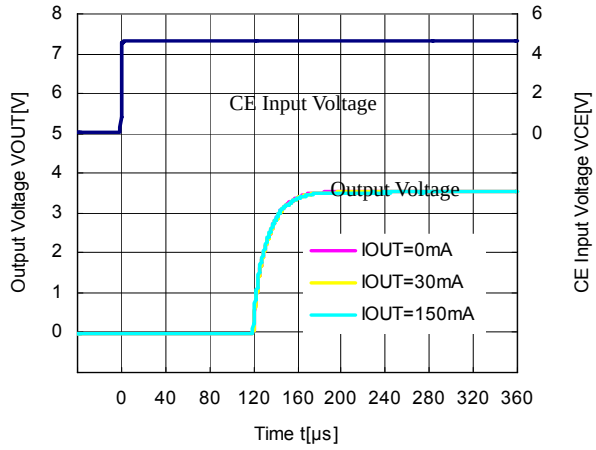
2.5V(VR2) version C, VIN=3.5V



3.6V(VR1/2) version A/B, VR1 (version C)

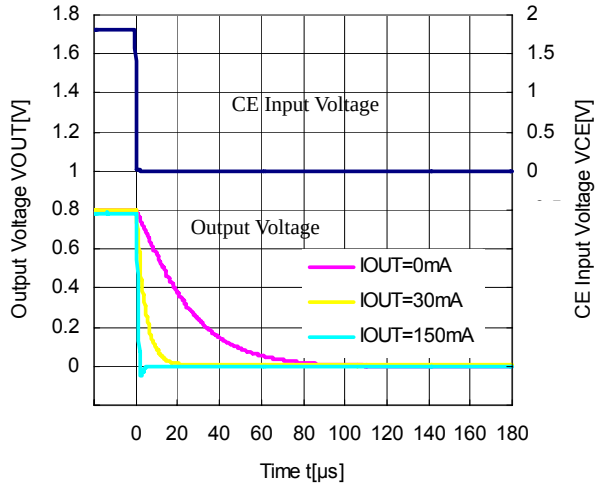


3.6V(VR2) version C, VIN=4.6V

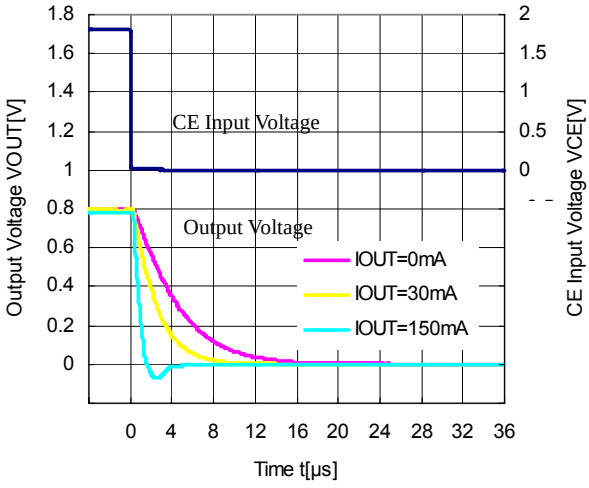


14) Turn off waveform with CE signal (Cin=Cout=0.22µF, Ta=25°C)

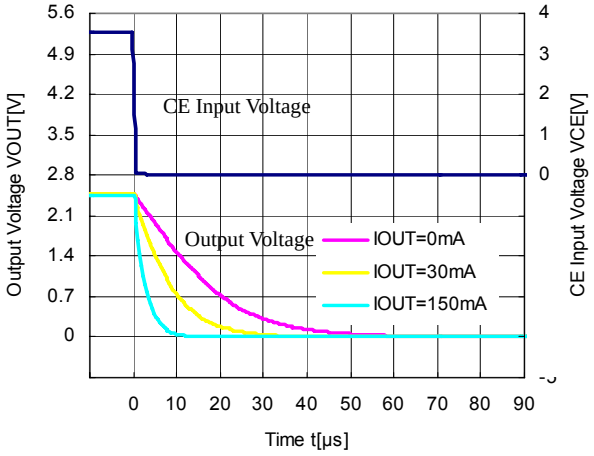
0.8V(VR1/2) version B, VR1 (version C)



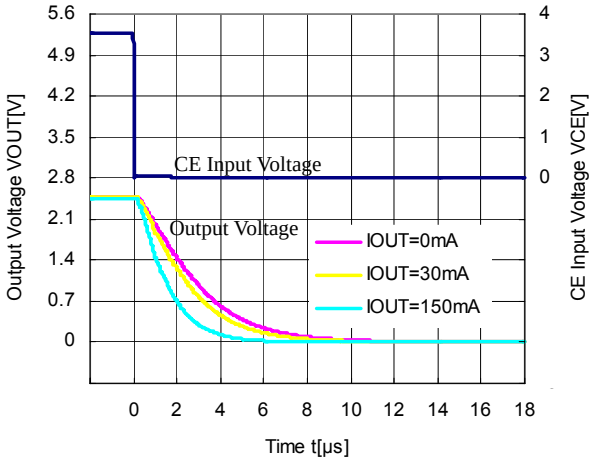
0.8V(VR2) version C, VIN=1.8V



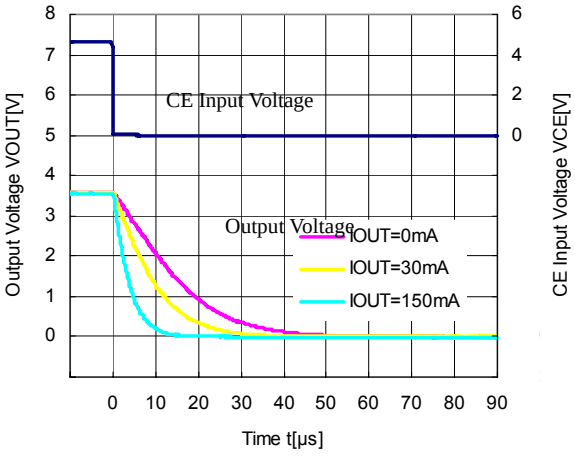
2.5V(VR1/2) version A/B, VR1 (version C)



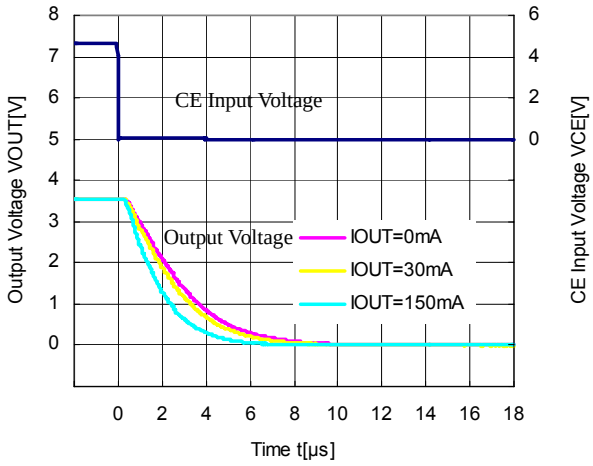
2.5V(VR2) version C



3.6V(VR1/2) version A/B, VR1(version C)

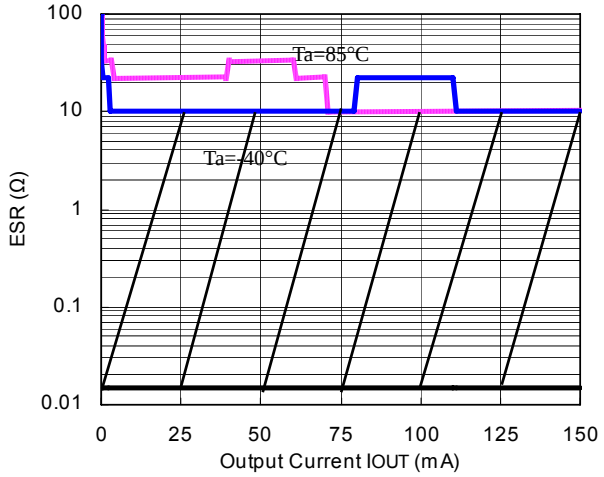


3.6V(VR2) version C

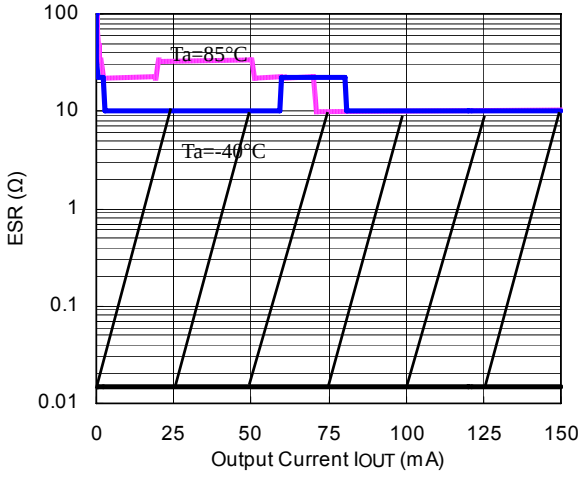


15) Stable area with the appropriate ESR value range of an external capacitor vs. output current/ CIN=COUT=0.22µF(GRM155B10J224KE01/Murata)

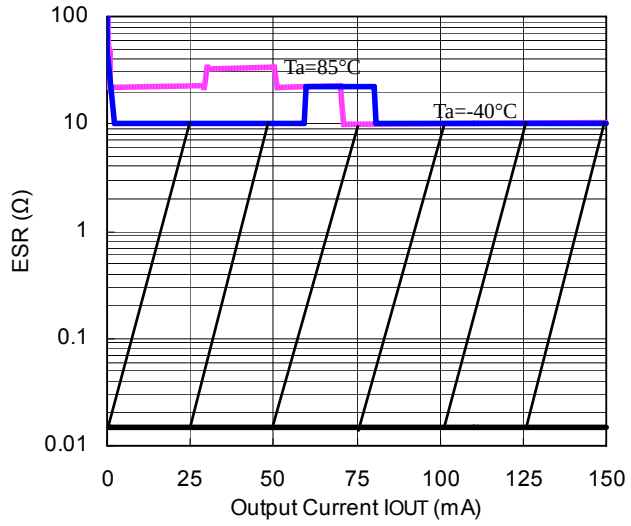
0.8V(VR1/VR2) VIN=1.4V-5.0V



2.5V(VR1/VR2) VIN=2.6V-5.0V



3.6V(VR1/VR2) VIN=3.7V-5.0V



POWER DISSIPATION (RP152N: SOT-23-6)

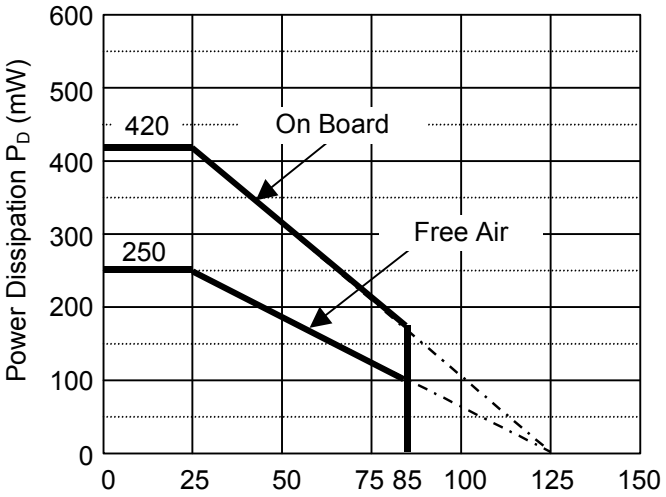
This specification is at mounted on board. Power Dissipation (P_D) depends on conditions of mounting on board. This specification is based on the measurement at the condition below:

Measurement Conditions

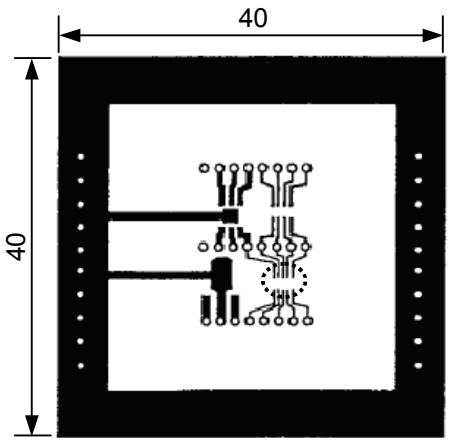
	Standard Land Pattern
Environment	Mounting on Board (Wind velocity=0m/s)
Board Material	Glass cloth epoxy plastic (Double sided)
Board Dimensions	40mm x 40mm x 1.6mm
Copper Ratio	Top side: Approx. 50%, Back side: Approx. 50%
Through-hole	ϕ0.5mm x 44pcs

Measurement Result (Ta=25°C, Tjmax=125°C)

	Standard Land Pattern	Free Air
Power Dissipation	420mW	250mW
Thermal Resistance	θja=(125−25°C)/0.42W=263°C/W	400°C/W



Power Dissipation



Measurement Board Pattern

IC Mount Area Unit: mm

POWER DISSIPATION (RP152L: DFN1212-6)

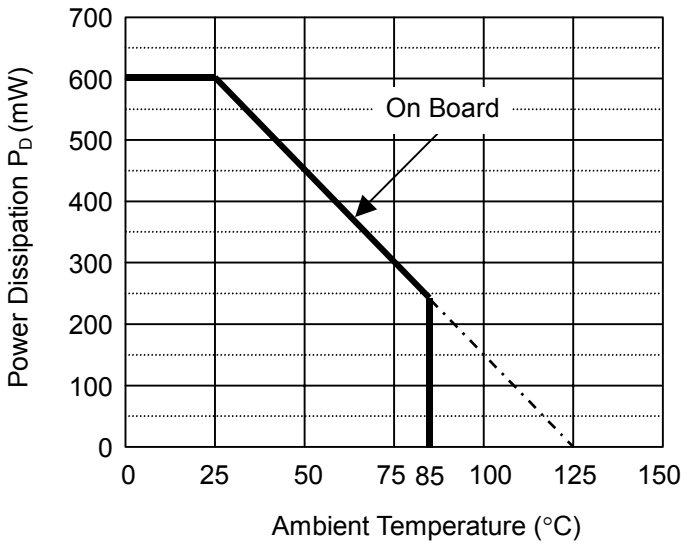
This specification is at mounted on board. Power Dissipation (P_D) depends on conditions of mounting on board. This specification is based on the measurement at the condition below:

Measurement Conditions

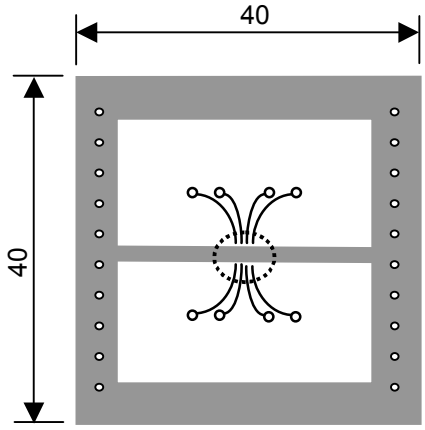
	Standard Test Land Pattern
Environment	Mounting on Board (Wind velocity=0m/s)
Board Material	Glass cloth epoxy plastic (Double sided)
Board Dimensions	40mm*40mm*1.6mm
Copper Ratio	Top side: Approx. 50%, Back side: Approx. 50%
Through-holes	ϕ 0.5mm * 28pcs

Measurement Result (Ta=25°C, Tjmax=125°C)

	Standard Test Land Pattern
Power Dissipation	600mW
Thermal Resistance	θja = (125-25°C)/0.6W = 167°C/W
	θjc = 30 °C/W



Power Dissipation



Measurent Board Pattern

IC Mount Area Unit : mm

POWER DISSIPATION (RP153L: DFN1216-8)

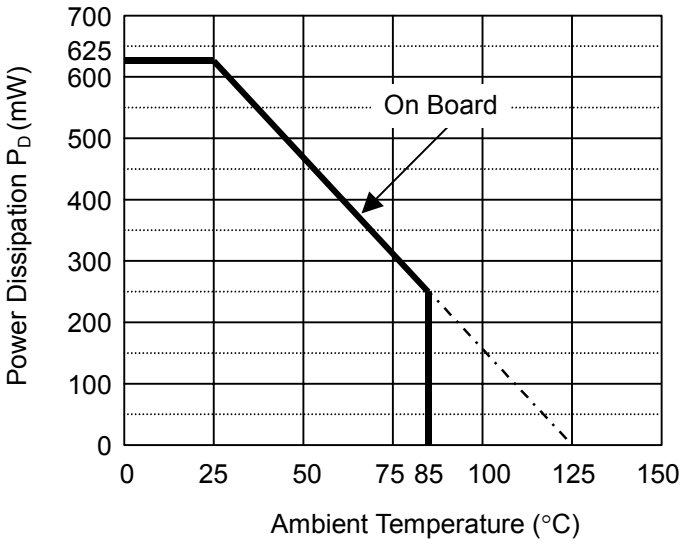
This specification is at mounted on board. Power Dissipation (P_D) depends on conditions of mounting on board. This specification is based on the measurement at the condition below:

Measurement Conditions

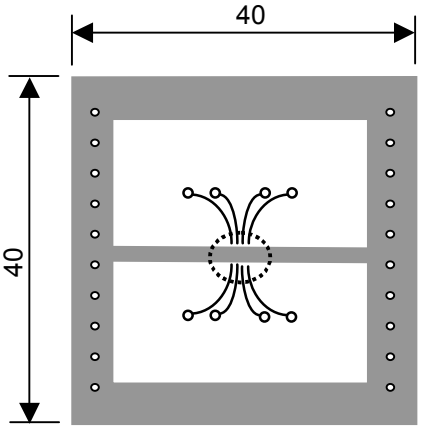
	Standard Test Land Pattern
Environment	Mounting on Board (Wind velocity=0m/s)
Board Material	Glass cloth epoxy plastic (Double sided)
Board Dimensions	40mm*40mm*1.6mm
Copper Ratio	Top side: Approx. 50%, Back side: Approx. 50%
Through-holes	ϕ 0.5mm * 28pcs

Measurement Result (Ta=25°C, Tjmax=125°C)

	Standard Test Land Pattern
Power Dissipation	625mW
Thermal Resistance	θja = (125-25°C)/0.6W = 167°C/W
	θjc = 30 °C/W



Power Dissipation



Measurent Board Pattern

IC Mount Area Unit : mm