

# Cost-Effective, 1.8A Sink/Source Bus Termination Regulator

## General Description

The RP1210 is a simple, cost-effective and high-speed linear regulator designed to generate termination voltage in double data rate (DDR) memory system to comply with the devices requirements. The regulator is capable of actively sinking or sourcing up to 1.8A while regulating an output voltage to within 20mV. The output termination voltage can be tightly regulated to track  $V_{DDQ}/2$  by two external voltage divider resistors or the desired output voltage can be programmed by externally forcing the REFEN pin voltage.

The RP1210 also incorporates a high-speed differential amplifier to provide ultra-fast response in line/load transient. Other features include extremely low initial offset voltage, excellent load regulation, current limiting in bi-directions and on-chip thermal shutdown protection.

## Ordering Information

RP1210	□	□
	Package Type	
	SP : SOP-8 (Exposed Pad-Option 2)	
	Operating Temperature Range	
	G : Green (Halogen Free with Commercial Standard)	

Note :

Richpower Green products are :

- ▶ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▶ Suitable for use in SnPb or Pb-free soldering processes.

## Features

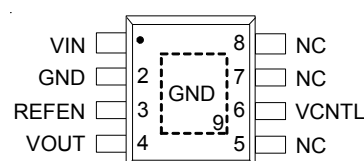
- Ideal for DDRII / DDRIII  $V_{TT}$  Applications
- Sink and Source Current :
  - ▶ 1.8A Sink/Source @  $V_{IN} = 1.8V$
  - ▶ 1.5A Sink/Source @  $V_{IN} = 1.5V$
  - ▶ 1.2A Sink/Source @  $V_{IN} = 1.2V$
- Integrated Power MOSFETs
- Generate Termination Voltage for DDR Memory Interfaces
- High Accuracy Output Voltage at Full-Load
- Output Adjustment by Two External Resistors
- Low External Component Count
- Shutdown for Suspend to RAM (STR) Functionality with High-Impedance Output
- Current Limiting Protection
- On-Chip Thermal Protection
- RoHS Compliant
- Stable with 2.2 $\mu$ F Output Ceramic Capacitor

## Applications

- Desktop PCs, Notebooks, and Workstations
- Graphics Card Memory Termination
- Set Top Boxes, Digital TVs, Printers
- Embedded Systems
- Active Termination Buses
- DDRII/DDRIII Memory Systems

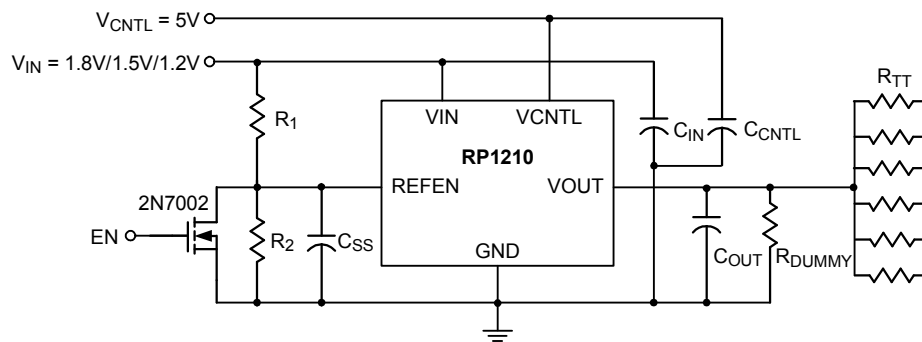
## Pin Configurations

(TOP VIEW)



SOP-8 (Exposed Pad-Option 2)

## Typical Application Circuit



$$R_1 = R_2 = 100k\Omega, R_{TT} = 50\Omega / 33\Omega / 25\Omega$$

$R_{DUMMY} = 1k\Omega$  as for  $V_{OUT}$  discharge when  $V_{IN}$  is not presented but  $V_{CNTL}$  is presented

$C_{OUT} = 10\mu F$  (Ceramic) under the worst case testing condition

$C_{IN} = 10\mu F, C_{CNTL} = 1\mu F, C_{SS} = 1nF$  to  $0.1\mu F$

## Test Circuit

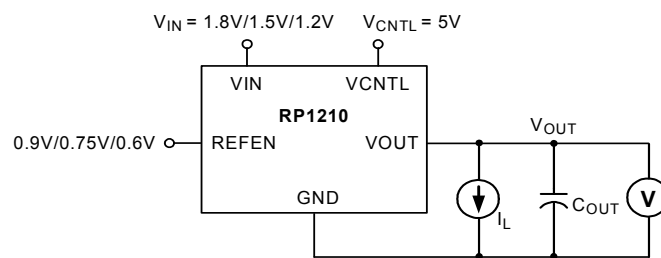


Figure 1. Output Voltage Tolerance,  $\Delta V_{LOAD}$

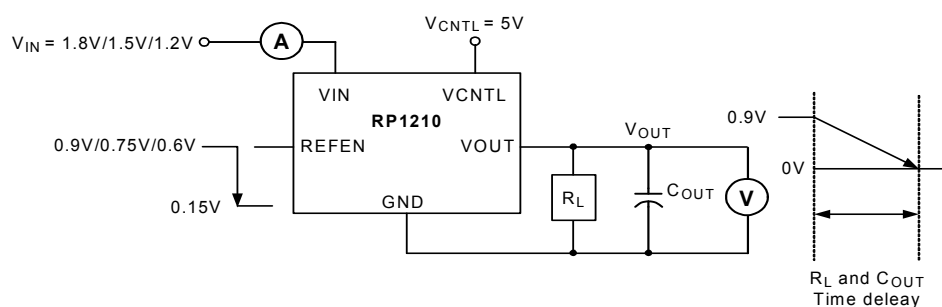


Figure 2. Current in Shutdown Mode,  $I_{STBY}$

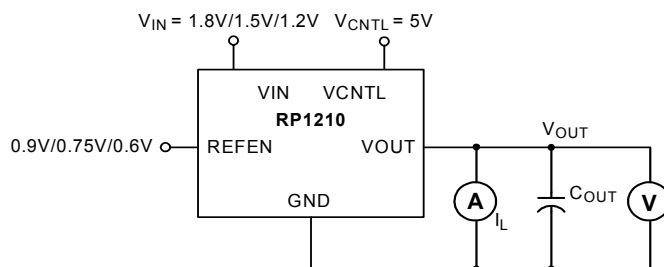


Figure 3. Current Limit for High Side,  $I_{LIM}$

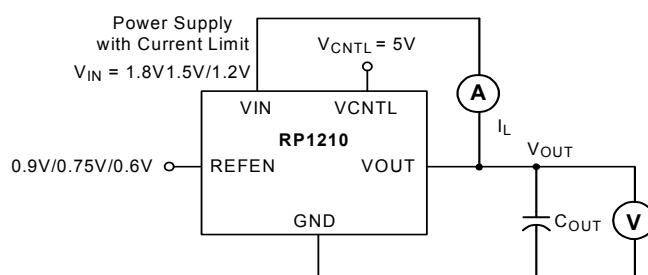


Figure 4. Current Limit for Low Side,  $I_{LIM}$

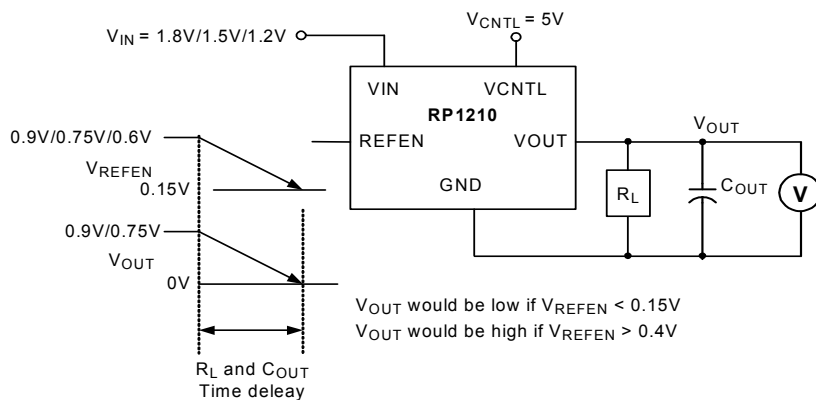
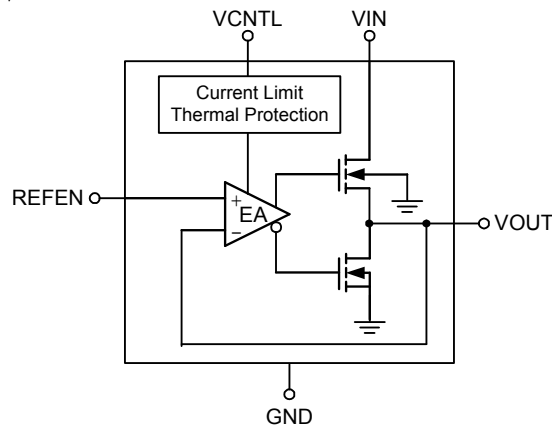


Figure 5. REFEN Pin Shutdown Threshold,  $V_{IH}$  &  $V_{IL}$

## Function Block Diagram



## Functional Pin Description

### VIN

Input voltage which supplies current to the output pin. Connect this pin to a well-decoupled supply voltage. To prevent the input rail from dropping during large load transient, a large, low ESR capacitor is recommended to use. The capacitor should be placed as close as possible to the VIN pin.

### GND (Exposed Pad)

Common Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

### VCNTL

VCNTL supplies the internal control circuitry and provides the drive voltage. The driving capability of output current is proportioned to the VCNTL. Connect this pin to 5V bias supply to handle large output current with at least 1 $\mu$ F capacitor from this pin to GND. An important note is that VIN should be kept lower or equal to VCNTL.

### REFEN

Reference voltage input and active low shutdown control pin. Two resistors dividing down the VIN voltage on this pin to create the regulated output voltage. Pulling this pin to ground turns off the device by an open-drain, such as 2N7002, signal N-MOSFET.

### VOUT

Regulator output. VOUT is regulated to REFEN voltage that is used to terminate the bus resistors. It is capable of sinking and sourcing current while regulating the output rail. To maintain adequate large signal transient response, typical value of 10 $\mu$ F ceramic capacitors are recommended to reduce the effects of current transients on VOUT.

## Absolute Maximum Ratings (Note 1)

• Input Voltage, $V_{IN}$	6V
• Control Voltage, $V_{CNTL}$	6V
• Power Dissipation, $P_D$ @ $T_A = 25^\circ\text{C}$	
SOP-8 (Exposed Pad)	1.163W
• Package Thermal Resistance (Note 4)	
SOP-8 (Exposed Pad), $\theta_{JA}$	86°C/W
SOP-8 (Exposed Pad), $\theta_{JC}$	15°C/W
• Junction Temperature	150°C
• Lead Temperature (Soldering, 10 sec.)	260°C
• Storage Temperature Range	- 65°C to 150°C
• ESD Susceptibility (Note 2)	
HBM (Human Body Mode)	2kV
MM (Machine Mode)	200V

## Recommended Operating Conditions (Note 3)

• Input Voltage, $V_{IN}$	1.0V to 5.5V
• Control Voltage, $V_{CNTL}$	5V $\pm$ 5%
• Junction Temperature Range	-40°C to 125°C
• Ambient Temperature Range	-40°C to 85°C

## Electrical Characteristics

( $V_{IN} = 1.8\text{V}/1.5\text{V}$ ,  $V_{CNTL} = 5\text{V}$ ,  $V_{REFEN} = 0.9\text{V}/0.75\text{V}$ ,  $C_{OUT} = 10\mu\text{F}$  (Ceramic),  $T_A = 25^\circ\text{C}$ , unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Input						
VCNTL Operation Current	ICNTL	IOUT = 0A	--	0.7	2.5	mA
VCNTL Power-on Reset	VPOR	VCNTL Rising	--	3.6	--	V
Standby Current (Note 7)	ISTBY	VREFEN < 0.15V (Shutdown), RLOAD = 180Ω	--	20	90	μA
Output						
Output Offset Voltage (Note 5)	VOS	IOUT = 0A	-20	--	+20	mV
Load Regulation (Note 6)	ΔVLOAD	VIN = 1.8V, VREFEN = 0.9V, IOUT = ±1.8A	-20	--	+20	mV
		VIN = 1.5V, VREFEN = 0.75V, IOUT = ±1.5A				
		VIN = 1.2V, VREFEN = 0.6V, IOUT = ±1.2A				
Protection						
Current Limit	ILIMIT	VIN = 1.8V, VREFEN = 0.9V	1.8	--	3.5	A
		VIN = 1.5V, VREFEN = 0.75V				
Short Circuit Current		VIN = 1.8V/1.5V/1.2V, VOUT < 0.2V	--	1.5	--	A
Thermal Shutdown Temperature	TSD	VCNTL = 5V	125	170	--	°C
Thermal Shutdown Hysteresis	ΔTSD	VCNTL = 5V	--	35	--	°C
REFEN Shutdown						
Shutdown Threshold	VIH	Enable	0.4	--	--	V
	VIL	Shutdown	--	--	0.15	

**Note 1.** Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

**Note 2.** Devices are ESD sensitive. Handling precaution is recommended.

**Note 3.** The device is not guaranteed to function outside its operating conditions.

**Note 4.**  $\theta_{JA}$  is measured in the natural convection at  $T_A = 25^\circ\text{C}$  on a high effective thermal conductivity test board (4 Layers, 2S2P) of JEDEC 51-7 thermal measurement standard. The case point of  $\theta_{JC}$  is on the exposed pad for SOP-8 (Exposed Pad) package.

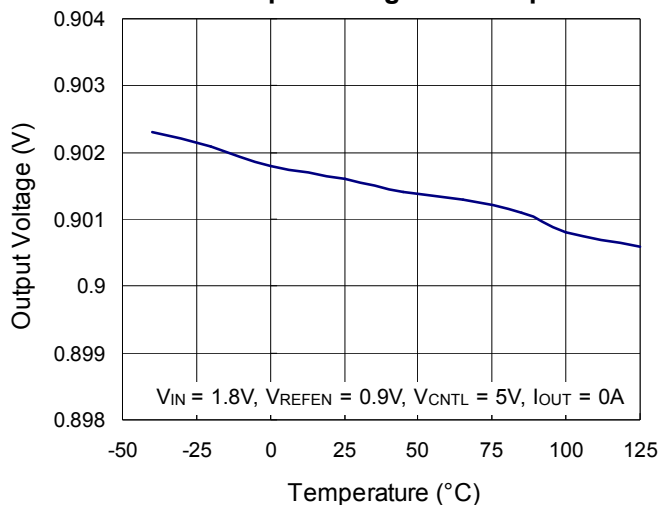
**Note 5.**  $V_{OS}$  offset is the voltage measurement defined as  $V_{OUT}$  subtracted from  $V_{REFEN}$ .

**Note 6.** Regulation is measured at constant junction temperature by using a 5ms current pulse. Devices are tested for load regulation in the load range from 0A to 1.8A peak.

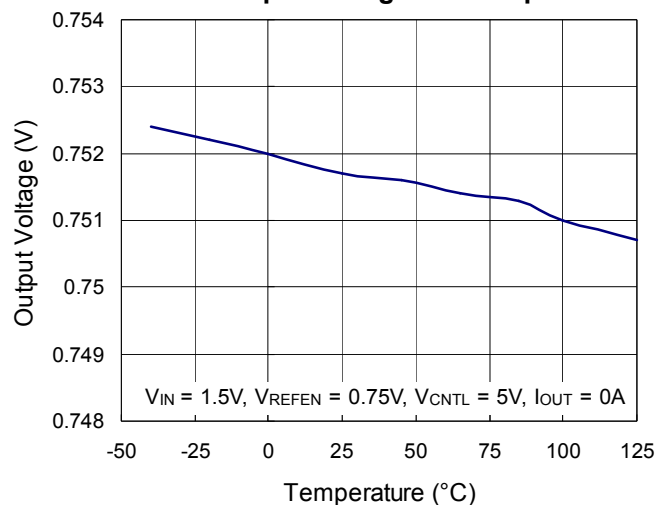
**Note 7.** Standby current is the input current drawn by a regulator when the output voltage is disabled by a shutdown signal on REFEN pin ( $V_{IL} < 0.15\text{V}$ ). It is measured with  $V_{IN} = 1.8\text{V}$ ,  $V_{CNTL} = 5\text{V}$ .

## Typical Operating Characteristics

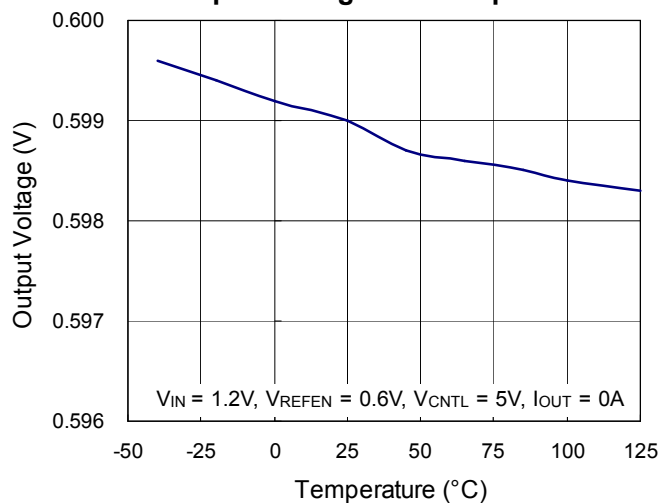
**DDR II Output Voltage vs. Temperature**



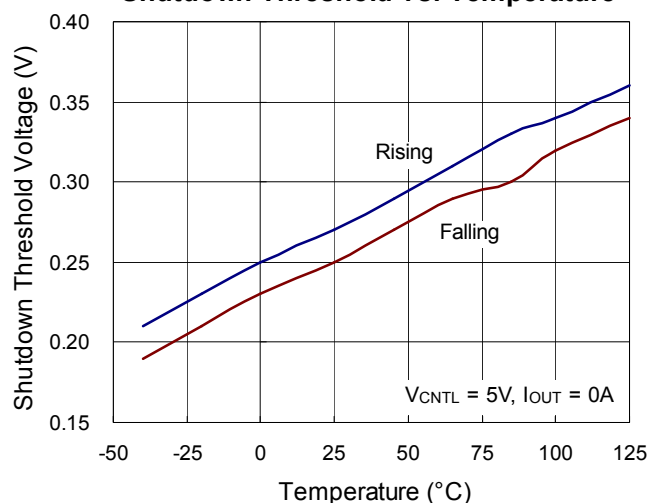
**DDR III Output Voltage vs. Temperature**



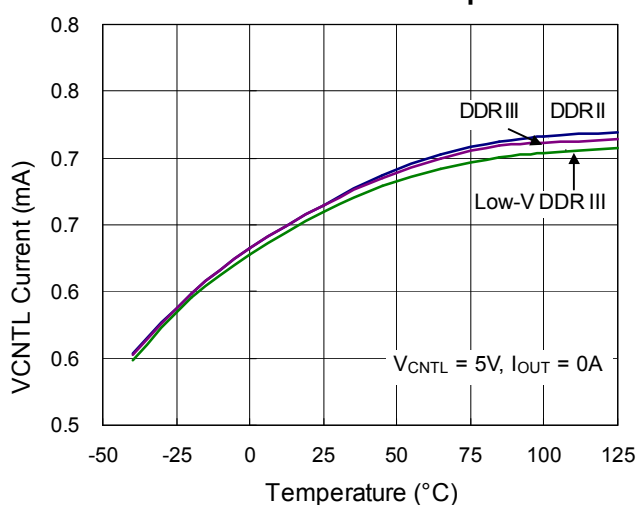
**Output Voltage vs. Temperature**



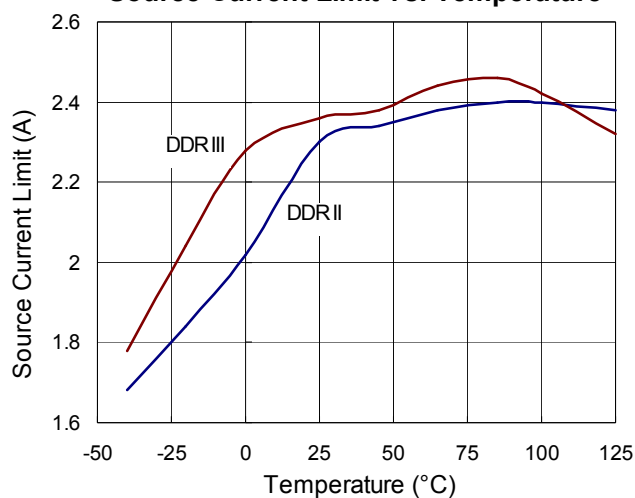
**Shutdown Threshold vs. Temperature**



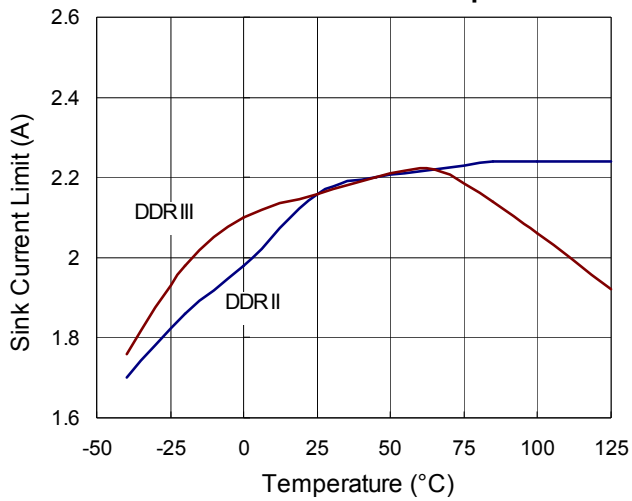
**VCNTL Current vs. Temperature**



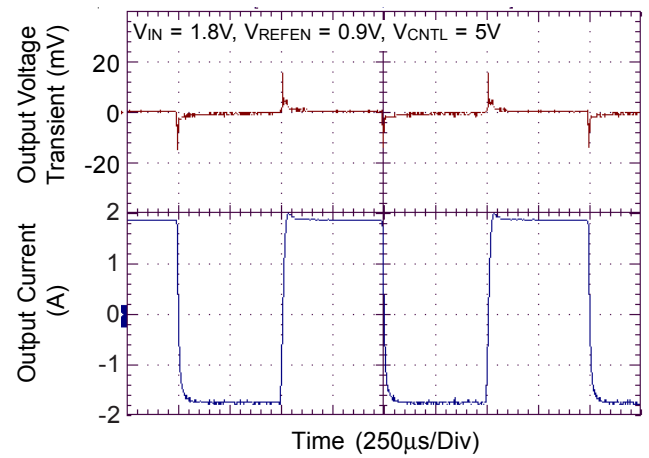
**Source Current Limit vs. Temperature**



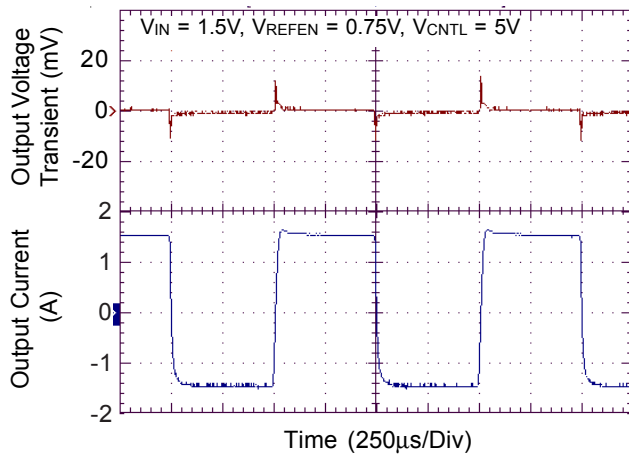
### Sink Current Limit vs. Temperature



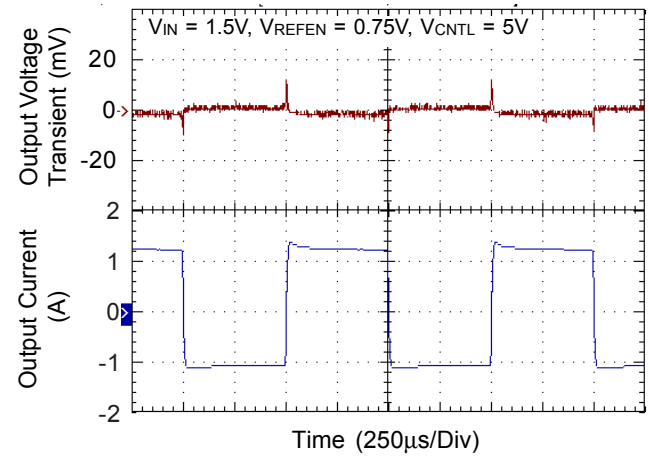
### 0.9V<sub>TT</sub> @ 1.8A Transient Response



### 0.75V<sub>TT</sub> @ 1.5A Transient Response



### 0.6V<sub>TT</sub> @ 1.2A Transient Response





## Application Information

### Output Voltage Setting

The RP1210 is a high-speed linear regulator designed to generate termination voltage in double data rate (DDR) memory system. Besides, the RP1210 could also serve as a general linear regulator. The RP1210 accepts an external reference voltage at the REFEN pin and provides an output voltage regulated to this reference voltage level as shown in Figure 6, where

$$V_{OUT} = V_{IN} \times R2 / (R1 + R2)$$

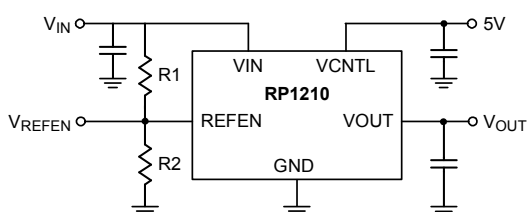


Figure 6. RP1210 operating as a linear regulator

### Shutdown Control

Refer to the "Typical Application Circuit". Make sure the current sinking capability of pull-down NMOS is enough for the chosen voltage divider to pull-down the voltage at REFEN pin below 0.15V to shutdown the device.

In addition, the capacitor  $C_{SS}$  and voltage divider form the low-pass filter.

### Current Limit & Short Circuit Protection

The RP1210 implements the current limit and output short protection circuit against the unexpected applications. The current limit circuit monitors and controls the pass transistor's gate voltage, providing the load current up to at least 1.8A. If the load current exceeds the current limit trip point, RP1210 will soon reduce the load current to around 1.5A constantly, refer to Figure 7.

If the output voltage is abruptly pulled down to less than 0.2V, the short circuit protection is triggered and then maintains the load current at 1.5A. It prevents RP1210 being damaged in case an output short to ground event occurs.

### Output Voltage vs. Output Current

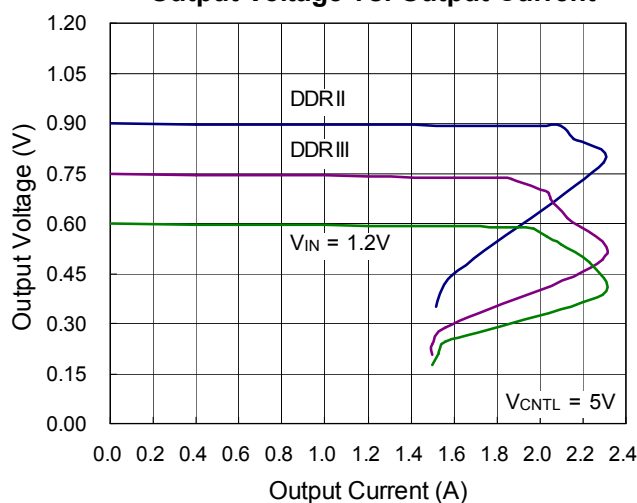


Figure 7

### Input Capacitor and Layout Consideration

Place the input bypass capacitor as close as possible to the RP1210. A low ESR capacitor larger than 20μF is recommended for the input capacitor. Use short and wide traces to minimize parasitic resistance and inductance. Inappropriate layout may result in large parasitic inductance and cause undesired oscillation between the RP1210 and the preceding power converter.

### Thermal Consideration

RP1210 regulators have internal thermal limiting circuitry designed to protect the device during overload conditions. For continued operation, do not exceed absolute maximum operation junction temperature of 125°C. The power dissipation definition in device is:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_Q$$

The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

$T_{J(MAX)}$  is the maximum operation junction temperature  $125^{\circ}\text{C}$ ,  $T_A$  is the ambient temperature and the  $\theta_{JA}$  is the junction to ambient thermal resistance. The junction to ambient thermal resistance for SOP-8 package (Exposed Pad) is  $86^{\circ}\text{C/W}$  on the standard JEDEC 51-7 (4 layers, 2S2P) thermal test board. The maximum power dissipation at  $T_A = 25^{\circ}\text{C}$  can be calculated by following formula:

$$P_{D(MAX)} = (125^{\circ}\text{C} - 25^{\circ}\text{C}) / (86^{\circ}\text{C/W}) = 1.163\text{W}$$

Figure 8 shows the package sectional drawing of SOP-8 (Exposed Pad). Every package has several thermal dissipation paths. As shown in Figure 9, the thermal resistance equivalent circuit of SOP-8 (Exposed Pad). The path 2 is the main path due to these materials thermal conductivity. We define the exposed pad is the case point of the path 2.

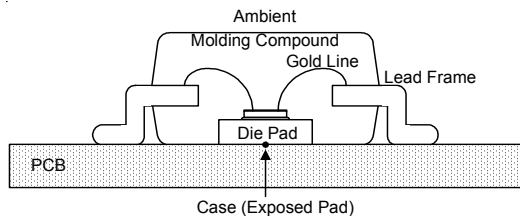


Figure 8. SOP-8 (Exposed Pad) Package Sectional Drawing

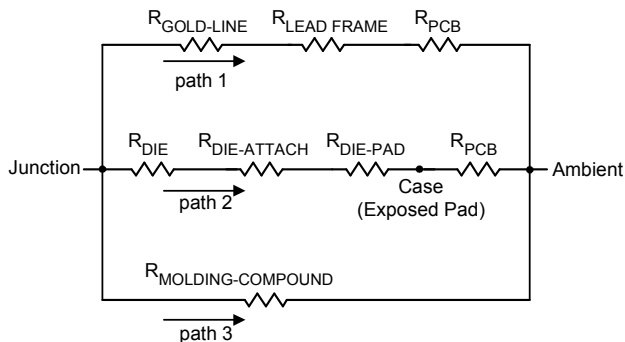


Figure 9. Thermal Resistance Equivalent Circuit

The thermal resistance  $\theta_{JA}$  of SOP-8 (Exposed Pad) is determined by the package design and the PCB design. However, the package design has been decided. If possible, it's useful to increase thermal performance by the PCB design. The thermal resistance can be decreased by adding copper under the exposed pad of SOP-8 package.

Figure 10 shows the relation between thermal resistance  $\theta_{JA}$  and copper area on a standard JEDEC 51-7 (4 layers, 2S2P) thermal test board at  $T_A = 25^{\circ}\text{C}$ . We have to consider the copper couldn't stretch infinitely and avoid the tin overflow. We use the "Dog-Bone" copper patterns on the top layer as shown in Figure 11.

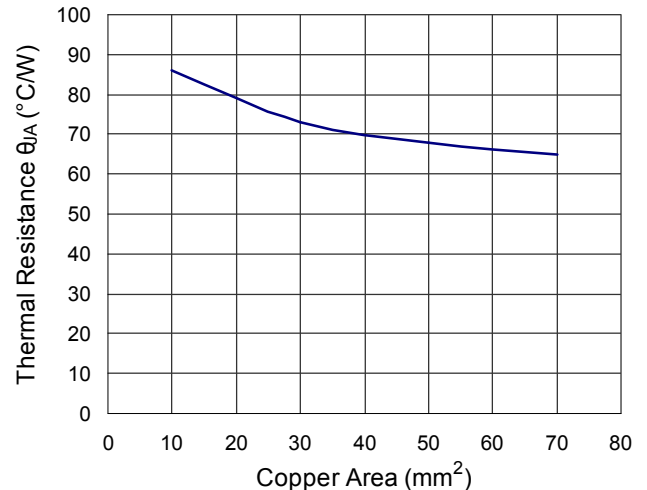


Figure 10. Relation Between Thermal Resistance  $\theta_{JA}$  and Copper Area

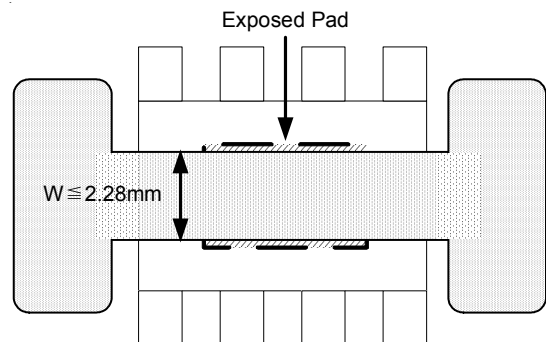
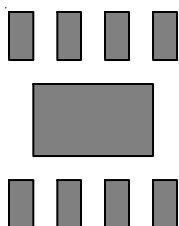
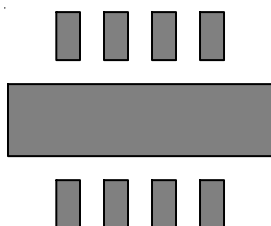


Figure 11. Dog-Bone Layout

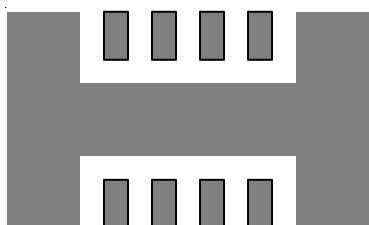
As shown in Figure 12, the amount of copper area to which the SOP-8 (Exposed Pad) is mounted affects thermal performance. When mounted to the standard SOP-8 (Exposed Pad) pad of 2 oz. copper (Figure 12.a),  $\theta_{JA}$  is  $86^{\circ}\text{C/W}$ . Adding copper area of pad under the SOP-8 (Exposed Pad) (Figure 12.b) reduces the  $\theta_{JA}$  to  $73^{\circ}\text{C/W}$ . Even further, increasing the copper area of pad to  $70\text{mm}^2$  (Figure 12.d) reduces the  $\theta_{JA}$  to  $65^{\circ}\text{C/W}$ .



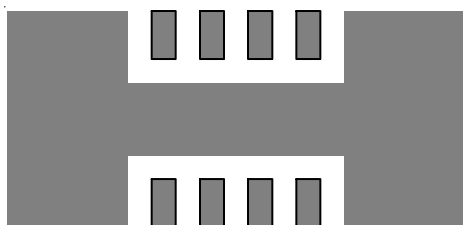
(a) Copper Area = 10mm<sup>2</sup>,  $\theta_{JA}$  = 86°C/W



(b) Copper Area = 30mm<sup>2</sup>,  $\theta_{JA}$  = 73°C/W



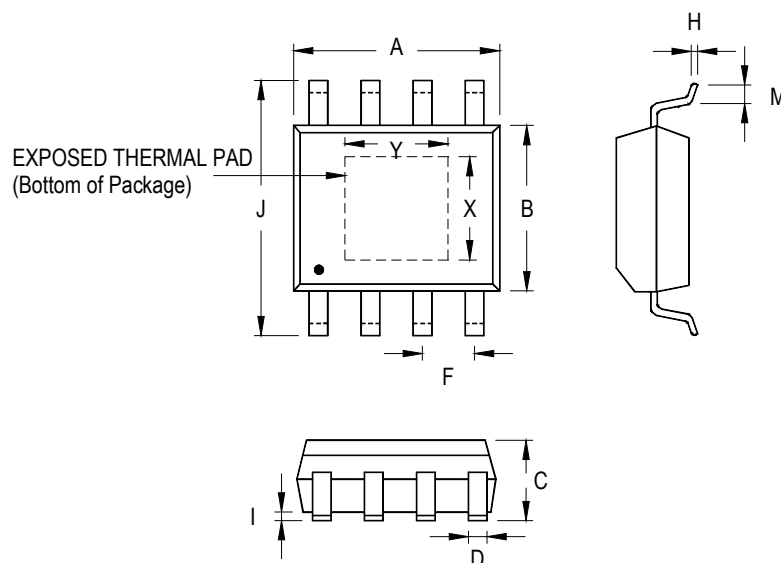
(c) Copper Area = 50mm<sup>2</sup>,  $\theta_{JA}$  = 68°C/W



(d) Copper Area = 70mm<sup>2</sup>,  $\theta_{JA}$  = 65°C/W

Figure 12. Thermal Resistance vs. Copper Area Layout  
Thermal Design

## Outline Dimension



Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		4.700	5.100	0.185	0.200
B		3.800	4.000	0.150	0.157
C		1.346	1.753	0.053	0.069
D		0.330	0.510	0.013	0.020
F		1.194	1.346	0.047	0.053
H		0.170	0.254	0.007	0.010
I		0.000	0.152	0.000	0.006
J		5.790	6.200	0.228	0.244
M		0.400	1.270	0.016	0.050
Option 1	X	2.000	2.300	0.079	0.091
	Y	2.000	2.300	0.079	0.091
Option 2	X	2.100	2.513	0.083	0.099
	Y	3.000	3.500	0.118	0.138

**8-Lead SOP (Exposed Pad) Plastic Package**

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