Rocktech Displays Limited
磐石电子有限公司

LCD Module Specification

Module P/N: RK028ML02

Version: 0.0

Description : 2.8 inch TFT 240*400 Pixels
With LED backlight

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Revision History

Date	Rev.	Page	Description
06/01/2011	0.0	All	First issue

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1. General Features

Item	Spec	Remark
Display Mode	Normally White transmissive	
Gray Scale Inversion Direction	6 O'CLOCK	
Input Signals	8/16 bit	
Outline Dimensions	42.5(H) x 71.4 (W) x2.0(D) Max.	
Active Area	36.72 mm(H)×61.2mm(W)	
Number of Pixels	240×RGB×400 Pixels	
Dot Pitch	0.153mm(H)×0.153mm(W)	
Pixel Arrangement	RGB Vertical stripes	
Drive IC	HX8352-B	

2. Absolute Maximum Ratings

The following are maximum values which, if exceeded may cause operation or damage to the unit.

ITEM	Sym.	Min.	Typ.	Max.	Unit	Remark
Power for Circuit Driving	Vcc	-0.3	-	4.6	V	
Power for Circuit Logic	Vt	-0.3	-	Vcc+0.3	V	
Storage Humidity	H_{ST}	10	-		%RH	At 25±5℃
Storage Temperature	T_{ST}	-30	-	80	℃	
Operating Ambient Humidity	H_{OP}	10	-		%RH	
Operating Ambient temperature	T_{OP}	-20	-	70	℃	

3. Electrical Specification

3.1 Driving TFT LCD Panel

Item		Sym.	Min	Typ.	Max	Unit	Note
Power for Circuit Driving		VCC	2.5	2.8	3.3	V	
Power for Circuit Logic		IOVCC	1.65	1.8	3.3	V	
Logic Input Voltage	Low Voltage	V_{IL}	-0.3	-	0.3IOVcc	V	
	High Voltage	V_{IH}	0.7IOVcc	-	IOVcc	V	
Logic Output Voltage	Low Voltage	V_{OL}	0	-	0.2IOVcc	V	
	High Voltage	V_{OH}	0.8IOVcc	-	-	V	
Power Consumption	Black Mode	P_b	T.B.D	T.B.D	T.B.D	mW	
	Standby Mode	P_w	T.B.D	T.B.D	T.B.D	mW	

3.2 Driving Backlight

Item	Sym.	Min	Typ.	Max	Unit	Note
Backlight driving voltage	V_F	3.0	3.2	3.4	V	
Backlight driving current	I_F	-	60	80	mA	
Backlight Power Consumption	W_{BL}	-	192	-	mW	
Lift Time	-	10,000	20,000	-		Note 3

Note 1: (Unless specified, the ambient temperature Ta=25℃)
Note 2: The recommended operating conditions refer to a range in which operation of this product is guaranteed. Should this range is exceeded, the operation cannot be guaranteed even if the values may be without the absolute maximum ratings.
Note 3: If LED is driven by high current, high ambient temperature & humidity condition. The life time of LED will be reduced. Operating life means brightness goes down to 50% initial brightness. Typical operating life time is estimated data.

4.Optical Specifications

Optical characteristics are determined after the unit has been 'ON' and stable for approximately 30 minutes in a dark environment at 25 ℃. The values specified are at an approximate distance 500mm from the LCD surface at a viewing angle of Φ and θ equal to 0°.

Item	Sym.	Values			Unit	Note
		Min.	Typ.	Max.		
1)Contrast Ratio	C/R	300	450	-		FIG.1
2)Module Luminance	L	200	240	-	cd/m^2	FIG.1
3)Response time	Tr+Tf	-	25	40	ms	FIG.2
4)Viewing Angle	θ_T	30	40	-	Degree	FIG.3
	θ_B	50	60	-		
	θ_L	50	60	-		
	θ_R	50	60	-		
5)Chromaticity	Wx	0.287	0.302	0.317		
	Wy	0.324	0.339	0.354		
	Rx	0.605	0.620	0.635		
	Ry	0.316	0.331	0.346		
	Gx	0.272	0.287	0.302		
	Gy	0.568	0.583	0.598		
	Bx	0.124	0.139	0.154		
	By	0.148	0.163	0.178		

◆ Measurement System

Notes:

1. Contrast Ratio(CR) is defined mathematically as :

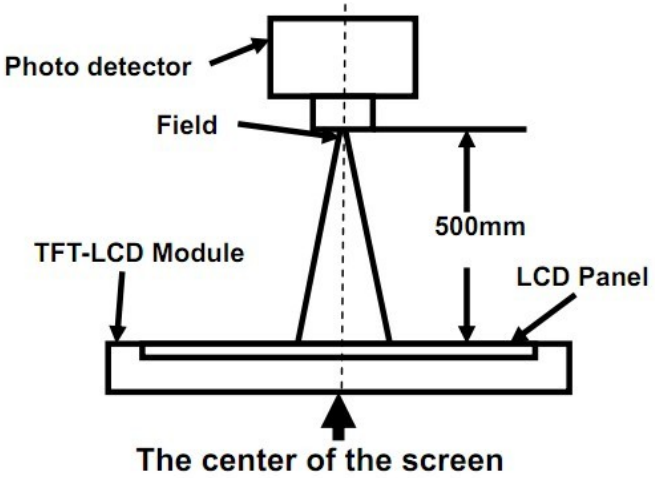
$$\text{Contrast Ratio} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

2. Surface luminance is the center point across the LCD surface 500mm from the surface with all pixels displaying white. For more information see FIG 1.

3. Response time is the time required for the display to transition from white to black (Rising Time, Tr) and from black to white (Falling Time, Tf). For additional information see FIG 2.

4. Viewing angle is the angle at which the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface. For more information see FIG 3.

FIG. 1 Optical Characteristic Measurement Equipment and Method



Item	Photo detector	Field
Contrast Ratio	SR-3A	1°
Luminance		
Chromaticity		
Lum Uniformity		
Response Time	BM-7A	2°

FIG. 2 The definition of Response Time

The response time is defined as the following figure and shall be measured by switching the input signal for “black” and “white”.

Response Time = Rising Time(Tr) + Falling Time(Tf)

- Rising Time(Tr) : Full White 90% → Full White 10% Transmittance.
- Falling Time(Tf) : Full White 10% → Full White 90% Transmittance.

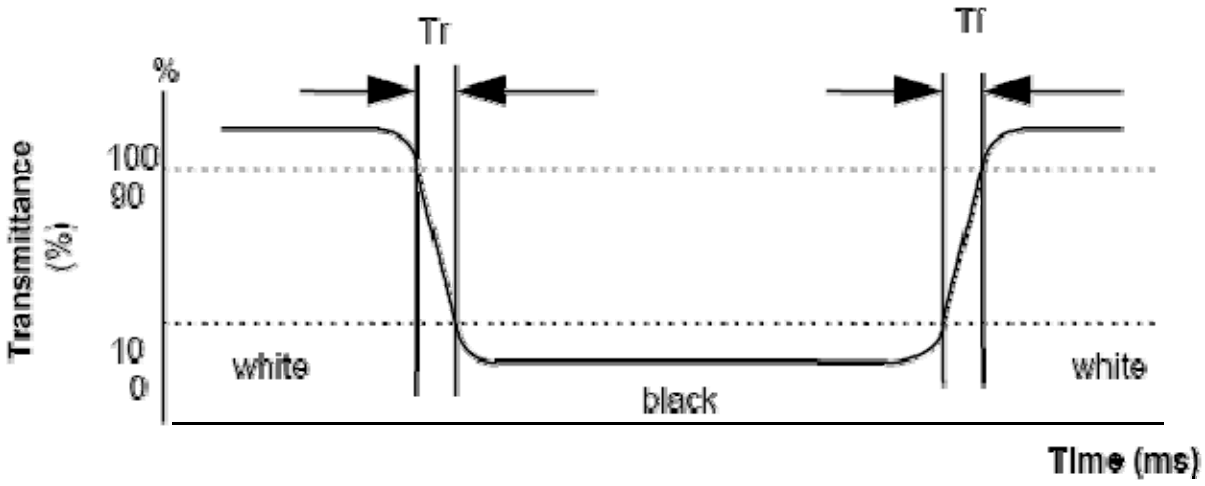
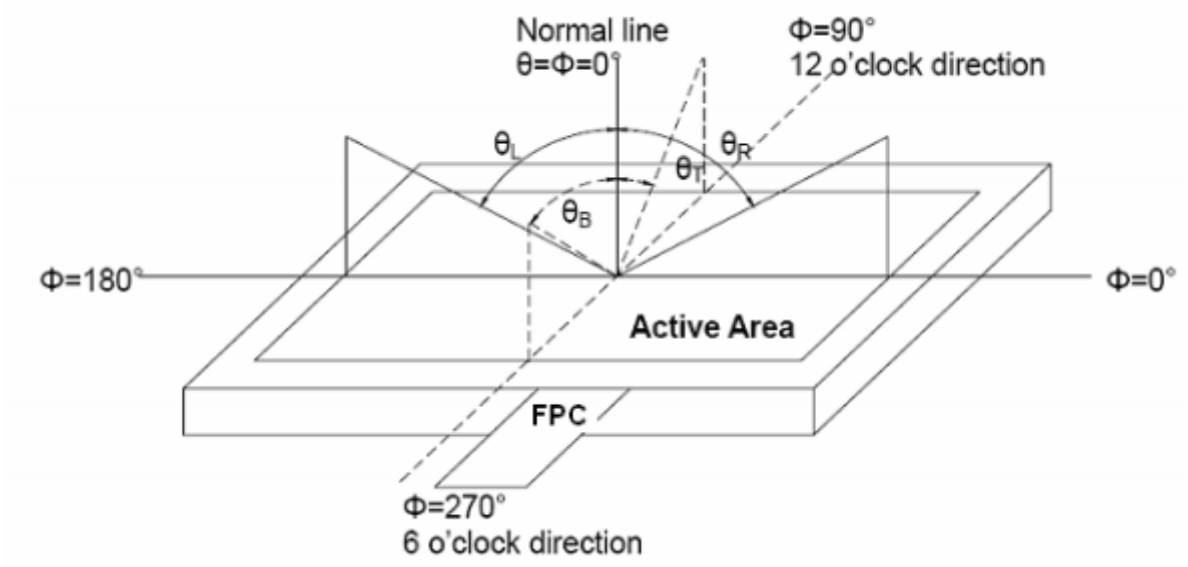
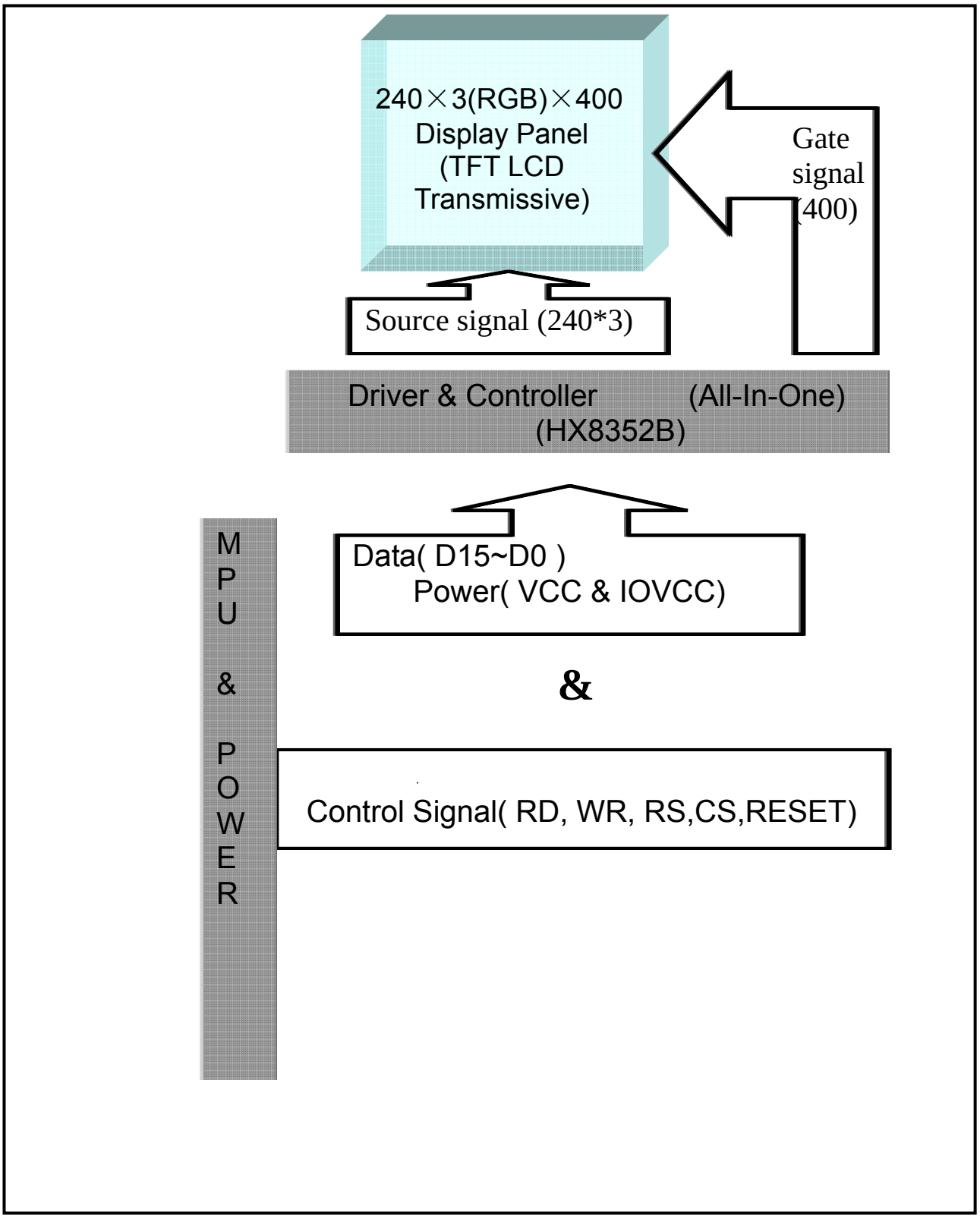


FIG. 3 The definition of Viewing Angle

Use Fig. 1(Test Procedure) under Measurement System to measure the contrast from the measuring direction specified by the conditions as the following figure.



5.Block Diagram



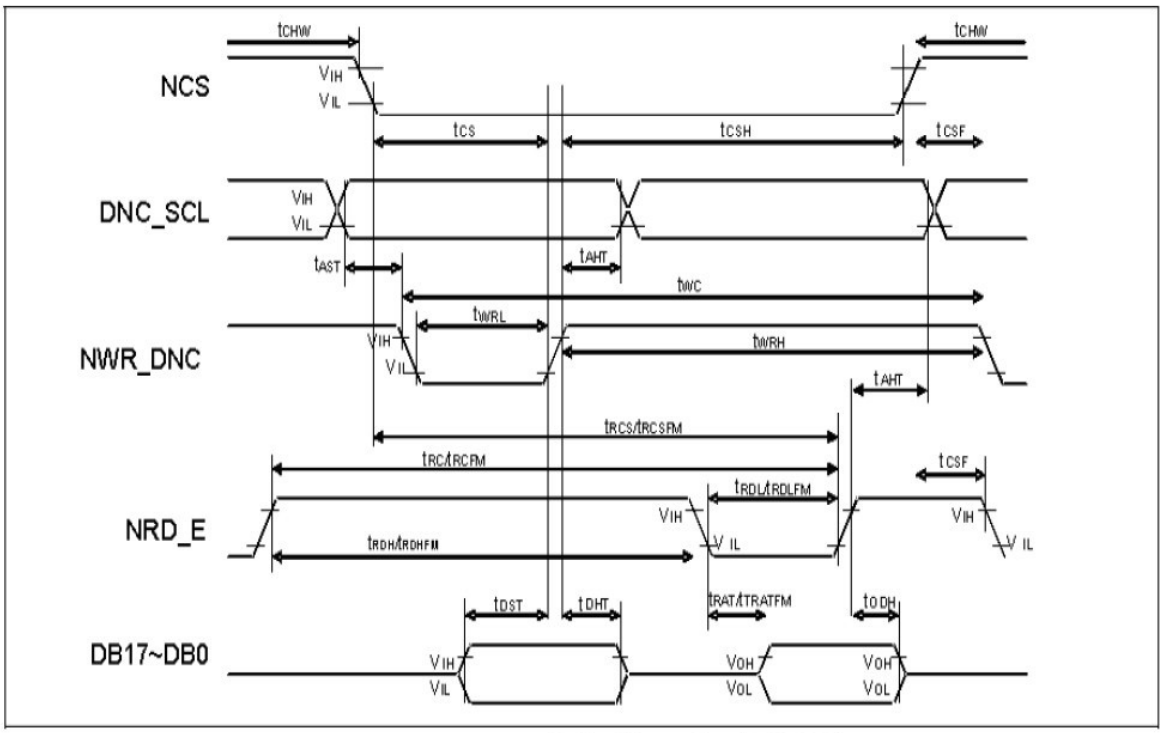
6.Pin Description

Item	Terminal	Functions
1	GND	Ground
2	IM0	8/16 select Pin
3	RESET	RESET PIN; Signal is active when low
4	RS	Register select Signal
5	WR	Write Data Input PIN
6	RD	Read Data Input PIN
7	DB0	DATA input BUS
8	DB1	DATA input BUS
9	DB2	DATA input BUS
10	DB3	DATA input BUS
11	DB4	DATA input BUS
12	DB5	DATA input BUS
13	DB6	DATA input BUS
14	DB7	DATA input BUS
15	DB8	DATA input BUS
16	DB9	DATA input BUS
17	DB10	DATA input BUS
18	DB11	DATA input BUS
19	DB12	DATA input BUS
20	DB13	DATA input BUS
21	DB14	DATA input BUS
22	DB15	DATA input BUS
23	CS	Chip Select Input PIN
24	FMARK	Tearing effect output
25	IOVCC	Power supply for input Pins
26	IC-ID	Connect to VIOCC or GND
27	VCC	Power supply
28	VLED+	B/L Power input PIN anode
29	VLED-	B/L Power input PIN cathode
30	NC	NC
31	GND	Ground

7.Timing Characteristics

7.1. Interface timing chart and Characteristics

Normal Write Mode, IOVCC=1.65V~3.3V, VCC=2.5V~3.3V



(VSSA=0V, IOVCC=1.65V to 3.3V, VCC=2.3V TO 3.3V, VCI=2.3V to 3.3V, T_A = -30 to 70°C)

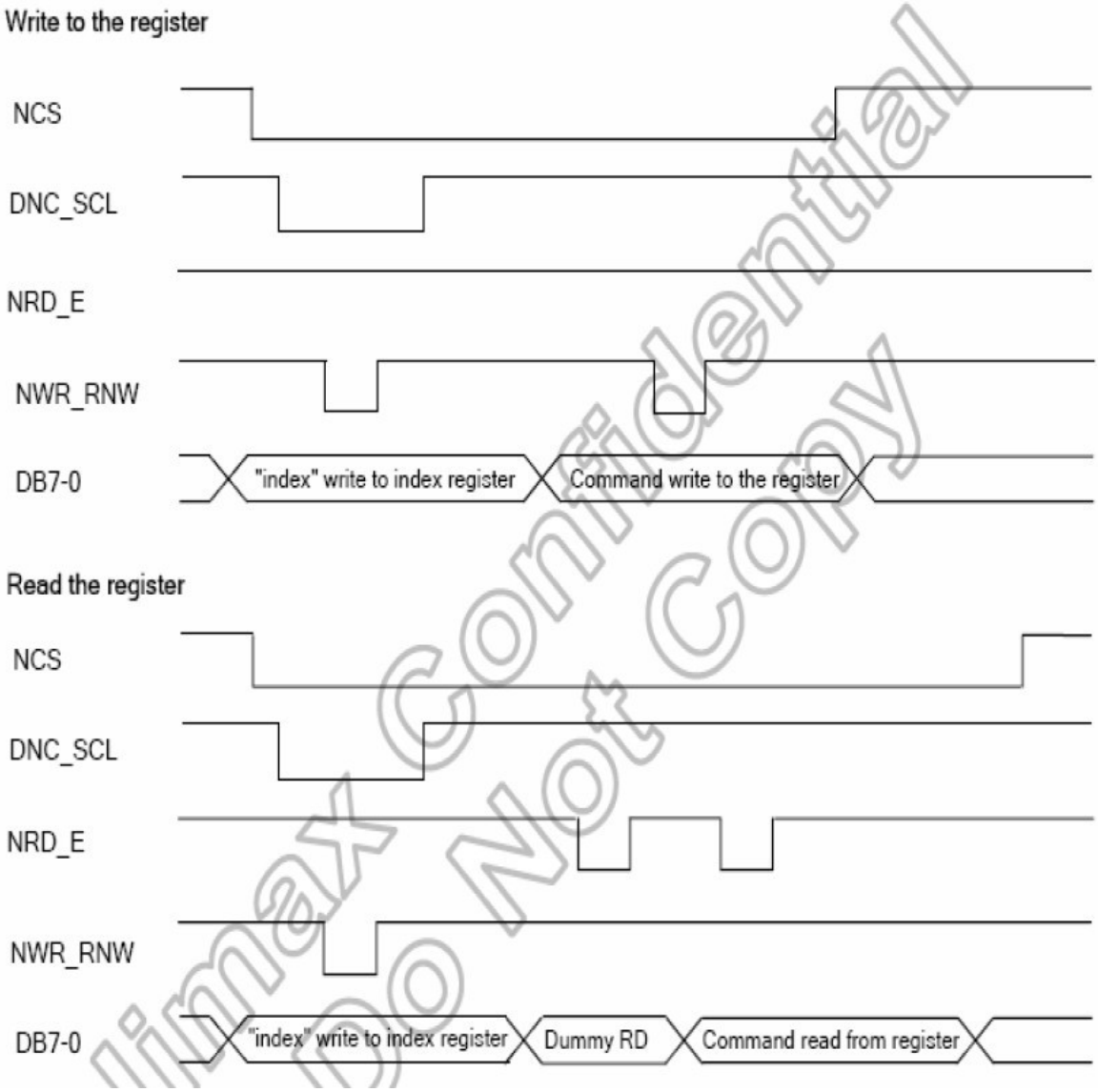
Signal	Symbol	Parameter	Min.	Max.	Unit	Description
DNC_SCL	t_{AST}	Address setup time	10	-	ns	-
	t_{AHT}	Address hold time (Write/Read)	10			
NCS	t_{CHW}	Chip select "H" pulse width	0	-	ns	-
	t_{CS}	Chip select setup time (Write)	35			
	t_{RCS}	Chip select setup time (Read ID)	100			
	t_{RCSFM}	Chip select setup time (Read FM)	100			
	t_{CSF}	Chip select wait time (Write/Read)	10			
	t_{CSH}	Chip select hold time	10			
NWR_RNW	t_{WC}	Write cycle	100	-	ns	-
	t_{WRH}	Control pulse "H" duration	20			
	t_{WRL}	Control pulse "L" duration	20			
NRD_E (ID)	t_{RC}	Read cycle (ID)	150	-	ns	When read ID data
	t_{RDH}	Control pulse "H" duration (ID)	40			
	t_{RDL}	Control pulse "L" duration (ID)	50			
NRD_E (FM)	t_{RCFM}	Read cycle (FM)	250	-	ns	When read from frame memory
	t_{RDHFM}	Control pulse "H" duration (FM)	50			
	t_{RDLFM}	Control pulse "L" duration (FM)	150			
DB17~0	t_{DST}	Data setup time	20	-	ns	For maximum C_L=30pF For minimum C_L=8pF
	t_{DHT}	Data hold time	20	-		
	t_{RAT}	Read access time (ID)	-	70		
	t_{RATFM}	Read access time (FM)	-	100		
	t_{ODH}	Output disable time	20	80		

Note: (1) The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
(2) Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.
(3) When normal operation, VDDD=1.65 ~ 2.0V, HX8352-A can meet above timing.

7.2 Parallel bus system interface

Operations	NWR_RNW	NRD_E	DNC_SCL
Writes Indexes into IR	0	1	0
Writes command into register or data into GRAM	0	1	1
Reads command from register or data from GRAM	1	0	1

Table 5.2 Data pin function for I80 series CPU



Register read/write timing in parallel bus system interface(I80 series MCU)

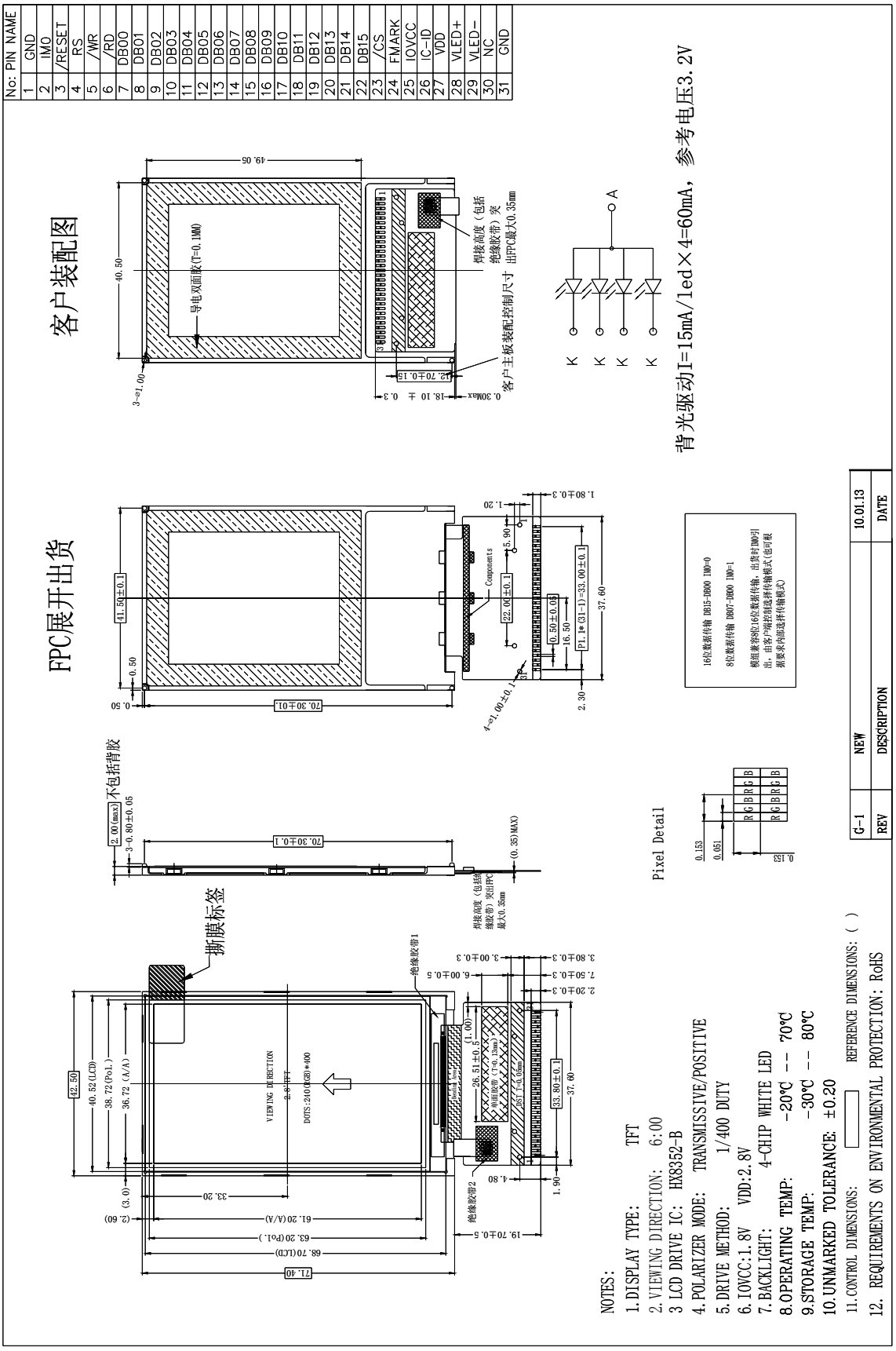
7.3 Instruction description

INSTRUCTION DESCRIPTION(Himax's HX8352-B)

Note: Please refer to Himax's HX8352-B data sheet for more details.

Address	Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
8'h00	Product ID	R	0	1	0	1	0	0	1	0
8'h01	Display mode	R/W	0	0	0	0	IDMON(0)	INVON (0)	NORON(1)	PTLON(0)
8'h02	Column Address Start(1)	R/W	SC[15:8] (8'b0)							
8'h03	Column Address Start(2)	R/W	SC[7:0] (8'b0)							
8'h04	Column Address End(1)	R/W	EC[15:8] (8'b0000_0000)							
8'h05	Column Address End(2)	R/W	EC[7:0] (8'b1110_1111)							
8'h06	Row Address Start(1)	R/W	SP[15:8] (8'b0)							
8'h07	Row Address Start(2)	R/W	SP[7:0] (8'b0)							
8'h08	Row Address End(1)	R/W	EP[15:8] (8'b0000_0001)							
8'h09	Row Address End(2)	R/W	EP[7:0] (8'b1010_1111)							
8'h0a	Partial Area Start Row(1)	R/W	PSL[15:8] (8'b0)							
8'h0b	Partial Area Start Row(2)	R/W	PSL[7:0] (8'b0)							
8'h0c	Partial Area End Row(1)	R/W	PEL[15:8] (8'b0000_0001)							
8'h0d	Partial Area End Row(2)	R/W	PEL[7:0] (8'b1010_1111)							
8'h0e	Vertical Scroll Top Fixed Area(1)	R/W	TFA[15:8] (8'b0)							
8'h0f	Vertical Scroll Top Fixed Area(2)	R/W	TFA[7:0] (8'b0)							
8'h10	Vertical Scroll Height Area(1)	R/W	VSA[15:8] (8'b0000_0001)							
8'h11	Vertical Scroll Height Area(2)	R/W	VSA[7:0] (8'b1011_0000)							
8'h12	Vertical Scroll Button Fixed(1)	R/W	BFA[15:8] (8'b0)							
8'h13	Vertical Scroll Button Fixed(2)	R/W	BFA[7:0] (8'b0)							
8'h14	Vertical Scroll Start Address(1)	R/W	VSP[15:8] (8b'0)							
8'h15	Vertical Scroll Start Address(2)	R/W	VSP[7:0] (8b'0)							
8'h16	Memory Access Control	R/W	MY(0)	MX(0)	MV(0)	GS(0)	BGR(0)	SS(0)	SRL_EN[0]	SM[0]
8'h17	OSC Control 1	R/W	RADJ[3:0](1111)							OSC_EN[0]
8'h18	OSC Control 2	R/W	0	UADJ[2:0](011)			CADJ[3:0](1000)			
8'h19	Power Control 1	R/W	GASENB(0)	0	0	PON (0)	DK (1)	XDK[0]	VL_TRI[0]	STB[1]
8'h1a	Power Control 2	R/W	0	VC3[2:0] (000)			0	VC1[2:0] (101)		
8'h1b	Power Control 3	R/W	BT[3:0] (0100)				0	AP[2:0] (000)		
8'h1c	Power Control 4	R/W	0	0	0	0	VRH[3:0] (1101)			
8'h1d	Power Control 5	R/W	0	0	0	BGP[3:0] (1000)				
8'h1e	Power Control 6	R/W	0	0	VCOMG (0)	VDV[4:0] (1_0000)				
8'h1f	VCOM Control	R/W	0	VCM[6:0](101_0101)						
8'h22	Data read/write	R/W	SRAM Write							
8'h23	Display Control 1	R/W	0	0	0	0	0	0	TEMODE(0)	TEON(0)
8'h24	Display Control 2	R/W	PT[1:0] (10)		GON (1)	DTE (0)	D[1:0] (00)		0	0
8'h25	Display Control 3	R/W	N_FP[7:0] (8'h02)							
8'h26	Display Control 4	R/W	P_FP[7:0] (8'h02)							
8'h27	Display Control 5	R/W	I_FP[7:0] (8'h02)							
8'h28	Display Control 6	R/W	N_BP[7:0] (8'h02)							
8'h29	Display Control 7	R/W	P_BP[7:0] (8'h02)							
8'h2a	Display Control 8	R/W	I_BP[7:0] (8'h02)							
8'h2b	Cycle Control 1	R/W	N_DC[7:0] (1011_1110)							
8'h2c	Cycle Control 2	R/W	P_DC[7:0] (1011_1110)							
8'h2d	Cycle Control 3	R/W	I_DC[7:0] (1011_1110)							
8'h2e	Cycle Control 4	R/W	FS1[1:0] (01)		FS0[1:0] (00)		I_RTN[3:0] (1000)			
8'h2f	Cycle Control 5	R/W	PI_RTN[3:0] (0000)				N_RTN[3:0] (0000)			
8'h30	Cycle Control 6	R/W	0	0	DIV_I[1:0](00)		0	0	0	I_NW(0)
8'h31	Cycle Control 7	R/W	0	0	DIV_N[1:0](00)		0	0	0	N_NW(1)
8'h32	Cycle Control 8	R/W	0	0	DIV_P[1:0](00)		0	0	0	P_NW(1)
8'h34	Cycle Control 10	R/W	EQS[7:0](0011_1000)							
8'h35	Cycle Control 11	R/W	EQP[7:0](0011_1000)							
8'h36	Cycle Control 12	R/W			PTG[1:0](10)		ISC[3:0] (0001)			
8'h37	Cycle Control 13	R/W	SON[7:0](8'b0011_1000)							
8'h38	Cycle Control 14	R/W	GDON[7:0] (8'b0000_0100)							
8'h39	Cycle Control 15	R/W	GDOF[7:0] (8'b1111_0110)							
8'h3a	Interface Control 1	R/W	CSEL[2:0](110)			0	DPL (0)	HSPL (0)	VSPL (0)	EPL (0)
8'h3c	Source Control 1	R/W	N_SAP[7:0](1100_0000)							

8.Outline Drawing



9. Reliability and Inspection Standard

No.	Test Item		Test Conditions	Remark
1	High Temperature	Storage	80℃, 120Hr	Note
		Operation	70℃, 120Hr	Note
2	Low Temperature	Storage	-30℃, 120Hr	Note
		Operation	-20℃, 120Hr	
3	High Temperature and High Humidity		60℃, 90%RH, 240Hr	Note
4	Peeling Off (Storage)		≧500gf/cm	Note
5	FPC Bending Test		≧6,000 times, 2/sec	Note
6	Vibration Test(Storage)		50HZ, 30min, Amplitude: 2 cm, X/Y/Z directions	Note
7	Drop Test		60cm/ 3Corner/ 8Face, 1Cycle	Note

Note:

1) The test samples should be applied to only one test item.
2) Sample size for each test item is 5~10pcs.
3) For Damp Proof Test, pure water(Resistance>1MΩ) should be used.
4) In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.
5) EL evaluation should be excepted from reliability test with humidity and temperature: Some defects such as black spot/blemish can happen by natural chemical reaction with humidity and fluorescence EL has.
6) After the reliability test, the test samples should be inspected after 2 hours at least.
7) Functional test is OK. Missing segment, shorts, unclear segment, non display, display abnormally, liquid crystal leak are not allowed.
8) After testing, the current Idd should be within initial value ±20%.
9) No low temperature bubbles ,end seal loose and fall, frame rainbow, ACF bubble growing are allowable in the appearance test.

10.PRECAUTIONS FOR USING LCD MODULES

Handing Precautions

(1) The display panel is made of glass and polarizer. As glass is fragile, it tends to become or chipped during handling especially on the edges. Please avoid dropping or jarring. Do not subject it to a mechanical shock by dropping it or impact.
(2) If the display panel is damaged and the liquid crystal substance leaks out, be sure not to get any in your mouth. If the substance contacts your skin or clothes, wash it off using soap and water.
(3) Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary. Do not touch the display with bare hands. This will stain the display area and degraded insulation between terminals (some cosmetics are determined to the polarizer).
(4) The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully. Do not touch, push or rub the exposed polarizers with anything harder than an HB pencil lead (glass, tweezers, etc.). Do not put or attach anything on the display area to avoid leaving marks on. Condensation on the surface and contact with terminals due to cold will damage, stain or dirty the polarizer. After products are tested at low temperature they must be warmed up in a container before coming is contacting with room temperature air.
(5) If the display surface becomes contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If it is heavily contaminated, moisten cloth with one of the following solvents
- Isopropyl alcohol
- Ethyl alcohol
Do not scrub hard to avoid damaging the display surface.
(6) Solvents other than those above-mentioned may damage the polarizer. Especially, do not use the following.
- Water
- Ketone
- Aromatic solvents
Wipe off saliva or water drops immediately, contact with water over a long period of time may cause deformation or color fading. Avoid contacting oil and fats.
(7) Exercise care to minimize corrosion of the electrode. Corrosion of the electrodes is accelerated by water droplets, moisture condensation or a current flow in a high-humidity environment.
(8) Install the LCD Module by using the mounting holes. When mounting the LCD module make sure it is free of twisting, warping and distortion. In particular, do not forcibly pull or bend the I/O cable or the backlight cable.
(9) Do not attempt to disassemble or process the LCD module.
(10) NC terminal should be open. Do not connect anything.
(11) If the logic circuit power is off, do not apply the input signals.
(12) Since LCM has been assembled and adjusted with a high degree of precision, avoid applying excessive shocks to the module or making any alterations or modifications to it.
- Do not alter, modify or change the shape of the tab on the metal frame.
- Do not make extra holes on the printed circuit board, modify its shape or change the positions of components to be attached.
- Do not damage or modify the pattern writing on the printed circuit board.
- Absolutely do not modify the zebra rubber strip (conductive rubber) or heat seal

connector.
- Except for soldering the interface, do not make any alterations or modifications with a soldering iron.
- Do not drop, bend or twist LCM.

Storage Precautions

When storing the LCD modules, the following precaution is necessary.
(1) Store them in a sealed polyethylene bag. If properly sealed, there is no need for the dessicant.
(2) Store them in a dark place. Do not expose to sunlight or fluorescent light, keep the temperature between 0°C and 35°C.
(3) The polarizer surface should not come in contact with any other objects. (We advise you to store them in the container in which they were shipped).

Others

Liquid crystals solidify under low temperature (below the storage temperature range) leading to defective orientation or the generation of air bubbles (black or white). Air bubbles may also be generated if the module is subject to a low temperature.
If the LCD modules have been operating for a long time showing the same display patterns, the display patterns may remain on the screen as ghost images and a slight contrast irregularity may also appear. A normal operating status can be regained by suspending use for some time. It should be noted that this phenomenon does not adversely affect performance reliability.
To minimize the performance degradation of the LCD modules resulting from destruction caused by static electricity etc., exercise care to avoid holding the following sections when handling the modules.
- Exposed area of the printed circuit board.
-Terminal electrode sections.