

RJM0404JSC

Silicon N/P Channel Power MOS FET (6 in 1 Type)
High Speed Power Switching

R07DS0338EJ0500

Rev.5.00

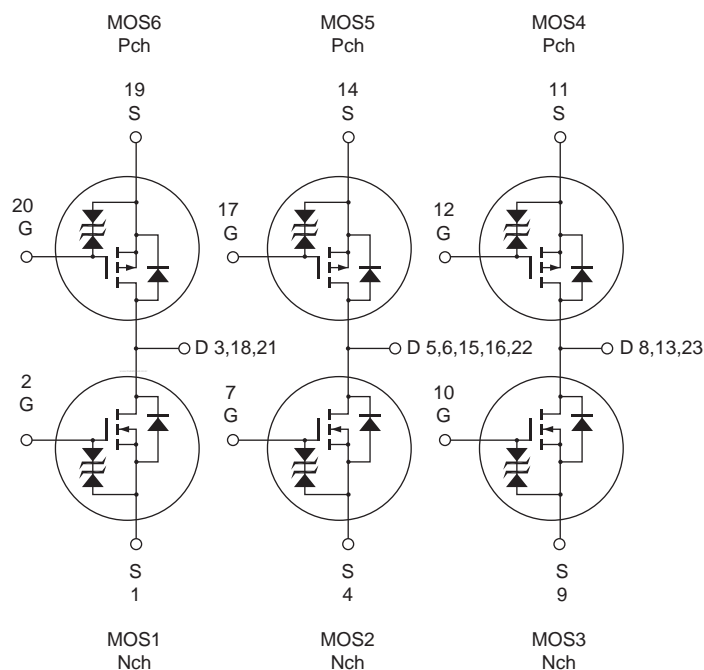
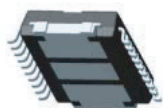
May 11, 2011

Features

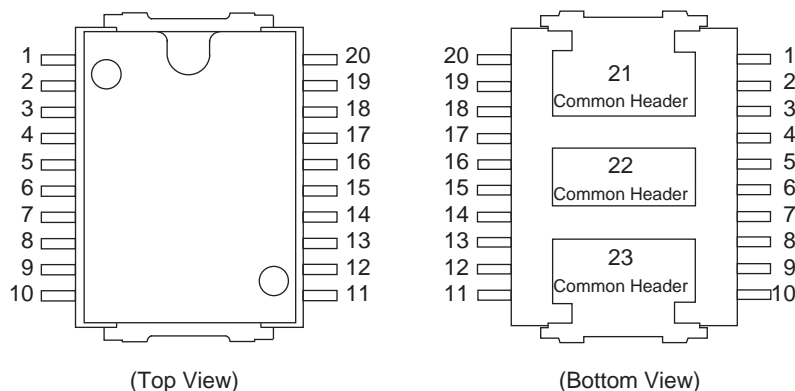
- For Automotive applications
- AEC-Q101 compliant
- N/P Channel MOS FET (6 in 1 Type). High density mounting
- Low on-resistance
- Capable of 4.5 V gate drive

Outline

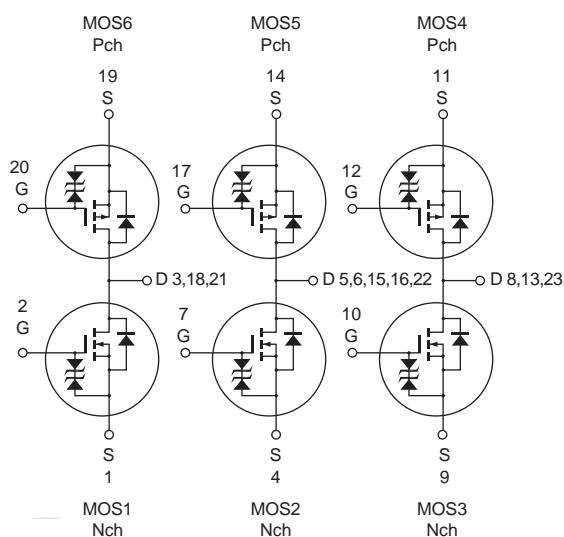
RENESAS Package Code: PRSP0020DF-A
(Package Name: HSOP-20)



Pin Arrangement



No.		
1	MOS1	Source
2	MOS1	Gate
3, 18	MOS1, 6	Drain
4	MOS2	Source
5, 6, 15, 16	MOS2, 5	Drain
7	MOS2	Gate
8, 13	MOS3, 4	Drain
9	MOS3	Source
10	MOS3	Gate
11	MOS4	Source
12	MOS4	Gate
14	MOS5	Source
17	MOS5	Gate
19	MOS6	Source
20	MOS6	Gate
21	MOS1, 6	Drain (Header)
22	MOS2, 5	Drain (Header)
23	MOS3, 4	Drain (Header)



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Value		Unit
		MOS1, 2, 3 (Nch)	MOS4, 5, 6 (Pch)	
Drain to source voltage	V_{DSS}	40	-40	V
Gate to source voltage	V_{GSS}	+20 / -5	-20 / +5	V
Drain current	I_D	20	-20	A
Drain peak current	$I_{D(pulse)}$ ^{Note1}	80	-80	A
Avalanche current	I_{AP} ^{Note3}	20	-20	A
Avalanche energy	E_{AR} ^{Note3}	53	53	mJ
Channel dissipation	P_{ch} ^{Note2}	54	54	W
Channel temperature	T_{ch} ^{Note4}	175	175	°C
Storage temperature	T_{stg}	-55 to +150	-55 to +150	°C

- Notes: 1. $PW \leq 10\mu s$ duty cycle $\leq 1\%$
 2. $T_c = 25^\circ C$: 1 Drive Operation.
 3. $T_{ch} = 25^\circ C$, $R_g \geq 50 \Omega$
 4. AEC-Q101 compliant

Thermal Impedance Characteristics

- Channel to case thermal impedance θ_{ch-c} : 2.78°C/W

Electrical Characteristics

• MOS1, MOS2, MOS3 (N Channel)

(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Zero gate voltage drain current	I_{DSS}	—	—	10	μA	$V_{DS} = 40 V, V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = +20 / -5 V, V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.5	V	$V_{DS} = 10 V, I_D = 1 mA$
Static drain to source on state resistance	$R_{DS(on)}$	—	17	21	$m\Omega$	$I_D = 10 A, V_{GS} = 10 V$ ^{Note5}
		—	24	34	$m\Omega$	$I_D = 10 A, V_{GS} = 4.5 V$ ^{Note5}
Input capacitance	C_{iss}	—	1400	—	pF	$V_{DS} = 10V, V_{GS} = 0,$ $f = 1 MHz$
Output capacitance	C_{oss}	—	230	—	pF	
Reverse transfer capacitance	C_{rss}	—	100	—	pF	
Total gate charge	Q_g	—	23	—	nC	$V_{DD} = 25 V, V_{GS} = 10 V,$ $I_D = 20 A$
Gate to source charge	Q_{gs}	—	3	—	nC	
Gate to drain charge	Q_{gd}	—	4	—	nC	
Turn-on delay time	$t_{d(on)}$	—	15	—	ns	$V_{GS} = 10 V, I_D = 10 A,$ $V_{DD} \cong 20 V, R_L = 2 \Omega,$ $R_G = 4.7 \Omega$
Rise time	t_r	—	35	—	ns	
Turn-off delay time	$t_{d(off)}$	—	50	—	ns	
Fall time	t_f	—	8	—	ns	
Body-drain diode forward voltage	V_{DF}	—	0.92	1.2	V	$I_F = 20 A, V_{GS} = 0$ ^{Note5}
Body-drain diode reverse recovery time	t_{rr}	—	20	—	ns	$I_F = 20 A, V_{GS} = 0$ $di_F/dt = 50 A/\mu s$

Note: 5. Pulse test

• MOS4, MOS5, MOS6 (P Channel)

(Ta = 25°C)

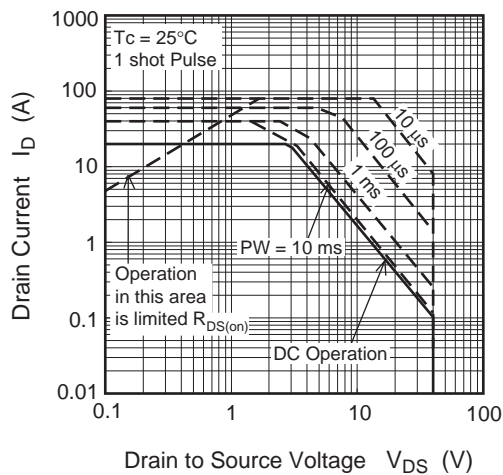
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Zero gate voltage drain current	I_{DSS}	—	—	-10	μA	$V_{DS} = -40 V, V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = -20 / +5 V, V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-1.0	—	-2.5	V	$V_{DS} = -10 V, I_D = -1 mA$
Static drain to source on state resistance	$R_{DS(on)}$	—	34	42	$m\Omega$	$I_D = -10 A, V_{GS} = -10 V$ ^{Note6}
		—	48	68	$m\Omega$	$I_D = -10 A, V_{GS} = -4.5 V$ ^{Note6}
Input capacitance	C_{iss}	—	1500	—	pF	$V_{DS} = -10 V, V_{GS} = 0,$ $f = 1 MHz$
Output capacitance	C_{oss}	—	230	—	pF	
Reverse transfer capacitance	C_{rss}	—	140	—	pF	
Total gate charge	Q_g	—	25	—	nC	$V_{DD} = -25 V, V_{GS} = -10 V,$ $I_D = -20 A$
Gate to source charge	Q_{gs}	—	5	—	nC	
Gate to drain charge	Q_{gd}	—	4	—	nC	
Turn-on delay time	$t_{d(on)}$	—	30	—	ns	$V_{GS} = -10 V, I_D = -10 A,$ $V_{DD} \cong -20 V, R_L = 2 \Omega,$ $R_G = 4.7 \Omega$
Rise time	t_r	—	55	—	ns	
Turn-off delay time	$t_{d(off)}$	—	50	—	ns	
Fall time	t_f	—	20	—	ns	
Body-drain diode forward voltage	V_{DF}	—	-0.97	-1.26	V	$I_F = -20 A, V_{GS} = 0$ ^{Note6}
Body-drain diode reverse recovery time	t_{rr}	—	30	—	ns	$I_F = -20 A, V_{GS} = 0$ $di_F/dt = 50 A/\mu s$

Note: 6. Pulse test

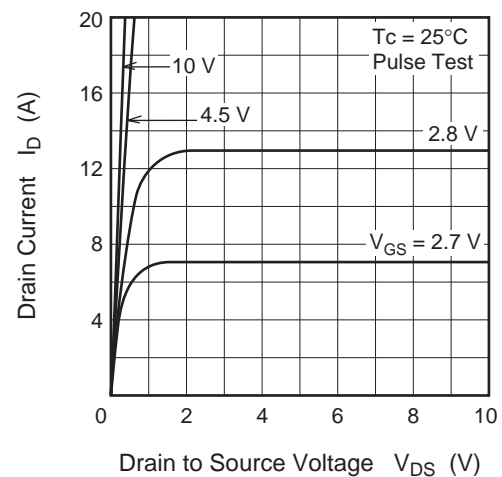
Main Characteristics

• MOS1, 2, 3 (Nch)

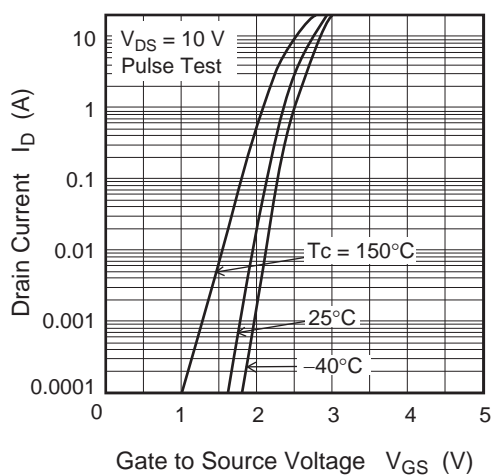
Maximum Safe Operation Area



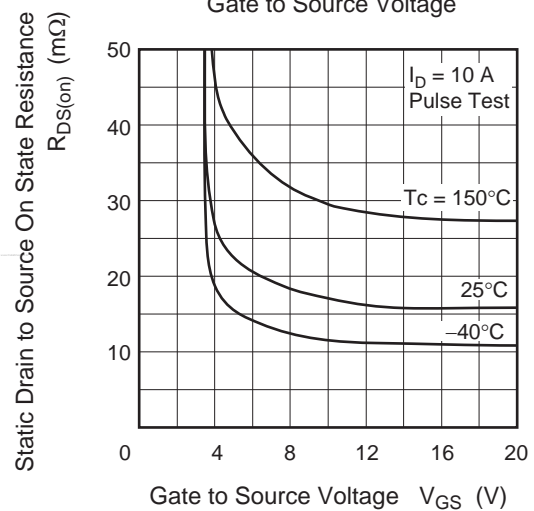
Typical Output Characteristics



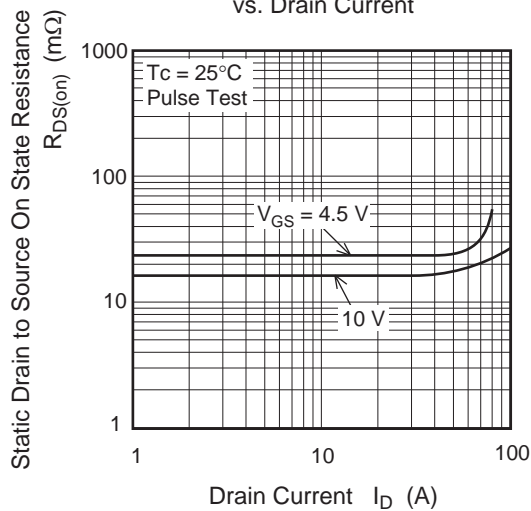
Typical Transfer Characteristics



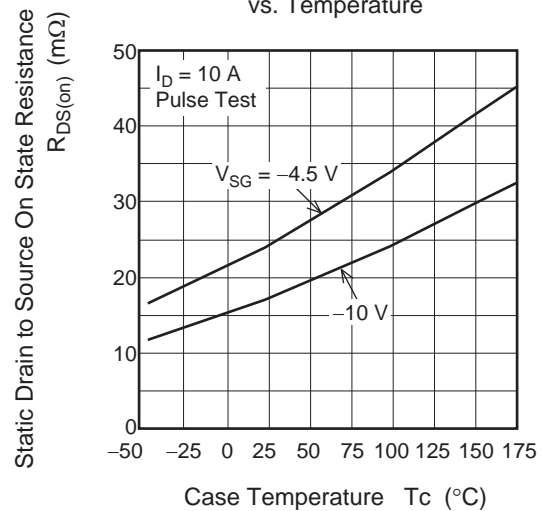
Static Drain to Source On State Resistance vs. Gate to Source Voltage



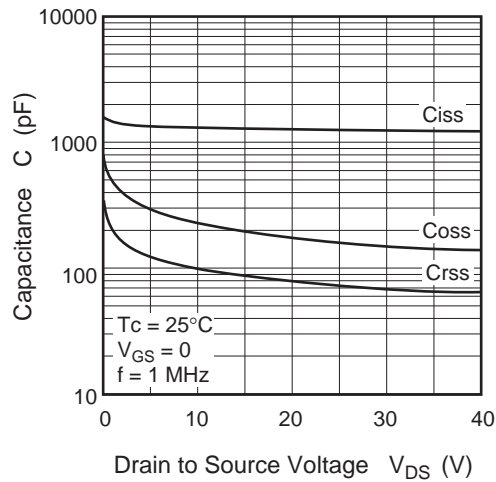
Static Drain to Source On State Resistance vs. Drain Current



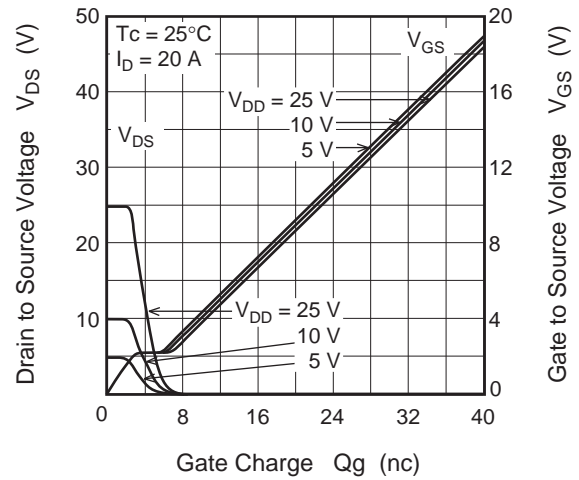
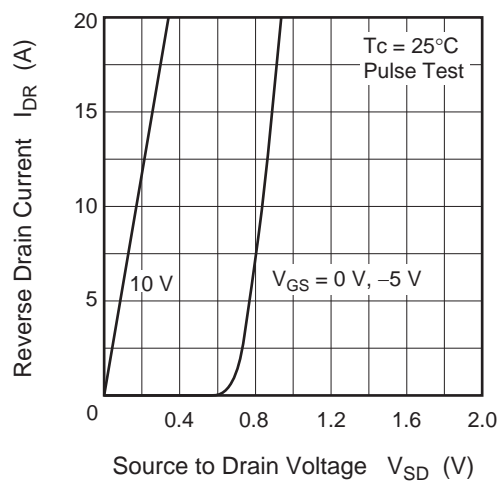
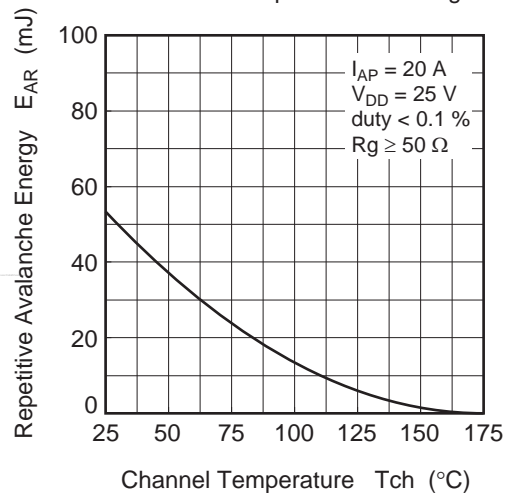
Static Drain to Source on State Resistance vs. Temperature



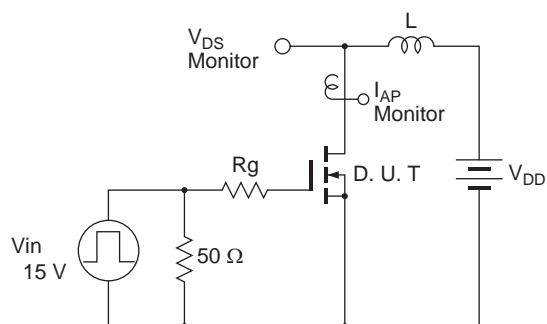
• MOS1, 2, 3(Nch)

Typical Capacitance vs.
Drain to Source Voltage

Dynamic Input Characteristics

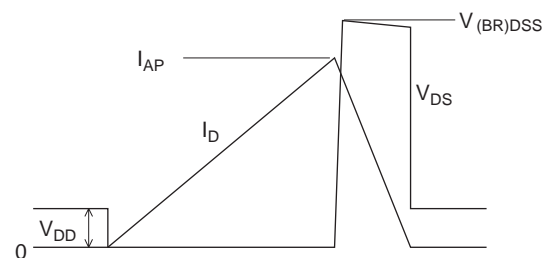
Reverse Drain Current vs.
Source to Drain VoltageAvalanche Energy vs.
Channel Temperature Derating

Avalanche Test Circuit

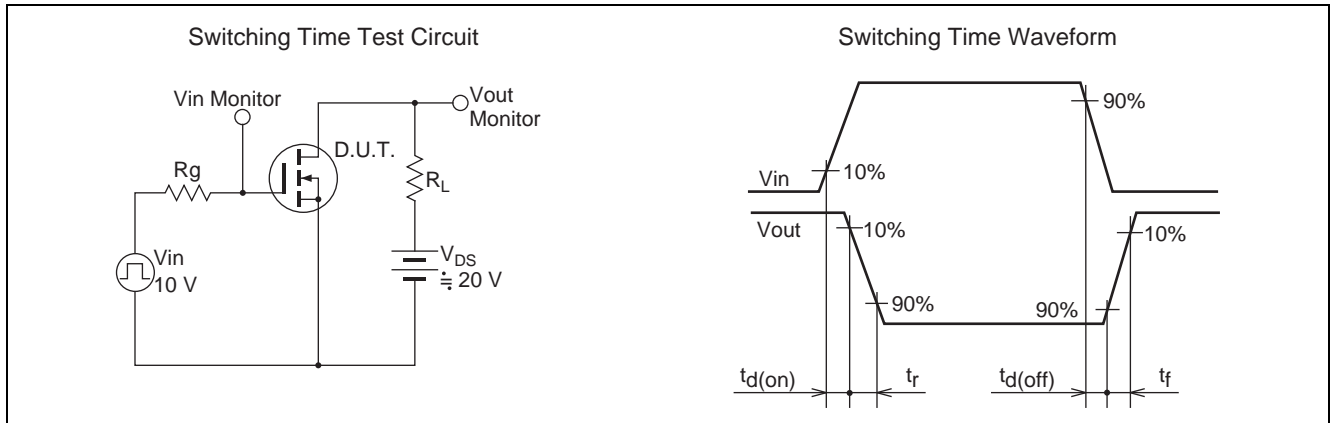


Avalanche Waveform

$$E_{AR} = \frac{1}{2} L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$

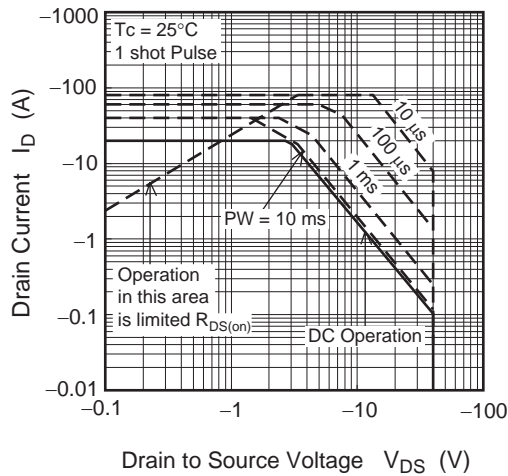


• MOS1, 2, 3 (Nch)

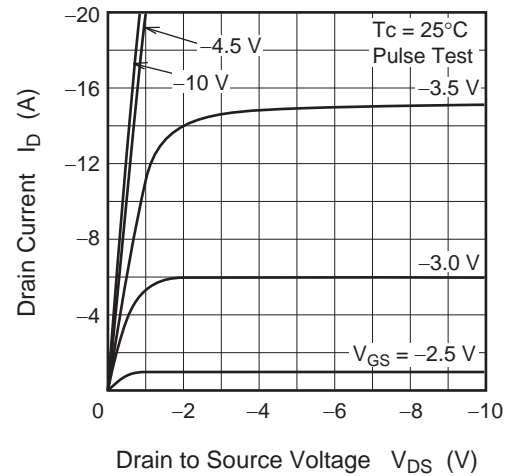


• MOS4, 5, 6 (Pch)

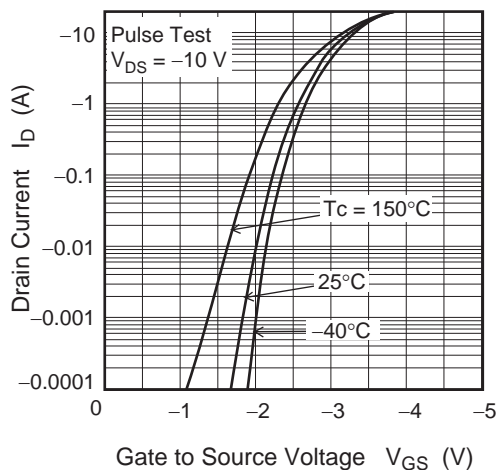
Maximum Safe Operation Area



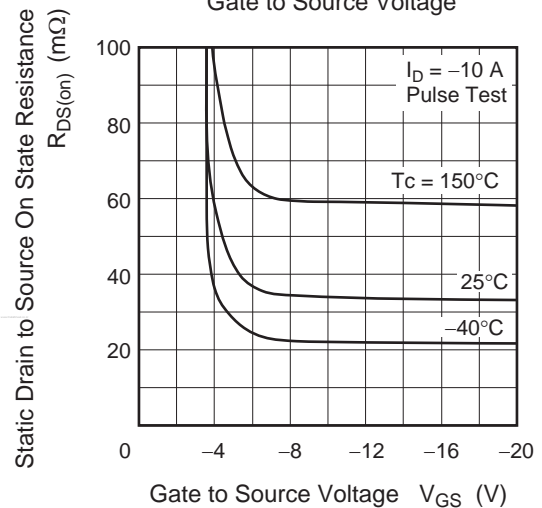
Typical Output Characteristics



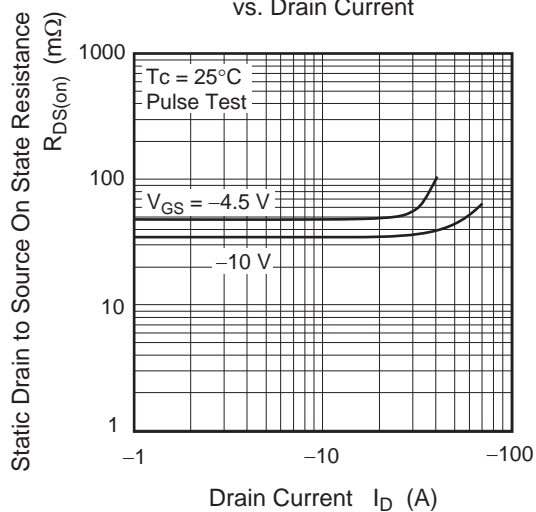
Typical Transfer Characteristics



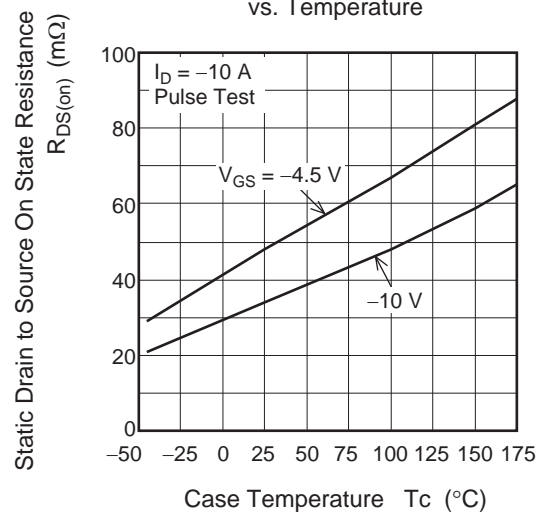
Static Drain to Source On State Resistance vs. Gate to Source Voltage



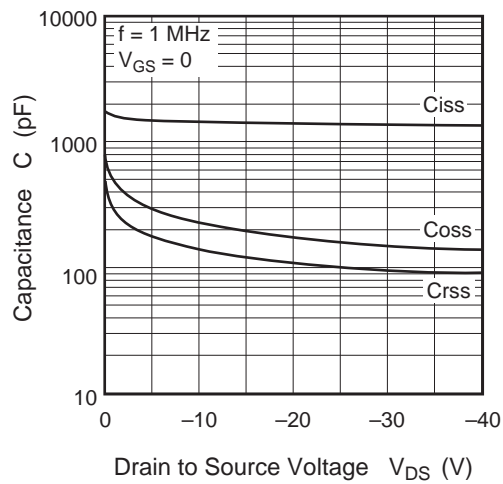
Static Drain to Source On State Resistance vs. Drain Current



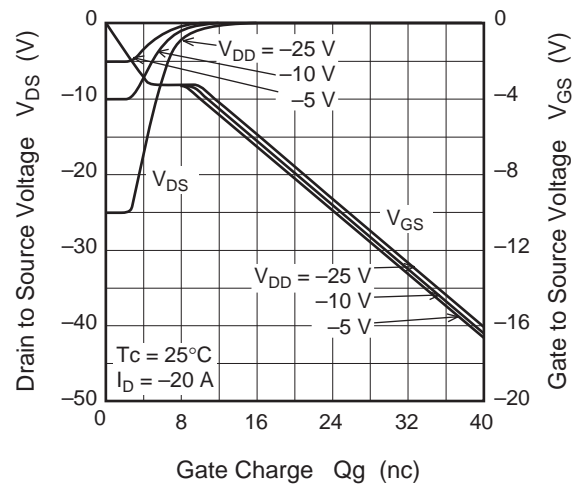
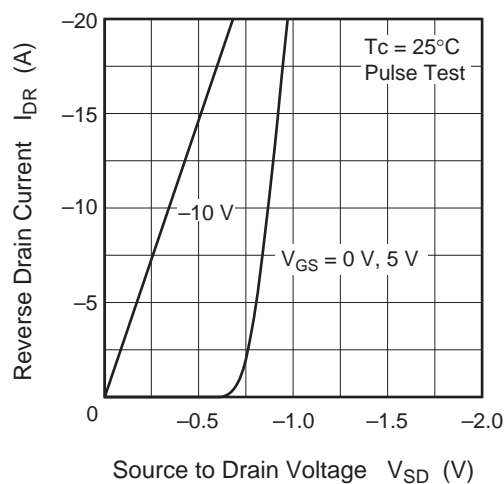
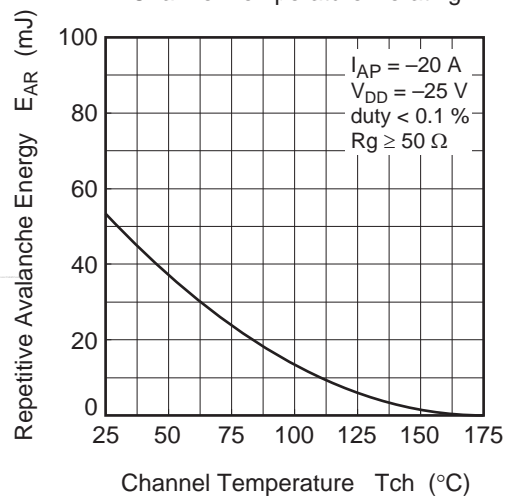
Static Drain to Source on State Resistance vs. Temperature



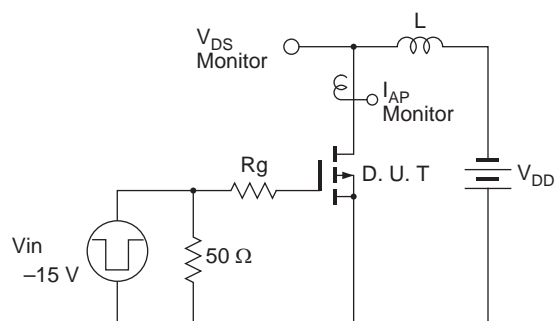
• MOS4, 5, 6 (Pch)

Typical Capacitance vs.
Drain to Source Voltage

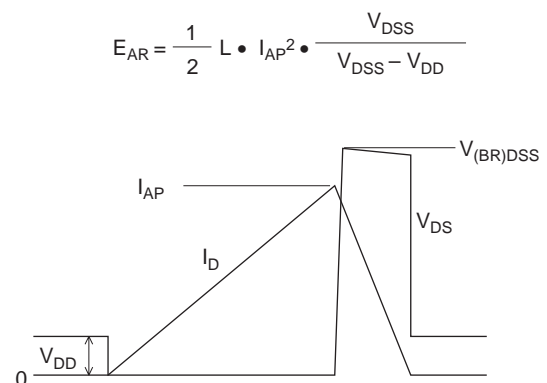
Dynamic Input Characteristics

Reverse Drain Current vs.
Source to Drain VoltageAvalanche Energy vs.
Channel Temperature Derating

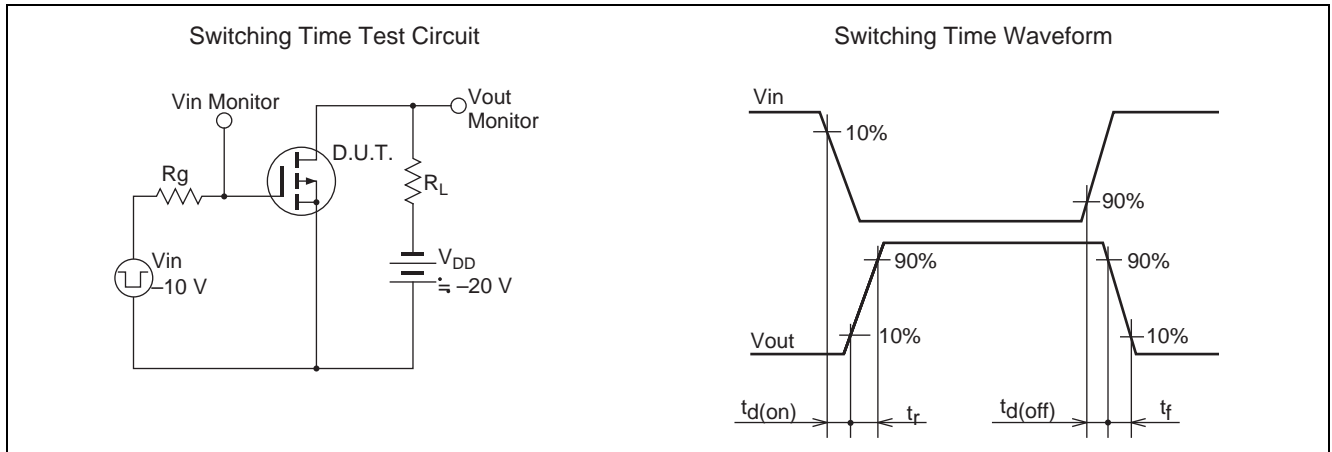
Avalanche Test Circuit



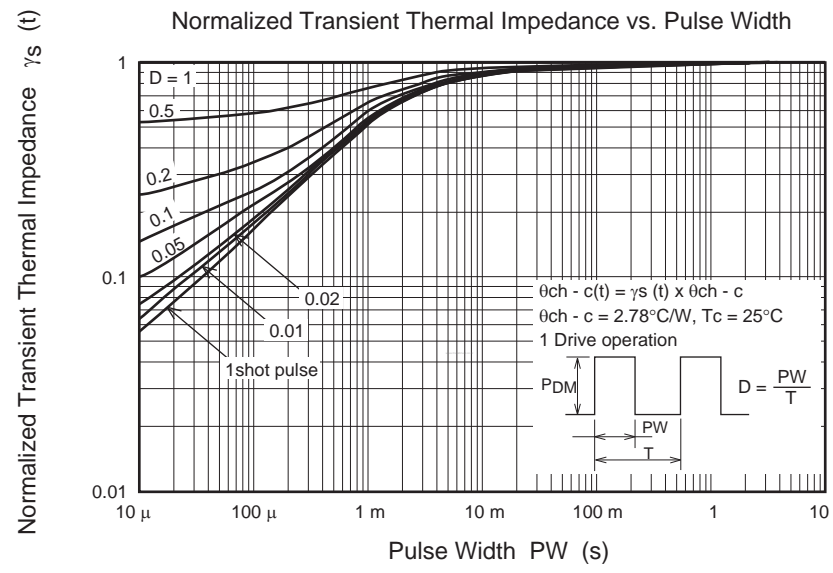
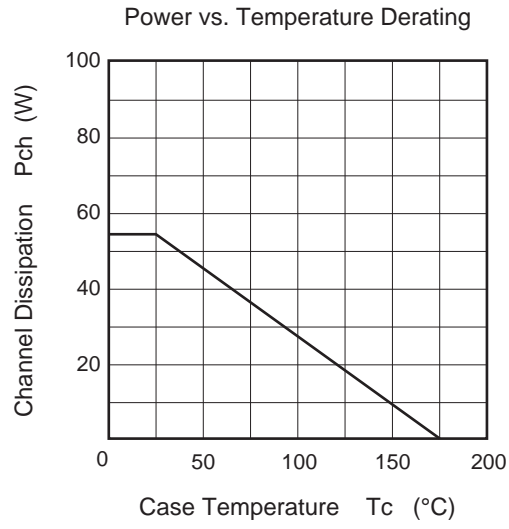
Avalanche Waveform



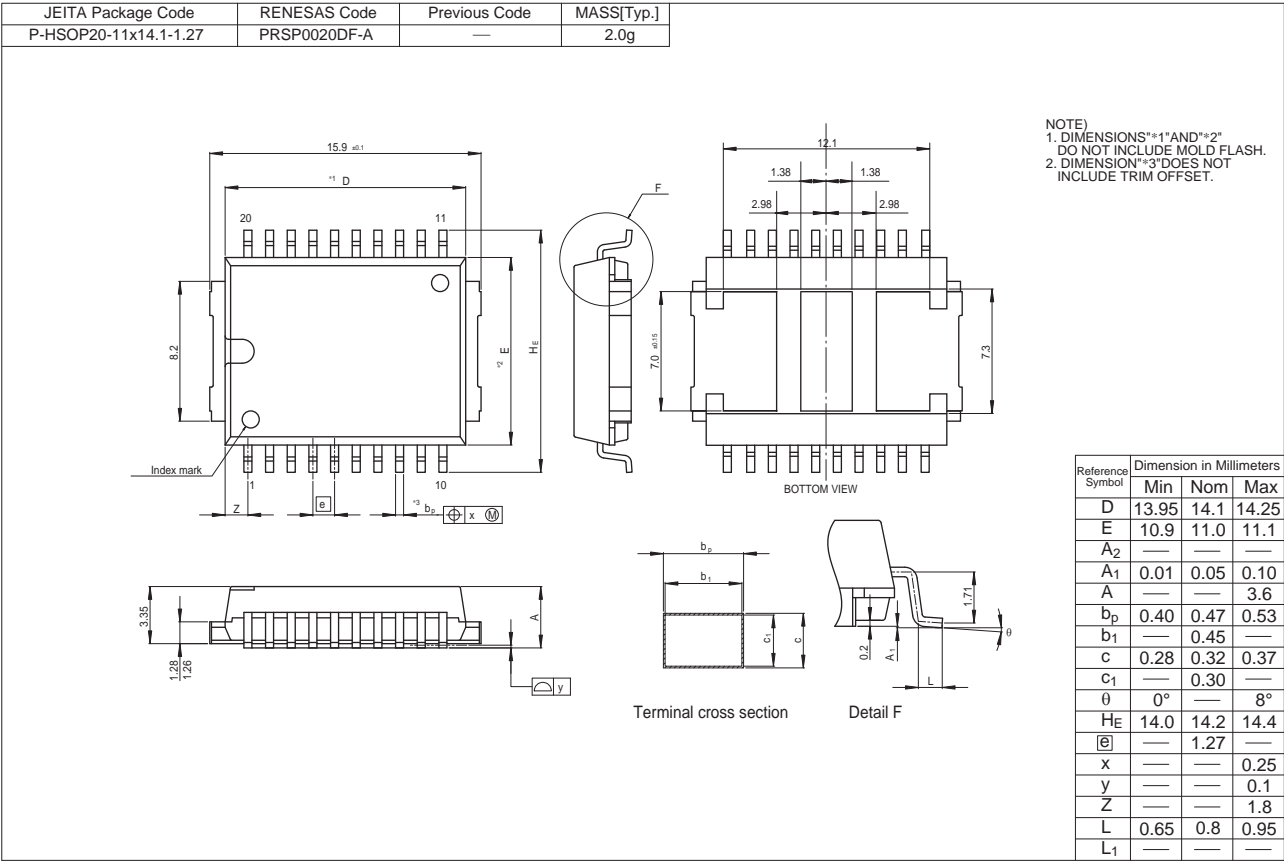
• MOS4, 5, 6 (Pch)



• Common



Package Dimensions



Ordering Information

Orderable Part Number	Quantity	Shipping Container
RJM0404JSC-00-12	700 pcs	Tray

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