

RJK5032DPD

500V - 3A - MOS FET
High Speed Power Switching

R07DS0836EJ0200

Rev.2.00

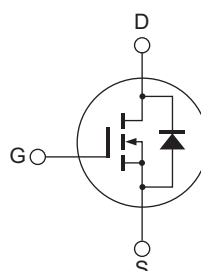
Aug 08, 2012

Features

- Low on-state resistance
 $R_{DS(on)} = 2.1 \Omega$ typ. (at $I_D = 1.5 A$, $V_{GS} = 10 V$, $T_a = 25^\circ C$)
- Low drive current
- High speed switching

Outline

RENESAS Package code: PRSS0004ZG-A
(Package name : MP-3A)



1. Gate
2. Drain
3. Source
4. Drain

Absolute Maximum Ratings

($T_a = 25^\circ C$)

Item	Symbol	Value	Unit
Drain to source voltage	V_{DSS}	500	V
Gate to source voltage	V_{GSS}	± 30	V
Drain current	I_D	3	A
Drain peak current	$I_{D(pulse)}$ ^{Note1}	6	A
Body-drain diode reverse drain current	I_{DR}	3	A
Body-drain diode reverse drain peak current	$I_{DR(pulse)}$ ^{Note1}	6	A
Avalanche current	I_{AP} ^{Note2}	3	A
Avalanche energy	E_{AR} ^{Note2}	0.5	mJ
Channel dissipation	P_{ch} ^{Note3}	40.3	W
Channel to case thermal Impedance	θ_{ch-c}	3.1	$^\circ C/W$
Channel temperature	T_{ch}	150	$^\circ C$
Storage temperature	T_{stg}	-55 to +150	$^\circ C$

Notes: 1. Pulse width limited by safe operating area.

2. $T_{ch} = 25^\circ C$, $T_{ch} \leq 150^\circ C$

3. Value at $T_c = 25^\circ C$

Electrical Characteristics

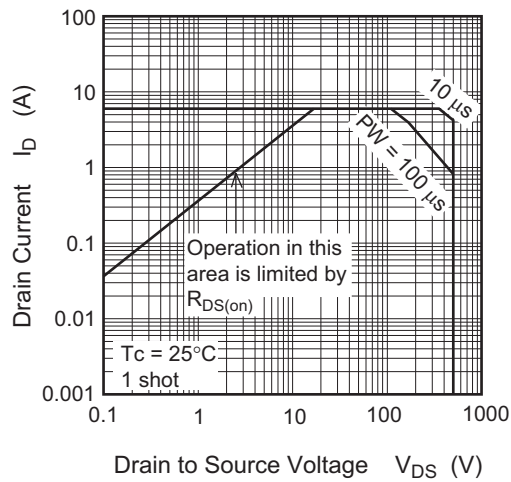
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	500	—	—	V	$I_D = 1 \text{ mA}$, $V_{GS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS} = 500 \text{ V}$, $V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 0.1	μA	$V_{GS} = \pm 30 \text{ V}$, $V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	3.5	—	4.5	V	$V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	2.1	2.8	Ω	$I_D = 1.5 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note 4}
Input capacitance	C_{iss}	—	280	—	pF	$V_{DS} = 25 \text{ V}$ $V_{GS} = 0$ $f = 1 \text{ MHz}$
Output capacitance	C_{oss}	—	33	—	pF	
Reverse transfer capacitance	C_{rss}	—	3.5	—	pF	
Turn-on delay time	$t_{d(on)}$	—	11	—	ns	$I_D = 1.5 \text{ A}$ $V_{GS} = 10 \text{ V}$ $R_L = 167 \Omega$ $R_g = 10 \Omega$
Rise time	t_r	—	12	—	ns	
Turn-off delay time	$t_{d(off)}$	—	23	—	ns	
Fall time	t_f	—	20	—	ns	
Total gate charge	Q_g	—	9.2	—	nC	$V_{DD} = 400 \text{ V}$ $V_{GS} = 10 \text{ V}$ $I_D = 3 \text{ A}$
Gate to source charge	Q_{gs}	—	1.8	—	nC	
Gate to drain charge	Q_{gd}	—	4.8	—	nC	
Body-drain diode forward voltage	V_{DF}	—	0.9	1.5	V	$I_F = 3 \text{ A}$, $V_{GS} = 0$ ^{Note 4}
Body-drain diode reverse recovery time	t_{rr}	—	200	—	ns	$I_F = 3 \text{ A}$, $V_{GS} = 0$ $di_F/dt = 100 \text{ A}/\mu\text{s}$

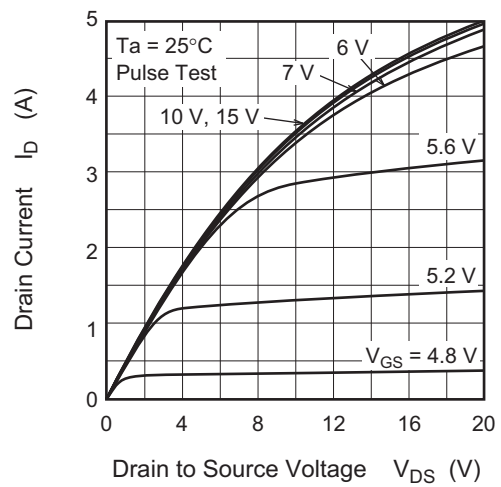
Note: 4. Pulse test

Main Characteristics

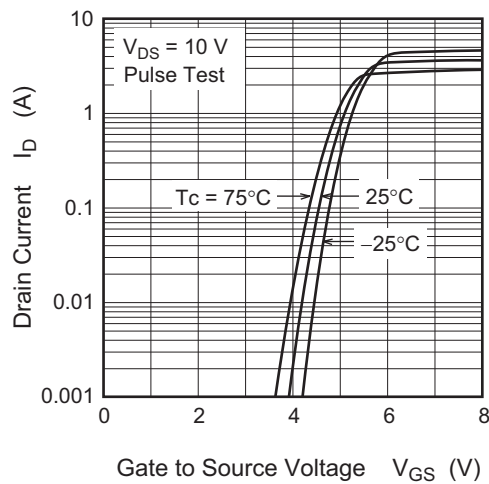
Maximum Safe Operation Area



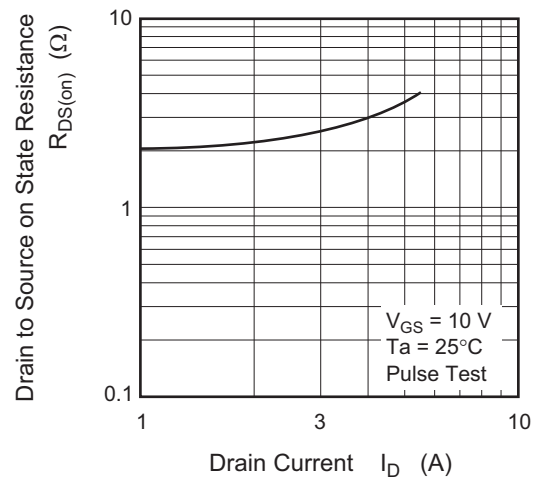
Typical Output Characteristics



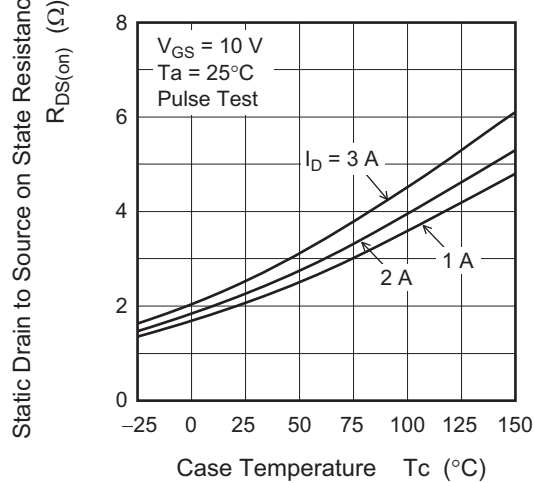
Typical Transfer Characteristics



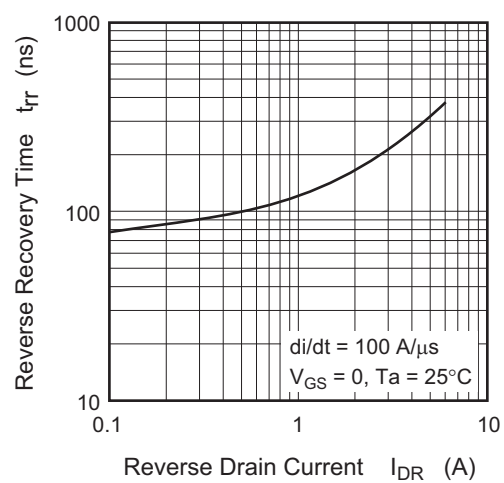
Static Drain to Source on State Resistance vs. Drain Current (Typical)

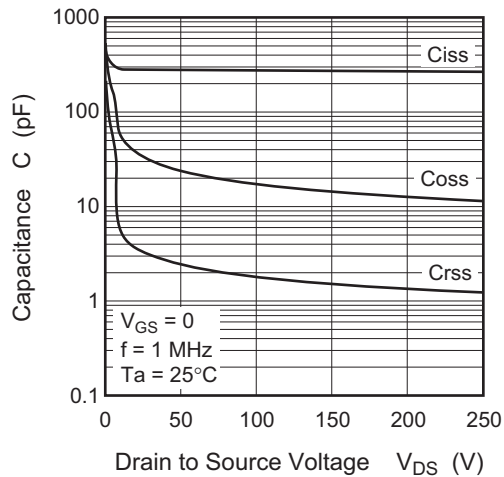


Static Drain to Source on State Resistance vs. Temperature (Typical)

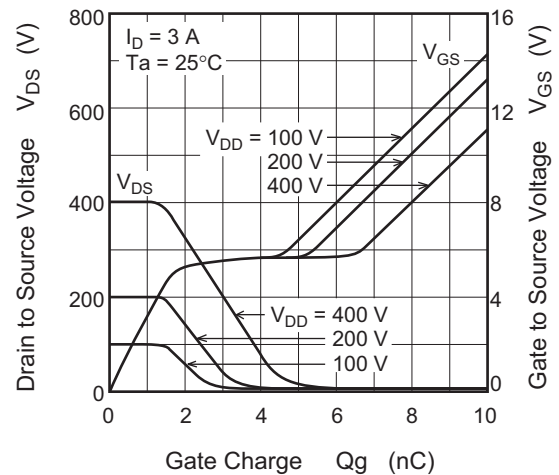
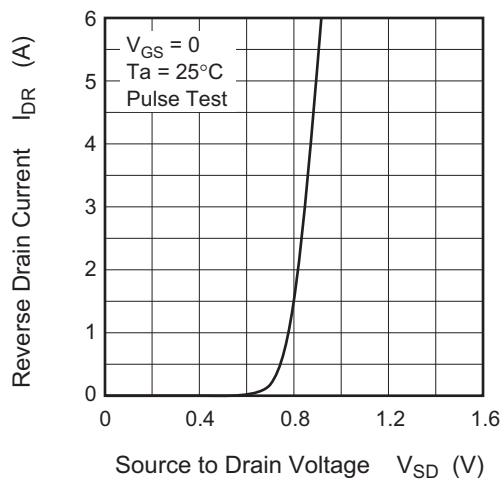
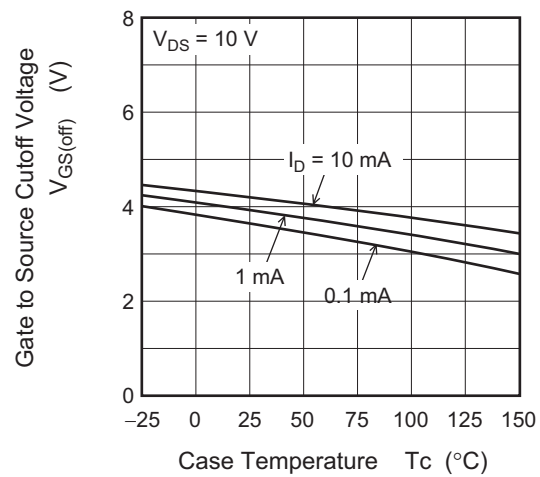


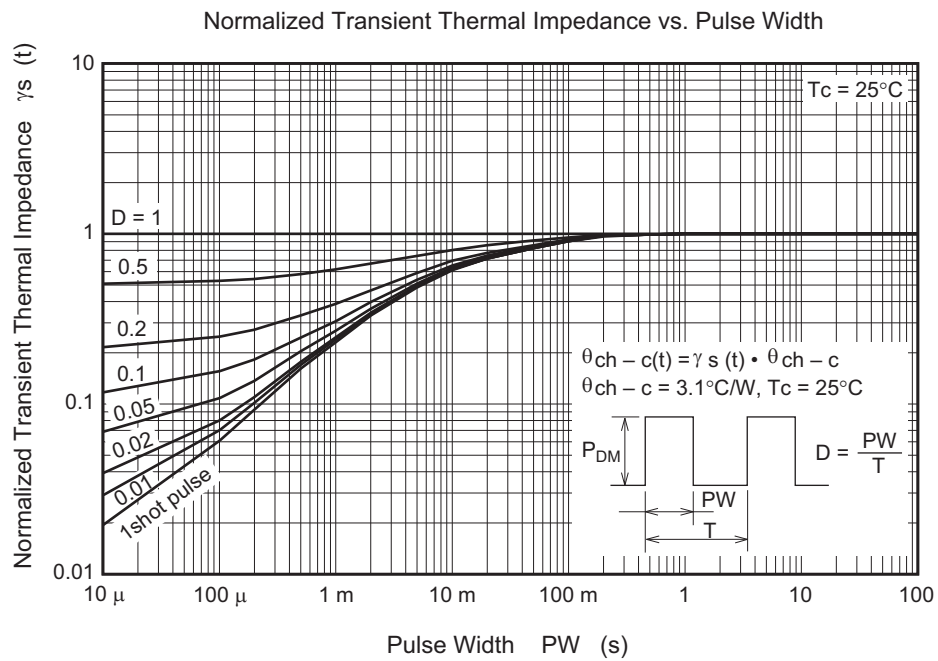
Body-Drain Diode Reverse Recovery Time (Typical)



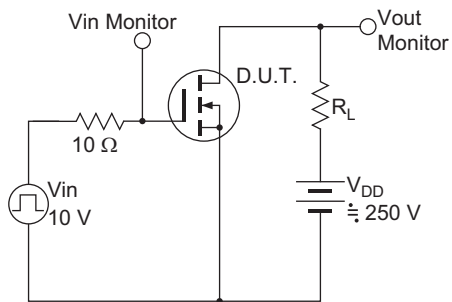
Typical Capacitance vs.
Drain to Source Voltage

Dynamic Input Characteristics (Typical)

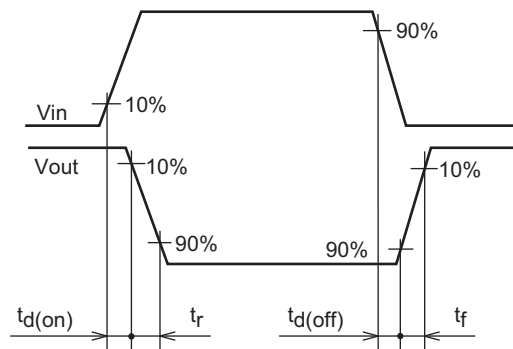
Reverse Drain Current vs.
Source to Drain Voltage (Typical)Gate to Source Cutoff Voltage
vs. Case Temperature (Typical)



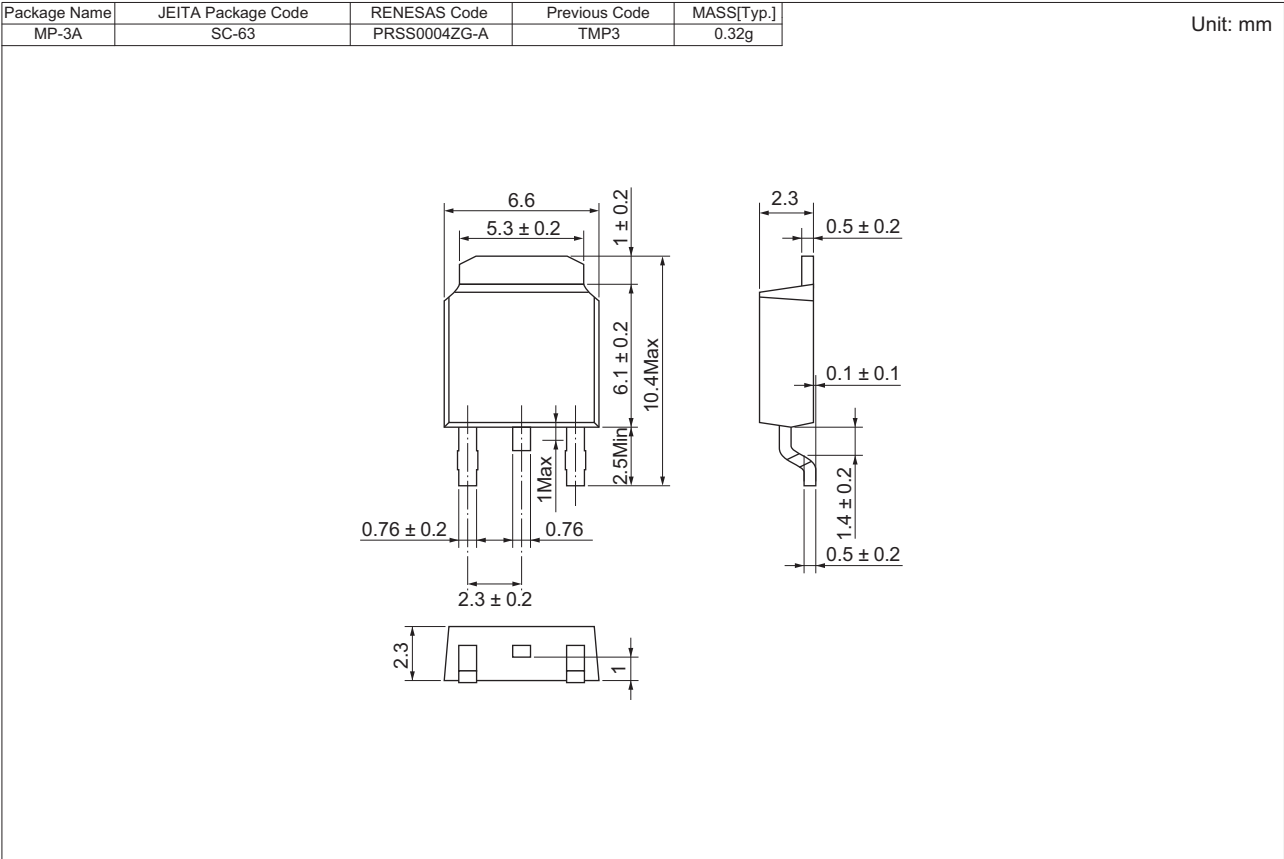
Switching Time Test Circuit



Waveform



Package Dimensions



Ordering Information

Orderable Part Number	Quantity	Shipping Container
RJK5032DPD-00#J2	3000 pcs	Taping

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