

RJK0629DPE

60V, 85A, 4.5m max.
N Channel Power MOS FET
High-Speed Switching Use

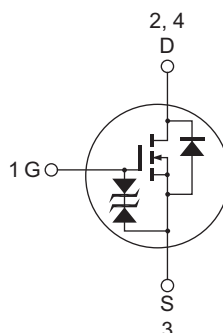
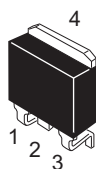
R07DS1060EJ0200
(Previous: REJ03G1874-0100)
Rev.2.00
Apr 09, 2013

Features

- V_{DS} : 60 V
- $R_{DS(on)}$: 4.5 m Ω (Max)
- I_D : 85 A

Outline

RENESAS Package code: PRSS0004AE-B
(Package name: LDKAK(S)-(1))



1. Gate
2. Drain
3. Source
4. Drain

Absolute Maximum Ratings

($T_a = 25^\circ\text{C}$)

| Item | Symbol | Value | Unit |
|---|-----------------------------------|-------------|--------------------|
| Drain to source voltage | V_{DS} | 60 | V |
| Gate to source voltage | V_{GS} | ± 20 | V |
| Drain current | I_D | 85 | A |
| Drain peak current | I_D (pulse) ^{Note1} | 340 | A |
| Body-drain diode reverse drain current | I_{DR} | 85 | A |
| Body-drain diode reverse drain peak current | I_{DR} (pulse) ^{Note1} | 340 | A |
| Avalanche current | I_{AP} ^{Note2} | 55 | A |
| Channel dissipation | P_{ch} ^{Note3} | 100 | W |
| Channel to case thermal impedance | θ_{ch-c} | 1.25 | $^\circ\text{C/W}$ |
| Channel temperature | T_{ch} | 150 | $^\circ\text{C}$ |
| Storage temperature | T_{stg} | -55 to +150 | $^\circ\text{C}$ |

Notes: 1. $PW \leq 10 \mu\text{s}$, duty cycle $\leq 1\%$
 2. $T_c = 25^\circ\text{C}$, $T_{ch} \leq 150^\circ\text{C}$, $L = 100 \mu\text{H}$
 3. Value at $T_c = 25^\circ\text{C}$

Electrical Characteristics

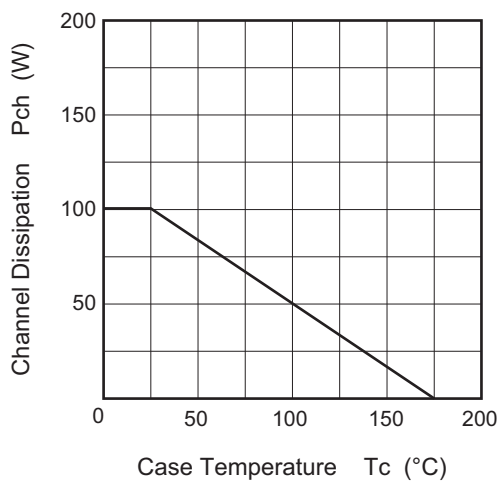
(Ta = 25°C)

| Item | Symbol | Min | Typ | Max | Unit | Test Conditions |
|--|---------------|----------|------|----------|------------|--|
| Drain to source breakdown voltage | $V_{(BR)DSS}$ | 60 | — | — | V | $I_D = 100\ \mu A$, $V_{GS} = 0$ |
| Gate to source breakdown voltage | $V_{(BR)GSS}$ | ± 20 | — | — | V | $I_G = \pm 100\ \mu A$, $V_{DS} = 0$ |
| Zero gate voltage drain current | I_{DSS} | — | — | 1 | μA | $V_{DS} = 60\ V$, $V_{GS} = 0$ |
| Gate to source leak current | I_{GSS} | — | — | ± 10 | μA | $V_{GS} = \pm 20\ V$, $V_{DS} = 0$ |
| Gate to source cutoff voltage | $V_{GS(off)}$ | 1.0 | — | 2.0 | V | $I_D = 1\ mA$, $V_{DS} = 10\ V$ |
| Static drain to source on state voltage | $V_{DS(on)}$ | — | 161 | 194 | mV | $I_D = 43A$, $V_{GS} = 10\ V$ ^{Note4} |
| Static drain to source on state resistance | $R_{DS(on)}$ | — | 3.75 | 4.5 | m Ω | $I_D = 43A$, $V_{GS} = 10\ V$ ^{Note4} |
| | | — | 4.9 | 6.6 | m Ω | $I_D = 43\ A$, $V_{GS} = 4.5\ V$ ^{Note4} |
| Input capacitance | C_{iss} | — | 4100 | — | pF | $V_{DS} = 10\ V$, $V_{GS} = 0$ $f = 1\ MHz$ |
| Output capacitance | C_{oss} | — | 1000 | — | pF | |
| Reverse transfer capacitance | C_{rss} | — | 780 | — | pF | |
| Total gate charge | Q_g | — | 85 | — | nC | $V_{DD} = 25\ V$, $V_{GS} = 10\ V$, $I_D = 85\ A$ |
| Gate to source charge | Q_{gs} | — | 11 | — | nC | |
| Gate to drain charge | Q_{gd} | — | 25 | — | nC | |
| Turn-on delay time | $t_{d(on)}$ | — | 20 | — | ns | $V_{DD} = 30V$, $I_D = 43A$, $V_{GS} = 10\ V$, $R_G = 4.7\ \Omega$ |
| Rise time | t_r | — | 40 | — | ns | |
| Turn-off delay time | $t_{d(off)}$ | — | 100 | — | ns | |
| Fall time | t_f | — | 40 | — | ns | |
| Body-drain diode forward voltage | V_{DF} | — | 0.92 | 1.2 | V | $I_F = 85\ A$, $V_{GS} = 0$ ^{Note4} |
| Body-drain diode reverse recovery time | t_{rr} | — | 50 | — | ns | $I_F = 85\ A$, $V_{GS} = 0$, $di_F/dt = 100\ A/\mu s$ |

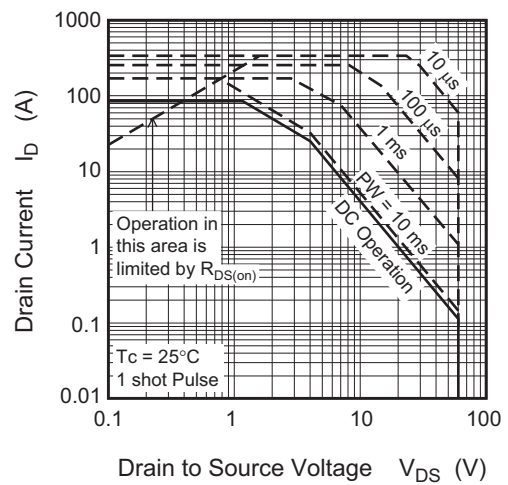
Note: 4. Pulse test

Main Characteristics

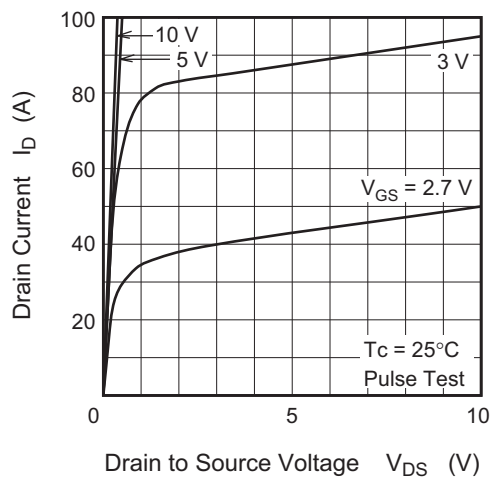
Power vs. Temperature Derating



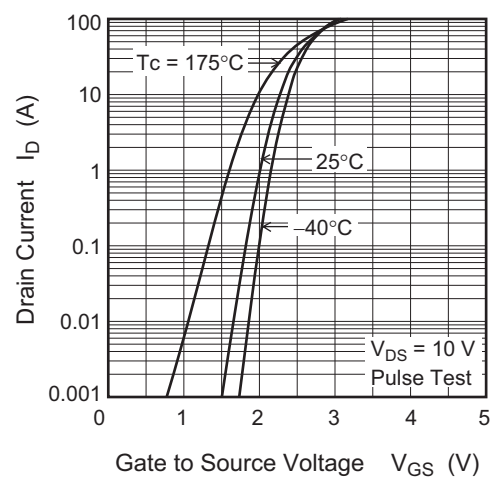
Maximum Safe Operation Area



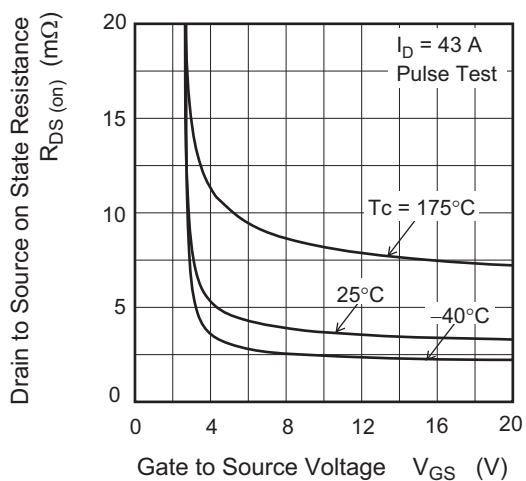
Typical Output Characteristics



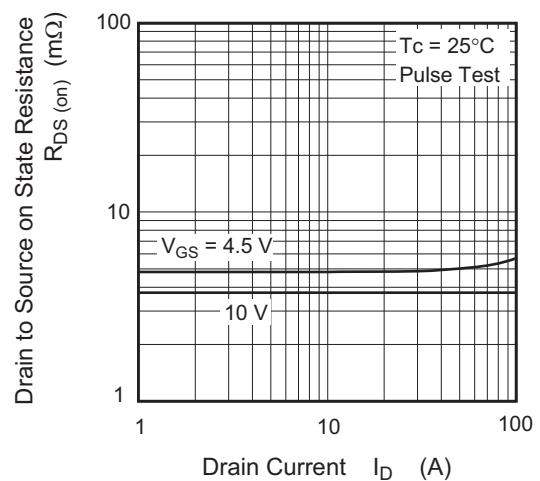
Typical Transfer Characteristics



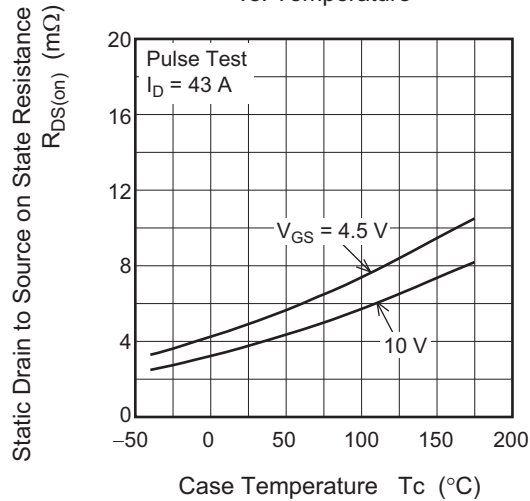
Static Drain to Source on State Resistance vs. Gate to Source Voltage



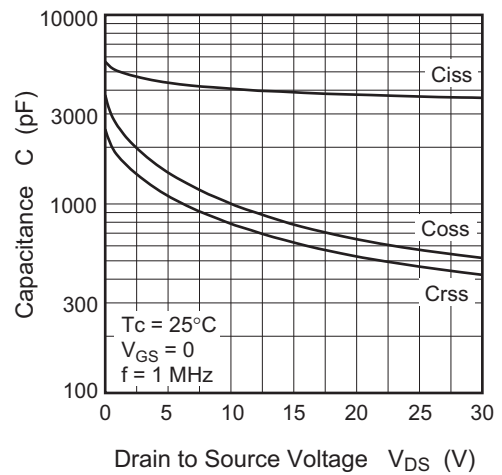
Static Drain to Source on State Resistance vs. Drain Current



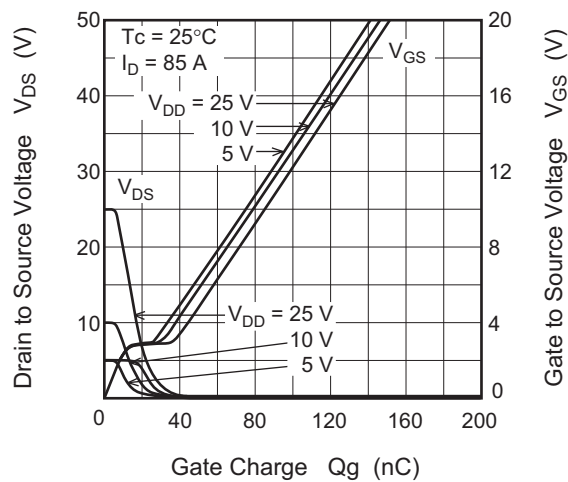
Static Drain to Source on State Resistance vs. Temperature



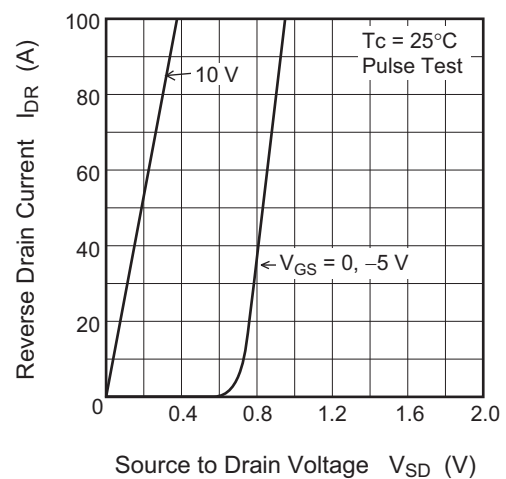
Typical Capacitance vs. Drain to Source Voltage



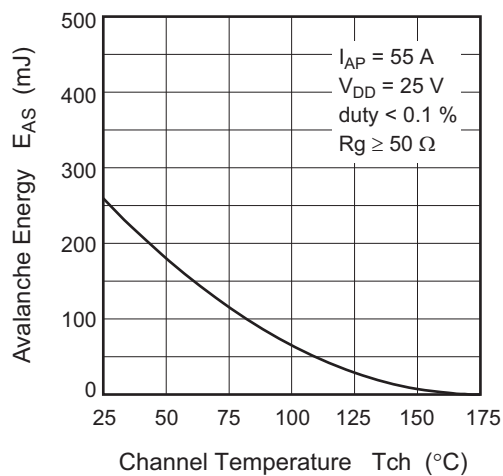
Dynamic Input Characteristics

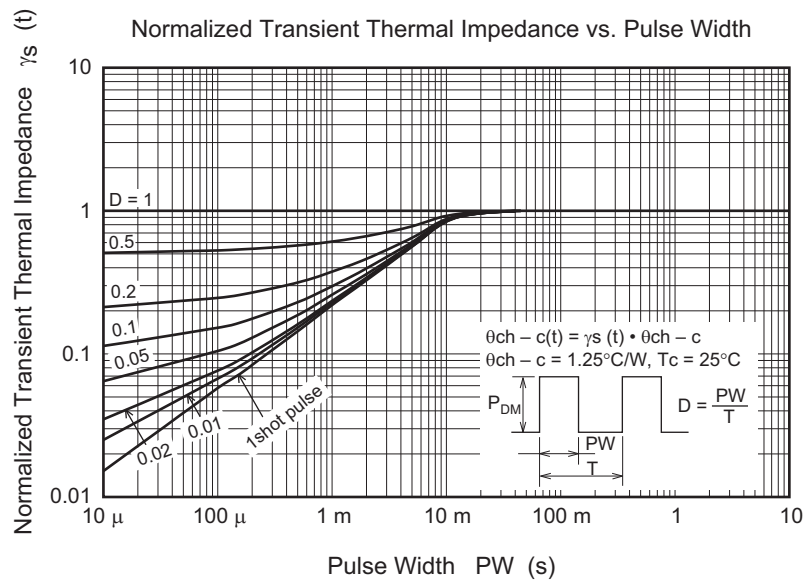


Reverse Drain Current vs. Source to Drain Voltage

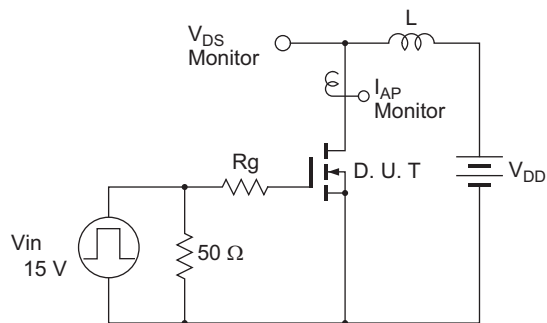


Maximum Avalanche Energy vs. Channel Temperature Derating



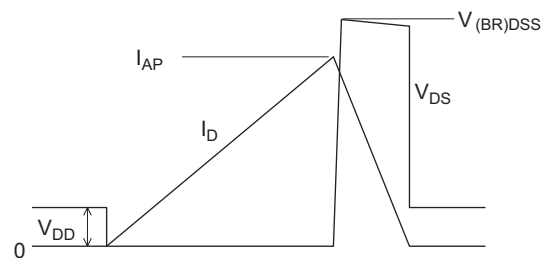


Avalanche Test Circuit

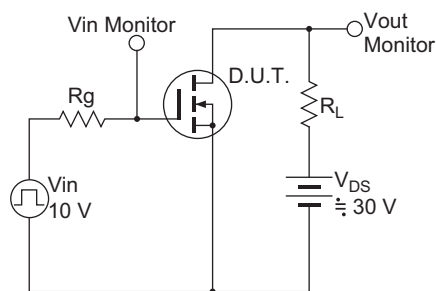


Avalanche Waveform

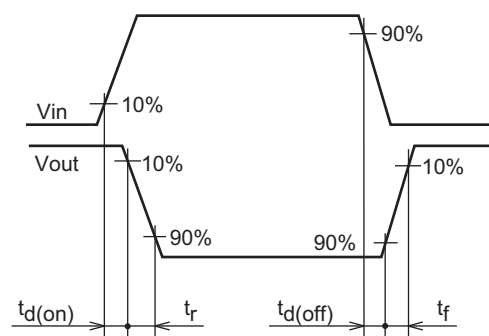
$$E_{AS} = \frac{1}{2} L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



Switching Time Test Circuit



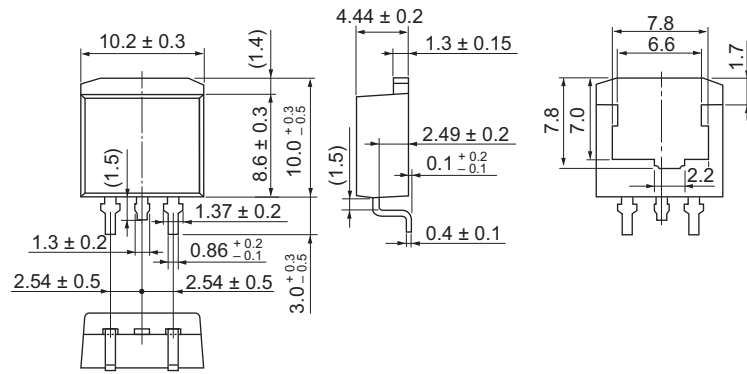
Switching Time Waveform



Package Dimensions

| Package Name | JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|--------------|--------------------|--------------|------------------------------|------------|
| LDBAK(S)-(1) | SC-83 | PRSS0004AE-B | LDBAK(S)-(1) / LDBAK(S)-(1)V | 1.30g |

Unit: mm



Ordering Information

| Part No. | Quantity | Shipping Container |
|------------------|----------|--------------------|
| RJK0629DPE-00-J3 | 1000 pcs | Taping |

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