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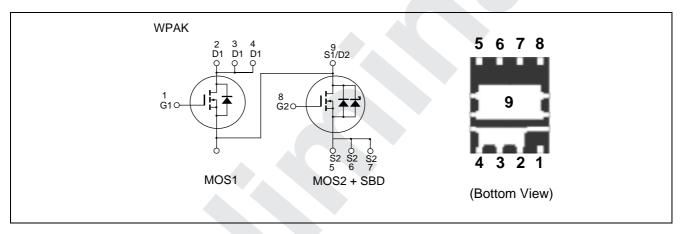
Silicon N Channel Power MOS FET with Schottky Barrier Diode High Speed Power Switching

> REJ03G1723-0101 Preliminary Rev.1.01 Jul 10, 2008

Features

- Low on-resistance
- Capable of 4.5 V gate drive
- High density mounting
- Pb-free
- Halogen-free

Outline



Absolute Maximum Ratings

				$(Ta = 25^{\circ}C)$	
		Ra			
Item	Symbol	MOS1	MOS2	Unit	
Drain to source voltage	V _{DSS}	30	30	V	
Gate to source voltage	V _{GSS}	±20	±20	V	
Drain current	ID	15	45	A	
Drain peak current	I _{D(pulse)} Note1	60	180	A	
Reverse drain current	I _{DR}	15	45	A	
Avalanche current	I _{AP} Note 2	11	20	A	
Avalanche energy	E _{AR} Note 2	12.1	40	mJ	
Channel dissipation	Pch Note3	10	30	W	
Channel temperature	Tch	150	150	°C	
Storage temperature	Tstg	-55 to +150	-55 to +150	°C	

Notes: 1. $PW \le 10 \ \mu s$, duty cycle $\le 1\%$

2. Value at Tch = 25° C, Rg $\geq 50 \Omega$

3. Tc = 25°C

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Electrical Characteristics

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Item	Symbol	Min	Тур	Max	Unit	Test Conditions
Drain to source breakdown voltage	V _{(BR)DSS}	30	_	_	V	$I_D = 10 \text{ mA}, V_{GS} = 0$
Gate to source leak current	I _{GSS}	_	—	±0.1	μΑ	$V_{GS} = \pm 20 V, V_{DS} = 0$
Zero gate voltage drain current	I _{DSS}	_	—	1	μΑ	$V_{DS} = 30 V, V_{GS} = 0$
Gate to source cutoff voltage	V _{GS(off)}	1.2	—	2.5	V	$V_{DS} = 10 \text{ V}, \text{ I}_{D} = 1 \text{ mA}$
Static drain to source on state	R _{DS(on)}	_	8.5	11.1	mΩ	$I_D = 7.5 \text{ A}, V_{GS} = 10 \text{ V}^{\text{Note4}}$
resistance	R _{DS(on)}	_	12	16.8	mΩ	$I_D = 7.5 \text{ A}, V_{GS} = 4.5 \text{ V}^{\text{Note4}}$
Forward transfer admittance	y _{fs}	_	TBD		S	$I_D = 7.5 \text{ A}, V_{DS} = 10 \text{ V}^{Note4}$
Input capacitance	Ciss	—	1010		pF	V _{DS} = 10 V
Output capacitance	Coss	—	190		pF	$V_{GS} = 0$
Reverse transfer capacitance	Crss	—	75		pF	f = 1 MHz
Gate Resistance	Rg	—	1.2		Ω	
Total gate charge	Qg	—	6.8		nC	V _{DD} = 10 V
Gate to source charge	Qgs	—	2.5		nC	$V_{GS} = 4.5 V$
Gate to drain charge	Qgd	—	1.5		nC	I _D = 15 A
Turn-on delay time	t _{d(on)}	—	TBD	-	ns	V _{GS} =10 V, I _D = 7.5 A
Rise time	tr	—	TBD		ns	$V_{DD} \cong 10 \text{ V}$
Turn-off delay time	t _{d(off)}	—	TBD		ns	R _L = 1.33 Ω
Fall time	t _f	_	TBD	-	ns	$R_g = 4.7 \Omega$
Body–drain diode forward voltage	V _{DF}	—	0.84	1.10	V	$I_F = 15 \text{ A}, V_{GS} = 0^{Note4}$
Body–drain diode reverse	t _{rr}	—	20		ns	I _F =15 A, V _{GS} = 0
recovery time						di _F / dt = 100 A/µs

Notes: 4. Pulse test

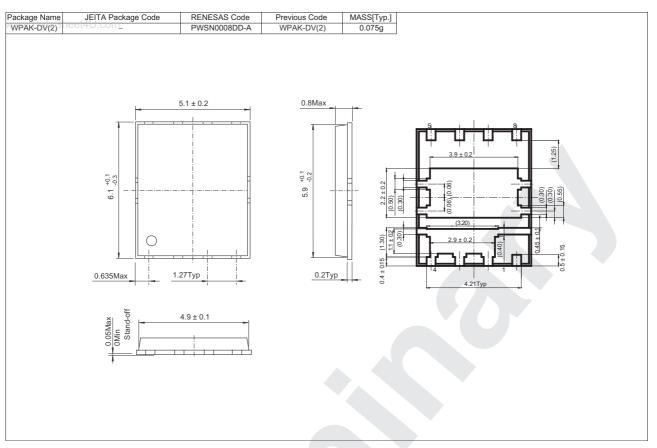
 $(Ta = 25^{\circ}C)$

• MOS2

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Item	Symbol	Min	Тур	Max	Unit	Test Conditions
Drain to source breakdown voltage	V _{(BR)DSS}	30	—		V	$I_D = 10 \text{ mA}, V_{GS} = 0$
Gate to source leak current	I _{GSS}		—	±0.1	μΑ	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0$
Zero gate voltage drain current	I _{DSS}	_	_	1	mA	$V_{DS} = 30 V, V_{GS} = 0$
Gate to source cutoff voltage	V _{GS(off)}	1.2	_	2.5	V	$V_{DS} = 10 \text{ V}, \text{ I}_{D} = 1 \text{ mA}$
Static drain to source on state	R _{DS(on)}	_	2.5	3.3	mΩ	I_D =22.5 A, V_{GS} = 10 V ^{Note4}
resistance	R _{DS(on)}	_	3.7	5.2	mΩ	$I_D = 22.5 \text{ A}, V_{GS} = 4.5 \text{ V}^{Note4}$
Forward transfer admittance	y _{fs}	_	TBD	_	S	$I_D = 22.5 \text{ A}, V_{DS} = 10 \text{ V}^{Note4}$
Input capacitance	Ciss	_	3200	_	pF	V _{DS} = 10 V
Output capacitance	Coss	_	720		pF	$V_{GS} = 0$
Reverse transfer capacitance	Crss	_	300	_	pF	f = 1 MHz
Gate Resistance	Rg	_	1.5	_	Ω	
Total gate charge	Qg	_	20	_	nC	V _{DD} = 10 V
Gate to source charge	Qgs	_	8.6	_	nC	$V_{GS} = 4.5 V$
Gate to drain charge	Qgd	_	6.5	_	nC	I _D = 45 A
Turn-on delay time	t _{d(on)}	_	TBD	_	ns	$V_{GS} = 10 \text{ V}, \text{ I}_{D} = 22.5 \text{ A}$
Rise time	tr	_	TBD		ns	$V_{DD} \cong 10 \text{ V}$
Turn-off delay time	t _{d(off)}	_	TBD	_	ns	$R_L = 0.44 \Omega$
Fall time	t _f	_	TBD		ns	$R_g = 4.7 \Omega$
Schottky Barrier diode forward voltage	VF		0.36		V	$I_F = 2 \text{ A}, V_{GS} = 0^{Note4}$
Body–drain diode reverse	t _{rr}	_	30		ns	$I_F = 45 \text{ A}, V_{GS} = 0$
recovery time						di _F / dt = 100 A/µs

Notes: 4. Pulse test

Package Dimensions



Ordering Information

Part No.	Quantity		Shipping Container
RJK0383DPA-00-J0	2500 pcs	Taping	

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