

RJK0332DPB

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Silicon N Channel Power MOS FET Power Switching

REJ03G1641-0400

Rev.4.00

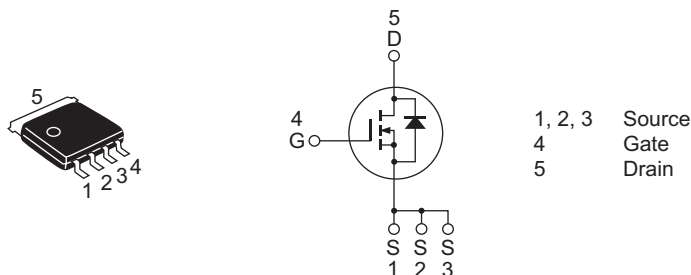
Apr 10, 2008

Features

- High speed switching
- Capable of 4.5 V gate drive
- Low drive current
- High density mounting
- Low on-resistance
 $R_{DS(on)} = 3.6 \text{ m}\Omega$ typ. (at $V_{GS} = 10 \text{ V}$)
- Pb-free

Outline

RENESAS Package code: PTZZ0005DA-A
(Package name: LPAK)



Absolute Maximum Ratings

($T_a = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	30	V
Gate to source voltage	V_{GSS}	± 20	V
Drain current	I_D	35	A
Drain peak current	$I_{D(pulse)}$ ^{Note 1}	140	A
Body-drain diode reverse drain current	I_{DR}	35	A
Avalanche current	I_{AP} ^{Note 2}	15	A
Avalanche energy	E_{AR} ^{Note 2}	22.5	mJ
Channel dissipation	P_{ch} ^{Note 3}	45	W
Channel to Case Thermal Resistance	θ_{ch-C}	2.78	$^\circ\text{C/W}$
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

Notes: 1. $PW \leq 10 \mu\text{s}$, duty cycle $\leq 1\%$
 2. Value at $T_{ch} = 25^\circ\text{C}$, $R_g \geq 50 \Omega$
 3. $T_c = 25^\circ\text{C}$

Electrical Characteristics

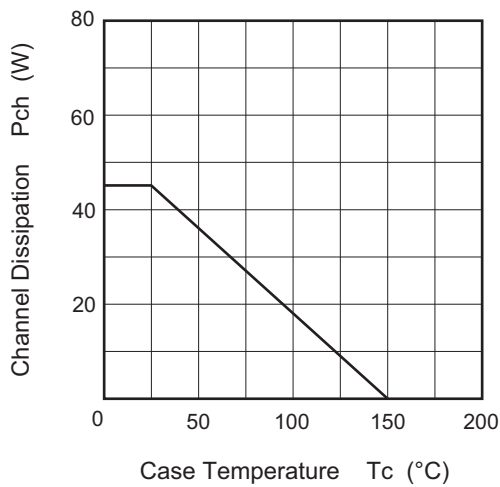
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 0.1	μA	$V_{GS} = \pm 20 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS} = 30 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.2	—	2.5	V	$V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	3.6	4.7	$\text{m}\Omega$	$I_D = 17.5 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note4}
	$R_{DS(on)}$	—	5.0	7.0	$\text{m}\Omega$	$I_D = 17.5 \text{ A}$, $V_{GS} = 4.5 \text{ V}$ ^{Note4}
Forward transfer admittance	$ y_{fs} $	—	70	—	S	$I_D = 17.5 \text{ A}$, $V_{DS} = 10 \text{ V}$ ^{Note4}
Input capacitance	C_{iss}	—	2180	—	pF	$V_{DS} = 10 \text{ V}$, $V_{GS} = 0$, $f = 1 \text{ MHz}$
Output capacitance	C_{oss}	—	420	—	pF	
Reverse transfer capacitance	C_{rss}	—	140	—	pF	
Gate Resistance	R_g	—	0.7	—	Ω	
Total gate charge	Q_g	—	14	—	nC	$V_{DD} = 10 \text{ V}$, $V_{GS} = 4.5 \text{ V}$, $I_D = 35 \text{ A}$
Gate to source charge	Q_{gs}	—	5.1	—	nC	
Gate to drain charge	Q_{gd}	—	3.0	—	nC	
Turn-on delay time	$t_{d(on)}$	—	5.8	—	ns	$V_{GS} = 10 \text{ V}$, $I_D = 17.5 \text{ A}$, $V_{DD} \cong 10 \text{ V}$, $R_L = 0.57 \Omega$, $R_g = 4.7 \Omega$
Rise time	t_r	—	3.8	—	ns	
Turn-off delay time	$t_{d(off)}$	—	40	—	ns	
Fall time	t_f	—	4.4	—	ns	
Body-drain diode forward voltage	V_{DF}	—	0.83	1.08	V	$I_F = 35 \text{ A}$, $V_{GS} = 0$ ^{Note4}
Body-drain diode reverse recovery time	t_{rr}	—	25	—	ns	$I_F = 35 \text{ A}$, $V_{GS} = 0$ $di_F/dt = 100 \text{ A}/\mu\text{s}$
Body-drain diode reverse recovery charge	Q_{rr}	—	19	—	nC	

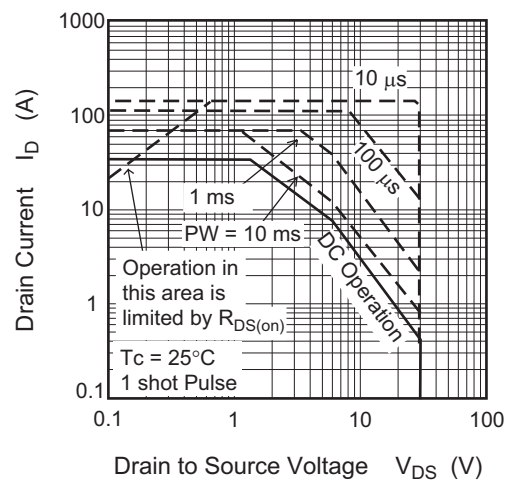
Notes: 4. Pulse test

Main Characteristics

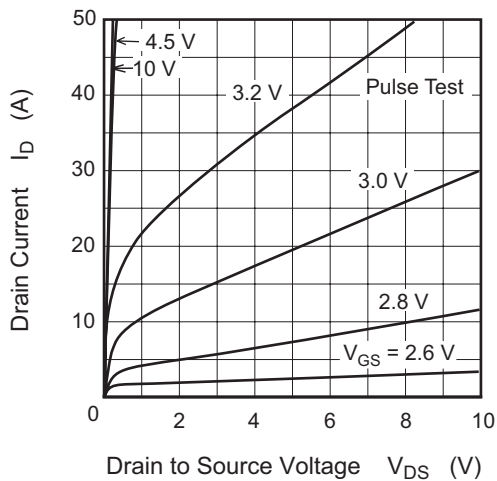
Power vs. Temperature Derating



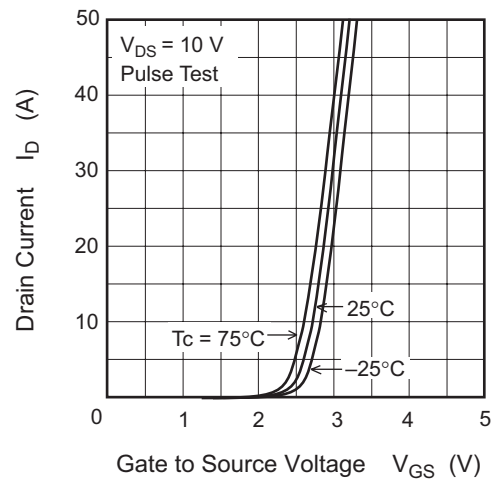
Maximum Safe Operation Area



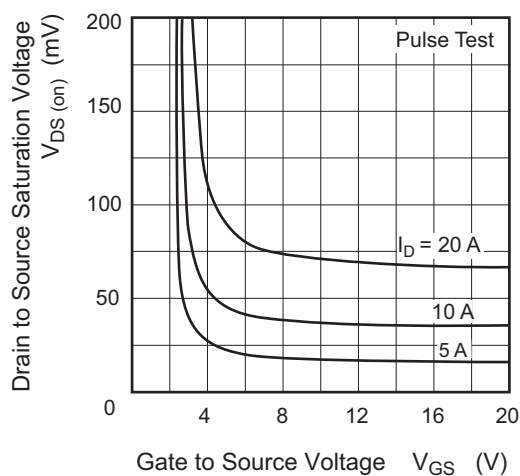
Typical Output Characteristics



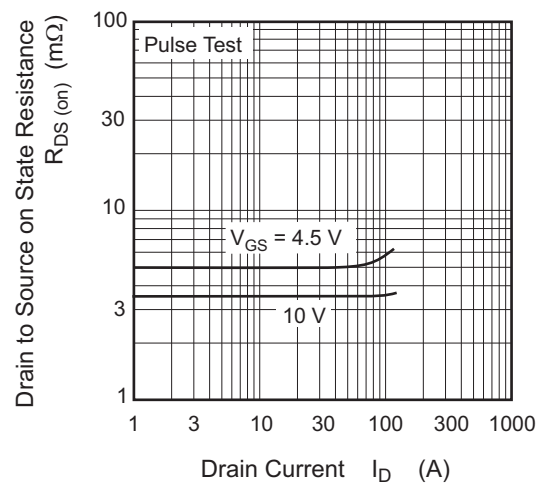
Typical Transfer Characteristics



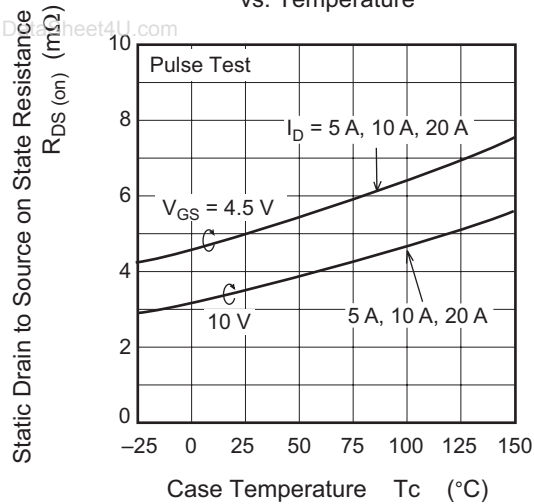
Drain to Source Saturation Voltage vs. Gate to Source Voltage



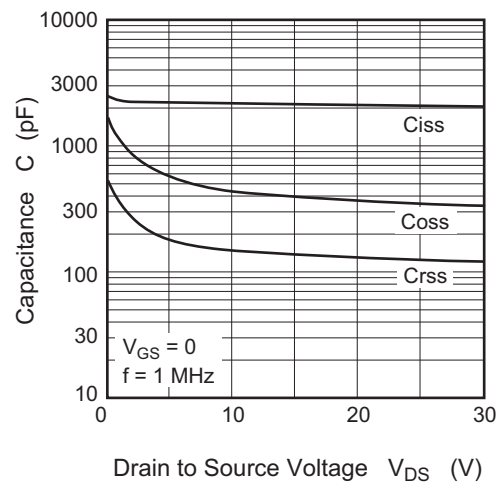
Static Drain to Source on State Resistance vs. Drain Current



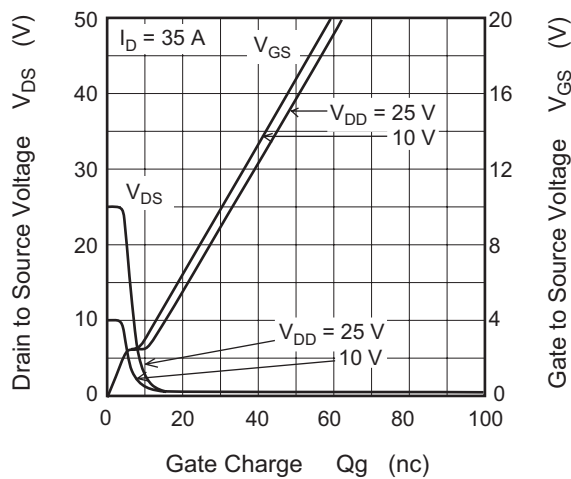
Static Drain to Source on State Resistance vs. Temperature



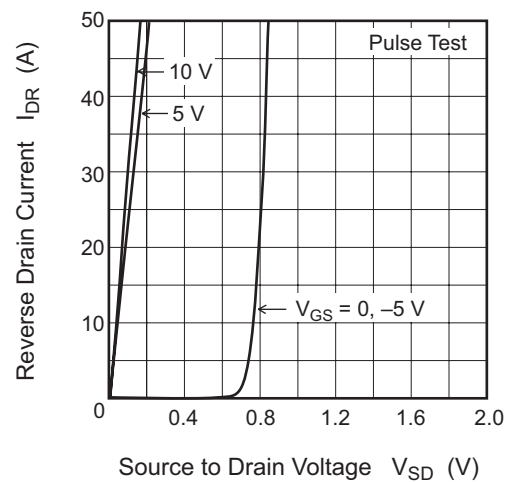
Typical Capacitance vs. Drain to Source Voltage



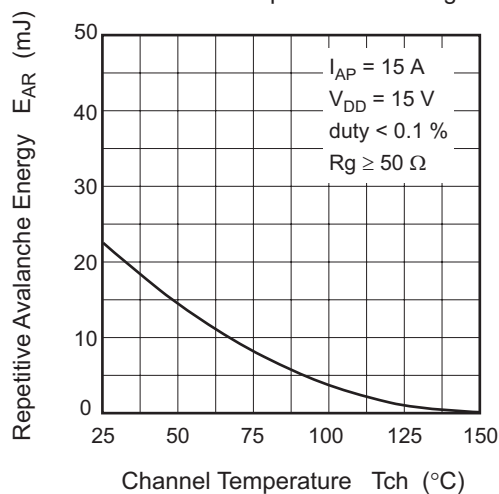
Dynamic Input Characteristics



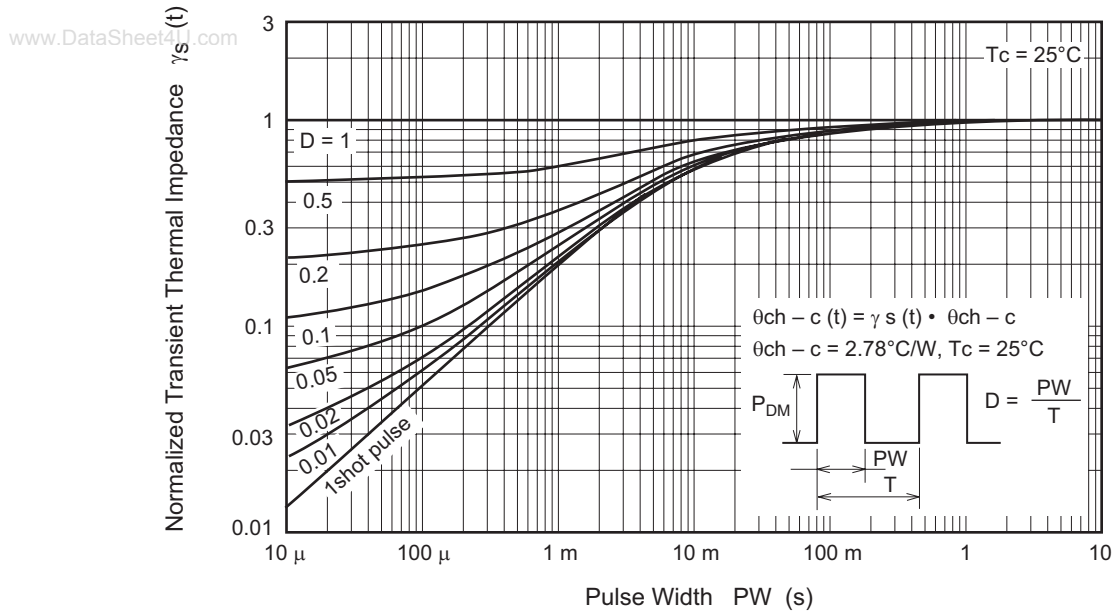
Reverse Drain Current vs. Source to Drain Voltage



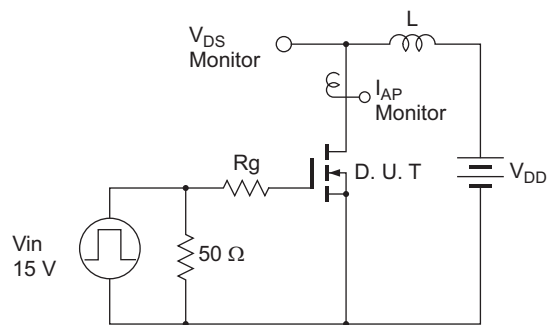
Maximum Avalanche Energy vs. Channel Temperature Derating



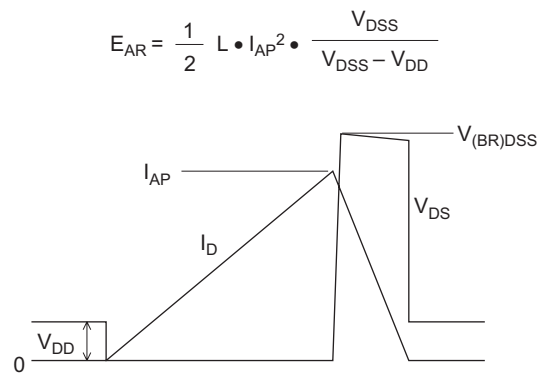
Normalized Transient Thermal Impedance vs. Pulse Width



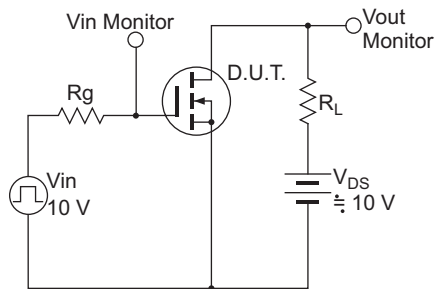
Avalanche Test Circuit



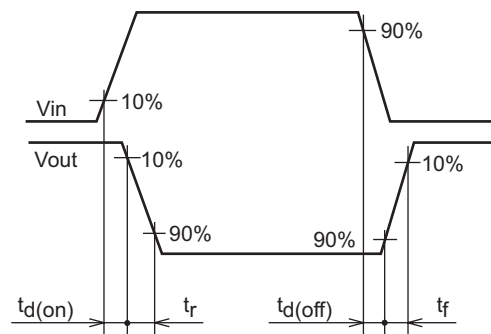
Avalanche Waveform



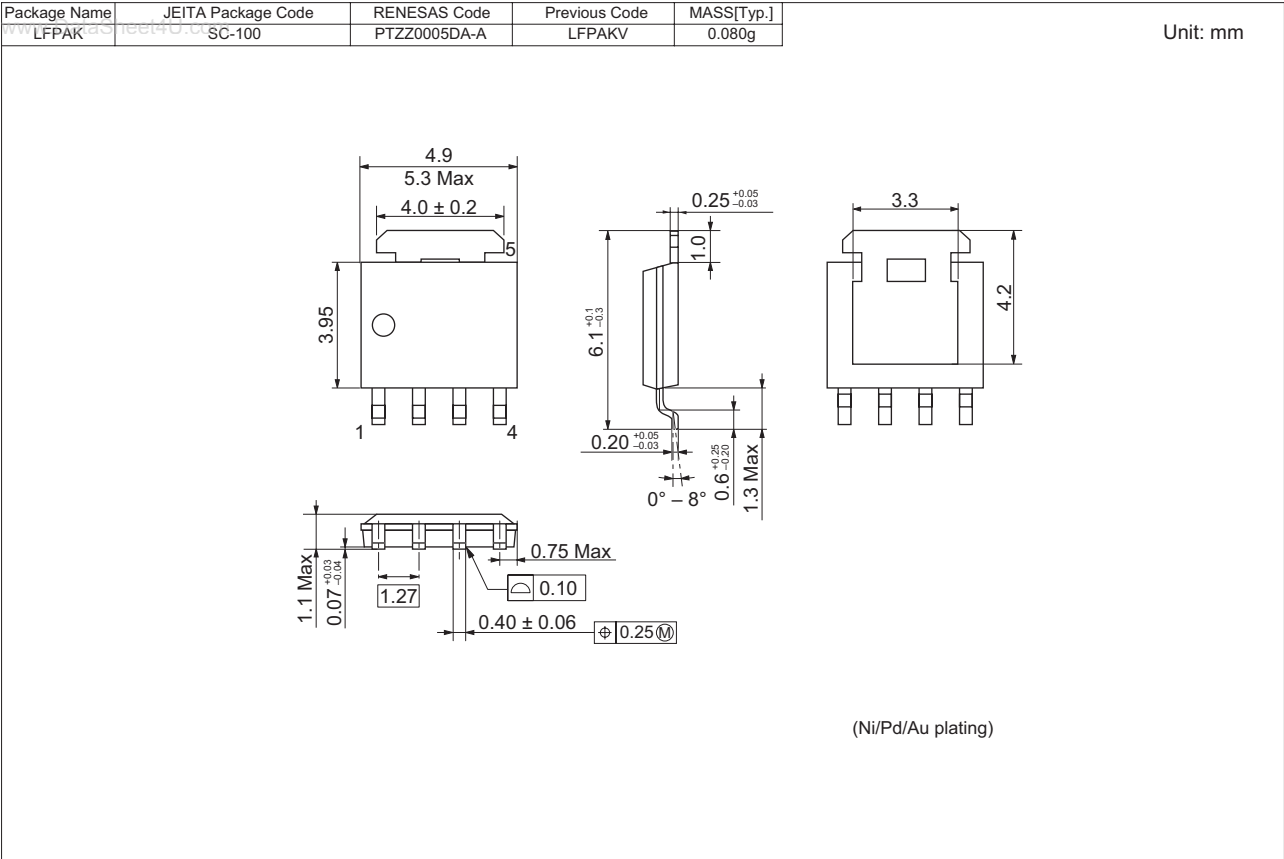
Switching Time Test Circuit



Switching Time Waveform



Package Dimensions



Ordering Information

Part No.	Quantity	Shipping Container
RJK0332DPB-00-J0	2500 pcs	Taping

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Renesas Technology America, Inc.
450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd, Pudong District, Shanghai, China 200120
Tel: <86> (21) 5877-1818, Fax: <86> (21) 6887-7858/7898

Renesas Technology Hong Kong Ltd.
7th Floor, North Tower, World Finance Centre, Harbour City, Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2377-3473

Renesas Technology Taiwan Co., Ltd.
10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 3518-3399

Renesas Technology Singapore Pte. Ltd.
1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Renesas Technology Korea Co., Ltd.
Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

Renesas Technology Malaysia Sdn. Bhd
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510