

RJK0234DNS

25V, 35A, 5.8mΩmax.
N Channel Power MOS FET
High Speed Power Switching

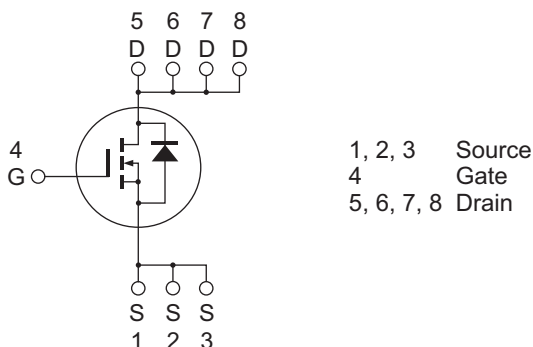
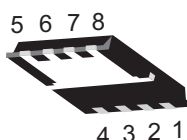
R07DS1073EJ0130
Rev.1.30
May 23, 2013

Features

- Very high speed switching
- Capable of 4.5 V gate drive
- Low drive current
- High density mounting
- Low on-resistance
- Pb-free
- Halogen-free

Outline

RENESAS Package code: PVS0008JD-A
(Package name: 8pin HVSON(3333))



1, 2, 3 Source
4 Gate
5, 6, 7, 8 Drain

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V _{DSS}	25	V
Gate to source voltage	V _{GSS}	+10,-8	V
Drain current	I _D	35	A
Drain peak current	I _{D(pulse)} ^{Note1}	140	A
Body-drain diode reverse drain current	I _{DR}	35	A
Avalanche current	I _{AP} ^{Note 2}	21	A
Avalanche energy	E _{AS} ^{Note 2}	55	mJ
Channel dissipation	P _{ch} ^{Note3}	30	W
Channel to case thermal impedance	θ _{ch-c} ^{Note3}	4.17	°C/W
Channel temperature	T _{ch}	150	°C
Storage temperature	T _{stg}	-55 to +150	°C

Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1%
2. Value at T_{ch} = 25°C, R_g ≥ 50 Ω
3. T_c = 25°C

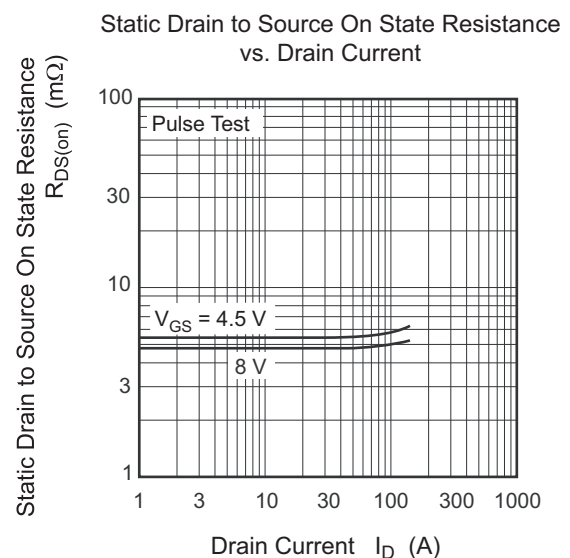
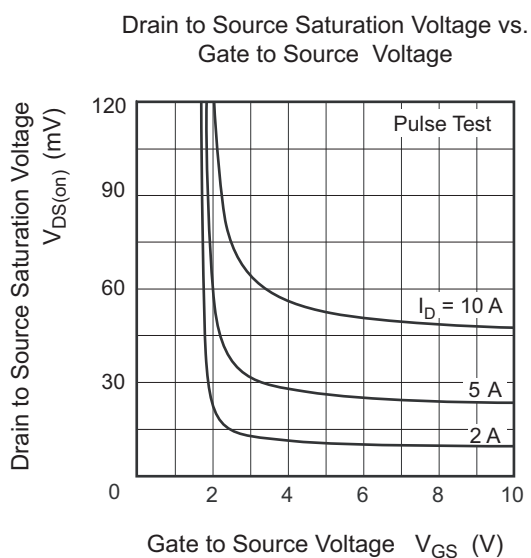
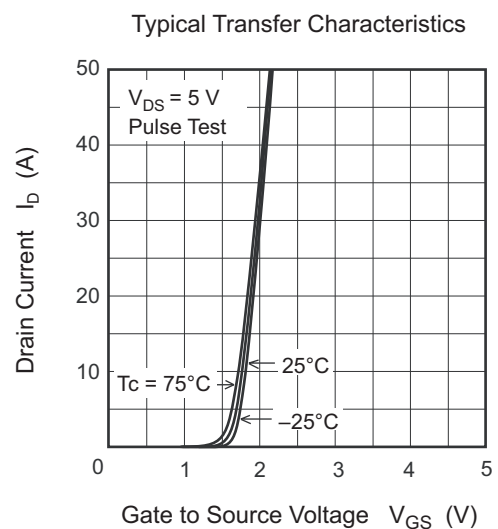
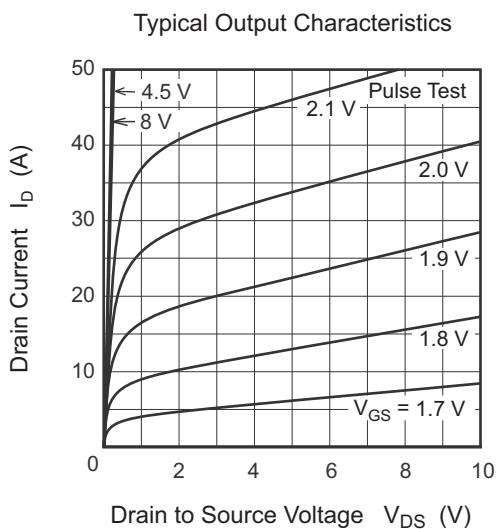
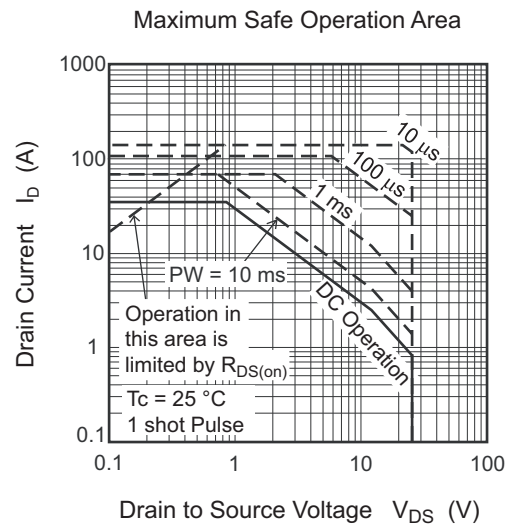
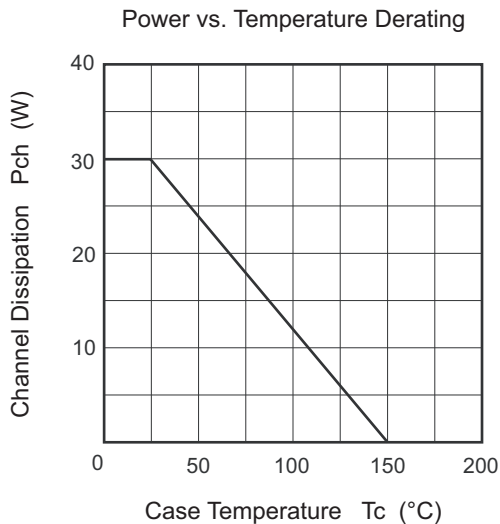
Electrical Characteristics

(Ta = 25°C)

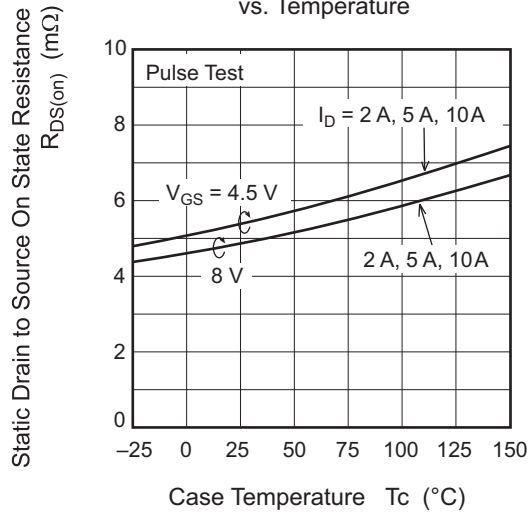
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	25	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 0.1	μA	$V_{GS} = +10/-8 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS} = 20 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	0.9	—	1.4	V	$V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	4.8	5.8	$\text{m}\Omega$	$I_D = 17.5 \text{ A}$, $V_{GS} = 8 \text{ V}$ ^{Note4}
	$R_{DS(on)}$	—	5.4	6.8	$\text{m}\Omega$	$I_D = 17.5 \text{ A}$, $V_{GS} = 4.5 \text{ V}$ ^{Note4}
Forward transfer admittance	$ y_{fs} $	—	80	—	S	$I_D = 17.5 \text{ A}$, $V_{DS} = 5 \text{ V}$ ^{Note4}
Input capacitance	C_{iss}	—	1050	1470	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	C_{oss}	—	880	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	66	—	pF	$f = 1 \text{ MHz}$
Gate Resistance	R_g	—	0.6	1.6	Ω	
Total gate charge	Q_g	—	7.3	—	nC	$V_{DD} = 10 \text{ V}$
Gate to source charge	Q_{gs}	—	1.9	—	nC	$V_{GS} = 4.5 \text{ V}$
Gate to drain charge	Q_{gd}	—	1.4	—	nC	$I_D = 35 \text{ A}$
Turn-on delay time	$t_{d(on)}$	—	2.8	—	ns	$V_{GS} = 8 \text{ V}$, $I_D = 17.5 \text{ A}$
Rise time	t_r	—	1.9	—	ns	$V_{DD} \cong 10 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	13.6	—	ns	$R_L = 0.57 \Omega$
Fall time	t_f	—	3.3	—	ns	$R_g = 4.7 \Omega$
Body-drain diode forward voltage	V_{DF}	—	0.84	1.09	V	$I_F = 35 \text{ A}$, $V_{GS} = 0$ ^{Note4}
Body-drain diode reverse recovery time	t_{rr}	—	10.5	—	ns	$I_F = 35 \text{ A}$, $V_{GS} = 0$ $di_F/dt = 500 \text{ A}/\mu\text{s}$

Notes: 4. Pulse test

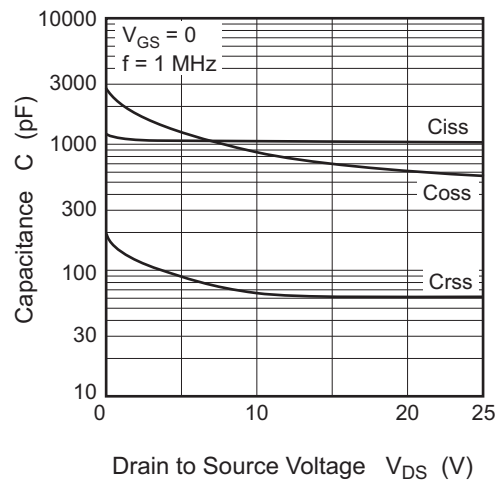
Main Characteristics



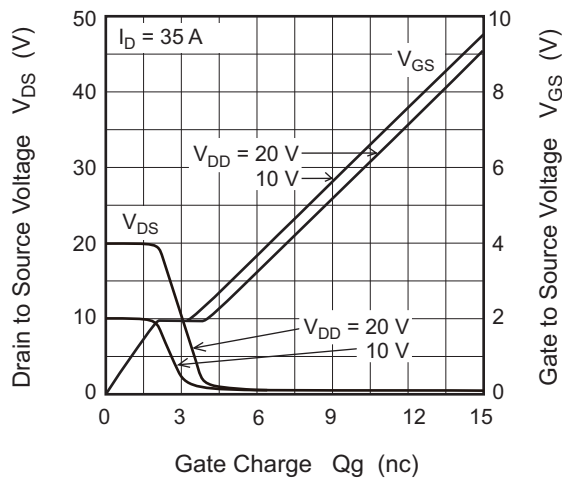
Static Drain to Source On State Resistance vs. Temperature



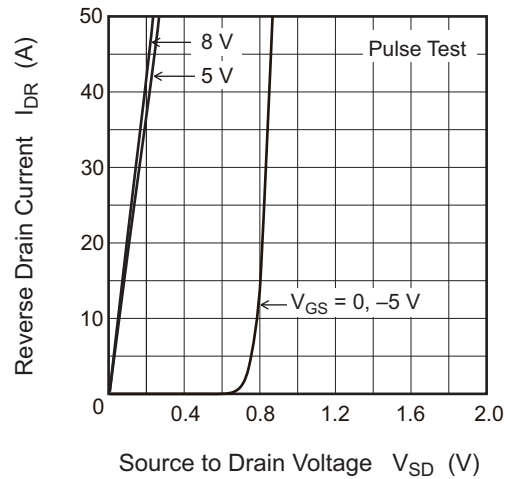
Typical Capacitance vs. Drain to Source Voltage



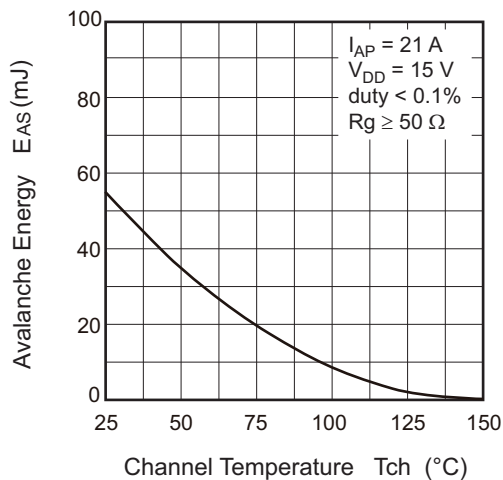
Dynamic Input Characteristics



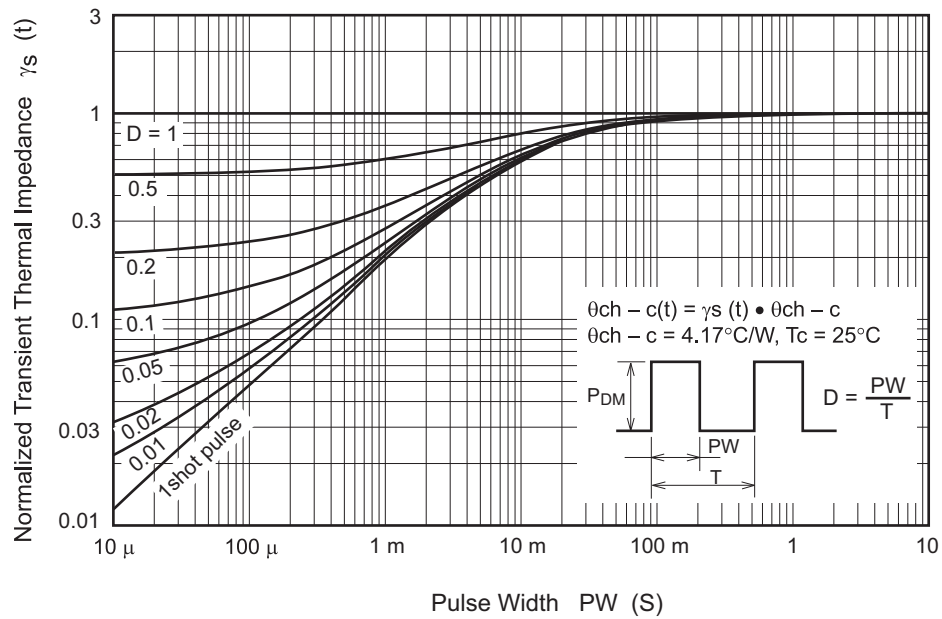
Reverse Drain Current vs. Source to Drain Voltage



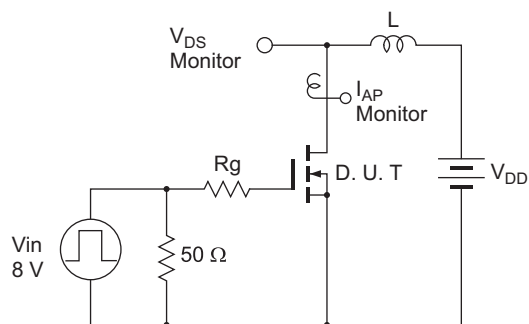
Maximum Avalanche Energy vs. Channel Temperature Derating



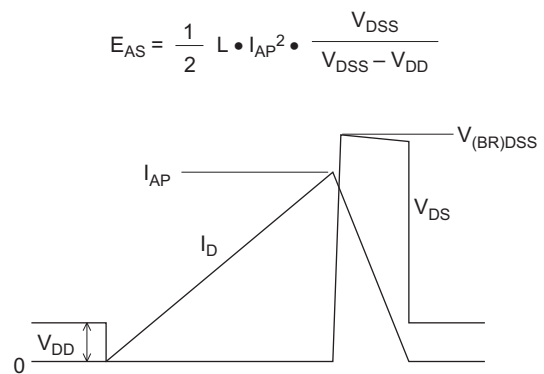
Normalized Transient Thermal Impedance vs. Pulse Width



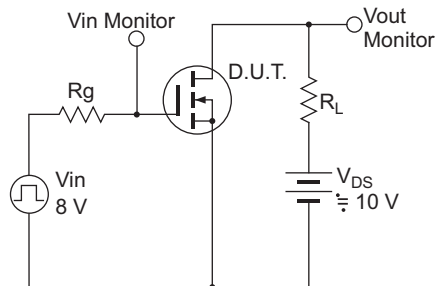
Avalanche Test Circuit



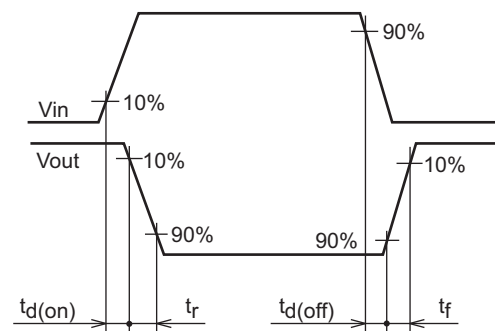
Avalanche Waveform



Switching Time Test Circuit



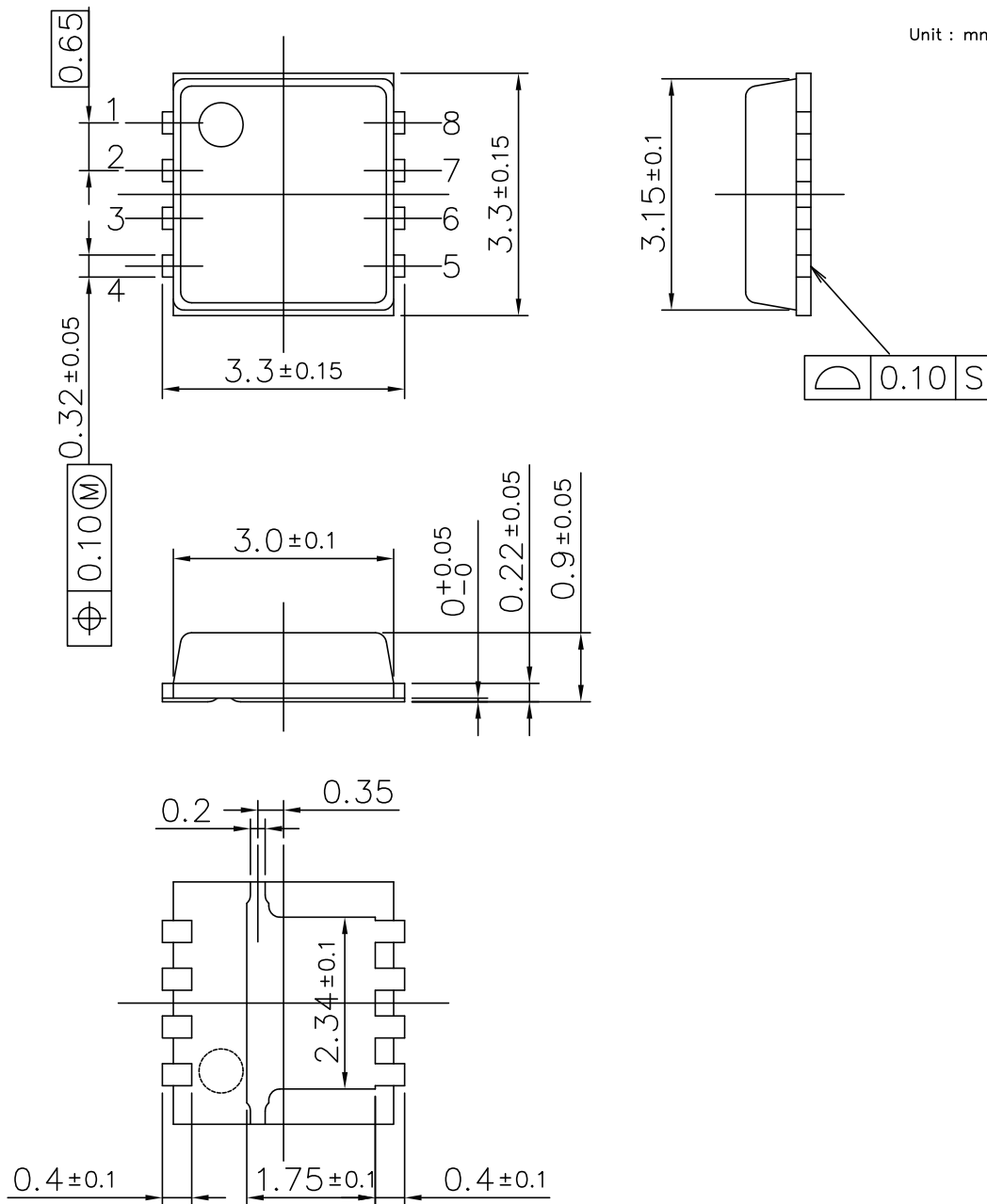
Switching Time Waveform



Package Dimensions

JEITA Package Code	Renesas Code	Previous Code	Mass(TYP.)[g]
—	PVSN0008JD—A	P8E1—65—432	0.028

Unit : mm



Ordering Information

Orderable Part Number	Quantity	Shipping Container	Package
RJK0234DNS-00-J5	3000 pcs	Taping	8pin HVSON(3333) 0.028g TYP

Note: The symbol of 2nd "-" is occasionally presented as "#".

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