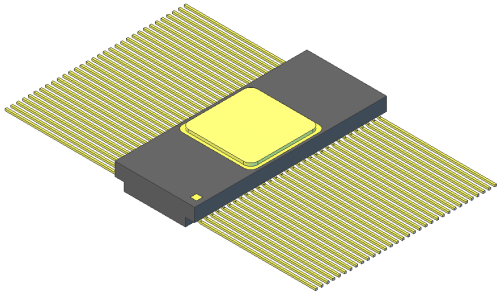
RHFLVDS228A

Rad-hard, dual 4x4 crosspoint switch LVDS

Datasheet - production data



Ceramic Flat-64

The upper metallic lid is electrically connected to ground.

Features

- LVDS input/output
- Multiple configuration: Mux, repeater and splitter
- ANSI TIA/EIA-644 compliant
- 400 Mbps LVDS (200 MHz)
- 200 MHz clock channel
- Cold spare on all pins
- Fail-safe function
- 3.3 V operating power supply
- 4.8 V absolute rating
- Hermetic package
- Power consumption: 220 mW at 3.3 V
- Large input common mode: -4 V to +5 V
- Guaranteed up to 300 krad TID
- SEL immune up to 135 MeV.cm²/mg
- SET/SEU immune up to 22 MeV.cm²/mg

Description

The RHFLVDS228A is an 8-channel, 4x4 crosspoint switch base, on low voltage differential signaling (LVDS) for low-power and high-speed communications. The two 4x4 multiplexers allow connection from any of the four inputs to any of the four outputs.

Packaged and qualified for use in aerospace environments in a low-power, fast-transmission standard, the RHFLVDS228A operates at 3.3 V power supply (3.6 V max. operating and 4.8 V AMR) and a common mode of -4 V to +5 V. The LVDS outputs operate over a controlled impedance of 100-ohm transmission media that may be printed circuit board traces, back planes, or cables.

The circuit features an internal fail-safe function to ensure a known state in case of an input short circuit or a floating input.

All pins have cold spare buffers to ensure they are in high impedance when V_{CC} is tied to GND. The RHFLVDS228A can operate over a wide temperature range of -55 °C to +125 °C and it is housed in an hermetic Ceramic Flat-64 package.

Table 1. Device summary

Reference	SMD pin	Quality level	Package	Lead finish	Mass	EPPL[1]	Temp. range
RHFLVDS228AK1	-	Engineering model	Ceramic Flat-64	Gold	-	-	-55 °C to 125 °C
RHFLVDS228AK01V[2]	TBD	QML-V flight				Target	

1. EPPL = ESA preferred part list
2. Not yet in full production

Contents

1 Functional description

Table 2. Mux truth table

SL1	SL2	SL3	SL4	OUT1	OUT2	OUT3	OUT4	Mode
0	0	0	0	IN1	IN1	IN3	IN3	Splitter
0	0	0	1	IN1	IN1	IN3	IN4	Splitter/repeater
0	0	1	0	IN1	IN1	IN1	IN1	Splitter
0	0	1	1	IN1	IN1	IN4	IN4	
0	1	0	0	IN1	IN2	IN3	IN3	Splitter/repeater
0	1	0	1	IN1	IN2	IN3	IN4	Repeater
0	1	1	0	IN1	IN2	IN4	IN3	Repeater/switch
0	1	1	1	IN1	IN2	IN4	IN4	Splitter/repeater
1	0	0	0	IN2	IN2	IN2	IN2	Splitter
1	0	0	1	IN2	IN1	IN3	IN4	Switch/repeater
1	0	1	0	IN2	IN1	IN4	IN3	Switch
1	0	1	1	IN3	IN3	IN3	IN3	Splitter
1	1	0	0	IN2	IN2	IN3	IN3	
1	1	0	1	IN2	IN2	IN3	IN4	Splitter/repeater
1	1	1	0	IN4	IN4	IN4	IN4	Splitter
1	1	1	1	IN2	IN2	IN4	IN4	

Note: 1 A floating SL pin is equivalent to a low logic level

2 Channels 5, 6, 7, and 8 behave like channels 1, 2, 3 and 4 respectively (see also Figure 1)

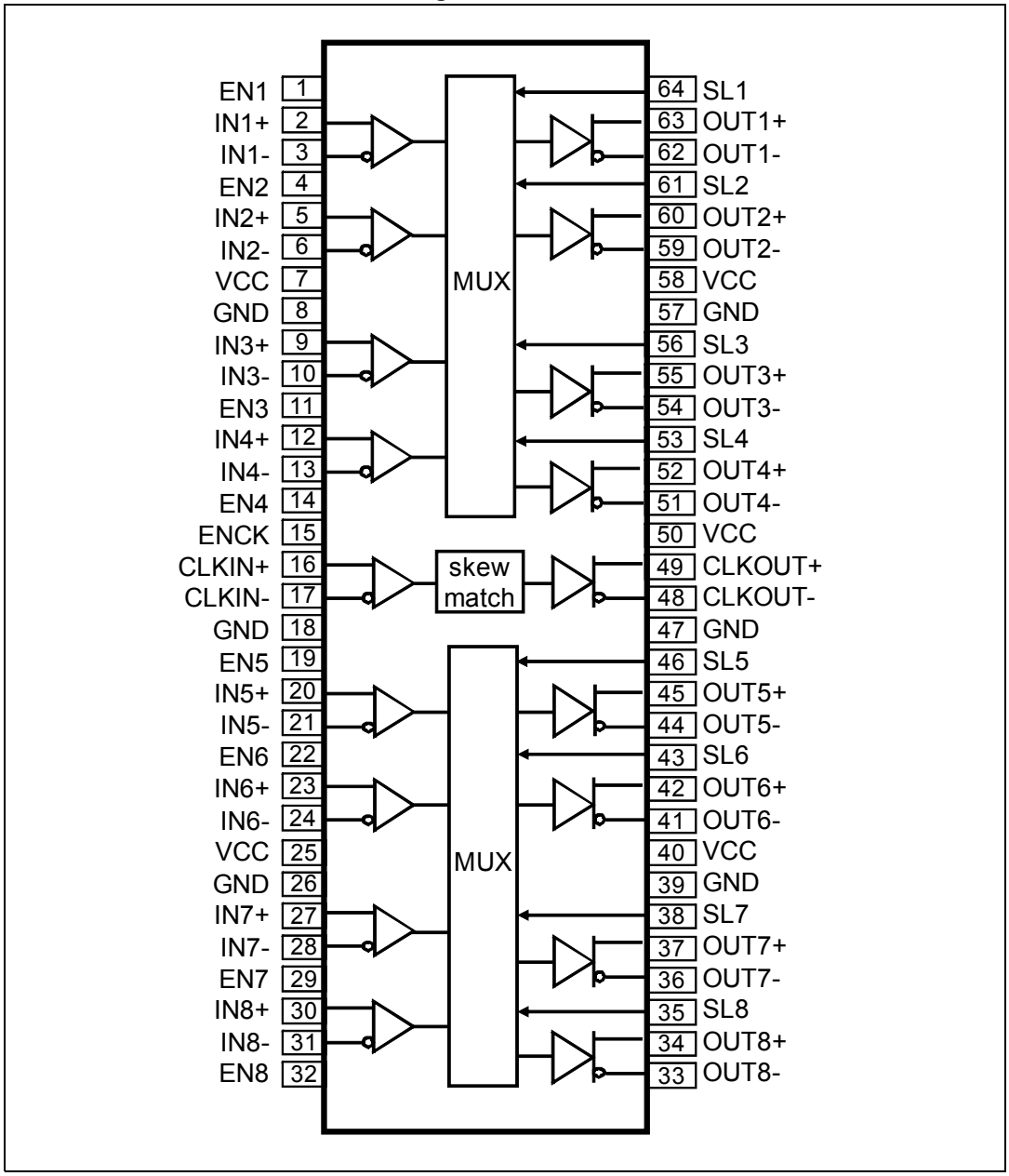
Table 3. Enable (EN) truth table

EN	Inputs	Outputs	
	(IN+) - (IN-)	OUT+	OUT-
L	X	Z	Z
H or floating (internal pull-up)	Vid ≥ 0.1 V	H	L
	Vid ≤-0.1 V	L	H
	-0.1V < Vid < +0.1 V	Unknown	
	Full fail-safe open/short or terminated	H	L

Note: Vid = (VIN+)-(VIN-), L = low level, H = high level, X = don't care, Z = high impedance

2 Pin configuration

Figure 1. Pinout



1. Power supplies are not internally separated. All Vcc pins must be connected to the same potential.

3 Maximum ratings and operating conditions

Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage(1)	4.8	V
V_i	TTL inputs (operating or cold-spare)	-0.3 to 4.8	
V_{CM}	LVDS common mode (operating or cold-spare)	-5 to +6	
T_{stg}	Storage temperature range	-65 to +150	°C
T_j	Maximum junction temperature	+150	
R_{thjc}	Thermal resistance junction to case(2)	20	°C/W
ESD	HBM: Human body model – All pins excepted LVDS inputs and outputs – LVDS inputs and outputs vs. GND	 2 8	kV
	CDM: Charge device model	500	V

1. All voltages, except the differential I/O bus voltage, are with respect to the network ground terminal.
2. Short-circuits can cause excessive heating. Destructive dissipation can result from short-circuits on the amplifiers.

Table 5. Operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage	3	3.3	3.6	V
V_{CM}	Static common mode	- 4		+ 5	
T_A	Ambient temperature range	-55		+125	°C

4 Electrical characteristics

Total dose (MIL-STD-883 TM 1019)

The products guaranteed in radiation within the RHA QML-V system fully comply with the MIL-STD-883 TM 1019 specification.

The RHFLVDS228A is RHA QML-V, tested and characterized in full compliance with the MIL-STD-883 specification, between 50 and 300 rad/s only (full CMOS technology).

All parameters provided in *Table 7: Electrical characteristics table* apply to both pre- and post-irradiation, as follows:

- All test are performed in accordance with MIL-PRF-38535 and test method 1019 of MIL-STD-883 for total ionizing dose (TID).
- The initial characterization is performed in qualification only on both biased and unbiased parts.
- Each wafer lot is tested at high dose rate only, in the worst bias case condition, based on the results obtained during the initial qualification.

Heavy ions

The behavior of the product when submitted to heavy ions is not tested in production. Heavy-ion trials are performed on qualification lots only.

Table 6. Radiations

Type	Characteristics	Value	Unit
TID	High-dose rate (50 - 300 rad/sec)	300	krad
Heavy ions	SEL immunity up to: (with a particle angle of 60 °, at 125 °C)	135	MeV.cm²/mg
	SEL immunity up to: (with a particle angle of 0 °, at 125 °C)	67	
	SET/SEU immunity up to: (at 25 °C)	22	

In *Table 7* below, V_{CC} = 3 V to 3.6 V, capa-load (CL) = 10 pF, typical values are at T_{amb} = +25 °C, min. and max values are at T_{amb} = - 55 °C and + 125 °C unless otherwise specified.

Table 7. Electrical characteristics table

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Whole circuit						
I_{CCL}	Total enabled supply current, drivers and receivers enabled, not switching	V_{ID} = 400 mV and load = 100 Ω on all channels		67	80	mA
I_{CCZ}	Total disabled supply current, loaded or not loaded, drivers and receivers disabled	V_{ID} = 400 mV EN and ENCK = GND			20	
Digital inputs EN, ENCK, and SL						
V_{IH}	Input voltage high		2		V_{CC}	V
V_{IL}	Input voltage low		GND		0.8	
I_{IH}	High level input current	V_{CC} = 3.6 V, V_{IN} = V_{CC}	-10		10	µA
I_{IL}	Low level input current	V_{CC} = 3.6 V, V_{IN} = 0	-10		10	
I_{OFF}	TTL inputs power off leakage current	V_{CC} = 0 V, EN and SL = 3.6 V	-10		10	
LVDS inputs						
V_{TL}	Differential input low threshold	V_{CM} = 1.2 V			-100	mV
		-4 V < V_{CM} < +5 V			-130	
V_{TH}	Differential input high threshold	V_{CM} = 1.2 V	+100			
		-4V < V_{CM} < +5 V	+130			
V_{CMR}	Common mode voltage range	V_{ID} = 200 mVp-p	- 4		+5	V
V_{CMREJ}	Common mode rejection(1)	F = 10 MHz			300	mVp-p
I_{ID}	Differential input current	V_{ID} = 400 mVp-p	-10		10	µA
I_{ICM}	Common mode input current	V_{IC} = - 4 V to + 5 V	-70		70	
I_{OFFIN}	LVDS input power-off leakage current(2)	V_{CC} = 0 V, V_{IN} = -4 V to 5 V	-60		60	
C_{IN}	Input capacitance			3		pF
LVDS outputs						
V_{OH}	Output voltage high				1.65	V
V_{OL}	Output voltage low		0.925			
V_{OD}	Differential output voltage		250		400	mV
DV_{OD}	Change of magnitude of V_{OD} for complementary output states				10	
V_{OS}	Offset voltage		1.125		1.45	V
DV_{OS}	Change of magnitude of V_{OS} for complementary output states				25	mV

Table 7. Electrical characteristics table (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{OS}	Output short-circuit current	V_{ID} = -400 mV and V_{OUT-} = 0 V V_{ID} = +400 mV and V_{OUT+} = 0 V	-9			mA
I_{OZ}	High impedance output current	Disabled, V_{OUT} = 3.6 V or 0V	-10		10	µA
I_{OFFOUT}	LVDS outputs power-off leakage current	V_{CC} = 0 V, V_{OUT} = 3.6 V	-50		+50	
T_S	Input to SL setup time(3)	Refer to *Figure 4*	1.6			ns
T_H	Input to SL Hold time(3)		1.5			
T_{Sw}	SL to Switched output(3)				5	
t_{PHLD}	Propagation delay time, high to low	V_{ID} = 200 mVp-p, input pulse from 1.1 V to 1.3 V, V_{CM}=1.2 V Load: refer to *Figure 2*	1.5		4	
t_{PLHD}	Propagation delay time, low to high		1.5		4	
t_{SK1}	Channel to channel skew(3)(4)	V_{ID} = 200 mVp-p Load: refer to *Figure 5*			0.5	
t_{SK2}	Chip to chip skew(3)(5)				0.7	
t_{SKD}	Differential skew(6) (t_{PHLD}-t_{PLHD})				0.5	
t_r	Output signal rise time	Refer to *Figure 3*		0.9		
t_f	Output signal fall time			0.9		
t_{PLZ}	Propagation delay time, low level to high impedance output	Refer to *Figure 5*			2.8	
t_{PHZ}	Propagation delay time, high level to high impedance output				2.8	
t_{PZH}	Propagation delay time, high impedance to high level output				2.5	
t_{PZL}	Propagation delay time, high impedance to low level output				2.5	
Fail-safe and cold-spare						
t_{D1}	Fail-safe to active time			1		µs
t_{D2}	Active to fail-safe time			1		

1. Guaranteed by characterization on bench.
2. All pins are floating except pin under test and V_{CC}.
3. Guaranteed by design.
4. t_{SK1} is the maximum delay time difference between drivers on the same device (with all inputs connected together).
5. t_{SK2} is the maximum delay time difference between outputs of all devices when they operate with the same supply voltage, at the same temperature.
6. t_{SKD} is the maximum delay time difference between t_{PHLD} and t_{PLHD} (see *Figure 3*).

Cold sparing

The RHFLVDS228A features a cold spare input and output buffer. In high reliability applications, cold sparing enables a redundant device to be tied to the data bus with its power supply at 0 V (V_{CC} = GND) without affecting the bus signals or injecting current from the I/Os to the power supplies. Cold sparing also allows redundant devices to be kept powered off so that they can be switched on only when required. This has no impact on the application. Cold sparing is achieved by implementing a high impedance between the I/Os and V_{CC}. ESD protection is ensured through a non-conventional dedicated structure.

Fail-safe

In many applications, inputs need a fail-safe function to avoid an uncertain output state when the inputs are not connected properly. In case of an LVDS input short circuit or floating inputs, the LVDS outputs remain in stable logic-high state.

5 Test circuit

Figure 2. Voltage and current definition

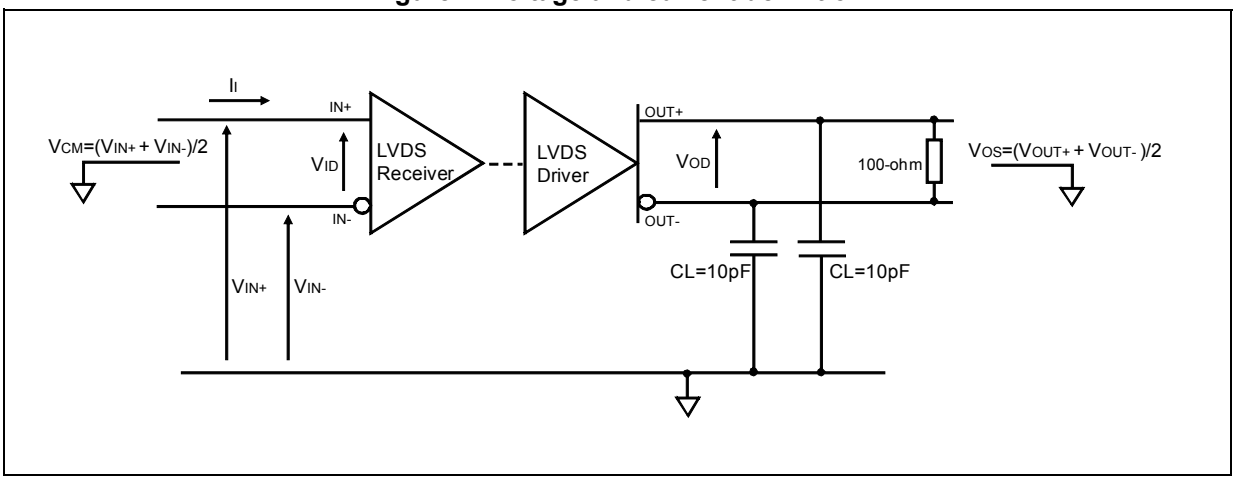
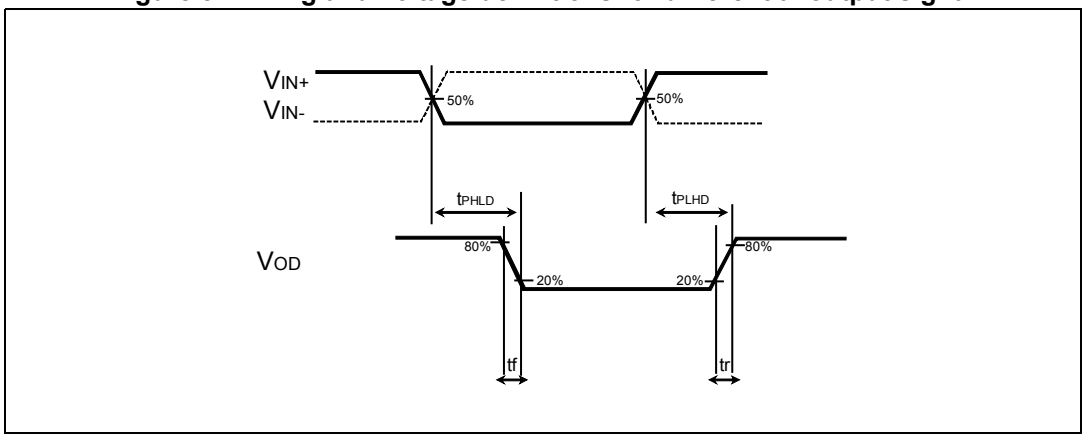


Figure 3. Timing and voltage definitions for differential output signal



1. All input pulses are supplied by a generator with the following characteristics: t_r or t_f ≤1 ns, f = 1 MHz, Z_O = 50 Ω and duty cycle = 50 %.
2. The product is guaranteed with C_L = 10 pF.

Figure 4. MUX switch timings

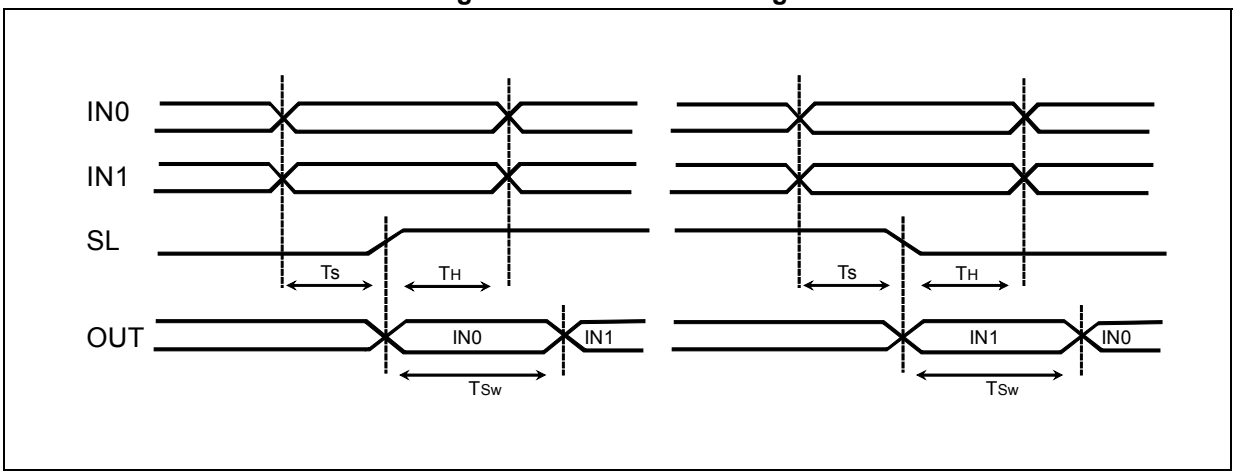
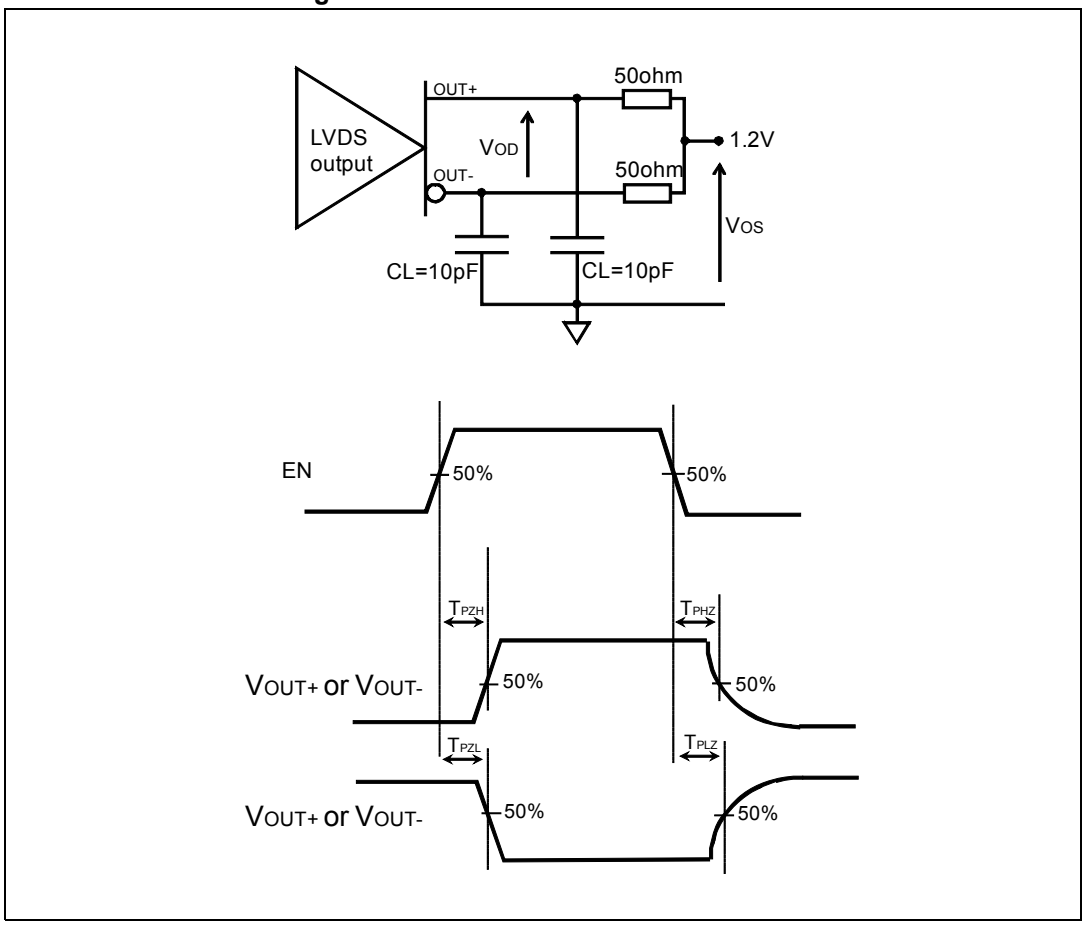


Figure 5. Enable and disable waveforms



1. All input pulses are supplied by a generator with the following characteristics on EN: t_r or $t_f \leq 1$ ns, F = 500 kHz, pulse width = 500 ns.

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.
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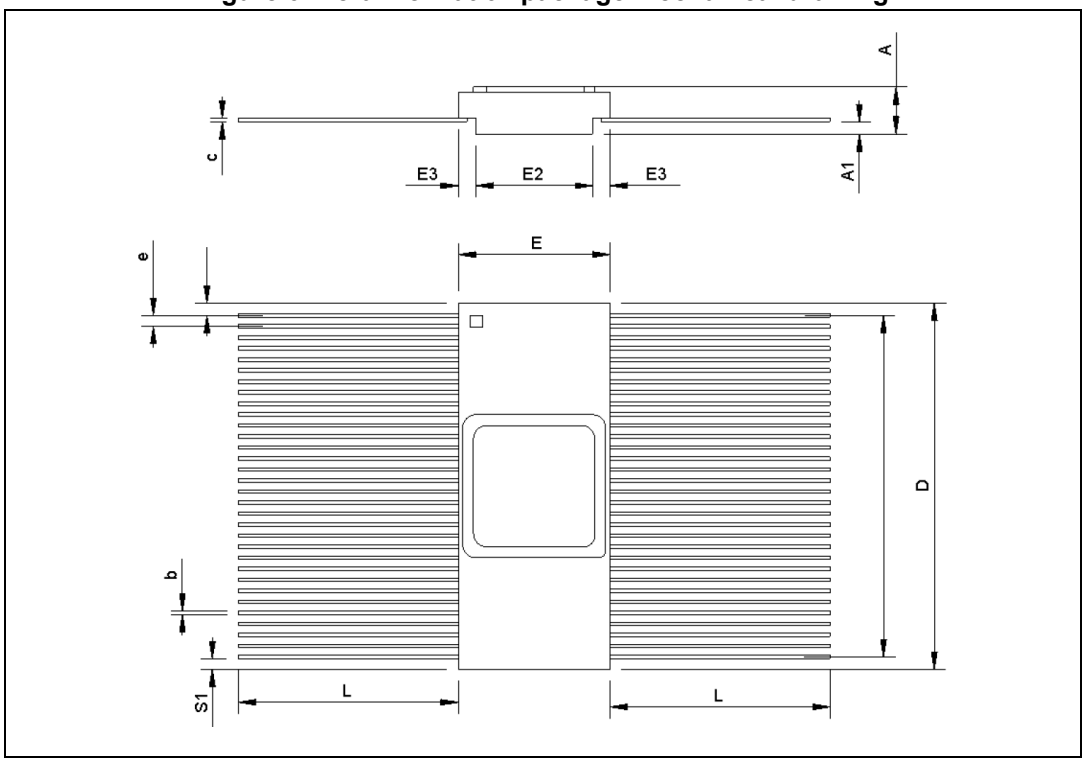
6.1 Ceramic Flat-64 package information

Figure 6. Ceramic Flat 64 package mechanical drawing



1. The upper metallic lid is electrically connected to ground.

Table 8. Ceramic Flat 64 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.41	2.66	2.92	0.095	0.105	0.115
A1	0.33	-	-	0.013	-	-
b	0.18	0.2	0.23	0.007	0.008	0.009
c	0.15	0.2	0.25	0.006	0.008	0.010
D	20.91	21.11	21.31	0.823	0.831	0.839
E	8.64	8.76	8.89	0.340	0.345	0.350
E2	6.57	6.72	6.87	0.259	0.265	0.270
E3	-	1.02	-	-	0.040	-
e	-	0.635	-	-	0.025	-
L	12.45	12.7	12.95	0.49	0.5	0.51
S1	-	0.61	-	-	0.024	-

7 Ordering information

Table 9. Order codes

Order code	Description	Temp. range	Package	Marking(1)	Packing
RHFLVDS228AK1	Engineering model	-55 °C to 125 °C	Ceramic Flat-64	RHFLVDS228AK1	Strip pack
RHFLVDS228AK01V(2)	QML-V flight			TBD	

1. Specific marking only. Complete marking includes the following:
   - SMD pin (on QML-V flight only)
   - ST logo
   - Date code (date the package was sealed) in YYWWA (year, week, and lot index of week)
   - QML logo (Q or V)
   - Country of origin (FR = France).
2. Not yet in full production

Note: Contact your ST sales office for information regarding the specific conditions for products in die form and QML-Q versions.

8 Shipping information

Date code

The date code is structured as follows:

- Engineering model: EM xyywwz
- QML flight model: FM yywwz

Where:

x = 3 (EM only), assembly location Rennes (France)

yy = last two digits of the year

ww = week digits

z = lot index of the week

9 Revision history

Table 10. Document revision history

Date	Revision	Changes
29-Oct-2013	1	Initial release

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