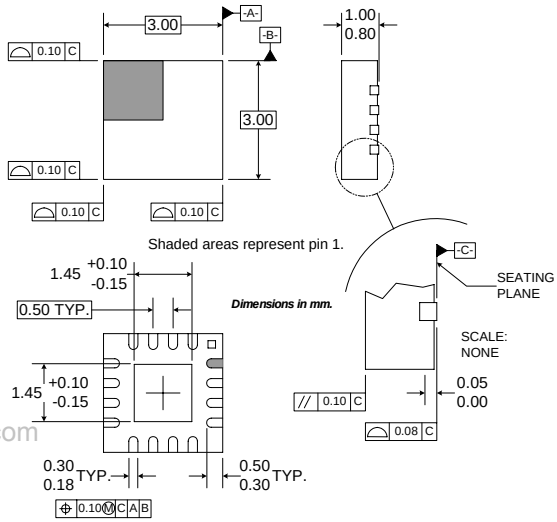
3V 1700MHz LINEAR POWER AMPLIFIER MODULE

Typical Applications

- 3V CDMA Korean-PCS Handset
- 3V CDMA2000/1XRTT K-PCS Handset
- 3V CDMA2000/1X-EV-DO K-PCS Handset
- Spread-Spectrum System

Product Description

The RF3165 is a high-power, high-efficiency linear amplifier module specifically designed for 3V handheld systems. The device is manufactured on an advanced third generation GaAs HBT process, and was designed for use as the final RF amplifier in 3V IS-95/CDMA 2000 1X handheld digital cellular equipment, spread-spectrum systems, and other applications in the 1750MHz to 1780MHz band. The RF3165 has a digital control line for low power applications to lower quiescent current. The RF3165 is assembled in at 16-pin, 3mmx3mm, QFN package.



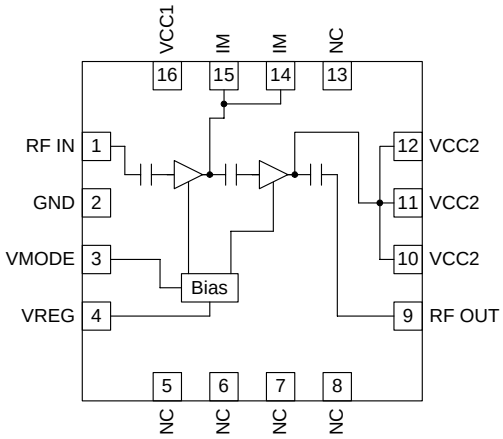
Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS
- ☐ InGaP/HBT
- ☐ GaN HEMT
- ☐ SiGe Bi-CMOS

Package Style: QFN, 16-Pin, 3x3

Features

- Input Internally Matched@50Ω
- Output Internally Matched
- 28dBm Linear Output Power
- 40% Peak Linear Efficiency
- 28dB Linear Gain
- -50dBc ACPR @ 1.25MHz



Functional Block Diagram

Ordering Information

RF3165	3V 1700MHz Linear Power Amplifier Module
RF3165PCBA-410	Fully Assembled Evaluation Board

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage (RF off)	+8.0	V
Supply Voltage (P_{OUT}≤31dBm)	+5.2	V
Control Voltage (V_{REG})	+3.9	V
Input RF Power	+10	dBm
Mode Voltage (V_{MODE})	+3.9	V
Operating Temperature	-30 to +110	℃
Storage Temperature	-40 to +150	℃
Moisture Sensitivity Level IPC/JEDEC J-STD-20	MSL 2 @260	°C

Caution! ESD sensitive device.

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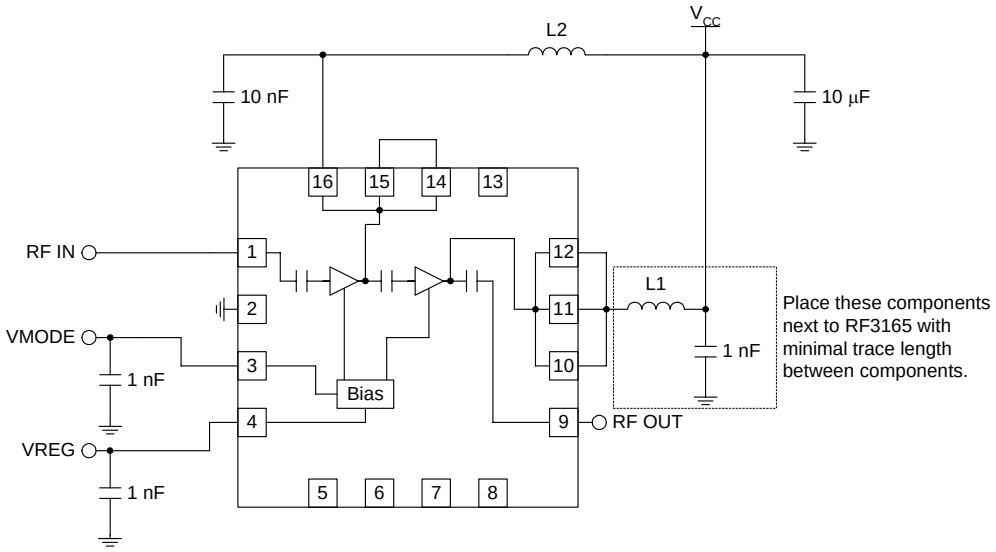
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
High Gain Mode (V_{MODE} Low)					T=25°C Ambient, V_{CC}=3.4V, V_{REG}=2.8V, V_{MODE}=0V, and P_{OUT}=28dBm for all parameters (unless otherwise specified).
Operating Frequency Range	1750		1780	MHz	
Linear Gain	26	28		dB	
Second Harmonics		-35		dBc	
Third Harmonics		-40		dBc	
Maximum Linear Output	28			dBm	
Linear Efficiency		40		%	
Maximum I_{CC}		460		mA	
ACPR @ 1.25MHz		-50		dBc	
ACPR @ 1.98MHz		-55		dBc	
ACPR @ 2.25MHz		-59		dBc	
Input VSWR		2:1			
Output VSWR Stability			6:1		No oscillation>-70dBc
			10:1		No damage
Noise Power		-138		dBm/Hz	At 90MHz offset.
Low Gain Mode (V_{MODE} High)					T=25°C Ambient, V_{CC}=3.4V, V_{REG}=2.8V, V_{MODE}=2.8V, and P_{OUT}=28dBm for all parameters (unless otherwise specified).
Operating Frequency Range	1750		1780	MHz	
Linear Gain		27		dB	
Second Harmonics		-35		dBc	
Third Harmonics		-40		dBc	
Maximum Linear Output	18	28		dBm	
Linear Efficiency		40		%	
ACPR @1.25MHz		-50		dBc	
ACPR @ 1.98MHz		-54		dBc	
ACPR @2.25MHz		-58		dBc	
Maximum I_{CC}		130		mA	P_{OUT}=16dBm
Linear Gain		26		dB	P_{OUT}=16dBm
Input VSWR		2:1			
Output VSWR Stability			6:1		No oscillation>-70dBc
			10:1		No damage

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Power Supply					
Supply Voltage	3.2	3.4	4.2	V	
High Gain Idle Current		65		mA	V_{MODE}=low and V_{REG}=2.8V
Low Gain Idle Current		55		mA	V_{MODE}=high and V_{REG}=2.8V
V_{REG} Current		2		mA	
V_{MODE} Current		250		uA	
RF Turn On/Off Time		1.2	6	uS	
DC Turn On/Off Time		2	40	uS	
Total Current (Power Down)		0.2	5	uA	
V_{REG} Low Voltage (Power Down)	0		0.5	V	
V_{REG} High Voltage (Recommended)	2.75	2.8	2.95	V	
V_{REG} High Voltage (Operational)	2.7		3.0	V	
V_{MODE} Voltage	0		0.5	V	High Gain Mode
V_{MODE} Voltage	2.0		3.0	V	Low Gain Mode

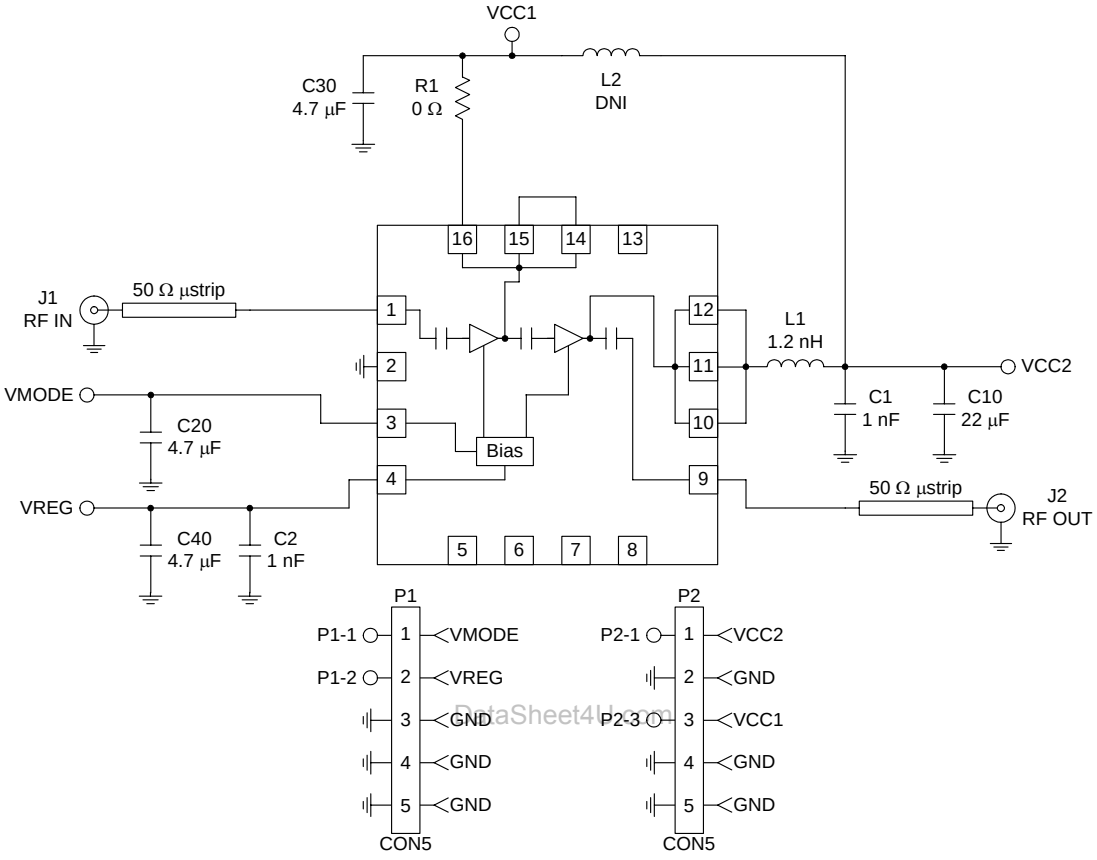
Pin	Function	Description	Interface Schematic
1	RF IN	RF input internally matched to 50Ω. This input is internally AC-coupled.	
2	GND	Ground connection.	
3	VMODE	For nominal operation (High Power mode), V_{MODE} is set LOW. When set HIGH, devices are biased lower to improve efficiency.	
4	VREG	Regulated voltage supply for amplifier bias circuit. In power down mode, both V_{REG} and V_{MODE} need to be LOW (<0.5V).	
5	NC	No connection. Do not connect this pin to any external circuit.	
6	NC	No connection. Do not connect this pin to any external circuit.	
7	NC	No connection. Do not connect this pin to any external circuit.	
8	NC	No connection. Do not connect this pin to any external circuit.	
9	RF OUT	RF output. Internally AC-coupled.	
10	VCC2	Output stage collector supply. Please see the schematic for required external components.	
11	VCC2	Same as pin 10.	
12	VCC2	Same as pin 10.	
13	NC	No connection. Do not connect this pin to any external circuit.	
14	IM	Interstage matching. Connect to pin 15.	
15	IM	Interstage matching. Connect to pin 14.	
16	VCC1	First stage collector supply. A 4.7μF decoupling capacitor is required.	
Pkg Base	GND	Ground connection. The backside of the package should be soldered to a top side ground pad which is connected to the ground plane with multiple vias. The pad should have a short thermal path to the ground plane.	

Application Schematic



L1 = 1.5nH is recommended, but any value between 1.2nH to 2.2nH may be used.
L2 = 6.8nH is recommended, but any value between 4.7nH to 8.2nH may be used.
L2 may not be needed if Pin 16 is not routed directly to Pins 10, 11, and 12.

Evaluation Board Schematic



Electrostatic Discharge Sensitivity

Human Body Model (HBM)
Figure 3 shows the HBM ESD sensitivity level for each pin to ground. The ESD test is in compliance with JESD22-A114.

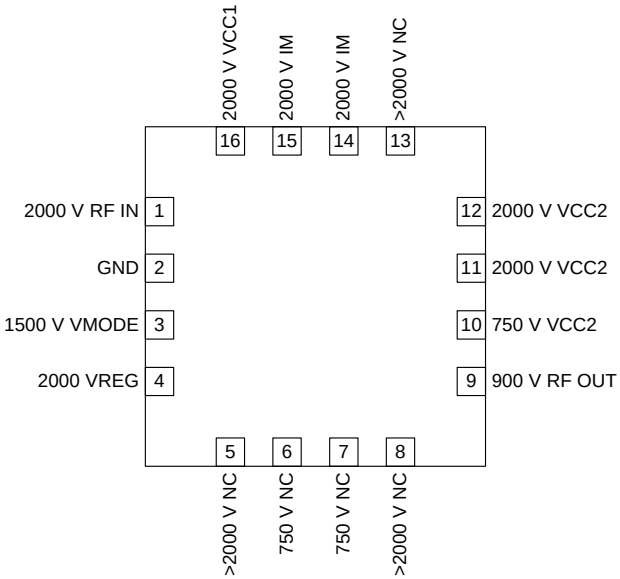


Figure 3. ESD Level - Human Body Model

Machine Model (MM)
Figure 4 shows the MM ESD sensitivity level for each pin to ground. The ESD test is in compliance with JESD22-A115.

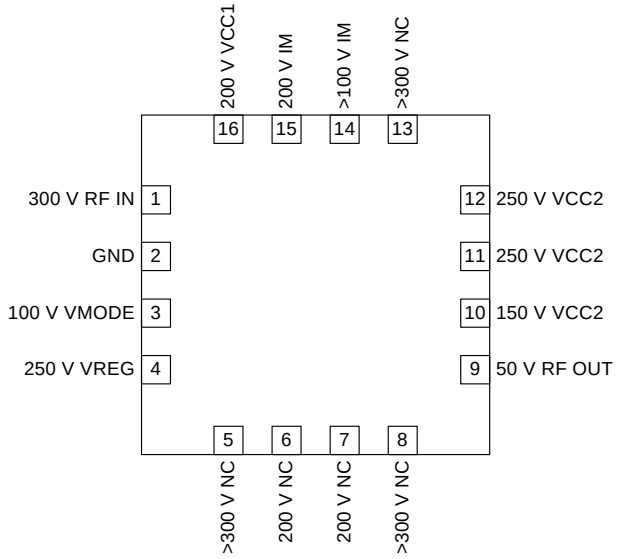


Figure 4. ESD Level - Machine Model

PCB Design Requirements

PCB Surface Finish

The PCB surface finish used for RFMD's qualification process is electroless nickel, immersion gold. Typical thickness is 3μinch to 8μinch gold over 180μinch nickel.

PCB Land Pattern Recommendation

PCB land patterns are based on IPC-SM-782 standards when possible. The pad pattern shown has been developed and tested for optimized assembly at RFMD; however, it may require some modifications to address company specific assembly processes. The PCB land pattern has been developed to accommodate lead and package tolerances.

PCB Metal Land Pattern

A = 0.64 x 0.28 (mm) Typ.
B = 0.28 x 0.64 (mm) Typ.
C = 0.78 x 0.64 (mm)
D = 0.64 x 1.28 (mm)
E = 1.50 (mm) Sq.

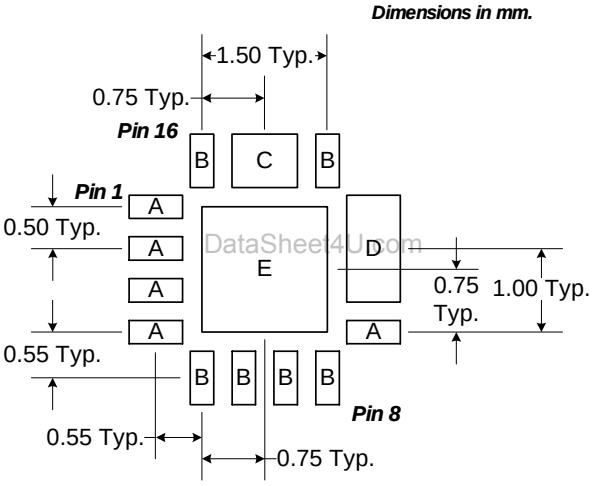


Figure 1. PCB Metal Land Pattern (Top View)

PCB Solder Mask Pattern

Liquid Photo-Imageable (LPI) solder mask is recommended. The solder mask footprint will match what is shown for the PCB metal land pattern with a 2mil to 3mil expansion to accommodate solder mask registration clearance around all pads. The center-grounding pad shall also have a solder mask clearance. Expansion of the pads to create solder mask clearance can be provided in the master data or requested from the PCB fabrication supplier.

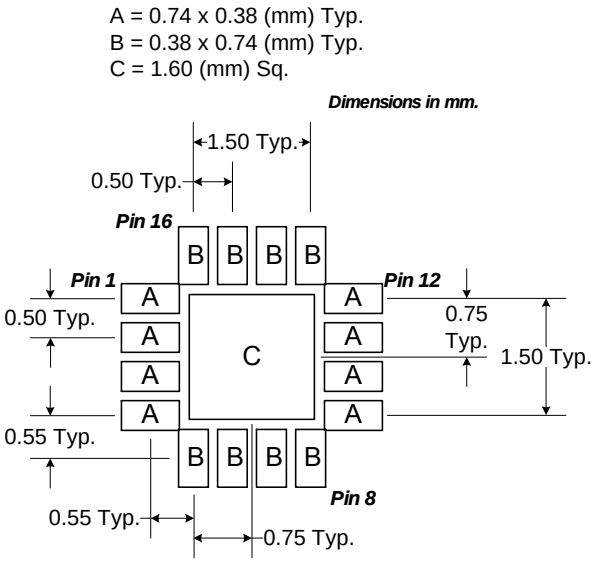


Figure 2. PCB Solder Mask Pattern (Top View)

Thermal Pad and Via Design

The PCB land pattern has been designed with a thermal pad that matches the die paddle size on the bottom of the device.

Thermal vias are required in the PCB layout to effectively conduct heat away from the package. The via pattern has been designed to address thermal, power dissipation and electrical requirements of the device as well as accommodating routing strategies.

The via pattern used for the RFMD qualification is based on thru-hole vias with 0.203mm to 0.330mm finished hole size on a 0.5mm to 1.2mm grid pattern with 0.025mm plating on via walls. If micro vias are used in a design, it is suggested that the quantity of vias be increased by a 4:1 ratio to achieve similar results.