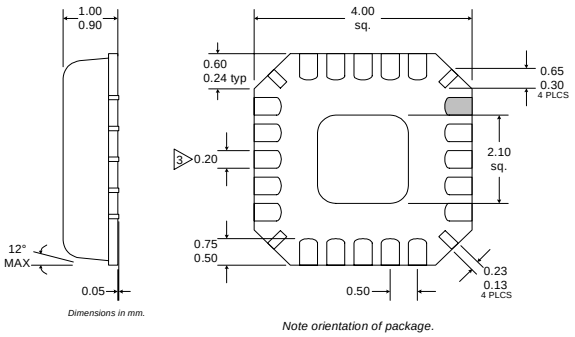
Typical Applications

- W-CDMA Systems

Product Description

The RF2690 is an integrated complete IF AGC amplifier and quadrature demodulator designed for the receive section of W-CDMA applications. It is designed to amplify received IF signals, while providing 70dB of gain control range, a total of 90dB gain, and demodulation to base-band I and Q signals. This circuit is designed as part of RFMD's single mode W-CDMA chipset, which includes the RF9678 as modulator and IF AGC and the RF2638 as upconvertor. The IC is manufactured on an advanced 25GHz F_T Silicon Bi-CMOS process, and is packaged in a 20-pin, 4mmx4mm, leadless chip carrier.

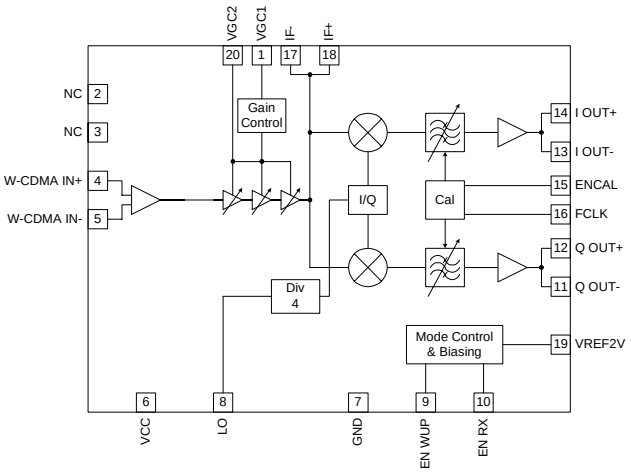


NOTES:
1. Shaded lead is Pin 1.
2. Pin 1 identifier must exist on top surface of package by identification mark or feature on the package body. Exact shape and size is optional.
3. Dimension applies to plated terminal: to be measured between 0.02 mm and 0.25 mm from terminal end.
4. Package Warpage: 0.05 mm max.
5. Die Thickness Allowable: 0.305 mm max.

Package Style: LCC, 20-Pin, 4x4

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ Si Bi-CMOS
- ☐ GaAs HBT
- ☐ SiGe HBT
- ☐ GaAs MESFET
- ☐ Si CMOS



Functional Block Diagram

Features

- Digitally Controlled Power Down Mode
- 2.7V to 3.3V Operation
- Digital LO Quadrature Divide-by-4
- IF AGC Amp with 70dB Gain Control
- 80dB Maximum Voltage Gain

Ordering Information

RF2690	W-CDMA Receive AGC and Demodulator
RF2690 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7628 Thorndike Road
Greensboro, NC 27409, USA

Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to +5	V_{DC}
Power Down Voltage (V_{PD})	-0.5 to V_{CC}+0.7	V_{DC}
Input RF Power	+3	dBm
Ambient Operating Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall Inputs and AGC					Temp=25°C, V_{CC}=3V, Z_{LOAD}=60kΩ diff., LO=760MHz@-10dBm, Z_{SOURCE}=500Ω diff.
IF Frequency		190		MHz	
W-CDMA IF Input Impedance		1200		Ω	Single-ended
		2400		Ω	Balance. An external resistor across the differential input is used to define the input impedance.
LO Frequency		760		MHz	
LO Input Level	-20	-10	0	dBm	
LO Input Impedance		50		Ω	Single-ended.
Maximum Voltage Gain	76	81		dB	Pin-to-Pin voltage gain. Note: 10dB additional voltage gain in input match 50Ω to 500Ω.
Minimum Voltage Gain	5	12	15		
Gain Variation versus V_{CC} and Temperature	-3	±1	+3	dB	
Gain Control Voltage	0.3		2.4	V	Defined with external 10kΩ resistor in series with V_{GC1} pin. Analog gain control.
Input IP3					Blockers at 10MHz and 20MHz offset.
	-52	-48		dBm	Maximum Gain. V_{GC}=2.4V
		-5	0	dBm	Minimum Gain. V_{GC}=0.3V
Noise Figure		5		dB	Maximum Gain. V_{GC}=2.4V
Inband Output 1dB Compression	1.5	2.0		V_{P-P}	Measured differentially.
Compression					Out of band blocker causing 1dB of inband gain compression. Blocker at 5MHz.
		-48		dBm	Maximum Gain. V_{GC}=2.4V
		-17		dBm	Minimum Gain. V_{GC}=0.3V
					Butterworth third order, F_C 2.5M±10%
Baseband 3dB Bandwidth	2.25	2.5	2.75	MHz	Calibrated. F_{CLK}=13MHz
Sideband Suppression			27	dB	A measure of IQ gain match and IQ quadrature accuracy. Measured for baseband frequencies 100kHz to 2.5MHz.
DC Offset			±40	mV	
Baseband External Load		20	60	kΩ	Resistive Load Impedance. Differentially across pins.
			5	pF	Capacitive Load Impedance. To ground.
Output DC Voltage	V_{CC}-1.3	V_{CC}-1.6	V_{CC}-1.9	V	
IQ Amplitude Balance		±0.2	±0.5	dB	V_{GC}=0.3V, P_{IN}=-40dBm
IQ Phase Balance		±2	±5	degree	V_{GC}=0.3V, P_{IN}=-40dBm

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Auto Calibration					
F_{CLK} Input Frequency[1]		13		MHz	
F_{CLK} Signal Level	0.4		1.0	V_{P-P}	
F_{CLK} Pin Input Impedance		20		kΩ	Single-ended.
Calibration Time			200	us	
Current, Auto Cal.			1	mA	Disabled after calibration.
Current, Once Auto Cal Finished			1	uA	
CALEN		TBD			
DC Specifications					
Supply Voltage	2.7	3.0	3.3	V	
Current Consumption					
Power Down		<1		µA	
W-CDMA Warm-up		5		mA	
W-CDMA		8		mA	
Logic Levels					
V_{EN} High Voltage	1.8		V_{CC}	V	
V_{EN} Low Voltage	0		0.5	V	

[1]Bondout option available for 15.36MHz, 18MHz and 19MHz.

Auto Calibration Mode

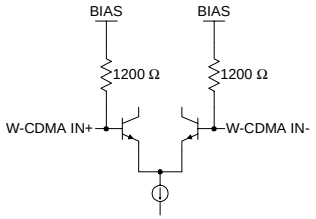
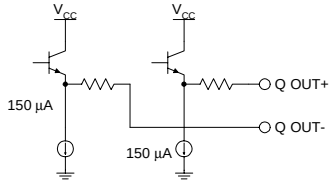
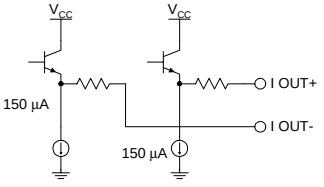
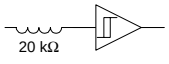
The filters are automatically tuned when the ENCAL pin goes high. The filters are reset to a nominal value whenever the ENCAL pin goes low. The auto calibration circuitry is independent of the EN WUP and the EN RX control pins.
The EN RX and ENCAL pins can be connected together if desired.

Mode Control Truth Table

Mode	EN RX	EN WUP
Power Down	0	X
W-CDMA RX Warm-Up	1	0
W-CDMA RX	1	1

Logic

EN RX	Chip Enable	If EN RX=0, then entire IC is powered down.
EN WUP	Warm-up Enable	If EN WUP=0, then IC is in warm-up mode.

Pin	Function	Description	Interface Schematic
1	VGC1	Analog gain control. Valid control voltage ranges are from 0.5V to 2.5V. These voltages are valid with a 10kΩ resistor in series with GC pin.	
2	NC	Unused. Connect to signal ground in application.	
3	NC	Unused. Connect to signal ground in application.	
4	W-CDMA IN+	W-CDMA balanced input pin. This pin is internally DC-biased and should be DC-blocked if connected to a device with a DC level present. For single-ended input operation, one pin is used as an input and the other W-CDMA input is AC coupled to ground. The balanced input impedance is 2.4kΩ, while the single-ended input impedance is 1.2kΩ.	
5	W-CDMA IN-	Same as pin 4, except complementary input.	See pin 4.
6	VCC	Supply	
7	GND	Connect to ground.	
8	LO	LO input pin. This input is internally DC-biased and should be DC-blocked if connected to a device with DC present. The frequency of the signal applied to this pin is internally divided by a factor of four, hence the LO applied should be four times the frequency of the IF.	
9	EN WUP	Warm-up mode enable. The input LO buffers and divider chains are enabled. When logic “low” (≤0.5V), chip is in warm-up mode. When logic “high” (VCC-0.3V), chip is in W-CDMA RX mode.	
10	EN RX	Chip enable. Power down. When logic “low” (≤0.5V), all circuits are turned off. When logic “high” (VCC-0.3V), all circuits are operating.	
11	Q OUT-	Complementary output to Q OUT+.	
12	Q OUT+	Balanced baseband output of Q mixer. This pin is internally DC-biased and should be DC-blocked externally. The output may be used single-ended by leaving one of the pins unconnected, however half of the output voltage will be lost.	
13	I OUT-	Complementary output to I OUT+.	
14	I OUT+	Balanced baseband output.	
15	ENCAL	Calibration enable.	
16	FCLK	F_{CLK} clock reference for the automatic calibration circuitry.	
17	IF-	Complementary output to IF+.	
18	IF+	IF test point output. This balanced node is pinned out to allow for monitoring of the AGC output signal as it enters the demodulator. During normal operation, this pin and its complementary output should be left floating and not connected.	

Pin	Function	Description	Interface Schematic
19	VREF2V	2V voltage reference decouple (i.e., 10nF to ground).	
20	VGC2	Gain control decouple (i.e., 10nF to ground).	
Pkg Base	Die Flag	Ground.	

Application Notes

Voltage Gain Measurement Set-up

The evaluation board uses a unity voltage gain Op-Amp to simulate the 60kΩ differential load impedance condition for the chip. The 50Ω output impedance of Op-Amp makes the use of a 50Ω spectrum analyzer power measurement possible. The power gain measured will be considered as RAW Gain. The input impedance of the chip is 500Ω differential by adding a parallel 680Ω resistor. The input transformer matches 50Ω to 500Ω and results in 10dB difference between voltage gain and power gain, hence, the voltage gain of the chip is RAW Gain minus 10dB. Because the input transformer loss is 0.8dB, it needs to be added to the gain. Since the Op-Amp has the unity voltage gain, the voltage at the evaluation board output is the same as the voltage at chip I or Q output. Therefore, the voltage gain of the chip with 60kΩ load can be calculated by

Gv=RAW Gain-10+0.8(dB)

Input IP3 Measurement

The input IP3 measurement is based on a two tone inter-modulation test condition from the 3GPP standard, which specifies two tones with offset frequencies at 10MHz and 20MHz. Due to the on-chip baseband filtering, the two tone output is attenuated and cannot be seen. Since the only parameter observable is the IM3 product, the input IP3 then is calculated by

IIP3=Pin+0.5*(Pin+RAW Gain-IM3)

Noise Figure Measurement

The noise figure measurement is based on the noise figure definition NF=N_O-N_I-Gain, where N_O is the output noise density, N_I is the input noise density (-174dBm/Hz when no input signal is applied) and Gain is the RAW Gain. The output noise density N_O is measured at 1MHz offset when no signal input is applied. The NF is calculated by NF=N_O-174dBm/Hz-RAW Gain. Since the I and Q re-combination will provide 3dB extra for signal-to-noise ratio, the actual noise figure is should be reduced by 3dB. In addition, noise figure should be reduced by the input transformer loss of 0.8dB. Therefore, the NF is calculated by

NF=N_O+174-RAW Gain-3-0.8(dB)

1dB Gain Compression Point Voltage at Baseband Output

The device has a relatively constant 1dB gain compression point versus V_{GC}. Gain compression is tested with a CW signal with 60kΩ load differential.

How to Calculate the Power Gain of the Demodulator

In the system analysis for cascaded gain, noise and IP, it is often required to calculate the power gain of the demodulator chip itself in matched load condition. Below is an example on how to determine this power gain value.

For this example, the load impedance is 60kΩ differential, the output AC impedance of the I or Q port is 500Ω, the measured RAW Gain is 95dB.

First, the power gain from the input of the chip to the input of Op-Amp needs to be calculated. Since the voltage at the 50Ω load and the voltage at Op-Amp input are the same, the difference of the power gain across the Op-Amp is the ratio of load impedances. Hence, the power gain to the Op-Amp input is 95dB-10log(60000/50)=95-30=65dB.

Second, the power gain of the demodulator itself with matched load is calculated. The mismatch coefficient a is determined by the mismatch coefficient equation

$$\alpha = 10\log\frac{4R_S R_L}{(R_S + R_L)^2} = 10\log\frac{4 \cdot 500 \cdot 60000}{(500 + 60000)^2} = -15dB$$

Since the power gain to the input of the Op-Amp $G_P' = \alpha G_P$, where G_P is the power gain of demodulator for matched load. Therefore, the demodulator power gain is 65+15=80dB.

AC Coupling in Evaluation Board

The output I and Q baseband signal is AC coupled for evaluation purposes only. The high-pass corner frequency is at $1/(2\pi RC) = 1/(6.28*30k\Omega*100nF) = 56Hz$.

I and Q Output DC Voltage and Its Offset

Although the I and Q output is AC coupled on the evaluation board, in most applications, it would be DC coupled to the ADC input buffer. The DC voltage at the IC output is V_{CC}-1.6V with a possible variation of ±0.3V due to temperature and tolerance. The differential circuit asymmetry would cause common mode DC offset to the extent of ±40mV.

Baseband Filter Calibration Process

The BB (baseband) filter calibration process is same for both WCDMA and GSM/DCS. After calibration is done, the WCDMA mode sets the circuitry to have a 3dB bandwidth of 2.5MHz, the GSM/DCS mode (if the chip has GSM/DCS mode) sets the circuitry to have a 3dB bandwidth of 250kHz.

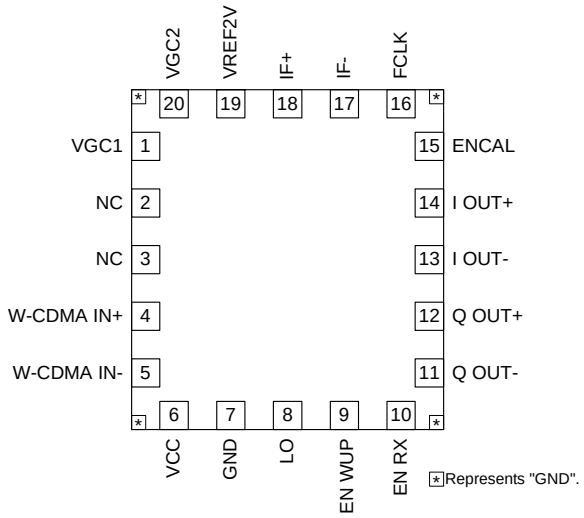
The BB filter in the I and Q path needs to be calculated every time after power down. When the FCLK pin is connected to a signal generator with 0dBm output level at 13.0MHz, a logic high at CALEN pin for 200µs will calibrate the filter to have 2.5MHz bandwidth with 10% accuracy when WCDMA mode is set, or to 250kHz bandwidth with 10% accuracy when GSM mode is set. The calibration is done when the chip is powered on only. Calibration is independent from all other conditions, e.g. the chip enable could be off.

The calibration circuitry consumes 400µA. When the calibration sequence is complete after 200µs, the I_{CC} drops to 0mA.

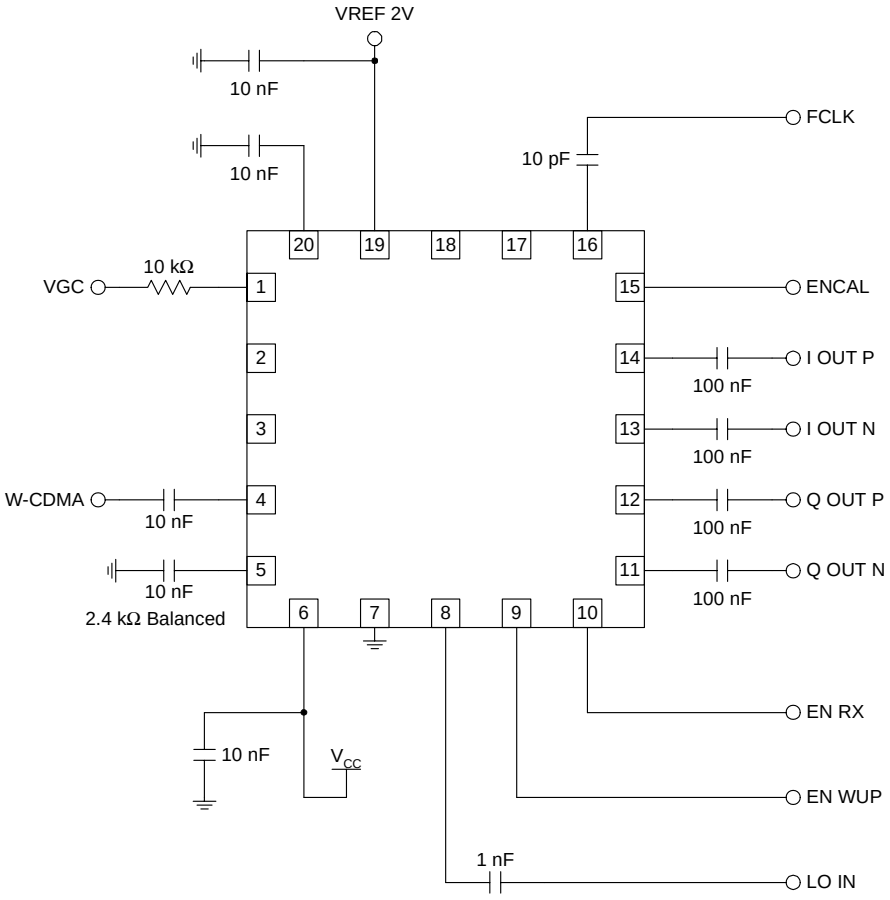
The 3dB bandwidth is defined to be from the reference level at 1MHz for WCDMA and at 50kHz for GSM/DCS. The 3dB bandwidth is independent of V_{GC} and V_{CC}.

The filter can also be calibrated with different clock frequencies from 10MHz to 30MHz to tune the bandwidth over -40% to +60% from its default 3dB bandwidth (2.5MHz for WCDMA and 250kHz for GSM). The 3dB bandwidth is linear with clock frequency.

Pin Out

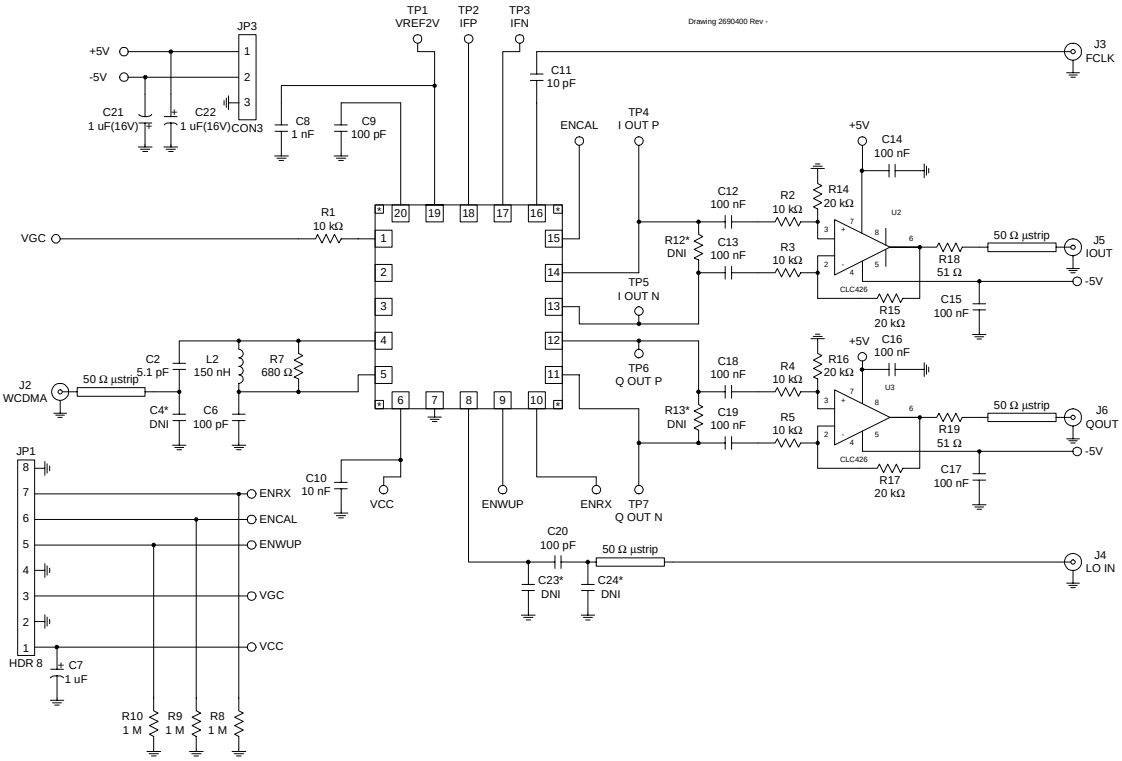

VGC2
VREF2V
IF+
IF-
FCLK
20
19
18
17
16
VGC1 1
NC 2
NC 3
W-CDMA IN+ 4
W-CDMA IN- 5
15 ENCAL
14 I OUT+
13 I OUT-
12 Q OUT+
11 Q OUT-
6
7
8
9
10
VCC
GND
LO
EN WUP
EN RX
*Represents "GND".

Application Schematic

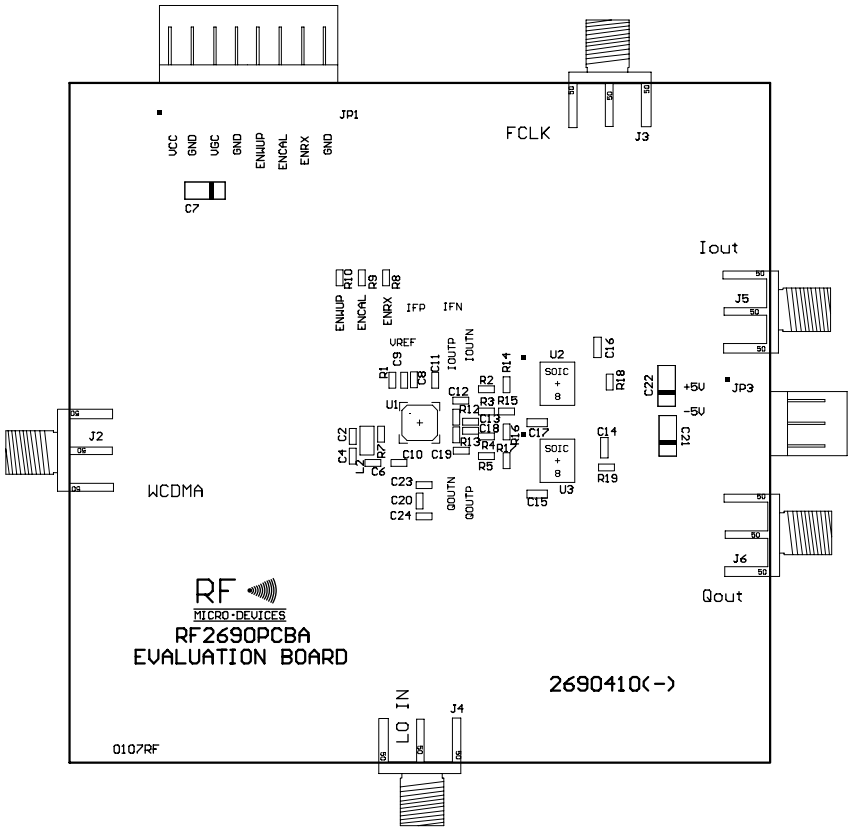


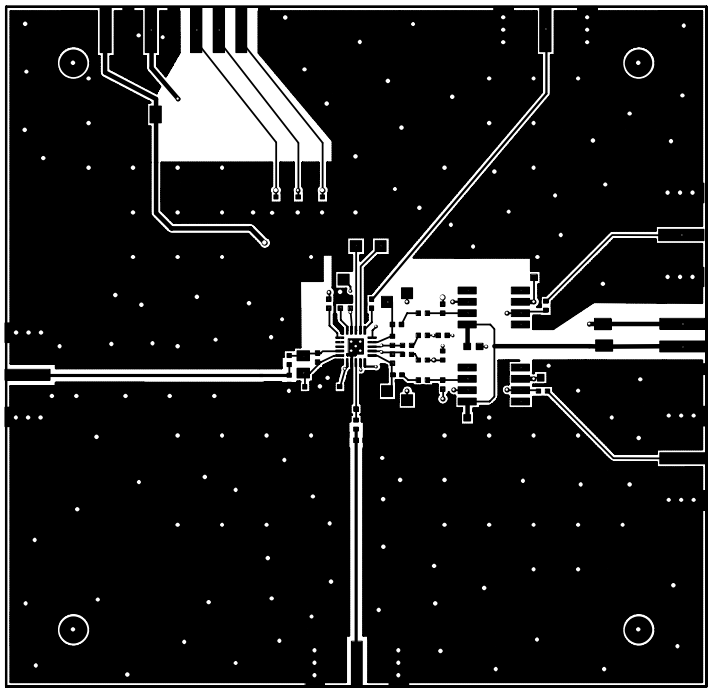
Evaluation Board Schematic

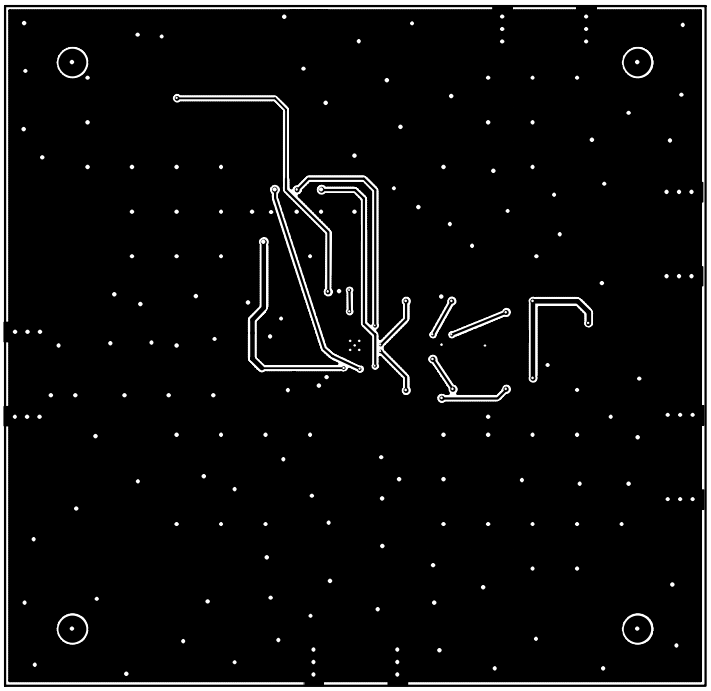
(Download Bill of Materials from www.rfmd.com.)



Evaluation Board Layout
Board Size 3.1” x 3.0”
Board Thickness 0.032”, Board Material FR-4

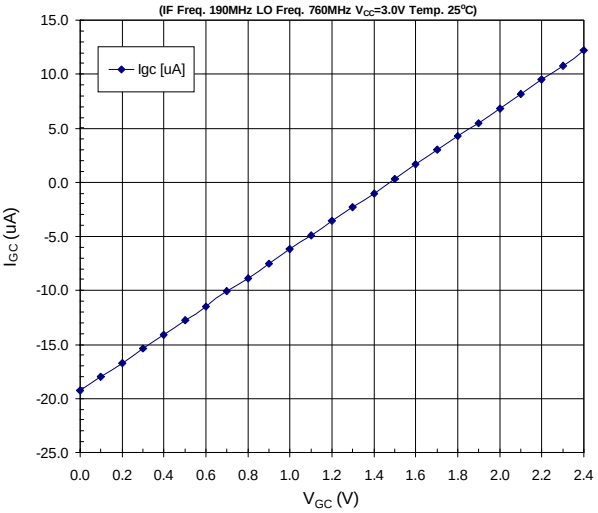






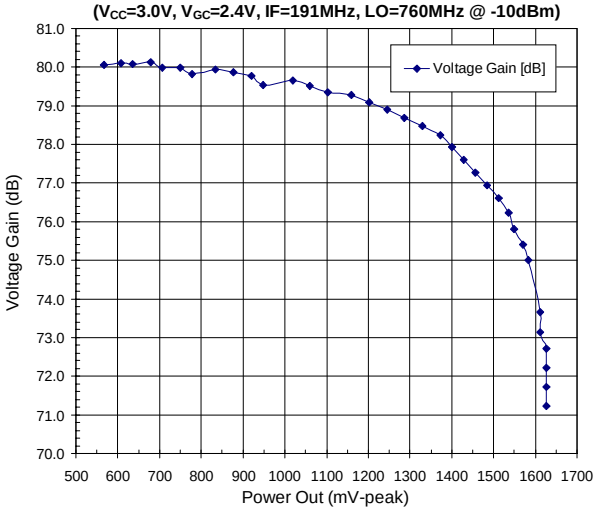
I_{GC} versus V_{GC}

(IF Freq. 190MHz LO Freq. 760MHz V_{CC}=3.0V Temp. 25°C)



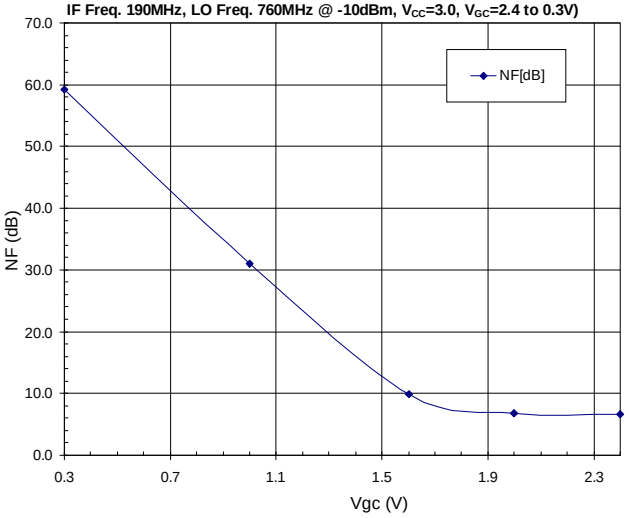
Voltage Gain versus P_{OUT} (1dB Compression)

(V_{CC}=3.0V, V_{GC}=2.4V, IF=191MHz, LO=760MHz @ -10dBm)



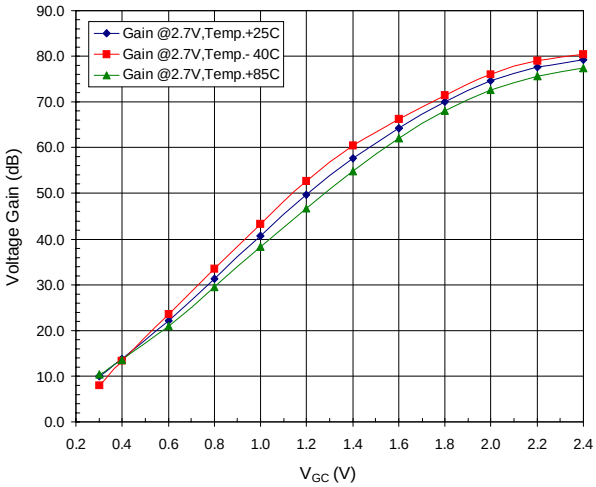
NF versus V_{GC}

IF Freq. 190MHz, LO Freq. 760MHz @ -10dBm, V_{CC}=3.0, V_{GC}=2.4 to 0.3V)



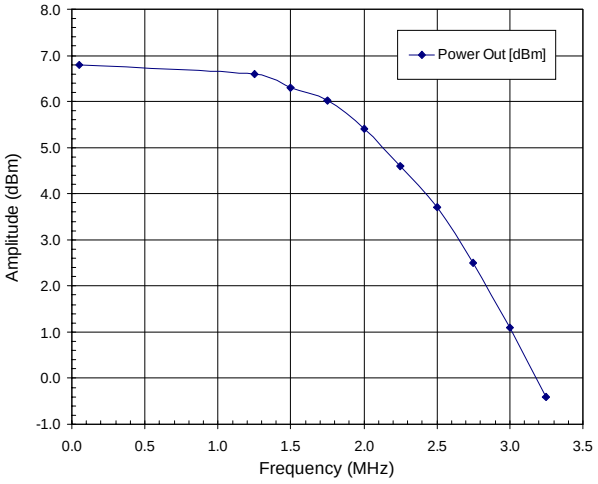
Voltage Gain versus V_{GC} (Temp. +25°C, - 40°C, +85°C)

(IF Freq. 190MHz, LO Freq. 760MHz @ -10dBm,V_{CC}=2.7V,V_{GC}=2.4V to 0.3V)



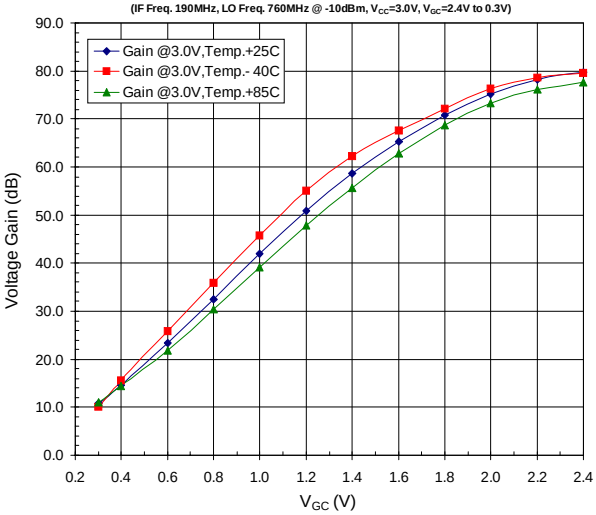
W-CDMA Baseband Filter Response (Calibrated)

(IF=190MHz to 195MHz, LO=760MHz @ -10dBm, V_{CC}=3.0V, V_{GC}=2.4V)



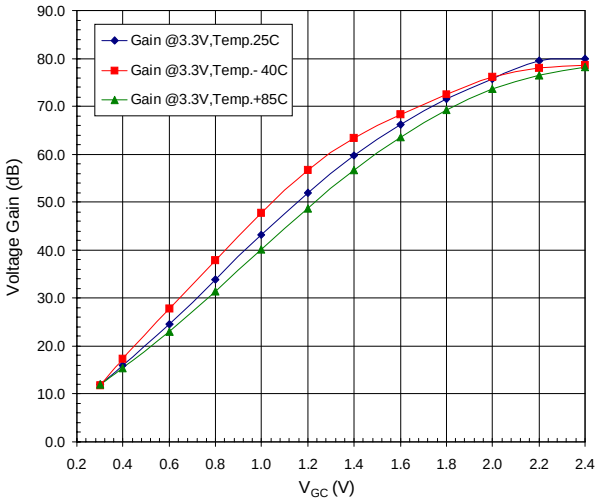
Voltage Gain versus V_{GC} (Temp. +25°C, - 40°C, +85°C)

(IF Freq. 190MHz, LO Freq. 760MHz @ -10dBm, V_{CC}=3.0V, V_{GC}=2.4V to 0.3V)



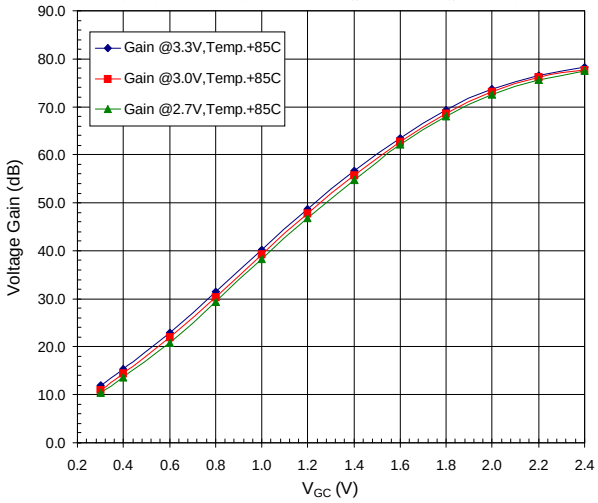
Voltage Gain versus V_{GC} (Temp.+25C, - 40C, +85°C)

IF Freq. 190MHz, LO Freq. 760MHz @ -10dBm, V_{CC}=3.3V, V_{GC}=2.4V to 0.3v)



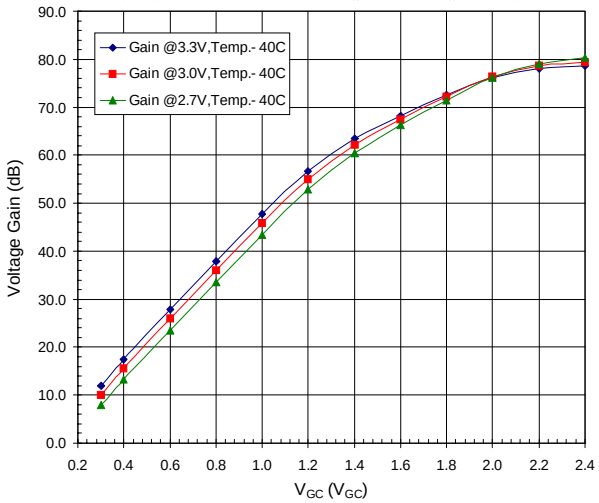
Voltage Gain versus V_{GC} (Temp. +85°C)

(IF Freq. 190MHz, LO Freq. 760MHz @ -10dBm, V_{CC}=3.3V, 3.0V, 2.7V, V_{GC}=2.4V to 0.3V)



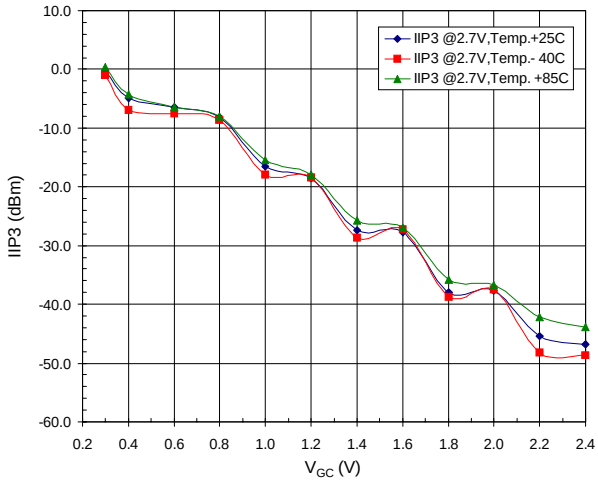
Voltage Gain versus V_{GC} (Temp. -40°C)

(IF Freq. 190MHz, LO Freq. 760MHz @ -10dBm, V_{CC}=3.3V, 3.0V, 2.7V, V_{GC}=2.4V to 0.3V)



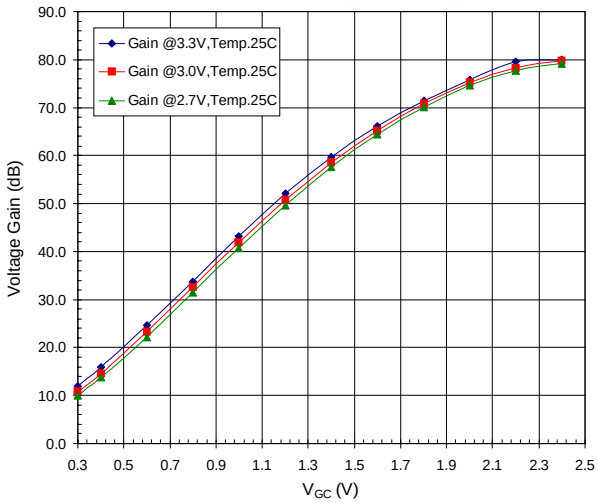
IIP3 versus V_{GC} (Temp. +25°C, - 40°C, +85°C)

(IF Freq.190MHz, LO Freq. 760MHz @ -10dBm, V_{CC}=2.7V, V_{GC}=2.4V to 0.3V)



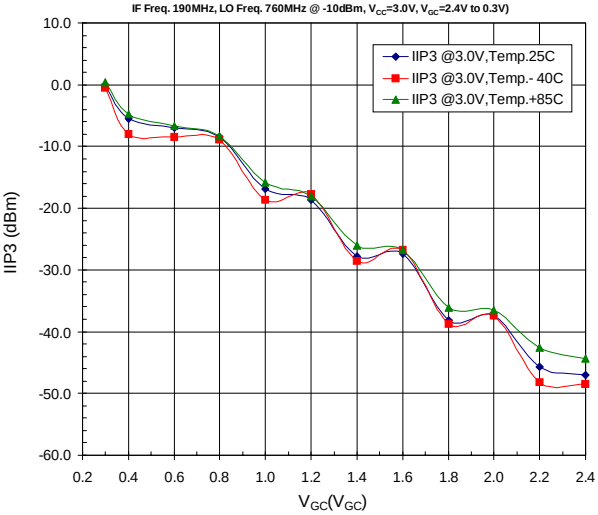
Voltage Gain versus V_{GC} (Temp. 25°C)

(IF Freq. 190MHz, LO Freq. 760MHz @ -10dBm, V_{CC}=3.3V, 3.0V, 2.7V & V_{GC}=2.4V to 0.3V)



IIP3 versus V_{GC} (Temp. +25°C, - 40°C, +85°C)

IF Freq. 190MHz, LO Freq. 760MHz @ -10dBm, V_{CC}=3.0V, V_{GC}=2.4V to 0.3V)



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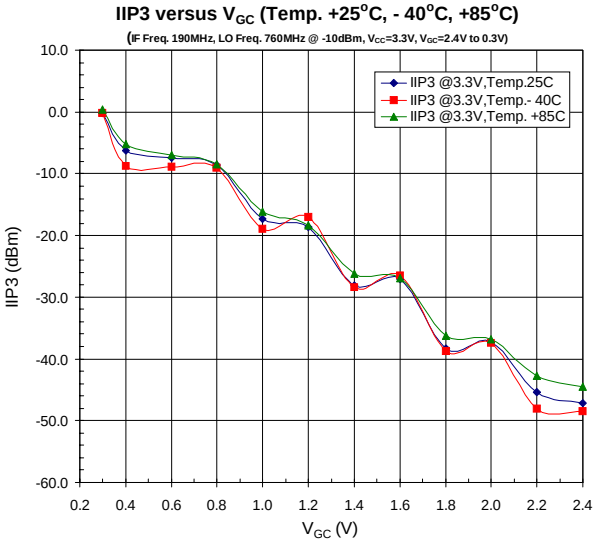
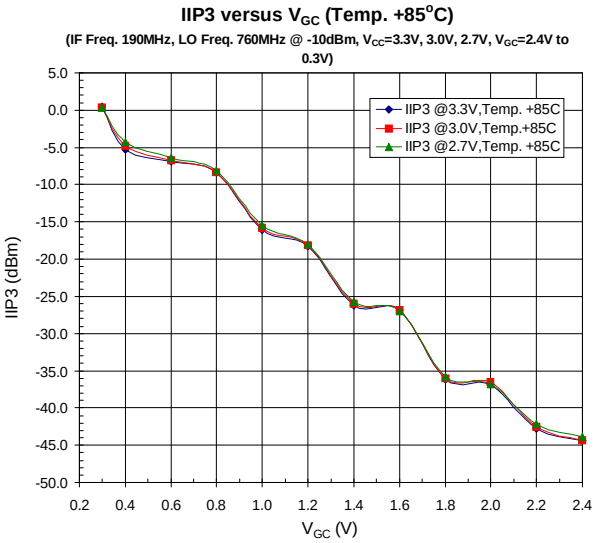
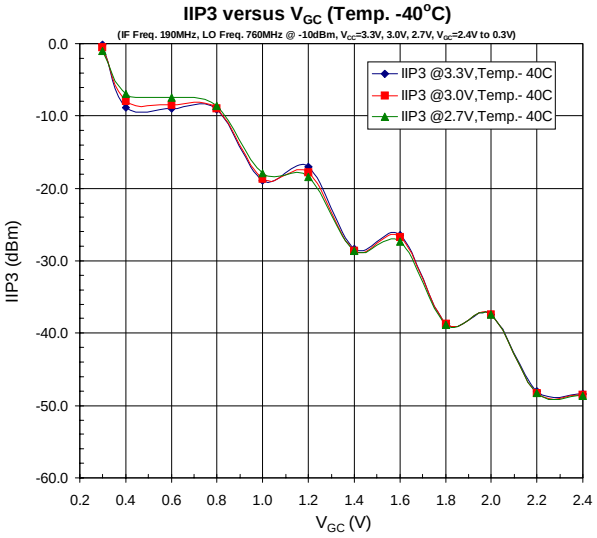
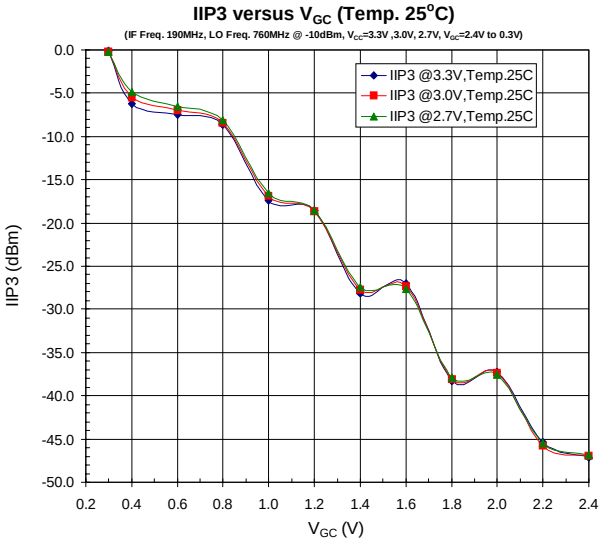
QUADRATURE DEMODULATORS


IIP3 versus V_{GC} (Temp. +25°C, - 40°C, +85°C)
(IF Freq. 190MHz, LO Freq. 760MHz @ -10dBm, V_{CC}=3.3V, V_{GC}=2.4V to 0.3V)
IIP3 @3.3V,Temp.25C
IIP3 @3.3V,Temp.- 40C
IIP3 @3.3V,Temp. +85C
IIP3 (dBm)
V_{GC} (V)


IIP3 versus V_{GC} (Temp. +85°C)
(IF Freq. 190MHz, LO Freq. 760MHz @ -10dBm, V_{CC}=3.3V, 3.0V, 2.7V, V_{GC}=2.4V to 0.3V)
IIP3 @3.3V,Temp. +85C
IIP3 @3.0V,Temp.+85C
IIP3 @2.7V,Temp. +85C
IIP3 (dBm)
V_{GC} (V)


IIP3 versus V_{GC} (Temp. -40°C)
(IF Freq. 190MHz, LO Freq. 760MHz @ -10dBm, V_{CC}=3.3V, 3.0V, 2.7V, V_{GC}=2.4V to 0.3V)
IIP3 @3.3V,Temp.- 40C
IIP3 @3.0V,Temp.- 40C
IIP3 @2.7V,Temp.- 40C
IIP3 (dBm)
V_{GC} (V)


IIP3 versus V_{GC} (Temp. 25°C)
(IF Freq. 190MHz, LO Freq. 760MHz @ -10dBm, V_{CC}=3.3V ,3.0V, 2.7V, V_{GC}=2.4V to 0.3V)
IIP3 @3.3V,Temp.25C
IIP3 @3.0V,Temp.25C
IIP3 @2.7V,Temp.25C
IIP3 (dBm)
V_{GC} (V)