

Preliminary



RF2352

4

GENERAL PURPOSE AMPLIFIERS

Typical Applications

- TDMA/CDMA/FM Driver Amplifier
- Low Noise Transmit Driver Amplifier
- General Purpose Amplification
- Commercial and Consumer Systems

Product Description

The RF2352 is a low noise driver amplifier for 900MHz CDMA/AMPS applications. The device is designed for operation from 2.7V to 3.6V, and features selectable high and low gain modes. In high gain mode, the device will provide about 19dB of gain, and the linearity and current drain are set with an external resistor, allowing the designer to select the optimum performance for a given application. In the low gain, or "bypass" mode, the gain is controlled by an external attenuator network, and the device draws essentially no current. The part is fabricated using a high performance silicon BiCMOS process, and is packaged in a 4mmx4mm, 16-pin, leadless chip carrier.





Features

- Low Noise and High Intercept Point
- Power Down Control
- Gain Control
- Single 2.7V to 3.6V Power Supply
- Extremely Small MLF16 Package

Ordering Information RF2352 **3V CDMA Driver Amplifier** RF2352 PCBA Fully Assembled Evaluation Board RF Micro Devices, Inc. Tel (336) 664 1233 7628 Thorndike Road Fax (336) 664 0454 Greensboro, NC 27409, USA http://www.rfmd.com

16 15 14 13 RF IN 2 12 **RF OUT** NC 3 11 VCC VREF 4 10 ATT OUT2 5 6 7 8 9 Б ≧ S GND ATT OUT1 ATT

Optimum Technology Matching® Applied

GaAs HBT

SiGe HBT

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GND

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RF GND

GaAs MESFET

Si CMOS

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Si BJT

Si Bi-CMOS

Functional Block Diagram

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to +4.5	V _{DC}
Input RF Level	0	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C



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Parameter	Specification	Unit	Condition			
Parameter	Min.	Тур.	Max.	Unit	Condition	
Overall					V _{CC} =3.0V, T=25°C, External Matching Components Required.	
High Gain Mode					V _{PD} =2.8V, P _{OUT} =+4dBm, I _{CC} =15mA	
Gain	18	20	22	dB	At 824MHz	
Noise Figure		1.9	2.9	dB		
Input VSWR		1.3	1.5			
Output VSWR		1.6	1.8			
Adjacent Channel Power Rejection (ACPR1)	57	60		dBc	900kHz offset	
Alternate Channel Power Rejection (ACPR2)	78	80		dBc	1.98MHz offset	
Gain	17	19	21	dB	At 874MHz	
Noise Figure		2.0	3.0	dB		
Input VSWR		1.6	1.8			
Output VSWR		1.5	1.7			
Adjacent Channel Power Rejection (ACPR1)	58	60		dBc	900kHz offset	
Alternate Channel Power Rejection (ACPR2)	76	77		dBc	1.98MHz offset	
Gain	16.5	18.5	20.5	dB	At 925MHz	
Noise Figure		2.2	3.2	dB		
Input VSWR		1.8	2.0			
Output VSWR		1.4	1.6			
Adjacent Channel Power Rejection (ACPR1)	57	60		dBc	900kHz offset	
Alternate Channel Power Rejection (ACPR2)	76	77		dBc	1.98MHz offset	
Bypass (Low Gain) Mode					V _{PD} =0V, Pins 6 and 8 shorted.	
Gain		-4.2		dB	At 824MHz	
Noise Figure		4.2		dB		
Input VSWR		1.2	1.4			
Output VSWR		1.4	1.6			
Gain		-3.7		dB	At 874MHz	
Noise Figure		3.7		dB		
Input VSWR		1.4	1.6			
Output VSWR		1.3	1.5			
Gain		-4.7	_	dB	At 925MHz	
Noise Figure		4.7		dB		
Input VSWR		1.5	1.7			
Output VSWR		1.4	1.6			
Power Supply						
Power Supply Range (V _{CC})	2.7	3.0	3.6	V		
Current Drain (I _{CC})		15.0	0.0	mA	V _{PD} =2.8V (High Gain Mode)	
		13.0	10			
Current Drain (I _{CC})	ļ		10	μA	V _{PD} =0V (Bypass Mode)	

4

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Pin	Function	Description	Interface Schematic
1	GND	Ground connection. For best performance, keep traces physically short and connect immediately to ground plane.	
2	RF IN	RF input pin. It is DC-coupled and looks like 50 Ω from 824MHz to 925MHz.	RF OUT Bias RF IN O
3	NC	Not connected.	
4	VREF	Provides the bias voltage for controlling the RF amplifier current drain. This pin is typically connected through a resistor to an external regulated power supply. It may be connected to the same power supply as the VCC pin. However, if more bias control is desired, it may be connected to a separate supply. With a series external resistor of 1500Ω and power supply of 3V applied, the amplifier current drain should be around 14 mA. By increasing the resistor, the amplifier current drain may be dropped. Conversely, by decreasing the resistor, the amplifier current may be increased to a maximum of 30 mA.	VREF
5	PD	Power down function. When 0V to 0.5V is applied, the device is in Bypass Mode: the amplifier is shut off and the MOSFET switches are activated. There is no DC current dissipation in this state. When 1.5V to 3V is applied, the device is switched to High Gain Mode: the amplifier is activated and the MOSFET switches are opened. This is the normal operating mode.	
6	ATT OUT1	Output of the first MOSFET switch. DC-coupled. When the PD pin is grounded (Bypass Mode), the MOSFET switches are shorted, sending any signals at the RF IN pin through the first MOSFET and off the chip. In cases where minimum RF attenuation is desired, this pin should be shorted with 50Ω microstrip to the ATT IN pin. This setup will yield approximately 4dB of insertion loss. If more attenuation is desired, a resistive pad between the ATT OUT1 and ATT IN pins can be added to the PC board.	
7	NC	Not connected.	
8	ATT IN	Input to the second MOSFET switch. DC-coupled. When the PD pin is grounded (Bypass Mode), the MOSFET switches are shorted. See the ATT OUT1 pin description for setup options.	
9	GND	Ground connection. For best performance, keep traces physically short and connect immediately to ground plane.	
10	ATT OUT2	Output of the second MOSFET switch. DC-coupled. When the PD pin is grounded (Bypass Mode), the MOSFET switches are shorted. This pin should be shorted with 50Ω microstrip to the amplifier load.	
11	VCC	Provides the power supply to the logic circuitry on the IC.	
12	RF OUT	Amplifier output pin. An open collector output that needs VCC applied to it through an inductor. Typically, a shunt inductor, series capacitor matching network is used to provide a 50Ω output match.	
13	NC	Not connected.	
14	NC	Not connected.	
15	RF GND	Amplifier ground. For best performance, keep traces physically short and connect immediately to ground plane.	
16	NC	Not connected.	
Pkg Base	GND	Ground connection for die flag. The backside of the package should be soldered to a top side ground pad which is connected to the ground plane with multiple vias.	

Application Schematic



Package base serves as die flag ground. The vias connecting the backside of the board should be large in diameter to allow for easier soldering. Evaluation Board Layout Board Size 2.0" x 2.0" Board Thickness 0.031"; Board Material FR-4





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4

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