RF2161

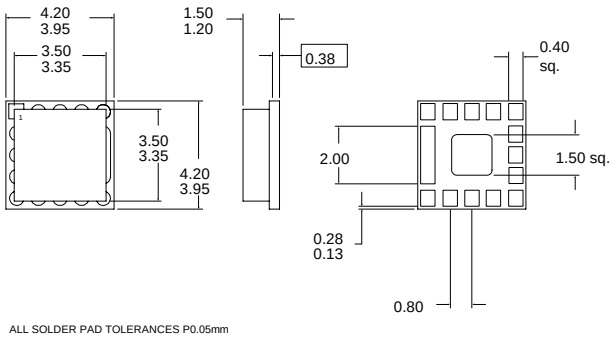
3V W-CDMA POWER 1900MHZ
3V LINEAR POWER AMPLIFIER

Typical Applications

- 3V 1850-1910 CDMA-2000 Handsets
- 3V 1920-1980 W-CDMA Handsets
- Spread Spectrum Systems
- Commercial and Consumer Systems
- Portable Battery-Powered Equipment

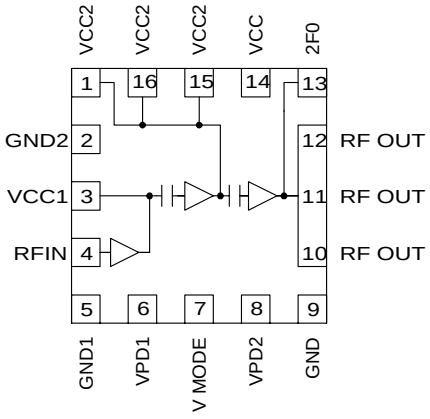
Product Description

The RF2161 is a high-power, high-efficiency linear amplifier IC targeting 3V handheld systems. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as the final RF amplifier in 3V CDMA-2000 and W-CDMA handsets, spread spectrum systems, and other applications in the 1920MHz to 1980MHz band. The device is self-contained with 50Ω input and the output can be easily matched to obtain optimum power, efficiency, and linearity characteristics over all recommended supply voltages.



Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Package Style: MP16KO1A

Features

- Single 3V Supply
- 27dBm Linear Output Power
- 30dB Linear Gain
- 35% Linear Efficiency
- On-board Power Down Mode

Ordering Information

RF2161	3V W-CDMA Power 1900MHZ 3V Linear Power Amplifier
RF2161 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
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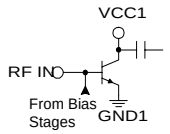
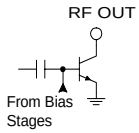
http://www.rfmd.com

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage (RF off)	+8.0	V_{DC}
Supply Voltage (P_{OUT}≤31dBm)	+5.0	V_{DC}
Mode Voltage (V_{MODE})	+3.0	V_{DC}
Control Voltage (V_{PD})	+3.0	V_{DC}
Input RF Power	+6	dBm
Operating Case Temperature	-30 to +100	°C
Storage Temperature	-30 to +150	°C

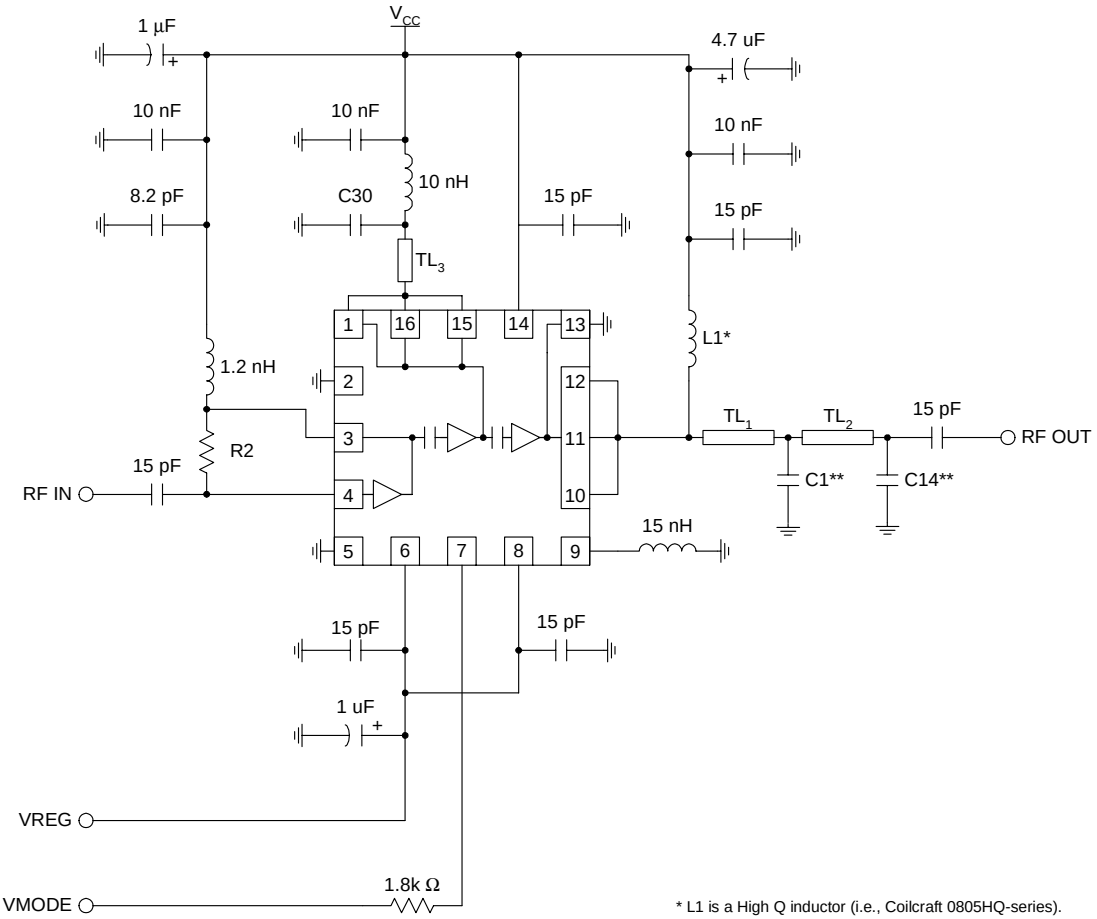
Caution! ESD sensitive device.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=3.4V unless otherwise specified
Usable Frequency Range	1850		2000	MHz	
Typical Frequency Range		1850 to 1910 1920 to 1980		MHz	
Linear Gain	28 26	30 28		dB dB	Mode=Low Mode=High
Second Harmonic (including second harmonic trap)		-35		dBc	
Third Harmonic		-40		dBc	
Fourth Harmonic		-45		dBc	
Maximum Linear Output Power (W-CDMA Modulation)	27			dBm	
Total Linear Efficiency	30	35		%	V_{MODE} High, P_{OUT}=27dBm
Adjacent Channel Power Rejection@5MHz		-40	-38	dBc	P_{OUT}=27dBm, W-CDMA Modulation 3G PP 3.2 03-00 DPCCH+1DPDCH
Adjacent Channel Power Rejection@10MHz		-50	-48	dBc	P_{OUT}=27dBm, W-CDMA Modulation 3G PP 3.2 03-00 DPCCH+1DPDCH
Noise Power		-137		dBm/Hz	P_{OUT}=+27dBm, Rx Band 2110MHz to 2170MHz
Maximum Linear Output Power (W-CDMA Modulation)		26		dBm	V_{CC}=3.0V
Total Linear Efficiency		35		%	
Input VSWR		< 2:1			
Output Load VSWR			5:1		No oscillations
Power Supply					
Power Supply Voltage	3.0	3.4	5.0	V	
Idle Current		120		mA	MODE = high
V_{PD} Current		13		mA	Total pins 6 and 8, V_{PD} = 2.8 V
Total Current (Power down)		10	10	µA	V_{PD} = low
V_{PD} "Low" Voltage		0	0.2	V	
V_{PD} "High" Voltage	2.7	2.8	2.9	V	
MODE "High" Voltage	2.5	2.8			
MODE "Low" Voltage		0	0.5		

Pin	Function	Description	Interface Schematic
1	VCC2	Power supply for second stage and interstage match. Pins 1, 15 and 16 should be connected by a common trace where the pins contact the printed circuit board.	
2	GND2	Ground for second stage. For best performance, keep traces physically short and connect immediately to ground plane. This ground should be isolated from the backside ground contact.	
3	VCC1	Power supply for first stage and interstage match. V_{CC} should be fed through a 1.2nH inductor terminated with a 8.2pF capacitor on the supply side. The inductor should be as close to the pin as possible.	See pin 4.
4	RF IN	RF input. An external series capacitor is required as a DC block. The input match can be improved to <2:1 by using a series capacitor and shunt inductor.	
5	GND1	Ground for first stage. For best performance, keep traces physically short and connect immediately to ground plane. This ground should be isolated from the backside ground contact.	See pin 4.
6	VPD1	Power Down control for first and second stages. When this pin is “low”, all first and second stage circuits are shut off. When this pin is 2.8V, all first and second stage circuits operate normally. V_{PD1} requires a regulated 2.8V for the amplifier to operate properly over all specified temperature and voltage ranges. A dropping resistor from a higher regulated voltage may be used to provide the required 2.8V.	
7	VMODE	V_{MODE} adjusts the bias to the 2nd and 3rd stages. For full power operation, MODE is set low. When operating in a lower output power mode (<+25dBm) this pin is set high to reduce bias current by up to 50%. An external series resistor is optional to limit the amount of current required. At low temperature (-30°C), it is recommended to set V_{MODE} low to maintain correct operation.	
8	VPD2	Power Down control for third stage. When this pin is “low”, all and third stage circuits are shut off. When this pin is 2.8V, all and third stage circuits operate normally. V_{PD} requires a regulated 2.8V for the amplifier to operate properly over all specified temperature and voltage ranges. A dropping resistor from a higher regulated voltage may be used to provide the required 2.8V. A 15pF high frequency bypass capacitor is recommended.	
9	GND	For best performance, keep traces physically short and connect immediately to ground plane. This ground should be isolated from the backside ground contact.	
10	RF OUT	RF output and power supply for final stage. This is the unmatched collector output of the third stage. A DC block is required following the matching components. The biasing may be provided via a parallel L-C set for resonance at the operating frequency of 1920MHz to 1980MHz. It is important to select an inductor with very low DC resistance with a 1A current rating. Alternatively, shunt microstrip techniques are also applicable and provide very low DC resistance. Low frequency bypassing is required for stability.	
11	RF OUT	Same as pin 10.	See pin 10.
12	RF OUT	Same as pin 10.	See pin 10.
13	2FO	Second harmonic trap. Keep traces physically short and connect immediately to ground plane. This ground should be isolated from backside ground contact.	
14	VCC	Supply for bias reference and control circuits. High frequency bypassing may be necessary.	
15	VCC2	Same as Pin 1.	
16	VCC2	Same as Pin 1.	

Pin	Function	Description	Interface Schematic
Pkg Base	**GND**	Ground connection. The backside of the package should be soldered to a top side ground pad which is connected to the ground plane with multiple vias. The pad should have a short thermal path to the ground plane.	

Application Schematic
W-CDMA (1920MHz to 1980MHz)

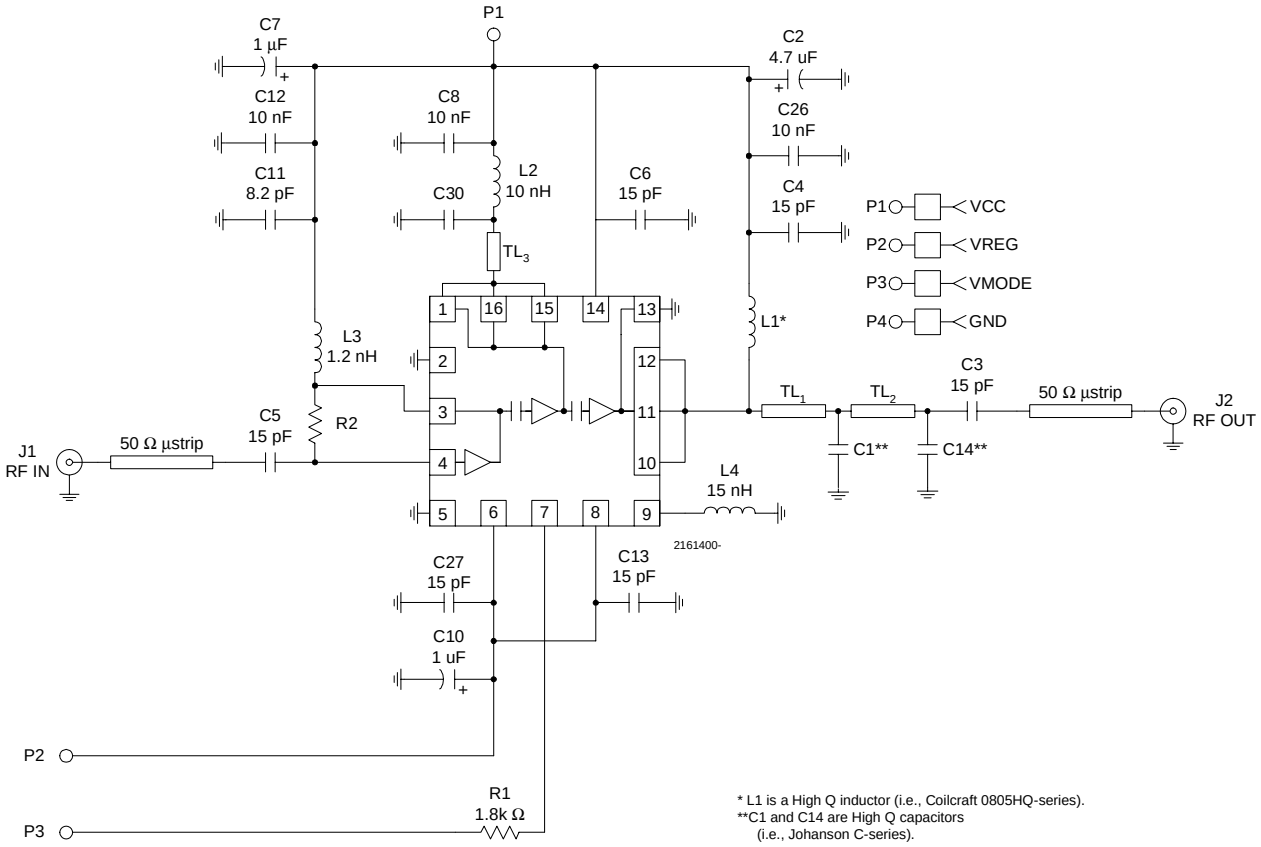


* L1 is a High Q inductor (i.e., Coilcraft 0805HQ-series).
**C1 and C14 are High Q capacitors
(i.e., Johanson C-series).

Board	R2 (Ω)	C30 (pF)	C1 (pF)	L1 (nH)	C14 (pF)
WCDMA	150	8.2	4.7	16	2.2

Transmission Line Length	TL_1	TL_2	TL_3
WCDMA	0.044"	0.140"	0.022"

Evaluation Board Schematic
W-CDMA (1920MHz to 1980MHz)



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Evaluation Board Layout
Board Size 2.00” x 2.00”

Board Thickness 0.028”, Board Material FR-4, Multi-Layer, Ground Plane at 0.014”