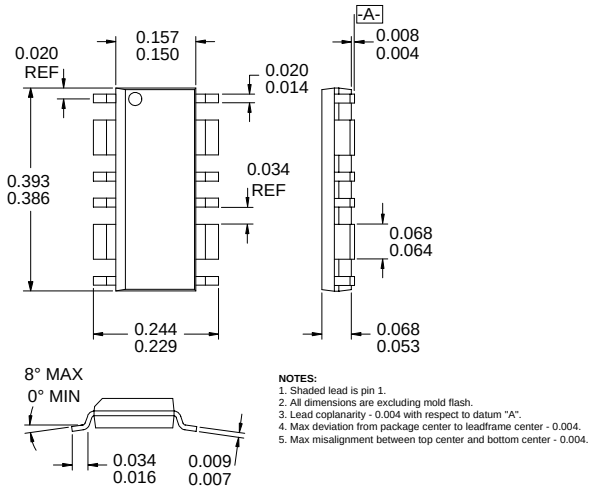
Typical Applications

- 4.8V CDMA PCS Handsets
- 4.8V TDMA PCS Handsets
- 4.8V PACS PCS Handsets
- Driver Amplifier in Cellular Base Stations
- Portable Battery-Powered Equipment

Product Description

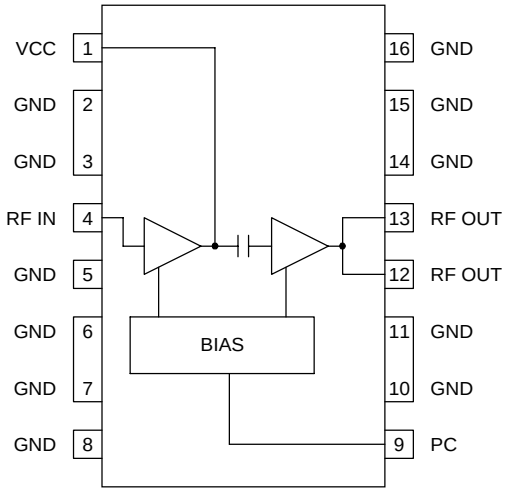
The RF2146 is a high-power, high-efficiency linear amplifier IC. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as the final RF amplifier in 4-cell CDMA handheld digital cellular equipment, spread-spectrum systems, and other applications in the 1500MHz to 2000MHz band. The device is self-contained with 50Ω input and the output can be easily matched to obtain optimum power, efficiency, and linearity characteristics.



Package Style: CJ2BAT0

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- Single 4V to 6.5V Supply
- 28.5dBm Linear Output Power
- 18.5dB Gain With Analog Gain Control
- 37% Linear Efficiency
- On-board Power Down Mode
- 1500MHz to 2000MHz Operation

Ordering Information

RF2146	PCS Linear Power Amplifier
RF2146 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage (No RF)	-0.5 to +8.0	V_{DC}
Supply Voltage (P_{OUT}<30dBm)	-0.5 to +7.5	V_{DC}
Power Control Voltage (V_{PC})	-0.5 to +5.0 or V_{CC}	V
DC Supply Current	500	mA
Input RF Power	+15	dBm
Output Load VSWR	10:1	
Ambient Operating Temperature	-30 to +90	℃
Storage Temperature	-40 to +150	℃

Caution! ESD sensitive device.

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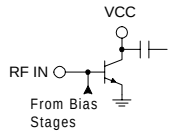
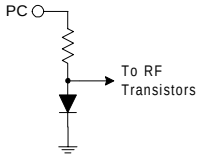
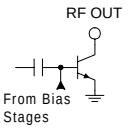
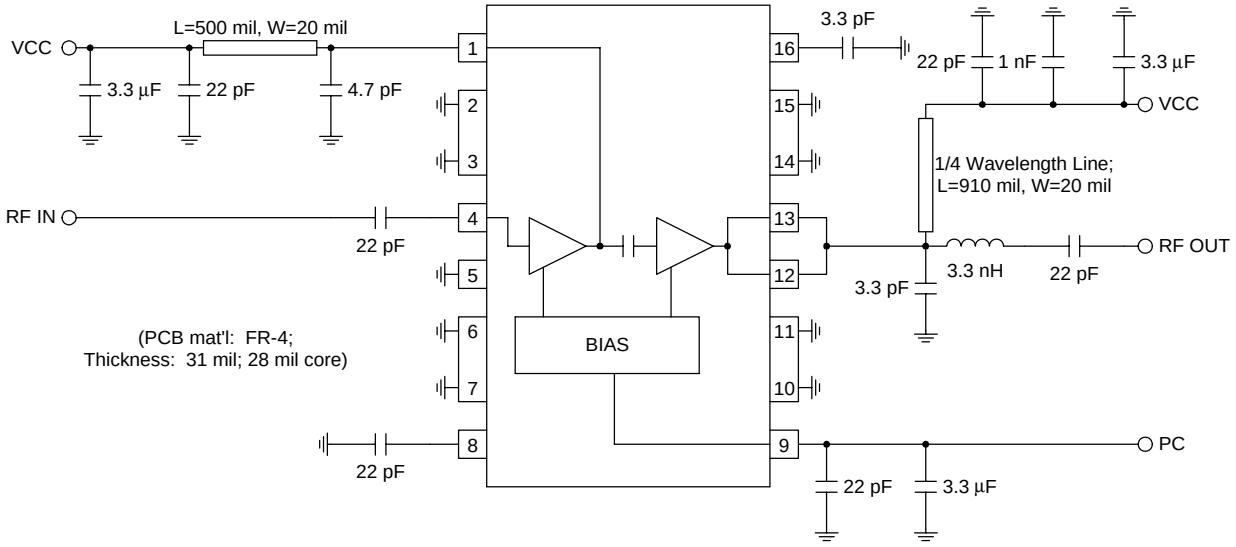
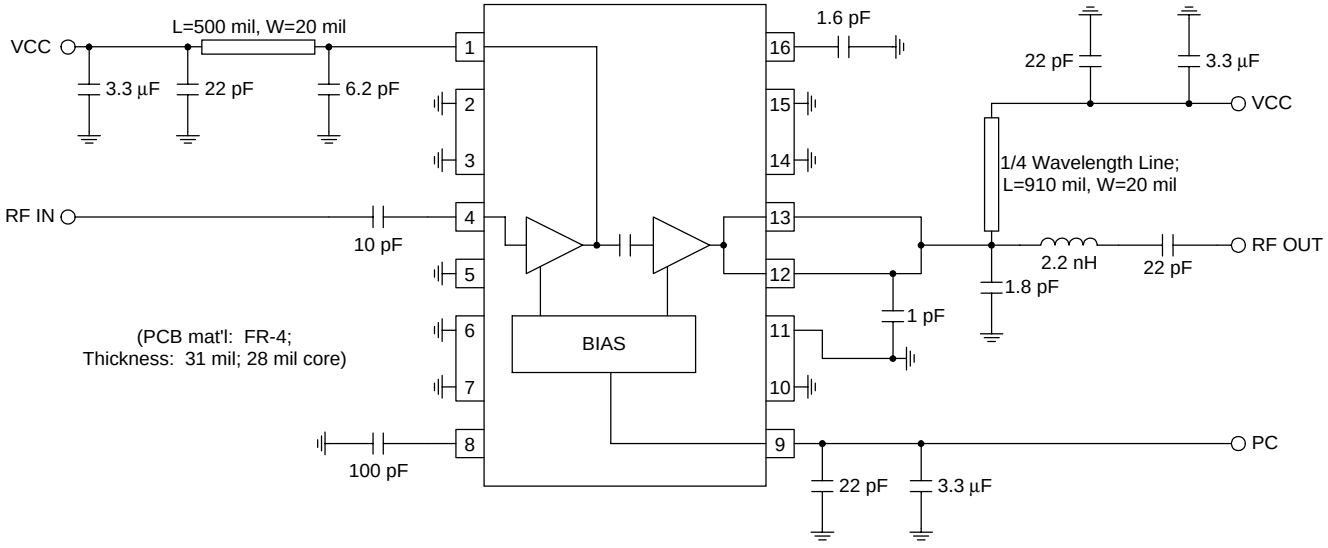
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25℃, V_{CC}=4.8V, V_{PC}=3.6V, P_{IN}=+10dBm, Freq=1880MHz
Usable Frequency Range		1500 to 2000		MHz	
Linear Gain		18.5	19	dB	
Maximum Linear Output Power		28.5			CDMA Modulation
Total Linear Efficiency		37		%	
Input Power for 28 dBm Output		+10		dBm	
Adjacent Channel Power Rejection	-45			dBc	CDMA Modulation, +28 dBm Output, At 1.25MHz Offset
Input VSWR		<2:1			
Second Harmonic		-35		dBc	Including Second Harmonic Trap
Power Down					
Off Isolation		25		dB	
Turn On Time		200		ns	Up to -0.5dB of Final Power
Turn Off Time		350		ns	Down to +0.5dB of Final Power
Total Current			TBD	µA	"OFF" State
V_{PC} "OFF" Voltage		0	0.2	V	Threshold Voltage at Input
V_{PC} "ON" Voltage	3.4	3.6	4.0	V	Threshold Voltage at Input
Power Supply					
Power Supply Voltage		4.0 to 6.5		V	Operating voltage
Current into V_{PC} pin		13		mA	"ON" State
Idle Current		70		mA	V_{PC}=3.6V, No RF Applied

Pin	Function	Description	Interface Schematic
1	VCC	Power supply for the driver stage, and interstage matching. Shunt capacitance is required on this pin. The value of the capacitance is frequency dependent. 4.7pF centers the gain at 1880 MHz.	
2	GND	Ground connection for final stage. Keep traces physically short and connect immediately to the ground plane for best performance.	
3	GND	Same as pin 2.	
4	RF IN	RF input. This is a 50Ω input, but the actual input impedance depends on the interstage matching network connected to pin 1. An external DC blocking capacitor is required if this port is connected to a DC path to ground or a DC voltage.	See pin 1.
5	GND	Ground connection for the driver stage. Keep traces physically short and connect immediately to the ground plane for best performance.	
6	GND	Same as pin 2.	
7	GND	Same as pin 2.	
8	BYP1	Bypass Pin. Part of the matching circuit for interstage match. DC connected to VCC1. Use a suitable bypass capacitor to ground. Keep capacitor as close to pin as possible.	See pin 1.
9	PC	Power Control. When this pin is "low", all circuits are shut off. A "low" is typically 0.5V. When this pin is "high", the part operates normally, and the pin consumes approximately 13mA during normal operation. This pin should never exceed 5V.	
10	GND	Same as pin 2.	
11	GND	Same as pin 2.	
12	RF OUT	RF Output and power supply for the output stage. The two output pins are combined, and bias voltage for the final stage is provided through these pins. An external matching network is required to provide the optimum load impedance; see the application schematics for details.	
13	RF OUT	Same as pin 12.	See pin 12.
14	GND	Same as pin 2.	
15	GND	Same as pin 2.	
16	BYP2	Bypass Pin. Part of the matching circuit for interstage match. DC connected to VCC1. For 1880 MHz operation, use a 3.3pF capacitor to ground. Keep capacitor as close to pin as possible.	See pin 1.

Application Schematic
1880MHz

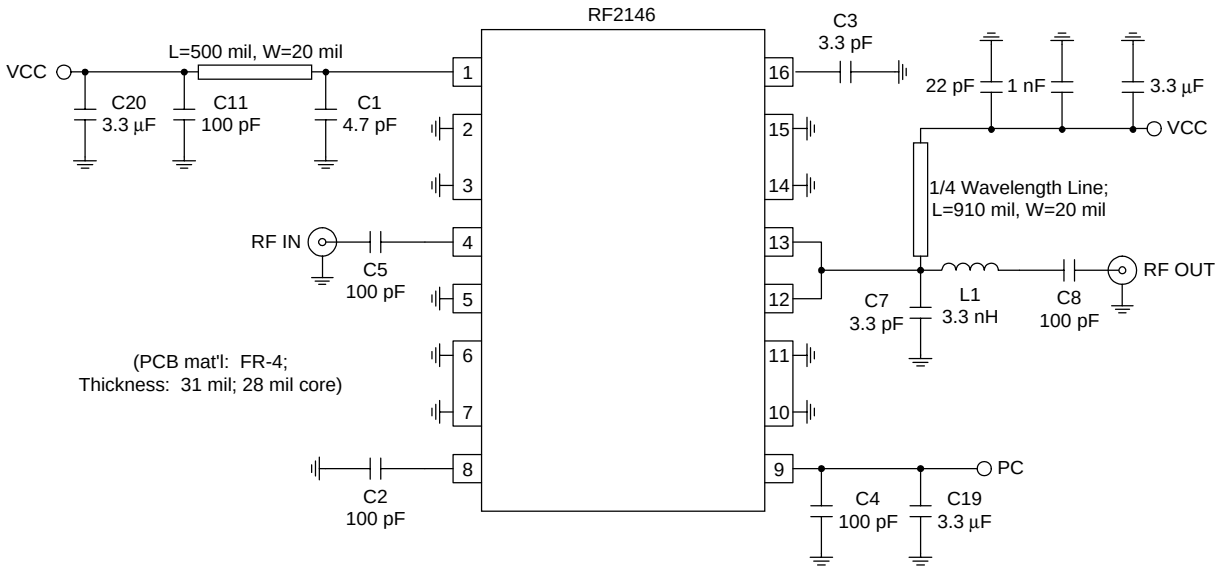


Application Schematic
2150MHz

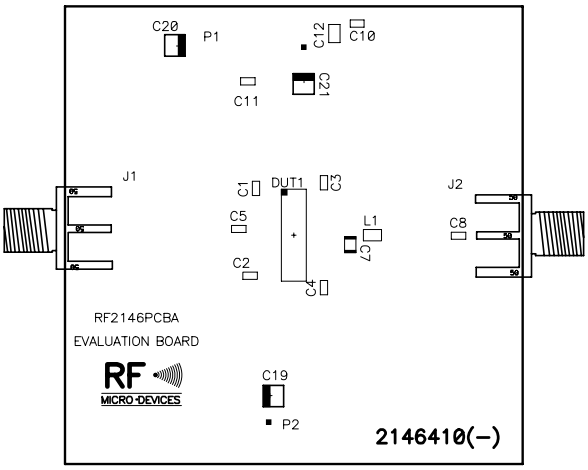


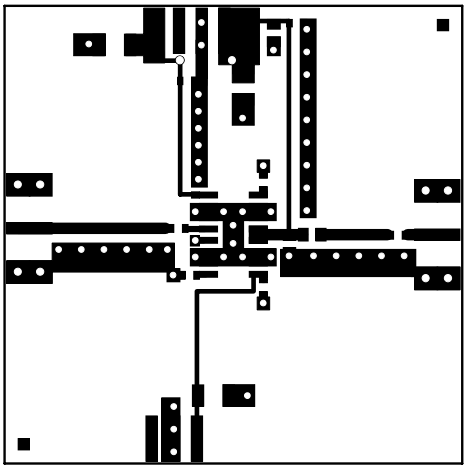
Evaluation Board Schematic

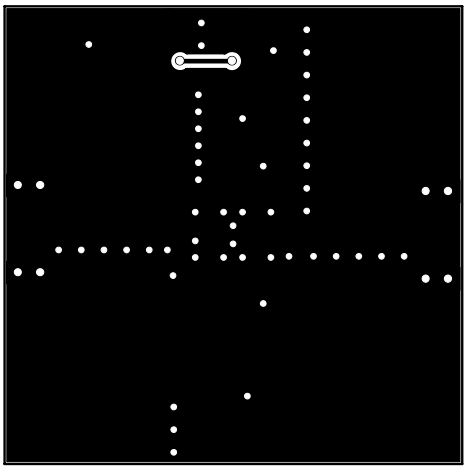
(Download Bill of Materials from www.rfmd.com.)



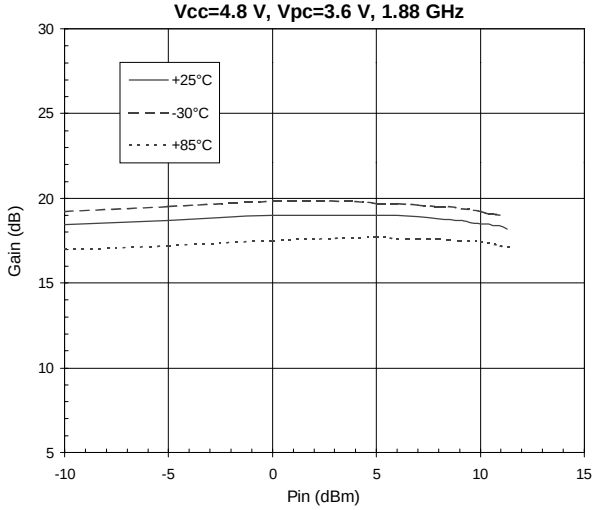
Evaluation Board Layout
2” x 2”



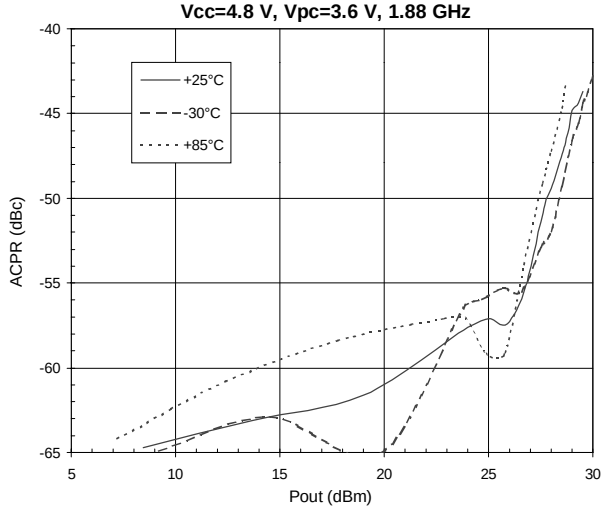




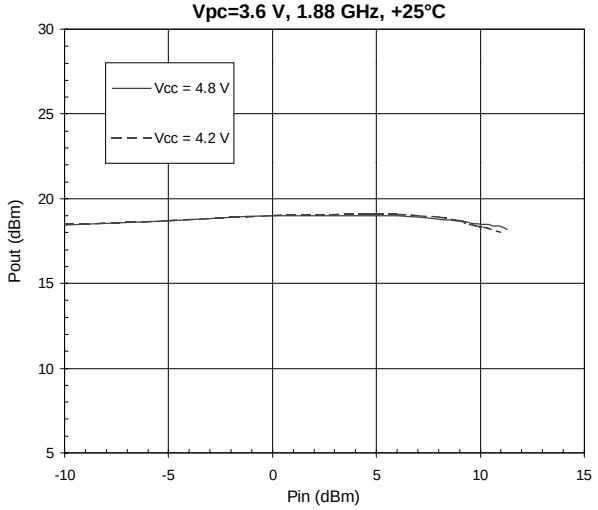
Gain vs. Pin
Vcc=4.8 V, Vpc=3.6 V, 1.88 GHz



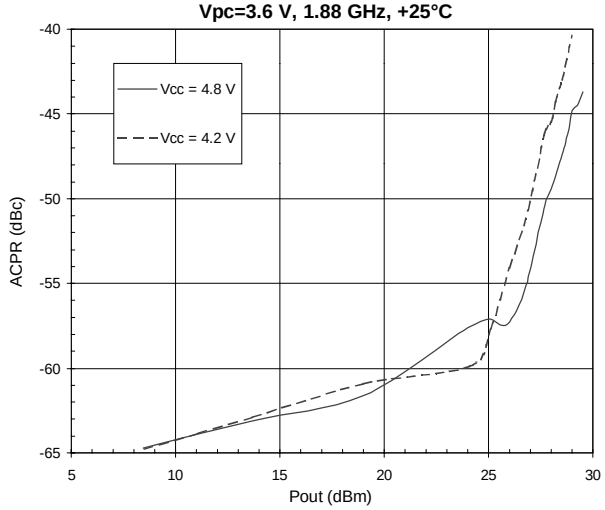
ACPR @ 1.25 MHz Offset vs. Pout
Vcc=4.8 V, Vpc=3.6 V, 1.88 GHz



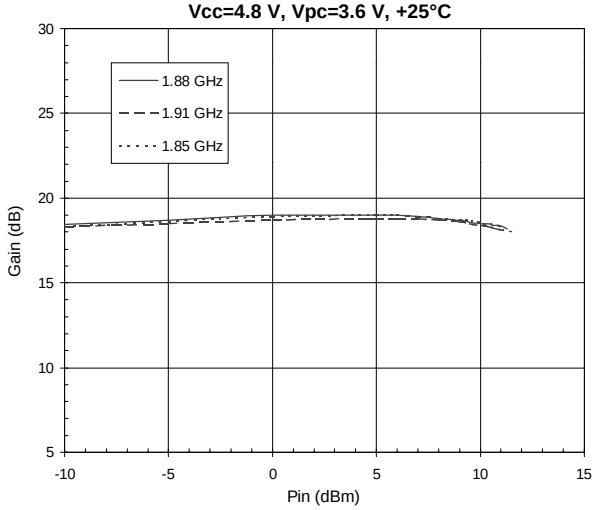
Gain vs. Pin
Vpc=3.6 V, 1.88 GHz, +25°C



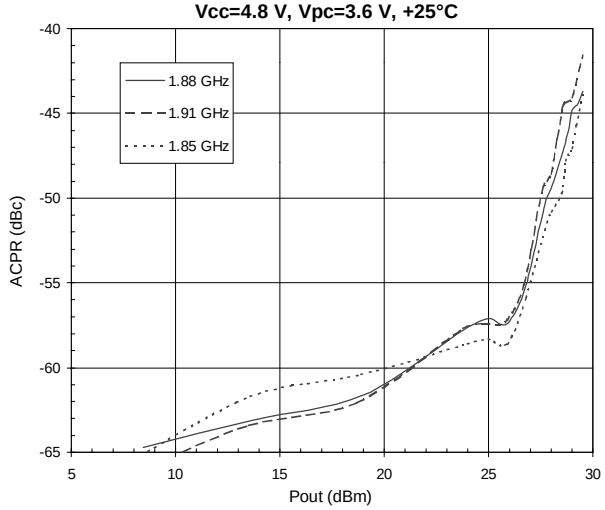
ACPR @ 1.25 MHz Offset vs. Pout
Vpc=3.6 V, 1.88 GHz, +25°C



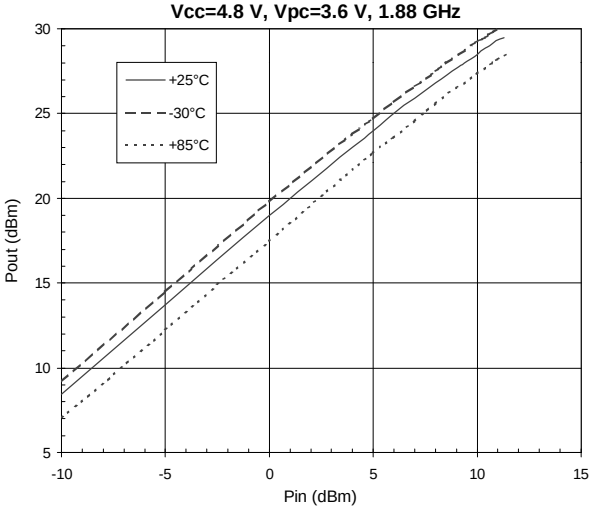
Gain vs. Pin
Vcc=4.8 V, Vpc=3.6 V, +25°C



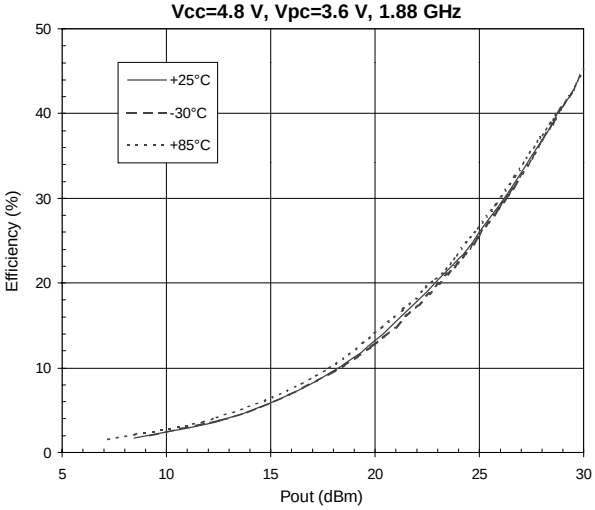
ACPR @ 1.25 MHz Offset vs. Pout
Vcc=4.8 V, Vpc=3.6 V, +25°C



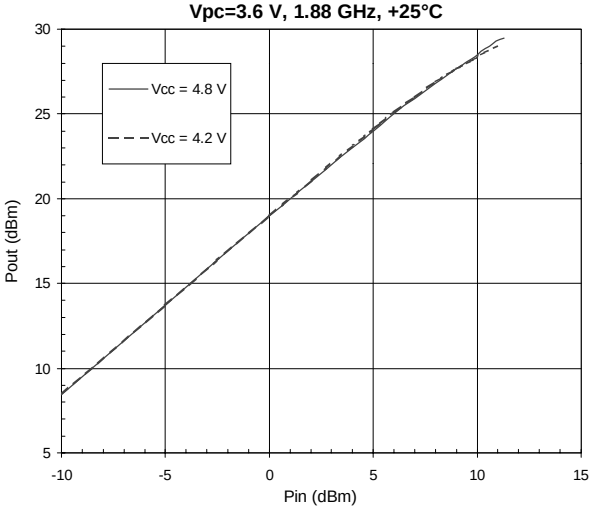
Pout vs. Pin
Vcc=4.8 V, Vpc=3.6 V, 1.88 GHz



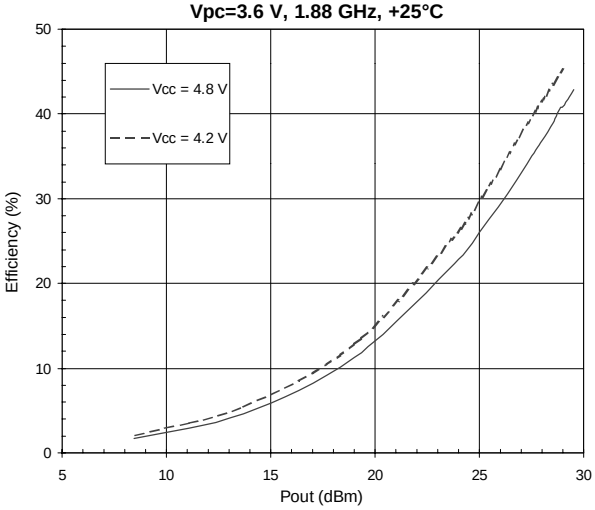
Efficiency vs. Pout
Vcc=4.8 V, Vpc=3.6 V, 1.88 GHz



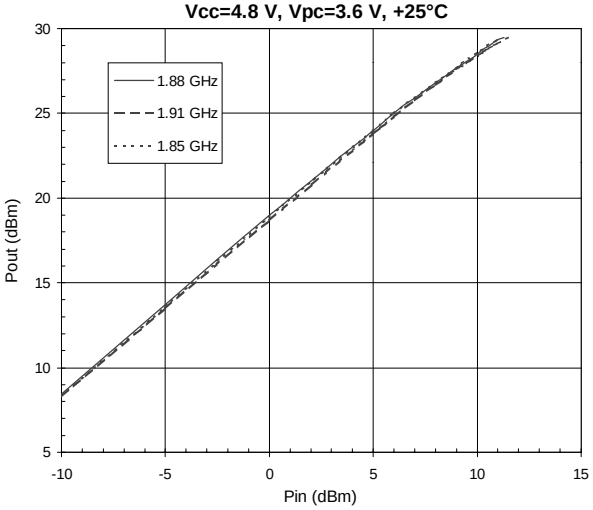
Pout vs. Pin
Vpc=3.6 V, 1.88 GHz, +25°C



Efficiency vs. Pout
Vpc=3.6 V, 1.88 GHz, +25°C



Pout vs. Pin
Vcc=4.8 V, Vpc=3.6 V, +25°C



Efficiency vs. Pout
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