RF2196

3V PCS LINEAR POWER AMPLIFIER

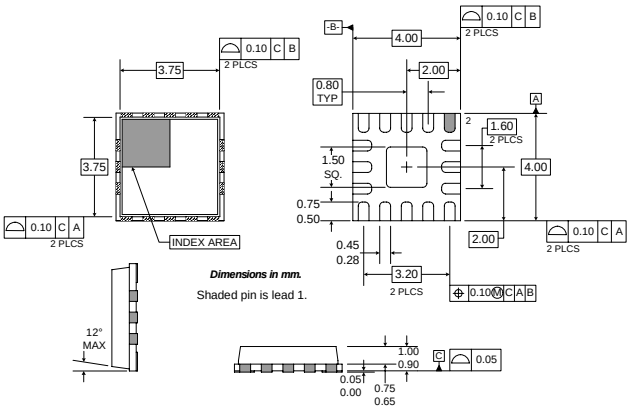
RoHS Compliant & Pb-Free Product

Typical Applications

- 3V CDMA PCS Handsets
- 3V CDMA KPCS Handsets
- 3V TDMA/GAIT PCS Handsets
- 3V CDMA 2000 PCS Handsets
- Spread-Spectrum Systems
- Portable Battery-Powered Equipment

Product Description

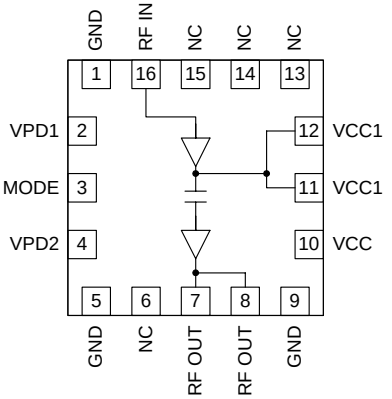
The RF2196 is a high-power, high-efficiency linear amplifier IC targeting 3V handheld systems. The device is manufactured on an advanced Gallium Arsenide process, and has been designed for use as the final RF amplifier in 3V CDMA and CDMA2000 handsets as well as other applications in the 1750MHz to 1910MHz band. The RF2196 has a low power mode to extend battery life under low output power conditions. The package is an ultra small 4mmx4mm, 16-pin QFN plastic package with backside ground.



Package Style: QFN, 16-Pin, 4x4

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS
- ☐ InGaP/HBT
- ☐ GaN HEMT
- ☐ SiGe Bi-CMOS



Functional Block Diagram

Features

- Single 3V Supply
- 29dBm Linear Output Power
- 35% Linear Efficiency
- Low Power Mode (Up to 20dBm)
- 55mA Idle Current

Ordering Information

RF2196	3V PCS Linear Power Amplifier
RF2196PCBA-41X	Fully Assembled Evaluation Board

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage (RF off)	+8.0	V_{DC}
Supply Voltage ($P_{OUT} \leq 31$dBm)	+5.2	V_{DC}
Mode Voltage (V_{MODE})	+4.2	V_{DC}
Control Voltage (V_{REG})	+3.0	V_{DC}
Input RF Power	+10	dBm
Operating Case Temperature	-30 to +110	℃
Storage Temperature	-30 to +150	℃

Caution! ESD sensitive device.

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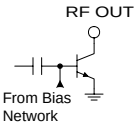
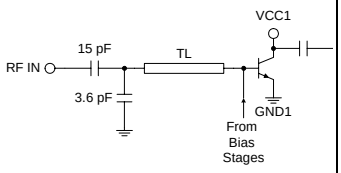
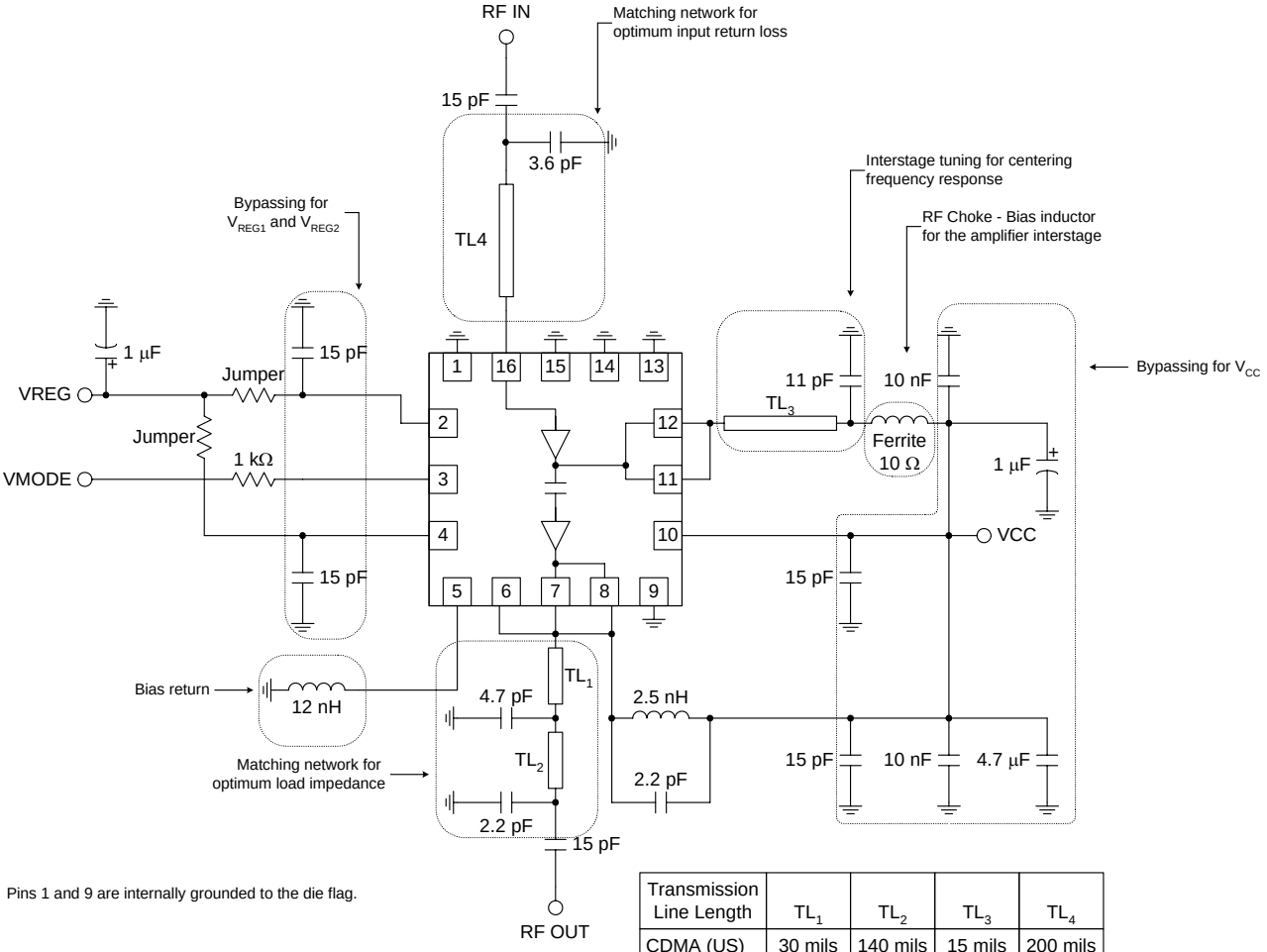
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
High Power State (V_{MODE} Low)					Case T=25°C, V_{CC}=3.4V, V_{REG}=2.85V, V_{MODE}=0V to 0.5V, Freq=1850MHz to 1910MHz (unless otherwise specified)
Frequency Range	1850		1910	MHz	
Linear Gain	25	27		dB	
Second Harmonic		-50		dBc	
Third Harmonic		-63		dBc	
Maximum Linear Output Power (CDMA Modulation)	29			dBm	
Total Linear Efficiency		35		%	P_{OUT}=29dBm
Adjacent Channel Power Rejection		-46	-44	dBc	ACPR@1.25MHz
		-62	-56	dBc	ACPR@2.25MHz
Input VSWR		<2:1			
Output VSWR			10:1		No damage.
			6:1		No oscillations. >-70dBc
Noise Power		-141		dBm/Hz	At 80MHz offset.
Low Power State (V_{MODE} High)					Case T=25°C, V_{CC}=3.4V, V_{REG}=2.85V, V_{MODE}=2V to 3V, Freq=1850MHz to 1910MHz (unless otherwise specified)
Frequency Range	1850		1910	MHz	
Linear Gain	16	20		dB	
Second Harmonic		-45		dBc	
Third Harmonic		-60		dBc	
Maximum Linear Output Power (CDMA Modulation)	16	20		dBm	
Max I_{CC}		160		mA	P_{OUT}=+16dBm (all currents included)
Adjacent Channel Power Rejection		<-50	-46	dBc	ACPR@1.25MHz
		<-60	-58	dBc	ACPR@2.25MHz
Input VSWR		2:1			
Output VSWR			10:1		No damage.
			6:1		No oscillations. >-70dBc

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
High Power State CDMA 2000 1x (V_{MODE} LOW)					Case T=25°C, V_{CC}=3.4V, V_{REG}=2.85V, V_{MODE}=0V to 0.5V, Freq=1850MHz to 1910MHz (unless otherwise specified)
Frequency Range	1850		1910	MHz	
Linear Gain		27		dB	
Pilot+DCCH 9600					
Maximum Linear Output Power (CDMA 2000 Modulation)	26.5			dBm	2.5dB Backoff included in IS95D 5.4dB peak to average at CCDF of 1%
Adjacent Channel Power Rejection		-49		dBc	ACPR@1.25MHz
		-61		dBc	ACPR@2.25MHz
Pilot+FCH 9600+SCH0 9600					
Maximum Linear Output Power (CDMA 2000 Modulation)	29			dBm	4.5dB peak to average at CCDF of 1%
Adjacent Channel Power Rejection		-46		dBc	ACPR@1.25MHz
		-63		dBc	ACPR@2.25MHz
Low Power State CDMA 2000 1x (V_{MODE} HIGH)					Case T=25°C, V_{CC}=3.4V, V_{REG}=2.85V, V_{MODE}=2V to 3V, Freq=1850MHz to 1910MHz
Frequency Range	1850		1910	MHz	
Linear Gain		19		dB	
Pilot+DCCH 9600					
Maximum Linear Output Power (CDMA 2000 Modulation)	16	20		dBm	5.4dB peak to average at CCDF of 1%
Adjacent Channel Power Rejection		-52		dBc	ACPR@1.25MHz
		-65		dBc	ACPR@2.25MHz
Pilot+FCH 9600+SCHO 9600					
Maximum Linear Output Power (CDMA 2000 Modulation)	16	20		dBm	4.5dB peak to average at CCDF of 1%
Adjacent Channel Power Rejection		-52		dBc	ACPR@1.25MHz
		-65		dBc	ACPR@2.25MHz
DC Supply					
Supply Voltage	3.0	3.4	4.2	V	
Quiescent Current		185		mA	V_{MODE}=Low
		55		mA	V_{MODE}=High
V_{REG} Current		5	10	mA	
V_{MODE} Current			1	mA	
Total Current (Power Down)			10	μA	V_{REG}=Low
V_{REG} "Low" Voltage	0		0.5	V	
V_{REG} "High" Voltage	2.75	2.85	2.95	V	
V_{MODE} "Low" Voltage	0		0.5	V	
V_{MODE} "High" Voltage	2.0		3.0	V	

Pin	Function	Description	Interface Schematic
1	GND	This pin is internally grounded to the die flag.	
2	VREG1	Power Down control for first stage. Regulated voltage supply for amplifier bias. In Power Down mode, both V_{REG} and V_{MODE} need to be LOW (<0.5V).	
3	MODE	For nominal operation (High Gain Mode), V_{MODE} is set LOW. When set HIGH, the driver and final are dynamically scaled to reduce the device size and as a result to reduce idle current.	
4	VREG2	Power Down control for the second stage. Regulated voltage supply for amplifier bias. In Power Down mode, both V_{REG} and V_{MODE} need to be LOW (<0.5V).	
5	GND	Connect to ground plane via 15nH inductor. DC return for the second stage bias circuit.	
6	NC	This pin has no internal bonding; therefore, this pin can be connected to output pin 7, connected to the ground plane, or not connected. Slight tuning of the output match may be required due to stray capacitance of the pin.	
7	RF OUT	RF output and power supply for final stage. This is the unmatched collector output of the second stage. A DC block is required following the matching components. The biasing may be provided via a parallel L-C set for resonance at the operating frequency of 1710MHz to 1910MHz. It is important to select an inductor with very low DC resistance with a 1A current rating. Alternatively, shunt microstrip techniques are also applicable and provide very low DC resistance. Low frequency bypassing is required for stability.	
8	RF OUT	Same as pin 7.	See pin 7.
9	GND	This pin is internally grounded to the die flag.	
10	VCC	Supply for bias reference and control circuits. High frequency bypassing may be necessary.	
11	VCC1	Power supply for first stage and interstage match. Pins 11 and 12 should be connected by a common trace where the pins contact the printed circuit board.	
12	VCC1	Same as pin 11.	
13	NC	It is recommended that these pins be connected to the ground plane for improved isolation between RF IN (pin 16) and the VCC1 pins (pins 11 and 12).	
14	NC	It is recommended that these pins be connected to the ground plane for improved isolation between RF IN (pin 16) and the VCC1 pins (pins 11 and 12).	
15	NC	It is recommended that these pins be connected to the ground plane for improved isolation between RF IN (pin 16) and the VCC1 pins (pins 11 and 12).	
16	RF IN	RF input. An external 15pF series capacitor is required as a DC block. In addition, the matching circuit shown is required to improve input VSWR.	
Pkg Base	GND	Ground connection. The backside of the package should be soldered to a top side ground pad which is connected to the ground plane with multiple vias. The pad should have a short thermal path to the ground plane.	

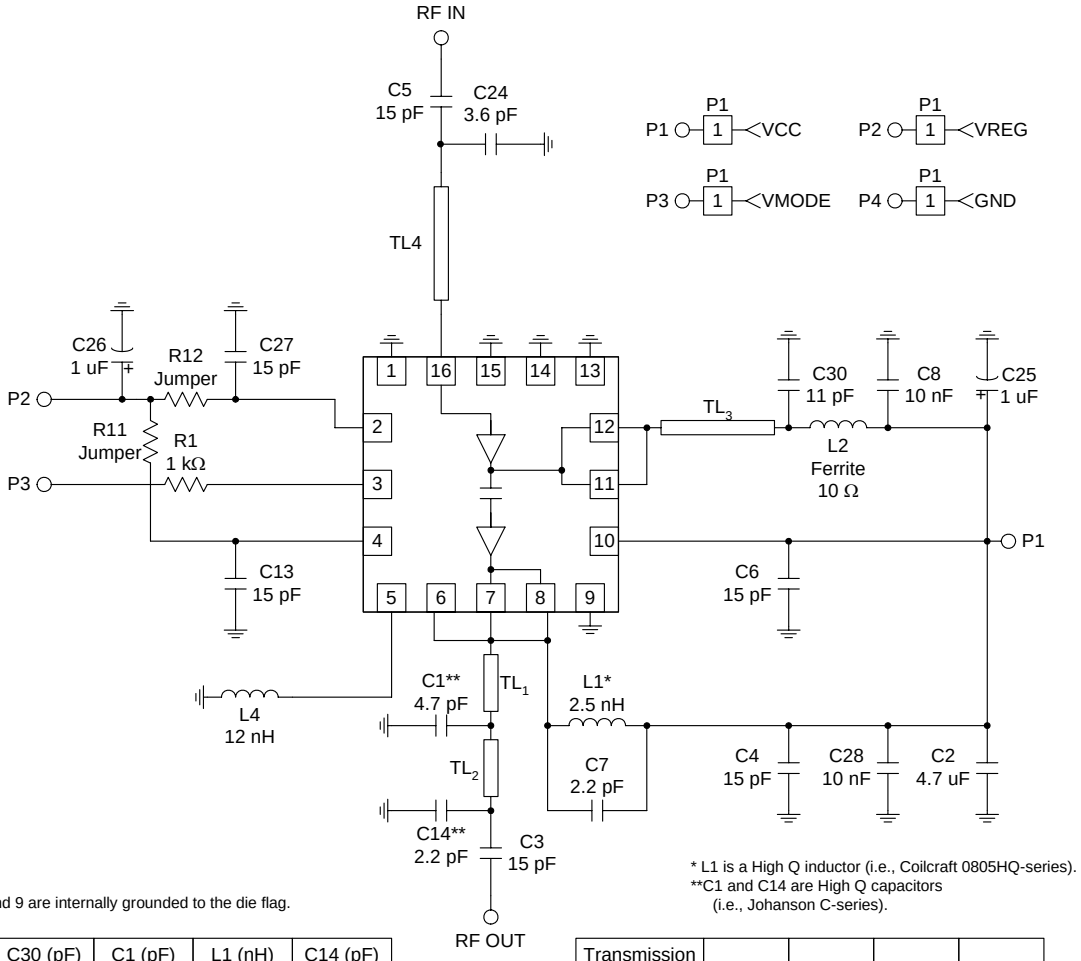
Application Schematic
US - CDMA



Pins 1 and 9 are internally grounded to the die flag.

Transmission Line Length	TL_1	TL_2	TL_3	TL_4
CDMA (US)	30 mils	140 mils	15 mils	200 mils

Evaluation Board Schematic
US - CDMA



Pins 1 and 9 are internally grounded to the die flag.

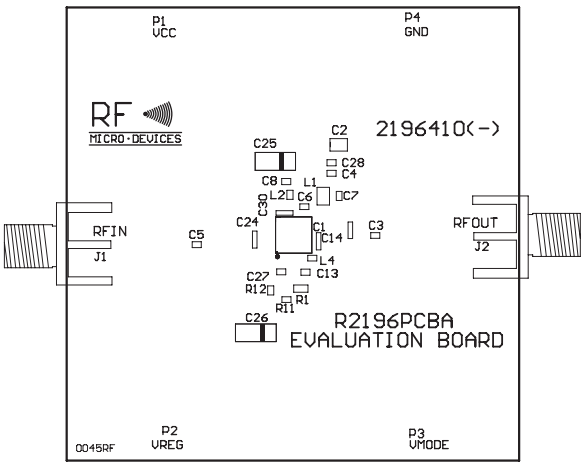
* L1 is a High Q inductor (i.e., Coilcraft 0805HQ-series).
**C1 and C14 are High Q capacitors
(i.e., Johanson C-series).

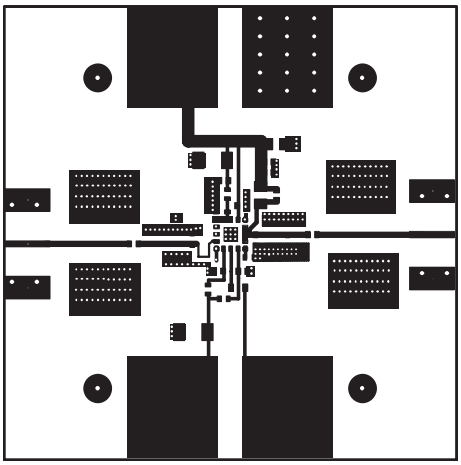
Board	C30 (pF)	C1 (pF)	L1 (nH)	C14 (pF)
CDMA (US)	11	4.7	2.5	2.2

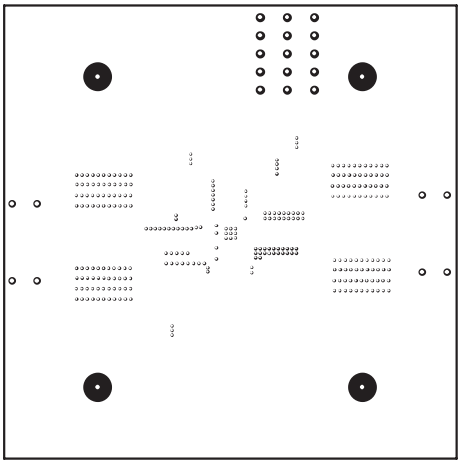
Transmission Line Length	TL_1	TL_2	TL_3	TL_4
CDMA (US)	30 mils	140 mils	15 mils	200 mils

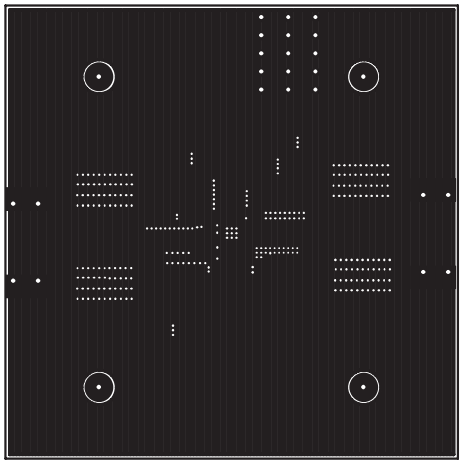
Evaluation Board Layout
Board Size 2.0” x 2.0”

Board Thickness 0.028”; Board Material FR-4; Multi-Layer; Ground Plane at 0.014”









PCB Design Requirements

PCB Surface Finish

The PCB surface finish used for RFMD's qualification process is electroless nickel, immersion gold. Typical thickness is 3μinch to 8μinch gold over 180μinch nickel.

PCB Land Pattern Recommendation

PCB land patterns are based on IPC-SM-782 standards when possible. The pad pattern shown has been developed and tested for optimized assembly at RFMD; however, it may require some modifications to address company specific assembly processes. The PCB land pattern has been developed to accommodate lead and package tolerances.

PCB Metal Land Pattern

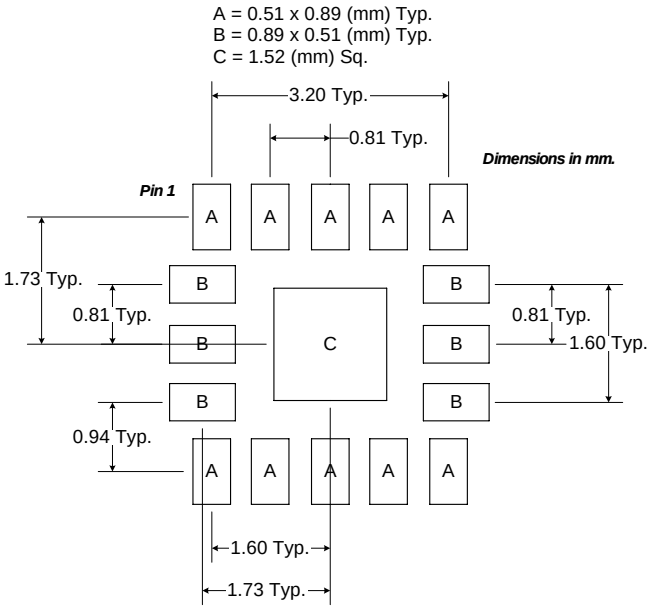


Figure 1. PCB Metal Land Pattern (Top View)

PCB Solder Mask Pattern

Liquid Photo-Imageable (LPI) solder mask is recommended. The solder mask footprint will match what is shown for the PCB Metal Land Pattern with a 3mil expansion to accommodate solder mask registration clearance around all pads. The center-grounding pad shall also have a solder mask clearance. Expansion of the pads to create solder mask clearance can be provided in the master data or requested from the PCB fabrication supplier.

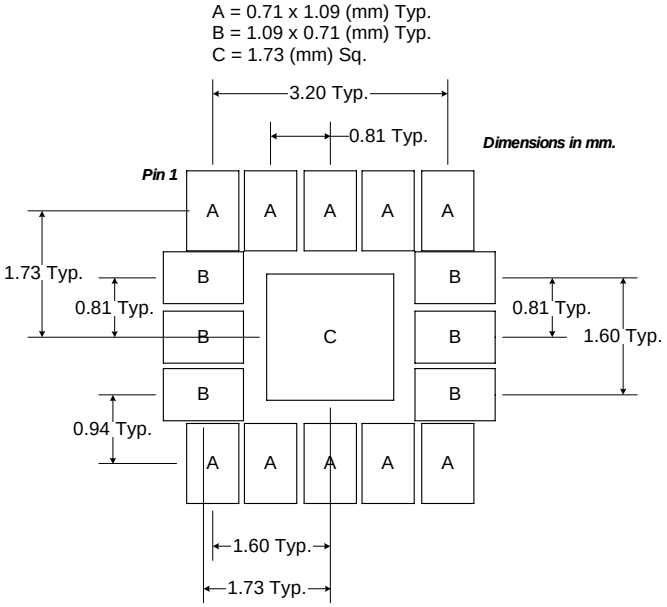


Figure 2. PCB Solder Mask (Top View)

Thermal Pad and Via Design

The PCB metal land pattern has been designed with a thermal pad that matches the exposed die paddle size on the bottom of the device.

Thermal vias are required in the PCB layout to effectively conduct heat away from the package. The via pattern has been designed to address thermal, power dissipation and electrical requirements of the device as well as accommodating routing strategies.

The via pattern used for the RFMD qualification is based on thru-hole vias with 0.203mm to 0.330mm finished hole size on a 0.5mm to 1.2mm grid pattern with 0.025mm plating on via walls. If micro vias are used in a design, it is suggested that the quantity of vias be increased by a 4:1 ratio to achieve similar results.