REG200RHA 1.8V 200 mA Linear Voltage Regulator

ATMX150RHA

Introduction

REG200RHA is a radiation-hardened linear voltage regulator including Power-on-Reset (POR) and Power Fail Detector (PFD) capability. It operates between 3V to 5.5V and provides a fixed 1.8V output voltage while sourcing up to 200 mA of load current.

A 470 nF external capacitor has to be connected to the regulator output V_{OUT} to ensure stability and noise rejection. The following table lists the physical parameters of the regulator.

Table 1. Physical Parameters

Parameter	Value
Supply Voltage	3V to 5.5V
Placement	Core (next to periphery)
Height	744.8 µm
Width	481.6
Area	0.359 mm^2

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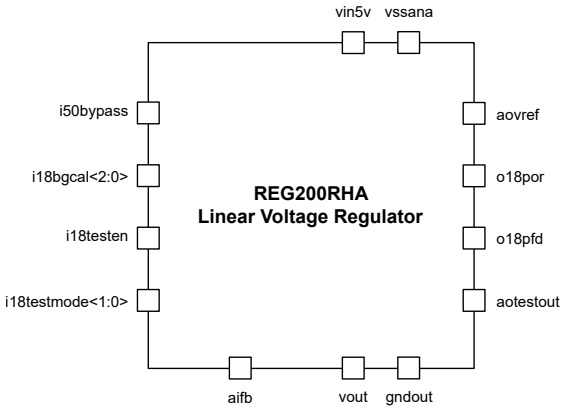
1. Pin Description

The following figure shows the package diagram of the regulator.

Figure 1-1. Package Diagram



The following table lists the pin details of the package.

Table 1-1. Pinout

Pin Name	I/O	Related Supply	Description
vin5v	I/O	—	Input power supply
vssana	I/O	—	Input ground
i18bgcal<2:0>	I	vout	Internal bandgap voltage reference calibration bits, see Table 3-1
i50bypass	I	vin5v	Enables Bypass mode when set to 1
i18testen	I	vout	Enables Test mode when set to 1
i18testmode<1:0>	I	vout	Test mode selection bits, see Table 4-1
vout	I/O	—	Regulated voltage output. Used as an input in Bypass mode
gndout	I/O	—	Regulated voltage ground
aifb	I	—	Regulated voltage sense input
aovref	O	—	Bandgap reference voltage output
o18por	O	vout	PoR signal equals to 1 during reset
o18pfd	O	vout	PFD equals to 1 when fail is detected
aotestout	O	—	Output pin in Test mode to get few regulator outputs

2. Operating Modes Description

The voltage regulator can operate in the following modes:

Table 2-1. Operating Mode Table

i50bypass	i18testen	Operating Mode
0	0	Normal mode: Regulator can provide full load. PoR and PFD functions are enabled. Bandgap reference voltage is available.
0	1	Test mode: Different voltages are accessible through aotestout pin, depending on i18testmode<1:0> setting. Full load capability is available. POR and PFD functions are disabled, `v(o18por) = v(o18pfd) = 0`. Bandgap reference voltage is available.
1	0	Bypass mode: No output regulated voltage, the 1.8V supply voltage is provided by an external source. POR and PFD functions are enabled. Bandgap reference voltage is available.
1	1	Bypass and Test mode: Useful to characterize internal blocks of the regulator, power supplied by vout. POR and PFD functions are disabled. Bandgap reference voltage is available.

Notes:

- The regulator must be supplied with power through the pin vin5v, even in Bypass mode.
- In Bypass mode, the power ON/OFF rising and falling edges, on the pin vout, induce charging current in the external decoupling capacitor C_L. This current must not be greater than I_{LOAD} max. (C_L and I_{LOAD} values are given in the section 4. Specifications.)

3. Bandgap Calibration

The voltage regulator embeds its own reference voltage. Three calibration bits are available to adjust the reference voltage (V_{REF}) and consequently the output regulated voltage (V_{OUT}). For precision applications, the calibration might be necessary to compensate the process fluctuation during the fabrication.

The dynamic adjustment of the output regulated voltage is not allowed. The calibration bits must be set before the voltage regulator start-up. The typical calibration step is vcal_step = 5 mV.

Table 3-1. Reference Voltage

i18bgcal<2>	i18bgcal<1>	i18bgcal<0>	Reference Voltage
0	0	0	V_{REF} + (3 x vcal_step)
0	0	1	V_{REF} + (1 x vcal_step)
0	1	0	V_{REF} + (1 x vcal_step)
0	1	1	V_{REF}
1	0	0	V_{REF} - (1 x vcal_step)
1	0	1	V_{REF} - (2 x vcal_step)
1	1	0	V_{REF} - (3 x vcal_step)
1	1	1	V_{REF} - (4 x vcal_step)

The calibration is done during the production final test. The relevant settings of i18bgcal<2:0> is stored in the product and used at each start-up.

4. Specifications

The following table lists the specification details over the operating temperature range (Tj = –55 °C to 145 °C), V_{IN} = 3.3V, and CL = 470 nF, unless otherwise noted.
The listed typical values are at Tj = 25 °C.

Table 4-1. Electrical Specifications

Parameter		Test Condition	Min	Typ	Max	Unit
V_{IN}	Input voltage range	—	3	—	5.5	V
I_{LOAD}	Output rated current	—	0	—	200	mA
$I_{load\_start\_up}$[1]	Maximum load current during start-up	Vin > 3V	—	—	3	mA
C_L	External decoupling capacitor	—	446.5	470	493.5	nF
R_{ESR}	Decoupling capacitor ESR	—	—	—	0.5	Ω
t_{RISE}	Input voltage rising	From 0V to V_{IN} min.	1e-6	—	1	s
V_{OUT}	Output regulated voltage	—	1.68	1.8	1.95	V
V_{REF}	Internal reference voltage	Tj = 25 °C	—	0.9	—	V
T_{COREF}	Reference temperature coefficient	—	—	121	—	ppm/°C
$\Delta V_{OUT(\Delta VIN)}$	Line regulation	3V ≤ V_{IN} ≤ 5.5V	—	1	—	%
	Transient line regulation	$\Delta V_{IN}/\Delta t$ = 1 V/µs	—	5	—	%
$\Delta V_{OUT(\Delta ILOAD)}$	Load regulation	0 mA ≤ I_{LOAD} ≤ 200 mA	—	1	—	%
	Transient load regulation	$\Delta I_{LOAD}/\Delta t$ = 100 mA/µs	—	5	—	%
V_{DO}	Dropout voltage (V_{IN} = V_{OUT} (nom) - 0.1V)	I_{LOAD} = 200 mA	—	—	500	mV
Z_{DO}	Output impedance in dropout	3V ≤ V_{IN} ≤ V_{OUT} + V_{DO}	—	1	—	Ω
I_{PWR}	Ground pins current	0 mA ≤ I_{LOAD} ≤ 200 mA, Normal mode	—	—	500	µA
I_{FB}	aifb pin current	—	—	—	10	µA
PSRR	Power Supply Rejection Ratio	F = 100 Hz, I_{LOAD} = 200 mA	40	—	—	dB
		F = 10 kHz, I_{LOAD} = 200 mA	20	—	—	
t_{STR}	Startup time	—	—	—	1	ms
V_{POR}	PoR threshold	—	—	1.60	—	V
t_{POR}	PoR delay time	—	—	—	500	µs
V_{PFDF}	PFD falling threshold	—	—	1.65	—	V
V_{PFDR}	PFD rising threshold	—	—	1.70	—	V

Note:

1. When o18por = 1, the regulator is in the start-up condition, meaning the POR threshold has not been reached.

Note: The output regulated voltage is V_{OUT} = 1.8V. It can vary between 1.68V and 1.95V because of IR drops, undershoots, and overshoots coming from the current consumption on the regulator output pin vout.
The minimum and maximum values of V_{OUT} have taken already into account the minimum and maximum variation of V_{REF}, T_{COREF}, $\Delta V_{OUT(\Delta VIN)}$, and $\Delta V_{OUT(\Delta ILOAD)}$. Typical values are given for information purpose only.

5. Radiation Hardness

The following table lists the radiation tolerance related specifications.

Table 5-1. Radiation Tolerance Specification

Parameter	Conditions	Range
TID	ESCC 22900 and MIL-STD-883 TM 1019 - RT Input supply voltage V_{IN} max and Dose Rate < 360 rad/h	100 krad(Si) RHA (tested 150 krad(Si))
SEL	ESCC 25100 and JESD57A Input supply voltage V_{IN} max and Tj = 125 °C	> 60 MeV.cm²/mg
SET/SEU	Input supply voltage V_{IN} min and Tj = 25 °C	> 60 MeV.cm²/mg

6. Typical Application

The following figures describe a 3.3V circuit with a 1.8V digital core power supplied by the REG200RHA. The voltages on the regulator pins (vin5v and i50bypass) must not exceed the I/O buffer power supply voltage (in this case, 3.3V).

The regulator output pin (vout) is connected to the VCC power rail and to the circuit power supply grid.

The external decoupling capacitors have to be connected to the power supply buffers of the regulator.

Figure 6-1. Typical Application Scheme

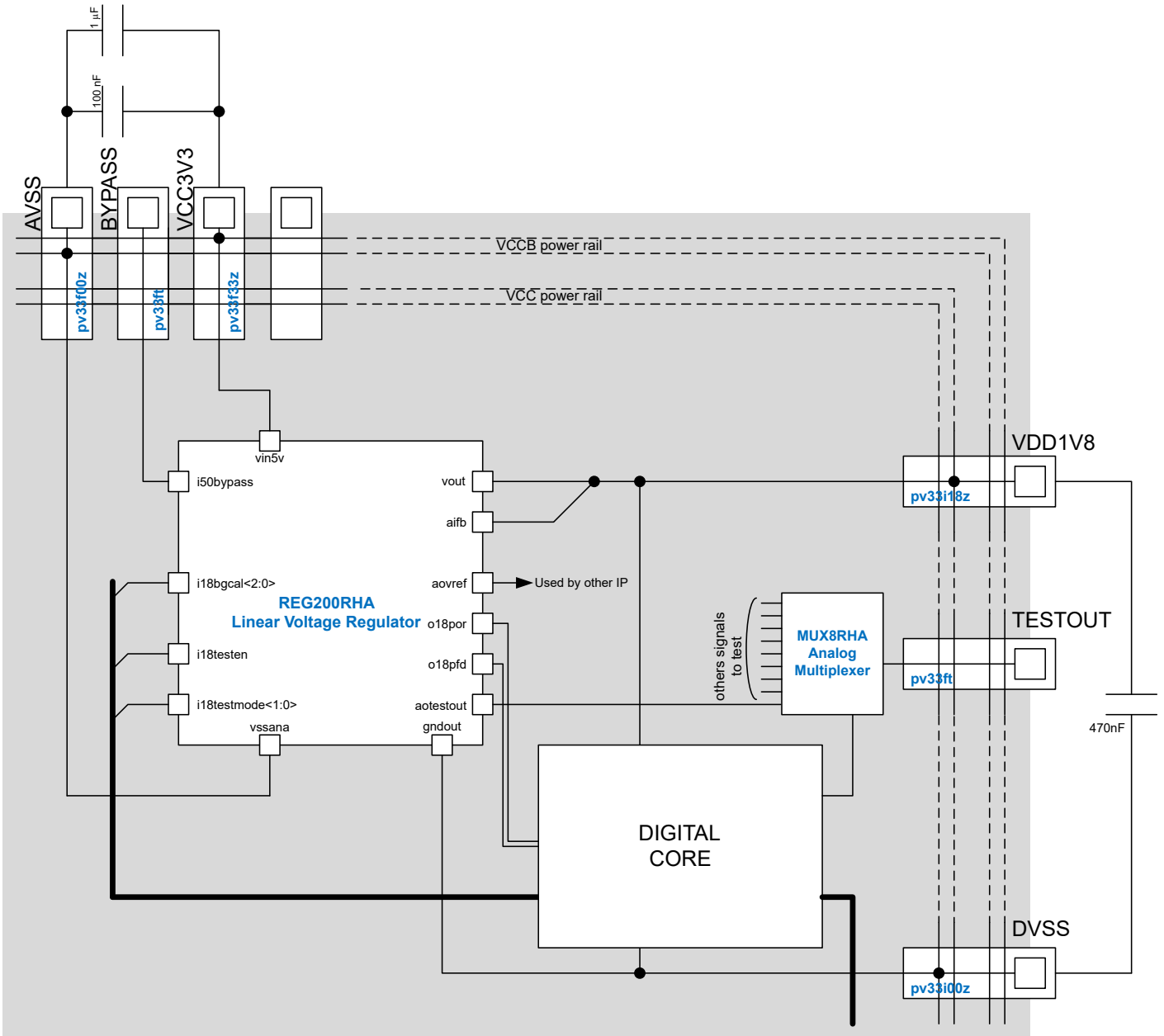
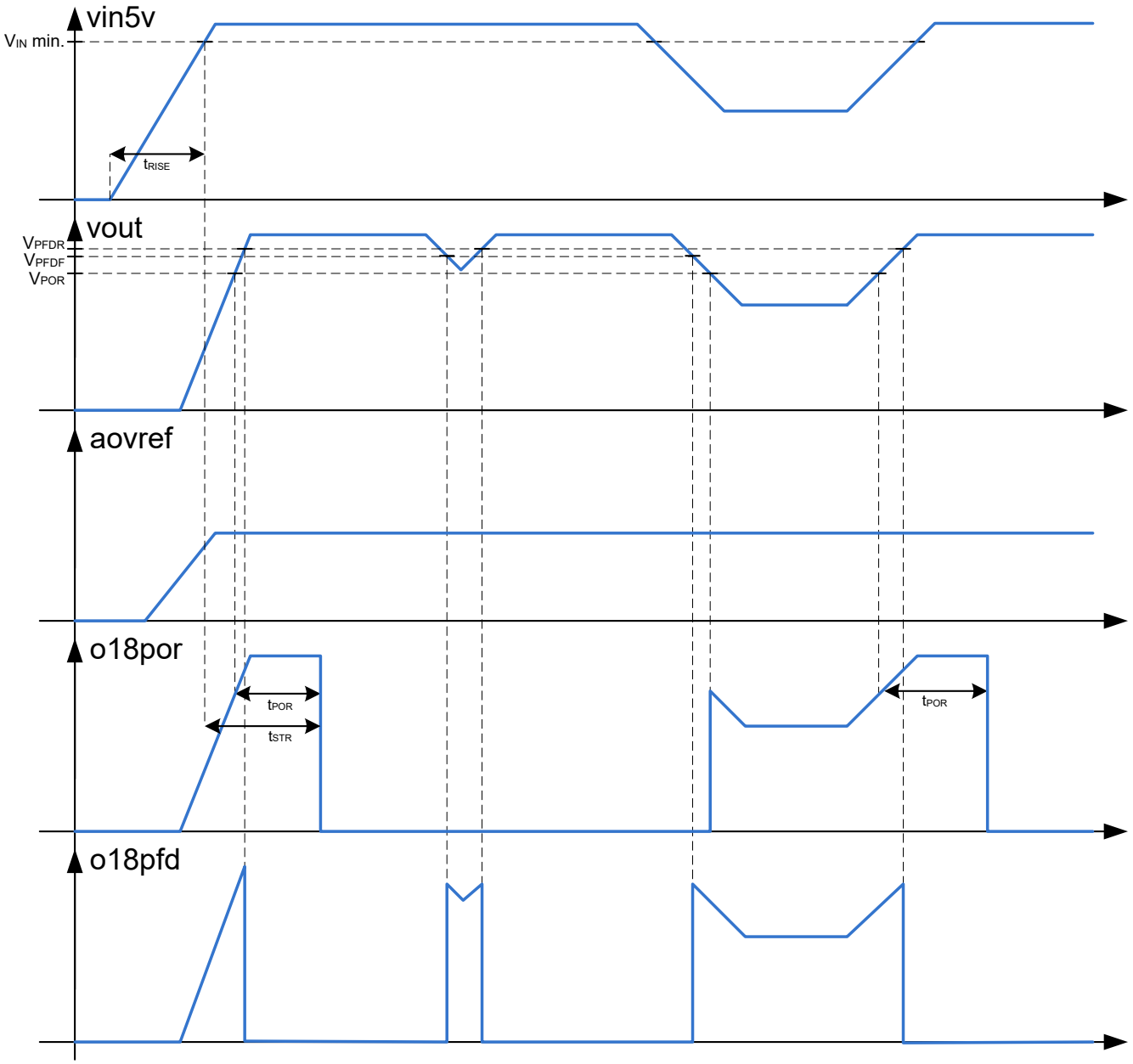


Figure 6-2. Typical Timing Characteristics



7. Testability Requirements

Unless otherwise specified at the DSR, the V_{OUT} parameter must be measured when the asic is in active and non-active mode and at the minmum and maximum values on the vin5v pin.

For this test, the pin oatestout must be accessible through a primary I/O.

8. Testability Information

The regulator have access to a test pin, aotestout, which allows to make measurement to characterize the regulator performance as listed in the following table.

Table 8-1. Test Mode Output Selection

i18testmode<1>	i18testmode<0>	Information Available on aotestout
0	0	Internal bandgap reference voltage
0	1	Internal POR signal
1	0	Internal Power Fail Detector signal
1	1	Regulated voltage feedback signal

When i18testmode<1:0> = (0, 0), the internal bandgap reference voltage is available on aotestout. The measurement must be done with high impedance probe (active probe recommended).

When i18testmode<1:0> = (0, 1), the internal POR signal is available on aotestout while the POR pin, o18por, is forced to 0. Therefore, the product can run normally while the POR voltage is measured.

When i18testmode<1:0> = (1, 0), the internal PFD signal is available on aotestout while the PFD pin, o18pfd, is forced to 0. Therefore, the product can run normally while PFD voltage is measured.

When i18testmode<1:0> = (1, 1), the regulated voltage feedback signal is available on aotestout. Therefore, the regulated voltage coming from the core is accessible while a current sinks through the pin V_{OUT} of the regulator.

9. Integration Guidelines

The following sections describe the various integration guidelines.

9.1 Placement and General Rules

This cell is very sensitive to electrical noise. Therefore, it must be placed in the quietest part of the circuit. It is preferably placed close to the I/O buffers that are connected to vin5v and vssana, in order to reduce the resistivity of the power lines.

The wires used to connect the voltage regulator must be as wide as their corresponding pins.

Note: Never place several voltage regulators in parallel to increase the current capability.

9.2 Supplies Routing and Decoupling

The power supply and ground pins (vin5v and vssana) as well as the regulated output and the created ground pins (vout and gndout) must be star-routed to their corresponding I/O buffers with less than 0.1 Ω of parasitic resistance.

External decoupling capacitors must be connected to ensure performance. A 100 nF capacitor in parallel with a 1 µF ceramic capacitor (X7R) is needed between the pins, vin5v and vssana. A 470 nF ceramic capacitor (X7R) is needed between the pins, vout and gndout. The ESR value must be kept within the boundary defined in Table 4-1.

All the decoupling capacitors must be as close as possible to the package.

All the decoupling capacitors must connect to a large area low impedance ground plane through or short trace to minimize inductance.

9.3 Analog Signals Routing

All the analog signals must be routed to have less than 1 Ω parasitic resistance, including associated I/O cell for core blocks.

All the analog signals must be routed to have less than 1 pF parasitic capacitance, not including associated I/O cell for core blocks.

The signal routed to the pin, aifb, is the regulated voltage feedback or FB signal. All the digital or the clock signals must be routed with 1 µm spacing away from the FB signal. In case of crossing the digital or the clock signals, a shield must be added, connected to the analog ground line, between the noisy net and the FB signal.

The output pin, aovref, provides a reference voltage. All the digital or the clock signals must be routed with 1 µm spacing away from the signal connected to aovref, V_{REF} signal. In case of crossing the digital or the clock signals, a shield must be added, connected to the analog ground line, between the noisy net and the V_{REF} signal.

In case of any of this condition is not met, contact the design group to investigate any potential performance impact.

9.4 Routing Constraints

The following table lists the routing constratints.

Table 9-1. Routing Constraints

Pin Name	Signal Type	Related Power Supply	Max DC Current Flowing (mA)	Max Allowed Routing Resistance (Ω)	Max Allowed Capacitance to Ground (pF)	Other constraints
vin5v	Supply	—	200	0.1	—	Star routed to power supply input
vssana	Ground	—	1	0.1	—	Star routed to power supply input
i18bgcal<2:0>	Digital	vout	—	—	—	—
i50bypass	Digital	vin5v	—	—	—	—
i18testen	Digital	vout	—	—	—	—
i18testmode<1:0>	Digital	vout	—	—	—	—
vout	Supply	—	200	0.1	—	Star routed to power supply input
gndout	Ground	—	1	0.1	—	Star routed to power supply input
aifb	Analog	—	0.01	10	0.1	No crossing with other signal, shielding to vssana must be inserted in that case. 1 um minimum spacing to other signal trace.
aovref	Analog	—	—	—	1	No crossing with other signal, shielding to vssana must be inserted in that case. 1 um minimum spacing to other signal trace.
o18por	Digital	vout	—	—	—	—
o18pfd	Digital	vout	—	—	—	—
aotestout	Analog	—	—	—	—	—

10. Revision History

Revision	Date	Description
B	09/2023	Added a new $I_{load\_start\_up}$ parameter in the Electrical Specification table. See Table 4-1.
A	07/2020	The following is a summary of changes in revision A of this document. • The template was updated. • The document number was updated from 41068 to DS60001639. • Bandgap table correction • The “testability” paragraph was replaced with “testability requirements”. For more information, see 7. Testability Requirements.

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