Intel StrataFlash® Wireless Memory System (LV18 SCSP)

1024-Mbit LVX Family with LPSDRAM

Datasheet

Product Features

- **Device Memory Architecture**
  - —Flash die density: 128-, 256-Mbit
  - —LPSDRAM die density: 128-, 256-Mbit
  - —Top or Bottom parameter flash configuration
- **Device Voltage**
  - —Core: V_{CC} = 1.8 V (typ.)
  - —I/O: V_{CCQ} = 1.8 V (typ.)
- **Device Common Performance**
  - —Buffered EFP: 5µs / Byte (typ.) per die
  - —Buffer Program: 7µs / Byte (typ.) per die
  - —Concurrent Buffered EFP: 6.4-Mbps effective with 4 flash dies
- **Device Common Architecture**
  - —Asymmetrical blocking structure
  - —16-KWord parameter blocks (Top or Bottom); 64-KWord main blocks
  - —Zero-latency block locking
  - —Absolute write protection with block lock down using F-VPP and F-WP#
- **Device Packaging**
  - —103 active balls; 9 x 12 ball matrix
  - —Area: 9 x 11 mm to 11 x 11 mm
  - —Height: 1.4 mm
- **SDRAM Architecture and Performance**
  - —Clock rate: 105 MHz
  - —Four internal banks
  - —Burst Length: 1, 2, 4, 8, or full page
- **Code Segment Flash Read Performance**
  - —85 ns initial access
  - —25 ns Asynchronous Page read
  - —14 ns Synchronous read (t_{CHQV})
  - —54 MHz (max.) CLK
- **Data Segment Flash Performance**
  - —170 ns initial access
  - —55 ns Asynchronous Page read
- **Code Segment Flash Architecture**
  - —Hardware Read-While-Write/Erase
  - —Multiple 8-Mbit / 16-Mbit partition sizes
  - —2-Kbit One-Time-Programmable Protection Register
- **Data Segment Flash Architecture**
  - —Software Read-While-Write/Erase
  - —Single partition size die
- **Flash Software**
  - —Intel® FDI, Intel® PSM, and Intel® VFM
  - —Common Flash Interface
  - —Basic/Extended Command Set
- **Quality and Reliability**
  - —Extended temperature: –25 °C to +85 °C
  - —Minimum 100 K flash block erase cycle
  - —0.13 µm ETOX™ VIII flash technology

Intel StrataFlash® Wireless Memory System (LV18 SCSP) with Low-Power SDRAM (LVX family) offers a variety of high performance code segment, large embedded data segment, and low-power SDRAM combinations in a common package on 0.13 µm ETOX™ VIII flash technology. The LVX family integrates up to two code segment flash dies, two data segment flash dies, and two low-power SDRAM dies or one SRAM die in a common x16D Performance ballout.

Notice: This document contains information on new products in production. The specifications are subject to change without notice. Verify with your local Intel sales office that you have the latest datasheet before finalizing a design.

300945-006
October 2004

Contents

Revision History

Date	Revision	Description
February, 2004	-001	Initial release.
February, 2004	-002	Corrected information in the Memory Map table, code and data segments, bottom parameter.
April, 2004	-003	Corrected errors in Table 1 and Table 26. The package dimension of part RD48F4444LVYBB0 RD48F4444LVYTB0 now reads 11x11x1.4 instead of 9x11x1.4.
June, 2004	-004	Updated Table 1 and Table 26. Added line item RD38F4460LVYGB0. Added G as an option to Figure 29 - Ordering Information. Added Figure 6, a top-top memory map diagram. Added top/top configuration feature to the title page "Product Features".
July, 2004	-005	Added the mechanical specification diagram, Figure 5 for the 11x11x1.4 mm option.
October, 2004	-006	Added line items 256L18/256V18/256SD, 256L18/256L18/256V18/256SD, and 256L18/256V18/256V18/256SD to the following tables: * **Table 1 "Available Product Ordering Information for the LVX Family with LPSDRAM" on page 12** * Table 26 "LVX Family with LPSDRAM: Available Product Ordering Information" on page 57. .

1.0 Introduction

This document provides preliminary information about the Intel StrataFlash® Wireless Memory System (LV18 SCSP) with Low-Power SDRAM (LVX family). This document describes the flash dies used in the code and large embedded data segments and the features, operations, and specifications within the subsystem. Also described in this document are the LPSDRAM characteristics and operations. The intent of this document is to provide information where these SCSP products differ from the Intel StrataFlash® Wireless Memory System (LV18) datasheet.

Refer to the latest revision of the Intel StrataFlash® Wireless Memory System Datasheet (order number 253854) for flash product details not included in this document.

1.1 Nomenclature

1.8 V Core	Voltage Range of 1.7 V – 1.95 V
1.8 V I/O	Voltage Range of 1.7 V – 1.95 V
Asserted	Signal with logical voltage level V_{IL}, or enabled
Deasserted	Signal with logical voltage level V_{IH}, or disabled
High-Z	Tri-stated or High Impedance
Low-Z	Driven
Non-Array Reads	Flash reads which return flash Device Identifier, CFI Query, Protection Register and Status Register information
Program	An operation to Write data to the flash array
Write	Bus cycle operation at the inputs of the flash die, in which a command or data are sent to the flash array
Block	Group of cells, bits, bytes or words within the flash memory array that get erased with one erase instruction
Parameter block	Any 16-Kword flash array block.
Main block	Any 64-Kword flash array block.
Top parameter	Previously referred to as a top-boot device, a device with flash parameter partition located at the highest physical address of its memory map for processor system boot up.
Bottom parameter	Previously referred to as a bottom-boot device, a device with flash parameter partition located at the lowest physical address of its memory map for processor system boot up.
Bottom-Top parameter	SCSP device configuration of two flash dies in the same segment arranged with the parameter partitions located at the lowest and highest physical address of its memory map.

Partition	A group of flash blocks that shares common Status Register read state.
Parameter partition	A flash partition containing parameter and main blocks.
Main partition	A flash partition containing only main blocks.
Die	Individual physical flash or RAM die used in a SCSP memory subsystem device
Segment	A section of the SCSP memory subsystem divided for different operating characteristics. The SCSP memory subsystem has three segments: a code segment, a data segment, and an xRAM segment.
Code segment	A segment that contains one or two flash memory dies optimized for fast code or data reads. Each die features multi-partitions synchronous read-while-write or burst read-while-erase capability.
Data segment	A segment contains one or two flash memory dies optimized for large embedded data. Each die feature single-partition asynchronous read, write, and erase operations.
xRAM segment	A segment contains one or two xRAM memory dies. The xRAM combinations could include SRAM, PSRAM, or LPSDRAM.
Subsystem	A stacked memory integration concept made up of multiple memory dies arranged in code, data, and xRAM segments.
Device	A specific stacked flash + xRAM memory density configuration combination within the LVX product family.

1.2 Acronyms

APS	Automatic Power Savings
Buffered EFP	Buffered Enhanced Factory Programming
CFI	Common Flash Interface
CR	Configuration Register
CUI	Command User Interface
DU	Do Not Use
ETOX	EPROM Tunnel Oxide
OTP	One-Time Programmable
PLR	Protection Lock Register
PR	Protection Register
RCR	Read Configuration Register
RFU	Reserved for Future Use (all unused active signals in a package ballout)

RWE	Read-While-Erase
RWW	Read-While-Write
SCSP	Stacked Chip Scale Package
SR	Status Register
SRD	Status Register Data
WSM	Write State Machine

1.3 Conventions

0x	Hexadecimal number prefix
0b	Binary number prefix
A5	Denotes one element of a signal group membership, in this case address bit 5.
ADV#	A name without a prefix denotes a global signal of the device; for example, Address Valid is global because there is no die specific reference.
bit	Binary unit, valid range [0, 1]
byte	Eight bits, valid range [0x00 - 0xFF]
Clear	Logical zero (0)
DQ[15:0]	Denotes a group of similarly named signals, such as data bus.
F[3:1]-CE#, F[2:1]-OE#	This is the method used to refer to more than one chip-enable or output enable at the same time. When each die is refer to individually, the reference will be F1-CE# and F1-OE# (for die #1), F2-CE# and F2-OE# (for die #2), and F3-CE# (for die #3), unless noted otherwise. “F” denotes the flash specific signal and “CE#” is the root signal name of the flash die Chip-Enable. Other notation includes: “S” to denote SRAM, “P” to denote PSRAM, “D” to denote LPSDRAM, and “R” to denote common RAM type signal names.
k (noun)	1000 (units)
Kb	1024 bits
KB	1024 bytes
Kbit	1024 bits
KByte	1024 bytes (8,192 bits)
Kword	1024 words (16,384 bits)
Mbit	1,048,576 bits
MByte	1,048,576 bytes (8,388,608 bits)

MWord	1,048,576 words (16,777,216 bits)
M (noun)	1 million
Mb	1,048,576 bits
MB	1,048,576 bytes
Set	Logical one (1)
SR[4]	Denotes an individual flash Status Register bit, in this case bit 4 of SR[7:0].
VCC	Signal or voltage connection
V_{CC}	Signal or voltage level
Word	Two bytes or sixteen bits, valid range [0x0000 - 0xFFFF]

2.0 Functional Overview

This section provides an overview of the features and capabilities of Intel StrataFlash® Wireless Memory System (LV18 SCSP) with Low-Power SDRAM LVX family; hereafter in this document, this device is called the LVX family with LPSDRAM device.

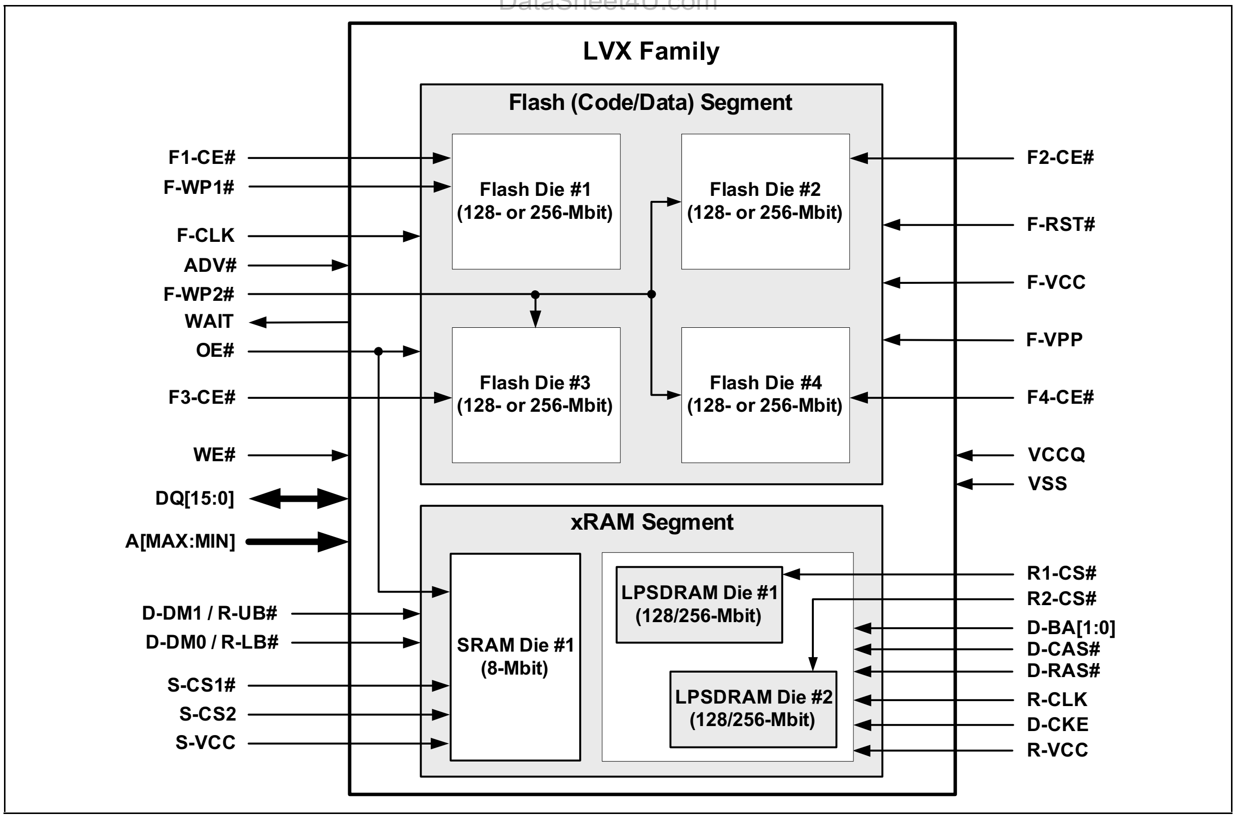
2.1 Product Description

The LVX family with LPSDRAM device incorporates flash dies used as code segment flash die and large embedded data segment flash die, along with LPSDRAM for a high performance, cost-effective high density solution. This stacked device utilizes the latest Intel StrataFlash® Wireless Memory System on 0.13 µm ETOX™ VIII process technology.

The code segment flash is a high performance, multi-partition, synchronous burst-mode Read-While-Write (RWW) or Read-While-Erase (RWE), while the large embedded data segment is a cost efficient, single partition, asynchronous memory die.

The package for this device is available in a x16D Performance ballout, supporting flash-only or flash with LPSDRAM stacked memory combinations. The Intel® SCSP package in a x16D performance ballout with a 0.8 mm ball pitch, 9 x 12 active ball matrix supports a memory subsystem up to 105 MHz on a x16-bit bus width. See Figure 1, "LVX Family with LPSDRAM Device Block Diagram" on page 11.

Figure 1. LVX Family with LPSDRAM Device Block Diagram



NOTE: You can request the stacked Flash + xRAM combinations based on memory die options shown in Figure 1. For current available Flash + xRAM combinations, refer to Table 1.

The LVX family with LPSDRAM device consists of a 1.8 V flash core device (F-V_{CC}) with 1.8 V and 3.0 V I/O options. The device is available with at least one flash die per code segment and/or one flash die per data segment. However, it has a maximum of two flash dies per code or data segments. See Table 2, "LV Flash Code and Data Die (F-CE#) Stacked Configuration" on page 15 for possible combinations.

Designed for low-voltage systems, the LVX supports read operations with F-V_{CC} at 1.8 V, and erase and program operations with F-V_{PP} at 1.8 V. Buffered Enhanced Factory Programming (Buffered EFP) provides the fastest flash array programming performance, with elevated F-V_{PP} at 9.0 V to increase factory throughput. With F-V_{PP} at 1.8 V, F-V_{CC} and F-V_{CC} can be tied together for a simple, ultra-low-power design. In addition to voltage flexibility, a dedicated F-V_{PP} connection provides complete data protection when F-$V_{PP} \leq V_{PPLK}$.

The Intel StrataFlash® Wireless Memory System provides data security through its individual zero-latency block lock capability. Each memory block can be unlocked, locked, or locked-down by hardware or software control.

Individualized F-CE# control allows the user to manage which flash die is asserted, furthering the flexibility of power management while controlling data integrity per segment with F-WP#. The F[2:1]-OE# in LVX products with a x16D Performance ballout ballout are common internally.

Table 1 lists the available LVX product family devices. If the product combinations you are seeking are not listed, the combination is not available at this time and you will need to contact your local Intel representative for details.

Table 1. Available Product Ordering Information for the LVX Family with LPSDRAM

I/O Voltage (V)	Flash Density (Mbit) and Family	RAM Density (Mbit) and RAM Type	Package			Part Number	Notes
			Size (mm)	Ballout Name	Ball Type		
1.8	256 L18 + 256 L18 + 256 V18 + 256 V18	—	11x11x1.4	x16D (103 Ball)	SCSP Leaded	RD48F4444LVYBB0 RD48F4444LVYTB0	
	256 L18 + 256 V18	128 SDRAM	9x11x1.4	x16D (103 Ball)	SCSP Leaded	RD38F4460LVYBB0 RD38F4460LVYTB0 RD38F4460LVYGB0	1
	256 L18 + 256 L18 + 256 V18	128 SDRAM	9x11x1.4	x16D (103 Ball)	SCSP Leaded	RD58F0012LVYBB0 RD58F0012LVYTB0	2
	256 L18 + 256 V18 + 256 V18	128 SDRAM	9x11x1.4	x16D (103 Ball)	SCSP Leaded	RD58F0016LVYBB0 RD58F0016LVYTB0	2

NOTES:

1. For the "custom" line item RD38F4460LVYGB0, the "G" designate the F-CE# parameter configuration where F1-CE# = Top parameter and F2-CE# = Top parameter. See Table 2 for details.
2. 58Fxxxx nomenclature is used when the stacked device has greater than three flash + RAM dies.

2.2 Unique Product Features

The code segment of the LVX includes the following enhanced features unless specifically noted otherwise:

- 64 unique (Intel pre-programmed) identifier bits and 2,112 user-programmable OTP bits for each code segment flash die.
- Traditional write, erase, and burst-mode read capabilities of Intel® Wireless Flash Memory (W18).
- Simultaneous RWW/RWE operations, enabling a burst read operation in one partition with simultaneous program or erase operations in other partitions.
- Burst-read across partition boundaries, but not across segment dies within the subsystem.
- User application code responsible for ensuring that burst-mode reads do not cross into a partition that is in program or erase mode.

The embedded data segment includes the following features unless specifically noted otherwise:

- High density offerings of up to 512 Mbits are designated specifically for large embedded data.
- Single partition asynchronous page-mode read operation, allowing for a cost-effective ideal storage format.
- Read-while-write or read-while-erase operations can be accomplished with software through program suspend and erase suspend operations.

2.3 Product Configurations and Memory Partitioning

The first flash die, by default is the first code segment flash die, which is a fast, execute-in-place (XIP) solution that is ideally suited toward an instruction fetch application. This portion is the user selected parameter configuration option, where the density can be made up of 128-Mbit dies or 256-Mbit dies, each containing one parameter partition and several main partitions.The parameter partition contains four 16-Kword parameter blocks and seven 64-Kword main blocks; all main partitions consist of eight 64-Kword main blocks.

The large embedded data die segment is a single partition asynchronous page-mode read device that is available in variations of 128-Mbit dies or 256-Mbit dies. The single partition is made up of four 16-Kword parameter blocks and 64-Kword main blocks. The data segment flash die parameter configuration will always be the opposite of the code segment flash die parameter configuration. See Table 2, "LV Flash Code and Data Die (F-CE#) Stacked Configuration" on page 15 for examples of configuration options.

Users have the choice of selecting either a top or a bottom parameter configuration for the code die segment. Depending on the choice of configuration, the data die(s) in the LVX device will be parametrically opposed. For instance, if the user selects top parameter configuration for the code die, the data die in the package will be configured as bottom parameter configuration, and vice-versa. This ensures the largest number of contiguous main block addresses for software efficiency.

The xRAM segment can consist of up to two low-power SDRAM (LPSDRAM) dies. The LPSDRAM can be either a 128-Mbit or a 256-Mbit die. For the code segment, partition configurations are as follows:

- 128-Mbit flash die partitions are 8 Mbits.
- 256-Mbit flash die partitions are 16 Mbits.
- Minimum code + data density combination is 384 Mbits.

Figure 2. Top Parameter Configurations

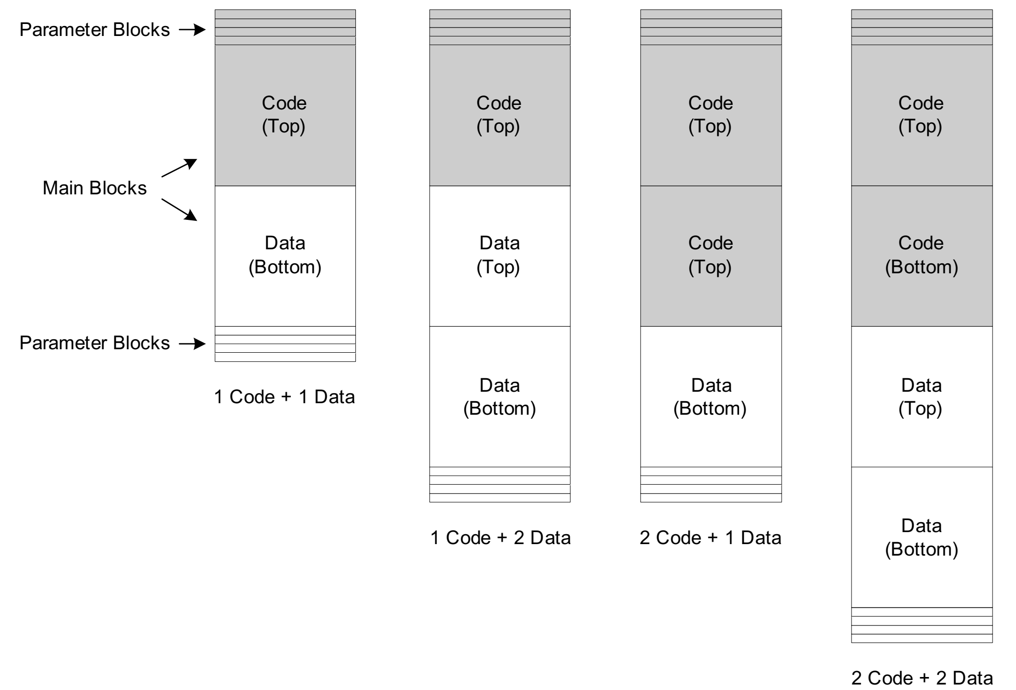


Figure 3. Bottom Parameter Configurations

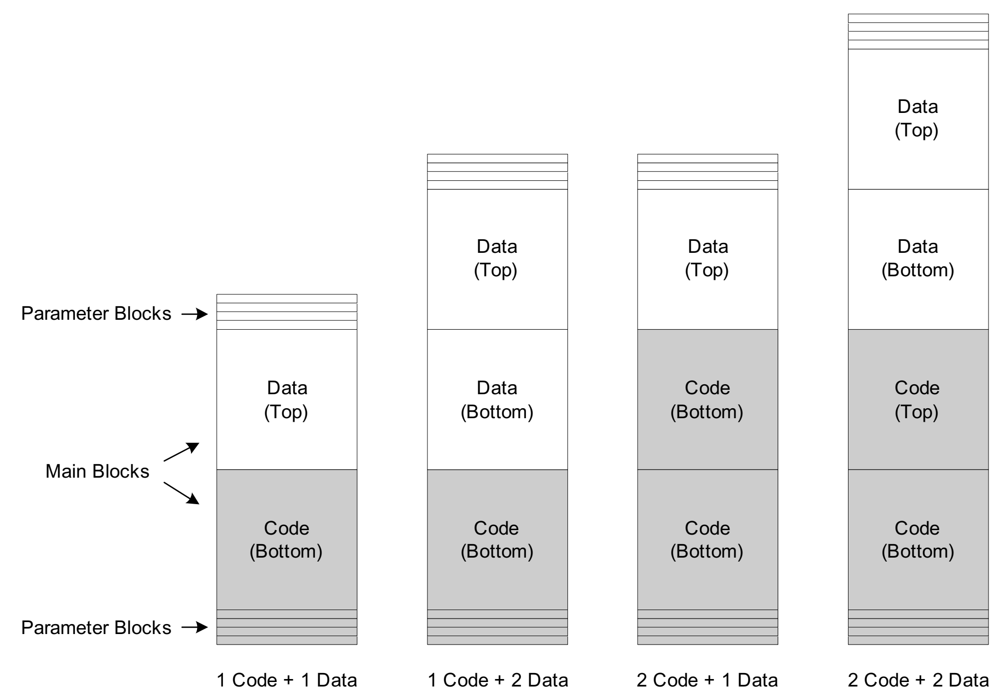


Table 2. LV Flash Code and Data Die (F-CE#) Stacked Configuration

Die Stack Configuration		Code Segment		Data Segment	
		1st Flash Code Die (user selected)	2nd Flash Code Die	1st Flash Data Die	2nd Flash Data Die
Top Parameter	Code + Data	F1-CE# (Top)	F2-CE# (Bottom)	—	—
	Code + Data + Data	F1-CE# (Top)	F2-CE# (Top)	F3-CE# (Bottom)	—
	Code + Code + Data	F1-CE# (Top)	F2-CE# (Top)	F3-CE# (Bottom)	—
	Code + Code + Data + Data	F1-CE# (Top)	F2-CE# (Bottom)	F3-CE# (Top)	F4-CE# (Bottom)
Bottom Parameter	Code + Data	F1-CE# (Bottom)	F2-CE# (Top)	—	—
	Code + Data + Data	F1-CE# (Bottom)	F2-CE# (Bottom)	F3-CE# (Top)	—
	Code + Code + Data	F1-CE# (Bottom)	F2-CE# (Bottom)	F3-CE# (Top)	—
	Code + Code + Data + Data	F1-CE# (Bottom)	F2-CE# (Top)	F3-CE# (Bottom)	F4-CE# (Top)
Top-Top Parameter (custom)	Code + Data	F1-CE# (Top)	F2-CE# (Top)	—	—
	Code + Data + Data	F1-CE# (Top)	F2-CE# (Top)	F3-CE# (Top)	—
	Code + Code + Data	F1-CE# (Top)	F2-CE# (Top)	F3-CE# (Top)	—
	Code + Code + Data + Data	F1-CE# (Top)	F2-CE# (Top)	F3-CE# (Top)	F4-CE# (Top)

Table 2 shows an example of the memory map and partitioning information for combinations with up to four flash dies in the LVX SCSP family with Synchronous LPSDRAM.

- Top parameter configuration. For two flash dies, flash die #1 (with F1-CE# as its Chip Enable) is configured as top parameter. Flash die #2 (with F2-CE# as its Chip Enable) is configured as bottom parameter.
- Bottom parameter configuration. For two flash dies, flash die #1 (with F1-CE# as its Chip Enable) is configured as bottom parameter. Flash die #2 (with F2-CE# as its Chip Enable) is configured as top parameter.
- Top-Top parameter configuration is a custom option, where all flash dies within the stacked device has the same parameter configuration. In this case, all dies are Top configured.

2.4 Memory Map

The LVX family with LPSDRAM device is available in several density and parameter configurations. The memory map is based on the stacking of individual 128- and 256-Mbit flash die density options. The memory map shows individual flash die configurations and block/partition allocations. See the following tables for further information:

- Table 3, “Code-Data (Top Parameter) SCSP Memory Map and Partitioning” on page 16
- Table 4, “Code-Data (Bottom Parameter) SCSP Memory Map and Partitioning” on page 17
- Table 5, “Code-Data (Top - Top Parameter) SCSP Memory Map and Partitioning” on page 18
- Table 6, “Code-Code-Data (Top Parameter) SCSP Memory Map and Partitioning” on page 19
- Table 7, “Code-Code-Data (Bottom Parameter) SCSP Memory Map and Partitioning” on page 20

Table 3. Code-Data (Top Parameter) SCSP Memory Map and Partitioning

Flash Die#	Die Stack Config.	Partitioning	Block Size (KW)	Partition Size (Mbit)	128-Mbit Flash Blk#	128-Mbit Flash Address Range	Partition Size (Mbit)	256-Mbit Flash Blk#	256-Mbit Flash Address Range
1	**Code (Top Parameter)**	Parameter Partition (Partition 0)	16	8	130	7FC000-7FFFFF	16	258	FFC000-FFFFFF
			⋮		⋮	⋮		⋮	⋮
			16		127	7F0000-7F3FFF		255	FF0000-FF3FFF
			64		126	7E0000-7EFFFF		254	FE0000-FEFFFF
			⋮		⋮	⋮		⋮	⋮
			64		120	780000-78FFFF		240	F00000-FFFFFF
		Main Partitions (Partition 1 to 7)	64		119	770000-77FFFF		239	EF0000-EFFFFF
			⋮		⋮	⋮		⋮	⋮
			64		64	400000-4FFFFF		128	800000-80FFFF
		Main Partitions (Partition 8 to 15)	64		63	3F0000-3FFFFF		127	F70000-F7FFFF
			⋮		⋮	⋮		⋮	⋮
			64		0	000000-00FFFF		0	000000-00FFFF
2	**Data (Bottom Parameter)**	Single Partition 4x16 Kword Parameter Blocks 127x64 Kword Main Blocks (128 Mb) 255x64 Kword Main Blocks (256 Mb)	64	128	130	7F0000-7FFFFF	256	258	FF0000-FFFFFF
			⋮		⋮	⋮		⋮	⋮
			64		67	400000-40FFFF		131	800000-80FFFF
			64		66	3F0000-3FFFFF		130	7F0000-7FFFFF
			⋮		⋮	⋮		⋮	⋮
			64		11	080000-08FFFF		19	100000-10FFFF
			64		10	070000-07FFFF		18	0F0000-0FFFFF
			⋮		⋮	⋮		⋮	⋮
			64		4	010000-01FFFF		4	010000-01FFFF
			16		3	00C000-00FFFF		3	00C000-00FFFF
			⋮		⋮	⋮		⋮	⋮
			16		0	000000-003FFF		0	000000-003FFF

Table 4. Code-Data (Bottom Parameter) SCSP Memory Map and Partitioning

Flash Die#	Die Stack Config.	Partitioning	Block Size (KW)	Partition Size (Mbit)	128-Mbit Flash		Partition Size (Mbit)	256-Mbit Flash	
					Blk#	Address Range		Blk#	Address Range
2	Data (Top Parameter)	Single Partition 4x16 Kword Parameter Blocks 127x64 Kword Main Blocks (128 Mb) 255x64 Kword Main Blocks (256 Mb)	16	8	130	7FC000-7FFFFF	16	258	FFC000-FFFFFF
			⋮		⋮	⋮		⋮	⋮
			16		127	7F0000-7F3FFF		255	FF0000-FF3FFF
			64		126	7E0000-7EFFFF		254	FE0000-FEFFFF
			⋮		⋮	⋮		⋮	⋮
			64		120	780000-78FFFF		240	F00000-FFFFFF
			64		119	770000-77FFFF		239	EF0000-EFFFFF
			⋮		⋮	⋮			⋮
			64		64	400000-4FFFFF		128	800000-80FFFF
			64		63	3F0000-3FFFFF		127	F70000-F7FFFF
			⋮		⋮	⋮		⋮	⋮
			64		0	000000-00FFFF		0	000000-00FFFF
1	Code (Bottom Parameter)	Main Partitions (Partitions 8 to 15)	64	128	130	7F0000-7FFFFF	256	258	FF0000-FFFFFF
			⋮		⋮	⋮		⋮	⋮
			64		67	400000-40FFFF		131	800000-80FFFF
		Main Partitions (Partitions 1 to 7)	64		66	3F0000-3FFFFF		130	7F0000-7FFFFF
			⋮		⋮	⋮		⋮	⋮
			64		11	080000-08FFFF		19	100000-10FFFF
		Parameter Partition (Partition 0)	64		10	070000-07FFFF		18	0F0000-0FFFFF
			⋮		⋮	⋮		⋮	⋮
			64		4	010000-01FFFF		4	010000-01FFFF
			16		3	00C000-00FFFF		3	00C000-00FFFF
			⋮		⋮	⋮		⋮	⋮
			16		0	000000-00FFFF		0	000000-00FFFF

Table 5. Code-Data (Top - Top Parameter) SCSP Memory Map and Partitioning

Flash Die#	Die Stack Config.	Partitioning	Block Size (KW)	Partition Size (Mbit)	128-Mbit Flash Blk#	128-Mbit Flash Address Range	Partition Size (Mbit)	256-Mbit Flash Blk#	256-Mbit Flash Address Range
1	Code (Top Parameter)	Parameter Partition (Partition 0)	16	8	130	7FC000-7FFFFF	16	258	FFC000-FFFFFF
			⋮		⋮	⋮		⋮	⋮
			16		127	7F0000-7F3FFF		255	FF0000-FF3FFF
			64		126	7E0000-7EFFFF		254	FE0000-FEFFFF
			⋮		⋮	⋮		⋮	⋮
			64		120	780000-78FFFF		240	F00000-FFFFFF
		Main Partitions (Partition 1 to 7)	64		119	770000-77FFFF		239	EF0000-EFFFFF
			⋮		⋮	⋮		⋮	⋮
			64		64	400000-4FFFFF		128	800000-80FFFF
		Main Partitions (Partition 8 to 15)	64		63	3F0000-3FFFFF		127	F70000-F7FFFF
			⋮		⋮	⋮		⋮	⋮
			64		0	000000-00FFFF		0	000000-00FFFF
2	Data (Top Parameter)	Single Partition 4x16 Kword Parameter Blocks 127x64 Kword Main Blocks (128 Mb) 255x64 Kword Main Blocks (256 Mb)	16	8	130	7FC000-7FFFFF	16	258	FFC000-FFFFFF
			⋮		⋮	⋮		⋮	⋮
			16		127	7F0000-7F3FFF		255	FF0000-FF3FFF
			64		126	7E0000-7EFFFF		254	FE0000-FEFFFF
			⋮		⋮	⋮		⋮	⋮
			64		120	780000-78FFFF		240	F00000-FFFFFF
			64		119	770000-77FFFF		239	EF0000-EFFFFF
			⋮		⋮	⋮			⋮
			64		64	400000-4FFFFF		128	800000-80FFFF
			64		63	3F0000-3FFFFF		127	F70000-F7FFFF
			⋮		⋮	⋮		⋮	⋮
			64		0	000000-00FFFF		0	000000-00FFFF

Table 6. Code-Code-Data (Top Parameter) SCSP Memory Map and Partitioning

Flash Die#	Die Stack Config.	Partitioning	Block Size (KW)	Partition Size (Mbit)	128-Mbit Flash Blk#	128-Mbit Flash Address Range	Partition Size (Mbit)	256-Mbit Flash Blk#	256-Mbit Flash Address Range
1	**Code (Top Parameter)**	Parameter Partition (Partition 0)	16	8	130	7FC000-7FFFFF	16	258	FFC000-FFFFFF
			⋮		⋮	⋮		⋮	⋮
			16		127	7F0000-7F3FFF		255	FF0000-FF3FFF
			64		126	7E0000-7EFFFF		254	FE0000-FEFFFF
			⋮		⋮	⋮		⋮	⋮
			64		120	780000-78FFFF		240	F00000-FFFFFF
		Main Partitions (Partition 1 to 7)	64		119	770000-77FFFF		239	EF0000-EFFFFF
			⋮		⋮	⋮		⋮	⋮
			64		64	400000-4FFFFF		128	800000-80FFFF
		Main Partitions (Partition 8 to 15)	64		63	3F0000-3FFFFF		127	F70000-F7FFFF
			⋮		⋮	⋮		⋮	⋮
			64		0	000000-00FFFF		0	000000-00FFFF
2	**Code (Top Parameter)**	Parameter Partition (Partition 0)	16	8	130	7FC000-7FFFFF	16	258	FFC000-FFFFFF
			⋮		⋮	⋮		⋮	⋮
			16		127	7F0000-7F3FFF		255	FF0000-FF3FFF
			64		126	7E0000-7EFFFF		254	FE0000-FEFFFF
			⋮		⋮	⋮		⋮	⋮
			64		120	780000-78FFFF		240	F00000-FFFFFF
		Main Partitions (Partition 1 to 7)	64		119	770000-77FFFF		239	EF0000-EFFFFF
			⋮		⋮	⋮		⋮	⋮
			64		64	400000-4FFFFF		128	800000-80FFFF
		Main Partitions (Partition 8 to 15)	64		63	3F0000-3FFFFF		127	F70000-F7FFFF
			⋮		⋮	⋮		⋮	⋮
			64		0	000000-00FFFF		0	000000-00FFFF
3	**Data (Bottom Parameter)**	Single Partition 4x16 Kword Parameter Blocks 127x64 Kword Main Blocks (128 Mb) 255x64 Kword Main Blocks (256 Mb)	64	128	130	7F0000-7FFFFF	256	258	FF0000-FFFFFF
			⋮		⋮	⋮		⋮	⋮
			64		67	400000-40FFFF		131	800000-80FFFF
			64		66	3F0000-3FFFFF		130	7F0000-7FFFFF
			⋮		⋮	⋮		⋮	⋮
			64		11	080000-08FFFF		19	100000-10FFFF
			64		10	070000-07FFFF		18	0F0000-0FFFFF
			⋮		⋮	⋮		⋮	⋮
			64		4	010000-01FFFF		4	010000-01FFFF
			16		3	00C000-00FFFF		3	00C000-00FFFF
			⋮		⋮	⋮		⋮	⋮
			16		0	000000-003FFF		0	000000-003FFF

Note: Other stacked memory combinations and parameter configurations can be created based on the memory map and partitions highlighted from Table 3 to Table 7.

Table 7. Code-Code-Data (Bottom Parameter) SCSP Memory Map and Partitioning

Flash Die#	Die Stack Config.	Partitioning	Block Size (KW)	Partition Size (Mbit)	128-Mbit Flash		Partition Size (Mbit)	256-Mbit Flash	
					Blk#	Address Range		Blk#	Address Range
3	Data (Top Parameter)	Single Partition 4x16 Kword Parameter Blocks 127x64 Kword Main Blocks (128 Mb) 255x64 Kword Main Blocks (256 Mb)	16	8	130	7FC000-7FFFFF	16	258	FFC000-FFFFFF
			⋮		⋮	⋮		⋮	⋮
			16		127	7F0000-7F3FFF		255	FF0000-FF3FFF
			64		126	7E0000-7EFFFF		254	FE0000-FEFFFF
			⋮		⋮	⋮		⋮	⋮
			64		120	780000-78FFFF		240	F00000-FFFFFF
			64		119	770000-77FFFF		239	EF0000-EFFFFF
			⋮		⋮	⋮		⋮	⋮
			64		64	400000-4FFFFF		128	800000-80FFFF
			64		63	3F0000-3FFFFF		127	F70000-F7FFFF
			⋮		⋮	⋮		⋮	⋮
			64		0	000000-00FFFF		0	000000-00FFFF
2	Code (Bottom Parameter)	Main Partitions (Partition 8 to 15)	64		130	7F0000-7FFFFF		258	FF0000-FFFFFF
			⋮		⋮	⋮		⋮	⋮
			64		67	400000-40FFFF		131	800000-80FFFF
		Main Partitions (Partition 1 to 7)	64		66	3F0000-3FFFFF		130	7F0000-7FFFFF
			⋮		⋮	⋮		⋮	⋮
			64		11	080000-08FFFF		19	100000-10FFFF
		Parameter Partition (Partition 0)	64		10	070000-07FFFF		18	0F0000-0FFFFF
			⋮		⋮	⋮		⋮	⋮
			64		4	010000-01FFFF		4	010000-01FFFF
			16		3	00C000-00FFFF		3	00C000-00FFFF
			⋮		⋮	⋮		⋮	⋮
			16		0	000000-003FFF		0	000000-003FFF
1	Code (Bottom Parameter)	Main Partitions (Partition 8 to 15)	64		130	7F0000-7FFFFF		258	FF0000-FFFFFF
			⋮		⋮	⋮		⋮	⋮
			64		67	400000-40FFFF		131	800000-80FFFF
		Main Partitions (Partition 1 to 7)	64		66	3F0000-3FFFFF		130	7F0000-7FFFFF
			⋮		⋮	⋮		⋮	⋮
			64		11	080000-08FFFF		19	100000-10FFFF
		Parameter Partition (Partition 0)	64		10	070000-07FFFF		18	0F0000-0FFFFF
			⋮		⋮	⋮		⋮	⋮
			64		4	010000-01FFFF		4	010000-01FFFF
			16		3	00C000-00FFFF		3	00C000-00FFFF
			⋮		⋮	⋮		⋮	⋮
			16		0	000000-003FFF		0	000000-003FFF

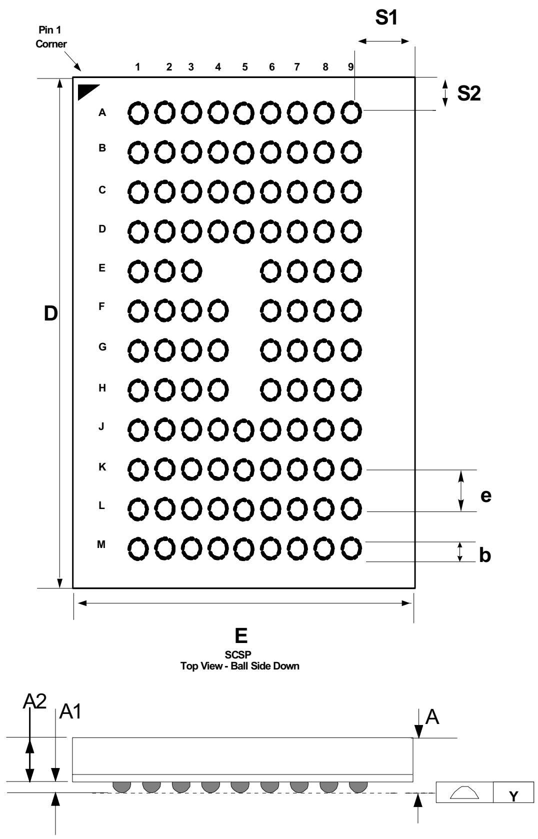
Note: Other stacked memory combinations and parameter configurations can be created based on the memory map and partitions highlighted from Table 3 to Table 7.

3.0 Package Information

LVX family with LPSDRAM device is available in the following standard SCSP x 16D Performance ballout packages:

- Figure 4, "LVX Family with LPSDRAM Device SCSP x16D Performance Drawing 9x11x1.4 mm" on page 21
- Figure 5, "LVX Family with LPSDRAM Device SCSP x16D Performance Drawing 11x11x1.4 mm" on page 22

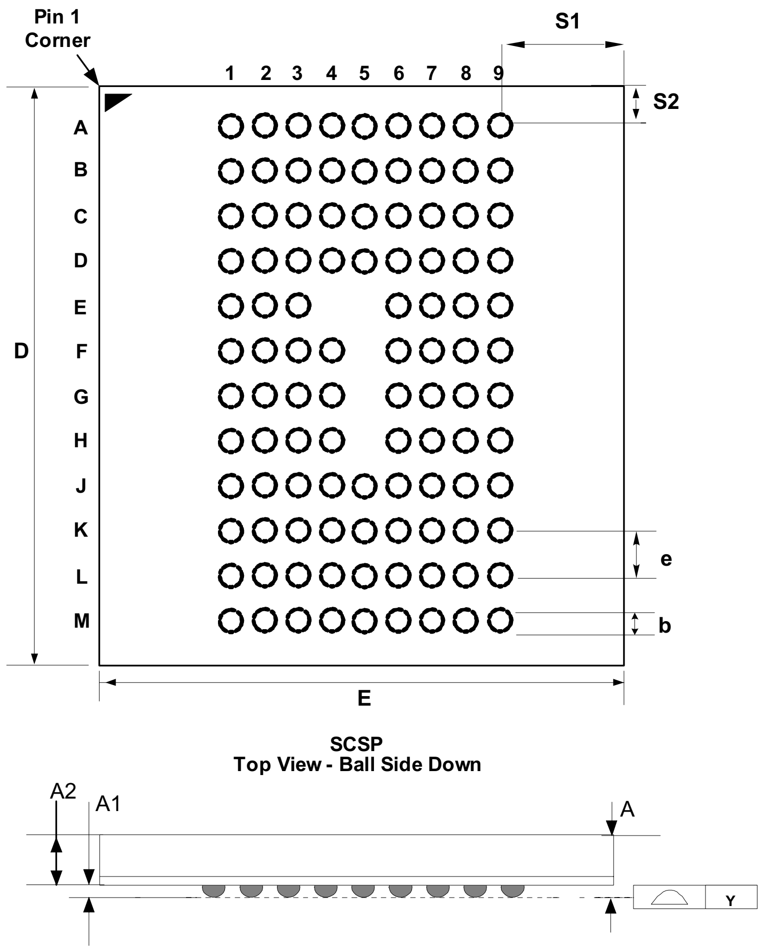
Figure 4. LVX Family with LPSDRAM Device SCSP x16D Performance Drawing 9x11x1.4 mm



Note: Drawing not to scale.

Dimensions	Symbol	Min	Nom	Max	Notes	Min	Nom	Max
Package Height	A			1.4				0.0551
Ball Height	A1	0.200				0.0079		
Package Body Thickness	A2		1.070				0.0421	
Ball (Lead) Width	b	0.325	0.375	0.425		0.0128	0.0148	0.0167
Package Body Length	D	10.90	11.00	11.10		0.4291	0.4331	0.4370
Package Body Width	E	8.90	9.00	9.10		0.3504	0.3543	0.3583
Pitch	e		0.800				0.0315	
Ball (Lead) Count	N		103				103	
Seating Plane Coplanarity	Y			0.100				0.0039
Corner to Ball Distance Along E	S1	1.200	1.300	1.400		0.0472	0.0512	0.0551
Corner to Ball Distance Along D	S2	1.000	1.100	1.200		0.0394	0.0433	0.0472

Figure 5. LVX Family with LPSDRAM Device SCSP x16D Performance Drawing 11x11x1.4 mm



Note: Drawing not to scale.

		Millimeters				Inches		
Dimensions	Symbol	Min	Nom	Max	Notes	Min	Nom	Max
Package Height	A			1.4				0.0551
Ball Height	A1	0.200				0.0079		
Package Body Thickness	A2		1.070				0.0421	
Ball (Lead) Width	b	0.325	0.375	0.425		0.0128	0.0148	0.0167
Package Body Length	D	10.90	11.00	11.10		0.4291	0.4331	0.4370
Package Body Width	E	10.90	11.00	11.10		0.4291	0.4331	0.4370
Pitch	e		0.800				0.0315	
Ball (Lead) Count	N		103				103	
Seating Plane Coplanarity	Y			0.100				0.0039
Corner to Ball Distance Along E	S1	2.200	2.300	2.400		0.0866	0.0906	0.0945
Corner to Ball Distance Along D	S2	1.000	1.100	1.200		0.0394	0.0433	0.0472

4.0 Ballout and Signal Descriptions

4.1 Signal Ballout

Intel StrataFlash® Wireless Memory System family is available in a x16D Performance ballout, shown in Figure 6, “x16D (103 Ball) Performance Signal Ballout for LVX Device Family” The single package ballout is ideal for space-constrained board applications where density upgrades without PCB redesign is preferred. The user must adapt for density upgrade flexibility in the PCB design.

Figure 6. x16D (103 Ball) Performance Signal Ballout for LVX Device Family

Pin 1

	1	2	3	4	5	6	7	8	9	
A	DU	A5	A7	A8	A20	A24	A25	A26	DU	A
B	A3	A4	A6	A18	A19	RFU	A23	A27	A17	B
C	A2	VSS	VSS	VSS	R-VCC	VSS	VSS	VSS	A16	C
D	A1	S-VCC	R-VCC	F-VCC	ADV#	F-VCC	R-VCC	RFU	A15	D
E	F-WP1#	WE#	R2-CS#	Depop		F4-CE# / A28	A22	A11	A14	E
F	F-WP2#	R1-CS#	D-CAS#	D-RAS#	Depop (RFUs)	S-CS1#	A21	A10	A13	F
G	RFU	F2-CE#	F1-CE#	D-BA0		D-CKE	F-RST#	A9	A12	G
H	RFU	S-CS2	F3-CE#	D-BA1		RFU	OE#	D-DM1 / R-UB#	D-DM0 / R-LB#	H
J	F-VPP	VCCQ	VCCQ	F-VCC	R-CLK	F-VCC	VCCQ	VCCQ	WAIT	J
K	DQ2	VSS	VSS	VSS	F-CLK	VSS	VSS	VSS	DQ13	K
L	DQ1	DQ3	DQ5	DQ6	DQ7	DQ9	DQ11	DQ12	DQ14	L
M	DU	DQ0	RFU	DQ4	DQ8	DQ10	RFU	DQ15	DU	M
	1	2	3	4	5	6	7	8	9	

Top View - Ball Side Down

Legend:	
	Active Balls
	De-Populated Balls
	Reserved for Future Use
	Do Not Use

4.2 Signal Descriptions

Table 8 describes the active signals used on the LVX family with LPSDRAM device.

Table 8. Signal Descriptions (Sheet 1 of 3)

Symbol	Type	Description	Notes
A[MAX:1]	Input	**ADDRESS:** Global device signals. Share inputs for all memory die addresses during read and write operations. LPSDRAM Address inputs also provide the op-code during a Mode Register Set or Special Mode Register Set command. • 256-Mbit die: AMAX = A24 • 128-Mbit die: AMAX = A23 • 64-Mbit die: AMAX = A22 • 32-Mbit die: AMAX = A21 • 8-Mbit die: AMAX = A19 • A[13:1] are the row and A[9:1] are the column addresses for 256-Mbit LPSDRAM • A[12:1] are the row and A[9:1] are the column addresses for 128-Mbit LPSDRAM • A11 defines the Auto Precharge. During a LPSDRAM Precharge command, A11 is sampled to determine if all banks are to be precharged (A11 = high).	1,2
DQ[15:0]	Input/ Output	**DATA INPUT/OUTPUTS:** Global device signals. Inputs data and commands during write cycles, outputs data during read cycles. Data signals float when the device or its output are deselected. Data are internally latched during writes on the device.	
ADV#	Input	**ADDRESS VALID:** Low-true input. (For stacked combinations without Synchronous PSRAM, ADV# is a flash-specific input.) During synchronous flash read operations, addresses are latched on the rising edge of ADV#, or on the next valid CLK edge, whichever occurs first. In asynchronous flash read operation, addresses are latched on the rising edge ADV#, or are continuously flow-through when ADV# is kept asserted.	
F[4:1]-CE#	Input	**FLASH CHIP ENABLE:** Low-true input. F[4:1]-CE# low selects the associated flash memory die. F[4:1]-CE# high deselects the associated flash die. When deasserted, the associated flash die is deselected, power is reduced to standby levels, data and WAIT outputs are placed in high-Z state. • F1-CE# is dedicated as flash Code die #1. • F[4:2]-CE# controls any subsequent flash die based on the user ordered SCSP flash type combination. • Any unused F-CE# should be pulled high to F-VCC through a 1K-ohm resistor for future design flexibility.	3
F-CLK, R-CLK	Input	**DEVICE CLOCK:** Synchronizes the selected memory die to the system bus clock in synchronous operations. Performance ballout: • F-CLK is a flash signal. Synchronizes the flash die to the system flash bus frequency in synchronous operations. • R-CLK is a LPSDRAM input signal. Synchronizes the LPSDRAM die to the system's memory bus clock. LPSDRAM is sampled on the positive edge of R-CLK.	
OE#	Input	**OUTPUT ENABLE:** Global device signal. Low-true input. OE# low enables the output drivers of the selected die. OE# high places the output drivers of the selected die in high-Z.	
F-RST#	Input	**FLASH RESET:** Flash specific signal. Low-true input. F-RST# low resets internal operations and inhibits write operations. F-RST# high enables normal operation. Exit from reset places the flash device in Asynchronous Read Array mode.	
WAIT	Output	**DEVICE WAIT:** Selectable high-true or low-true output. (For stacked combinations without Synchronous PSRAM, WAIT is a flash specific input.) During synchronous-burst reads (array or non-array), WAIT-asserted indicates invalid read data. During Asynchronous Page reads and writes, WAIT is deasserted. Wait is High-Z whenever F-CE# or F-OE# / OE# is deasserted.	

Table 8. Signal Descriptions (Sheet 2 of 3)

Symbol	Type	Description	Notes
WE#	Input	**WRITE ENABLE:** Global device signal. Low-true input. WE# low selects the associated memory die for write operation. WE# high deselect the associated memory die, data are placed in high-Z state. With LPSDRAM operation, WE# is latched on the positive clock edge in conjunction with the D-RAS# and D-CAS# signals. The WE# input is used to select the Bank Activate or Precharge command and Read or Write command.	
F-WP[2:1]#	Input	**WRITE PROTECT:** Low-true input. F-WP# controls the lock-down protection mechanism of the selected flash die. When low, F-WP# enables the lock-down mechanism where locked down blocks cannot be unlocked with software commands. When high, F-WP# disables the lock-down mechanism, allowing locked down blocks to be unlocked with software commands. F-WP1# controls the code segment flash die #1, while F-WP2# controls subsequent code or data segment flash dies.	
D-CKE	Input	**LPSDRAM Clock Enable:** High-true input • If D-CKE goes low synchronously with clock, the internal clock is suspended from the next clock cycle. • The state of the outputs and the burst address is halted. • When all banks are in the idle state, D-CKE is high, the LPDRAM enters into Power-Down and Self Refresh modes. • D-CKE is synchronous except after the device enters Power-Down and Self Refresh modes, where D-CKE becomes asynchronous until exiting the same mode. The input buffers, including R-CLK, are disabled during Power-Down and Self Refresh modes, providing low standby power.	
D-BA[1:0]	Input	**LPSDRAM Bank Select:** D-BA0 and D-BA1 defines to which bank the Bank Activate, Read, Write, or Bank Precharge command is being applied. The bank address D-BA0 and D-BA1 is used latched in Mode Register set.	
D-RAS#	Input	**LPSDRAM Row Address Strobe:** Low-true input. • The D-RAS# signal defines the operation commands, with the D-CAS# and WE# signals. • The D-RAS# is latched at the rising edges of R-CLK. When D-RAS# and Dx-CS# / Rx-CS# are asserted and D-CAS# is deasserted, either the Bank Activate command or the Precharge command is selected by the WE# signal. • WE# is deasserted, the Bank Activate command is selected and the bank designated by D-BA[1:0] is turned on to the active state.	
D-CAS#	Input	**LPSDRAM Column Address Strobe:** Low-true input. • D-CAS# signal defines the operation commands in conjunction with the D-RAS# and WE# signals and is latched at the rising edges of R-CLK. • D-RAS# is deasserted and Dx-CS# / Rx-CS# is asserted, the column access is started by asserting D-CAS#. Read or Write command then is selected by asserting WE# low or high.	
R[2:1]-CS#	Input	**RAM Chip Select:** Low-true input. x16D Performance ballout: • R[2:1]-CS# R[2:1]-CS# low selects the associated LPSDRAM memory die. All commands are masked when R[2:1]-CS# high. R[2:1]-CS# provides for external bank selection on systems with multiple banks. It is considered part of the command code. • R1-CS# controls LPSDRAM die #1. • R2-CS# controls LPSDRAM die #2.	

Table 8. Signal Descriptions (Sheet 3 of 3)

Symbol	Type	Description	Notes
D-DM[1:0]	Input	**LPSDRAM Data Input/Output Mask:** Data Input Mask. • D-DM[1:0] are byte selects. Input data is masked when D-DM[1:0] are sampled high during a write cycle. D-DM1 masks DQ[15-8], and D-DM0 masks DQ[7-0]. • The D-DM[1:0] latency for Read is 2 Clocks and for Write is 0 Clocks.	4
S-CS1# S-CS2	Input	**SRAM CHIP SELECTS:** SRAM specific signal. Low-true input. When both SRAM chip selects are asserted, SRAM internal control logic, input buffers, decoders, and sense amplifiers are active. When either or both SRAM chip selects are deasserted (S-CS1# = V_{IH} and/or S-CS2 = V_{IH}), the SRAM is deselected and its power is reduced to standby levels. S-CS1# and S-CS2 are available on stacked combinations with SRAM die, and are RFU on stacked combinations without SRAM die.	
R-UB# R-LB#	Input	**SRAM UPPER/ LOWER BYTE ENABLES:** Low - true inputs. • During SRAM read and write cycles, R-UB# low enables the SRAM high-order byte on DQ[15:8], and R-LB# low enables the SRAM low-order byte on DQ[7:0]. R-UB# and R-LB# are available on stacked combinations with SRAM die, and are RFUs on stacked combinations without SRAM die.	3,4
F-VPP	Power	**FLASH ERASE/ PROGRAM Voltage Level:** Flash specific signal. Valid F-VPP voltage on this ball allows block erase or program functions. Flash memory array contents cannot be altered when F-$V_{PP} \le V_{PPLK}$. Block erase and program at invalid F-VPP voltage should not be attempted.	
F-VCC	Power	**FLASH CORE Voltage Level:** Flash specific signals. Flash core source voltage. Flash operations are inhibited when F-$V_{CC} \le V_{LKO}$. Operations at invalid F-VCC voltage should not be attempted.	
VCCQ	Power	**OUTPUT Voltage Level:** Global device signals. Device output-driver source voltage. This balls can be tied directly to the respective memory type x-VCC if operating within its x-VCC range.	
D-VCC, R-VCC	Power	**RAM Power Supply:** Supplies power to the RAM dies. Performance ballout: • D-VCC supplies power for LPSDRAM operation. x16D Performance ballout: • R-VCC supplies power for xRAM operation.	
S-VCC	Power	**SRAM Power Supply:** Supplies power to the SRAM die. S-VCC is available on stacked combinations with SRAM die, and is RFU on stacked combinations without SRAM die.	
VSS	Power	**Ground:** Connect to system ground. Do not float any VSS connection.	
DU	—	**Do Not Use:** This ball must be left floating. This ball should not be connected to any power supplies, signals, or other balls.	
RFU	—	**Reserved for Future Use:** Reserved by Intel for future device functionality and enhancement.	

NOTE:
1. All unused signals or RFUs should be held either to a static VIL or VIH for future design flexibility and migrations.
2. A1 is the lowest order x16 address.
3. F4-CE# is a shared signal with A28 for the 103-Active Ball High Performance DRAM package.
4. D-DM[1:0] are shared signals with R-UB# and R-LB# respectively.

5.0 Maximum Ratings and Operating Conditions

5.1 Absolute Maximum Ratings

Warning: Stressing the device beyond the “Absolute Maximum Ratings” may cause permanent damage. These are stress ratings only.

NOTICE: This document contains information available at the time of its release. The specifications are subject to change without notice. Verify with your local Intel sales office that you have the latest datasheet before finalizing a design.

Table 9. Absolute Maximum Ratings

Parameter	Min	Max	Unit	Notes
Temperature under Bias Expanded	–25	+85	°C	
Storage Temperature	–55	+125	°C	
Voltage On Any Signal (except F-V_{CC}, F-V_{PP}, R-V_{CC} and V_{CCQ})	–0.2	+2.1	V	1
F-V_{CC} Voltage	–0.2	+2.50	V	1
V_{CCQ}, R-V_{CC} Voltage	–0.2	+2.45	V	1
F-V_{PP} Voltage	–0.2	+10.0	V	1,2,3
I_{SH} Output Short Circuit Current	–	50	mA	4

NOTES:
1. Voltage is referenced to V_{SS}.
2. During power transitions, minimum DC voltage may undershoot to –2.0 V for periods < 20 ns; maximum DC voltage may overshoot to V_{CC} (operating max) + 2.0 V for periods < 20 ns.
3. During power transitions, minimum DC voltage may undershoot to –1.0 V for periods < 20 ns; maximum DC voltage may overshoot to V_{CCQ} (operating max) + 1.0 V for periods < 20 ns.
4. During power transitions, minimum DC voltage may undershoot to –2.0 V for periods < 20 ns; maximum DC voltage may overshoot to V_{PP2} (operating max) + 2.0 V for periods < 20 ns.
5. F-VPP can be V_{PP2} for 1000 cycles on main blocks, 2500 cycles on parameter blocks.
6. Output shorted for no more than one second. No more than one output shorted at a time.

5.2 Operating Conditions

Warning: Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

Table 10. Extended Temperature Operation

Symbol	Parameter		Flash + xRAM Min	Flash + xRAM Max	Units
T_C	Operating Temperature		–25	+85	°C
F-V_{CC}	Flash Supply Voltage		1.7	2.0	V
V_{CCQ} R-V_{CC}	Flash and LPSDRAM I/O Voltage LPSDRAM Supply Voltage		1.7	1.9	V
V_{PPL}	F-V_{PP} Voltage Supply (Logic Level)		0.9	2	V
V_{PPH}	Factory word programming F-V_{PP}		8.5	9.5	V
Block Erase Cycles	Main and Parameter Blocks	F-V_{PP} = F-V_{CC}	100,000	—	Cycles
	Main Blocks	F-V_{PP} = V_{PPH}	—	1000	
	Parameter Blocks	F-V_{PP} = V_{PPH}	—	2500	

NOTE: Operating voltage are for flash + flash only stacked device. Refer to document numbers 253852 and 253853 for flash + RAM stacked combinations.

6.0 Electrical Specifications

6.1 DC Voltage and Current Characteristics

Refer to the *Intel StrataFlash® Wireless Memory (L18) Datasheet* (order number 251902) for flash DC characteristics. Table 11, "LPSDRAM DC Characteristics" and Table 12, "LPSDRAM Self Refresh Current" on page 30 show DC voltage and current characteristics for LPSDRAM.

The DC current characteristics referenced in this document are for individual flash and RAM die in the SCSP device. The total device current is determined by sum of the active and inactive currents of each flash and RAM die in the SCSP device.

NOTICE: Individual DC Characteristics of all dies in a SCSP device need to be considered accordingly, depending on the SCSP device stacked combinations and operations.

Table 11. LPSDRAM DC Characteristics (Sheet 1 of 2)

Parameter	Description	Test Conditions and Density		Min	Typ	Max	Unit	Notes
D-V_{CC} / R-V_{CC}	Voltage Range			1.7	1.8	1.9	V	
I_{CC1} (One Bank Active)	Operating Current at min cycle time Burst Length = 1	I_{IO} = 0mA t_{CK} = min	128-Mbit	—	—	60	mA	
			256-Mbit	—	—	75		
I_{CC2P}	Precharge Standby Current: Power-Down Mode (All banks idle)	D-CKE = L, Dx-CS#/Rx-CS# = H t_{CK} = min	128-Mbit	—	—	600	µA	
			256-Mbit	—	—	700		
I_{CC2N}	Precharge Standby Current: Non-Power-Down Mode (All banks idle)	D-CKE = H, Dx-CS# = H t_{CK} = min	128-Mbit	—	—	15	mA	
			256-Mbit	—	—	15		
I_{CC3P}	Active Standby Current in Power-Down Mode (All banks active)	D-CKE = L, t_{CK} = min	128-Mbit	—	—	5	mA	
			256-Mbit	—	—	5		
I_{CC3N}	Active Standby Current: Non-Power-Down Mode (All banks active)	D-CKE = H, t_{CK}=min	128-Mbit	—	—	20	mA	3
			256-Mbit	—	—	25		
I_{CC4} (4 Banks active)	Operating Current Page Burst Mode	I_{IO} = 0mA t_{CK} = min	128-Mbit	—	—	70	mA	
			256-Mbit	—	—	80		
I_{CC5}	Auto Refresh Current	$t_{RC} > t_{RCmin}$	128-Mbit	—	—	130	mA	2
			256-Mbit	—	—	150		
I_{CC6}	Self Refresh Current	Address & Data toggling at min cycle time	128-Mbit	—	—	500	µA	4
			256-Mbit	—	—	600		
I_{CC7}	Deep Power-Down Current	Address & Data toggling at min cycle time	128-Mbit	—	—	10	µA	
			256-Mbit	—	—	10		
V_{OH}	Output High Voltage	I_{OH} = -100 µA	—	V_{CCQ} – 0.2	—	—	V	

Table 11. LPSDRAM DC Characteristics (Sheet 2 of 2)

V_{OL}	Output Low Voltage	I_{OL} = 100 µA, V_{CCQmin}	—	–0.1	—	0.2	V	
V_{IH}	Input High Voltage	—	—	V_{CCQ} – 0.3	—	V_{CCQ} + 0.2	V	
V_{IL}	Input Low Voltage	—	—	-0.2	—	0.3	V	
I_{IL}	Input Leakage Current	–0.2 V < V_{IN} < V_{CCQ}+0.2 V	—	–1.5	—	+1.5	µA	1

NOTES:
1. Input leakage currents include Hi-Z output leakage for bi-directional buffers with tri-state outputs.
2. Input signals are toggled at max frequency to simulate SCSP condition, where another device may be active.
3. No accesses in progress.
4. See Table 12, “LPSDRAM Self Refresh Current” on page 30.

Table 12. LPSDRAM Self Refresh Current

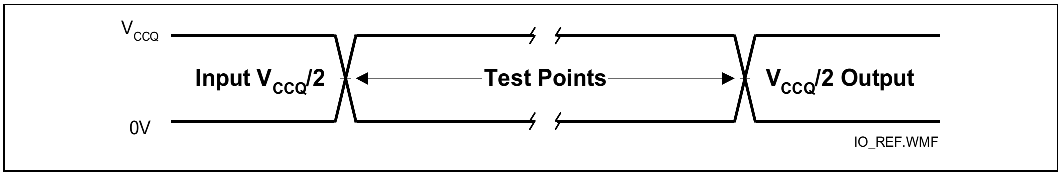
Parameter	Description	Test Condition	Set Temperature	# of Banks			Unit
				All Banks Refreshed	Banks 0 & 1 Refreshed	Bank 0 Refreshed	
I_{CC6} (128-Mbit)	Self Refresh Current (All Banks Refreshed)	D-CKE < 0.2V t_{CK} = Infinity	85 °C max	500	400	300	µA
			70 °C max	440	350	280	
			45 °C max	390	290	260	
			15 °C max	350	240	240	
I_{CC6} (256-Mbit)	Self Refresh Current (All Banks Refreshed)	D-CKE < 0.2V t_{CK} = Infinity	85 °C max	600	450	315	µA
			70 °C max	525	375	295	
			45 °C max	450	300	270	
			15 °C max	375	250	250	

NOTE: Other than I_{CC6} for all Banks at 85 °C, the Self Refresh currents are verified during device characterization and not 100% tested.

7.0 AC Characteristics

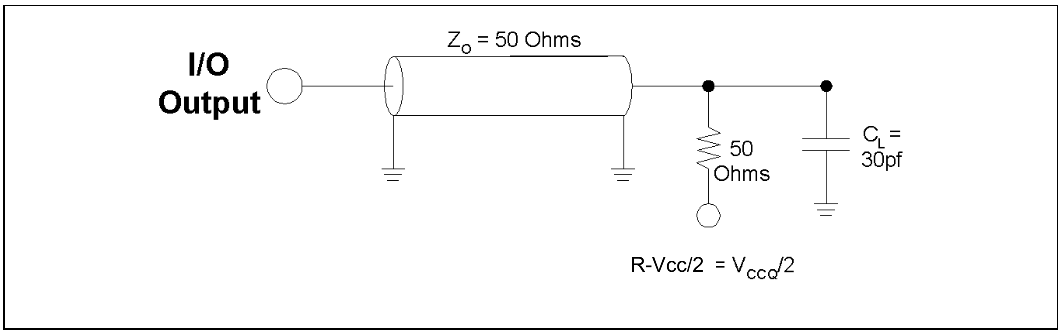
7.1 Device AC Test Conditions

Figure 7. AC Input/Output Reference Waveform



NOTE: AC test inputs are driven at V_{CCQ} for Logic "1" and 0.0 V for Logic "0." Input/output timing begins/ends at $V_{CCQ}/2$. Input rise and fall times (10% to 90%) < 5 ns. Worst case speed occurs at $F\text{-}V_{CC} = F\text{-}V_{CC\,MIN}$.

Figure 8. Transient Equivalent Testing Load Circuit[1,2]



NOTES:
1. Test configuration component value for worst case speed conditions.
2. C_L includes jig capacitance.

7.2 Capacitance

NOTICE: Refer to the Intel StrataFlash® Wireless Memory System datasheet (order number 253854) for flash capacitance details.

Table 13. LPSDRAM Capacitance

Symbol	Parameter	MAX	Unit	Condition
C_{IN}	Input Capacitance	5	pF	V_{IN} = 0 V
C_{OUT}	Output Capacitance	7	pF	V_{OUT} = 0 V

NOTE: Sampled, not 100% tested. T_C = +25 °C, f = 1 MHz.

7.3 Flash AC Read Operations

Refer to the Intel StrataFlash® Wireless Memory System datasheet (order number 253854) for flash read and write AC Characteristics.

7.4 Flash AC Write Operations

Refer to the Intel StrataFlash® Wireless Memory System datasheet (order number 253854) for flash read and write AC Characteristics.

7.5 LPSDRAM AC Characteristics

Table 14, "LPSDRAM AC Characteristics—Read-Only Operations" on page 32 and Table 15, "LPSDRAM AC Characteristics—Write Operations" on page 33 list the AC characteristics for the LPSDRAM die.

Table 14. LPSDRAM AC Characteristics—Read-Only Operations (Sheet 1 of 2)

Symbol	Parameter		Min	Max	Unit
t_{RC}	Clock Cycle Time	CL = 3 (125 MHz)	9.5 (105)	—	ns
		CL = 2 (100 MHz)	15 (66)	—	
		CL = 1 (50 MHz)	—	—	
t_{CKH}	Clock High Level Pulse Width		3	—	ns
t_{CKL}	Clock Low Level Pulse Width		3	—	ns
t_T	Transition Time		0.5	1.0	ns
t_{CKEH}	D-CKE Hold Time		1	—	ns
t_{CKES}	D-CKE Setup Time		2	—	ns
t_{AH}	Address Hold Time		1	—	ns
t_{AS}	Address Setup Time		2	—	ns
t_{IH}	Data Input Hold Time		1	—	ns
t_{IS}	Data Input Setup Time		2	—	ns
t_{CMH}	Dx-CS#,D-RAS#,D-CAS#,WE#,D-DM Hold time		1	—	ns
t_{CMS}	Dx-CS#,D-RAS#,D-CAS#,WE#,D-DM Setup time		2	—	ns
t_{AC}	Clock to valid output delay (positive edge of clock)	CL = 3	—	7	ns
		CL = 2	—	9	
		CL = 1	—	—	
t_{OH}	Data Out Hold Time		2.5	—	ns
t_{LZ}	Clock to Output in Low-Z		1	—	ns
t_{HZ}	Clock to Output in High-Z	CL = 3	—	7	ns
		CL = 2	—	9	
		CL = 1	—	—	
t_{RAS}	Row Active time (Active to Precharge cmd)		60	100k	ns
t_{RC}	Row Cycle time (Active to Active cmd on same bank)		90	—	ns
t_{RCD}	Row to column delay (Active to Read/Write)		30	—	ns
t_{RP}	Row Precharge Time		30	—	ns
t_{REF}	Refresh Period (4096 rows)		—	64	ms

Table 14. LPSDRAM AC Characteristics—Read-Only Operations (Sheet 2 of 2)

Symbol	Parameter	Min	Max	Unit
t_{RFC}	Auto Refresh Period	110	—	ns
t_{SREX}	Self Refresh Exit time (Self refresh to Active)	120	—	ns

NOTES:
1. The minimum number of clock cycles is determined by dividing the minimum time required by clock cycle time.
2. LPSDRAM AC specs are guaranteed only when Normal Output Driver Strength is used. See Table 25.

Table 15. LPSDRAM AC Characteristics—Write Operations

Symbol	Parameter		Min	Max	Unit
t_{WR}	Write Recovery Time		20	—	ns
t_{RRD}	Active bank a to Active Bank b command		20	—	ns
t_{DAL}	Last data input to Active Delay		—	$t_{WR} + t_{RP}$	
t_{CDL}	Last data input to New Read/Write Command		—	1	t_{CK}
t_{BDL}	Last data input to Burst Terminate Command		—	1	t_{CK}
t_{CCD}	Read/Write command to Read/Write command		—	1	t_{CK}
t_{DQW}	D-DM write mask latency		—	0	t_{CK}
t_{DQZ}	D-DM data out mask latency		—	2	t_{CK}
t_{MRD}	Load Mode Register Command to Active/Refresh Command		—	2	t_{CK}
t_{WR}	Write Recovery Time	$t_{WR} / t_{CK} < 1$	—	1	t_{CK}
		$1 < t_{WR} / t_{CK} < 2$	—	2	
t_{PHZ}	Data out to High Z from Precharge command	CL = 3	—	3	t_{CK}
		CL = 2	—	2	
		CL = 1	—	—	
t_{INI}	Initialization Delay		200	—	µs

NOTES:
1. The minimum number of clock cycles is determined by dividing the minimum time required by clock cycle time.
2. LPSDRAM AC specs are guaranteed only when Normal Output Driver Strength is used. See Table 25.

8.0 Power and Reset Specifications

Refer to the latest revision of the *Intel StrataFlash® Wireless Memory System (LV18/LV30 SCSP; 1024-Mbit LV Family Datasheet* (order number 253854) for details not included in this document.

9.0 Operations Overview

9.1 Bus Operations

Bus operations for this L18 SCSP LVX family (x16) device involve the control of flash and LPSDRAM inputs. The bus operations and commands are shown in the following tables:

- Table 16, "Flash and LPSDRAM Bus Operations" on page 35
- Table 17, "LPSDRAM Functional Mode Description: Current State bank n, Command to Bank n" on page 38
- Table 18, "LPSDRAM Functional Mode: Current State bank n, Command to Bank m" on page 39

Fully synchronous operations are performed by the LPSDRAM to latch the commands at the positive edges of R-CLK. Refer to the *Intel StrataFlash® Wireless Memory (L18) Datasheet* (order number 251902) for complete descriptions of flash modes and commands, command bus-cycle definitions and flowcharts that illustrate operational routines.

Table 16, "Flash and LPSDRAM Bus Operations" summarizes the bus operations and voltage levels that must be applied to individual flash die in each mode.

Refer to the *Intel StrataFlash® Wireless Memory System Datasheet* (order number 253854) for complete descriptions of flash modes and commands, for command bus-cycle definitions, and flowcharts that illustrate operational routines.

Each flash die within the LVX system shares basic asynchronous read and write operations unless otherwise specified.

Table 16. Flash and LPSDRAM Bus Operations (Sheet 1 of 3)

Device	Mode	F-RST#	Fx-CE#	OE#	ADV#	F-VPP	WAIT	WE#	$D\text{-}CKE_{n-1}$	$D\text{-}CKE_n$	Dx-CS#	D-RAS#	D-CAS#	D-DM[1:0]	D-BA[1:0]	A11	Address	Data	Notes
Flash Die (Code)	Sync Array Read	H	L	L	L	X	Active	H										Flash D_{OUT}	1,4,6, 16
	Async Read	H	L	L	X	X	Deasserted	H	LPSDRAM outputs must be in High-Z									Flash D_{OUT}	1,4,5, 6,16
	Write	H	L	H	L	V_{PP1}/ V_{PP2}	High-Z	L										Flash D_{IN}	2,3,5, 6
	Output Disable	H	L	H	X	X	High-Z	H										Flash High-Z	6
	Standby	H	H	X	X	X	High-Z	X	Any LPSDRAM mode allowed									Flash High-Z	6
	Reset	L	X	X	X	X	High-Z	X										Flash High-Z	6
Flash Die (Data)	Sync Array Read	H	L	L	L	X	Deasserted	H										Flash D_{OUT}	1,4,6, 16
	Async Read	H	L	L	X	X	Deasserted	H	LPSDRAM outputs must be in High-Z									Flash D_{OUT}	1,4,5, 6,16
	Write	H	L	H	L	V_{PP1}/ V_{PP2}	Deasserted	L										Flash D_{IN}	2,3,5, 6
	Output Disable	H	L	H	X	X	High-Z	H										Flash High-Z	6
	Standby	H	H	X	X	X	High-Z	X	Any LPSDRAM mode allowed									Flash High-Z	6
	Reset	L	X	X	X	X	High-Z	X										Flash High-Z	6

Table 16. Flash and LPSDRAM Bus Operations (Sheet 2 of 3)

Device	Mode	F-RST#	Fx-CE#	OE#	ADV#	F-VPP	WAIT	WE#	D-CKE$_{n-1}$	D-CKE$_n$	Dx-CS#	D-RAS#	D-CAS#	D-DM[1:0]	D-BA[1:0]	A11	Address	Data	Notes
LPSDRAM Die (#1 or #2)	Active	Flash outputs must be in High-Z						H	H	X	L	L	H	X	V	Row Address		RAM D_{OUT}	6,7
	Read							H	H	X	L	H	L	L/H	V	L	Col Addr	RAM D_{OUT}	6,7,8, 10
	With Auto Precharge															H			
	Write							L	H	X	L	H	L	L/H	V	L	X	RAM D_{IN}	6,9,10
	With Auto Precharge															H			
	Burst Stop							L	H	H	L	H	H	X	X	X	X	RAM High-Z	6
	Precharge One Bank							L	H	X	L	L	H	X	V	L	X	RAM High-Z	6
	All Banks														X	H			
	Auto Refresh	Flash must be in High-Z						H	H	H	L	L	L	X	X	X	X	RAM High-Z	6,13
	Self Refresh Entry							H	H	L	L	L	L	X	X	X	X	RAM High-Z	6,13
	Self Refresh Exit							H	L	H	L	H	H	X	X	X	X	RAM High-Z	6
		Any flash mode allowed						X			H	X	X						

Table 16. Flash and LPSDRAM Bus Operations (Sheet 3 of 3)

Device	Mode	F-RST#	Fx-CE#	OE#	ADV#	F-VPP	WAIT	WE#	D-CKE$_{n-1}$	D-CKE$_n$	Dx-CS#	D-RAS#	D-CAS#	D-DM[1:0]	D-BA[1:0]	A11	Address	Data	Notes
LPSDRAM Die (#1 or #2)	Load Mode Register	Flash outputs must be in High-Z						L	H	X	L	L	L	X	Operand Code			RAM High-Z	6,11,12
	Input/ Output Enable							X	H	X				L	X			RAM High-Z	6,10
	Input Inhibit/ Output High-Z	Any flash mode allowed						X	H	X				H	X			RAM High-Z	6,10
	Clock Suspend Entry							X	H	L	H	X	X	X	X	X	X	RAM High-Z	6,14
		Flash outputs must be in High-Z						V			L	V	V						
	Clock Suspend Exit							X	L	H	X	X	X	X	X	X	X	RAM High-Z	6
	Power-Down Entry	Any flash mode allowed						X	H	L	H	X	X	X	X	X	X	RAM High-Z	6,15
		Flash outputs must be in High-Z						H			L	H	H						
	Power-Down Exit	Any flash mode allowed						X	L	H	H	X	X	X	X	X	X	RAM High-Z	6
		Flash outputs must be in High-Z						H			L	H	H						
	Deep Power-Down Entry							L	H	L	L	H	H	X	X	X	X	RAM High-Z	6
	Deep Power-Down Exit							X	L	H	X	X	X	X	X	X	X	RAM High-Z	6
	Device Deselect	Any flash mode allowed						X	H	X	H	X	X	X	X	X	X	RAM High-Z	6
	No Operation	Flash outputs must be in High-Z						H	H	X	L	H	H	X	X	X	X	RAM High-Z	6

NOTES:
1. WAIT is only valid during synchronous flash reads. Refer to the discrete datasheet for detailed WAIT functionality.
2. OE# and WE# (Flash and SRAM) should never be asserted simultaneously.
3. X can be V_{IL} or V_{IH} for inputs, V_{PP1}, V_{PP2} or V_{PPLK} for F-V_{PP}.
4. Flash CFI query and Status Register accesses use DQ[7:0] only, all other reads use DQ[15:0].
5. Refer to L18 datasheets for valid D_{IN} during flash writes.
6. All states and sequences not shown are illegal or reserved.
7. A[13:1] provide row address for 256-Mbit LPSDRAM. A[12:1] provide row address for 128-Mbit LPSDRAM. A[9:1] provide column address for 128-Mbit or 256-Mbit LPSDRAM.
8. Select bank and column address, and start Read. A11 High enables auto precharge.
9. Select bank and column address, and start Write. A11 High enables auto precharge.
10. Activate or deactivate the data during Writes with zero-clock delay and during Reads with two-clock delay. D-DM0 corresponds to DQ[7:0], D-DM1 corresponds to DQ[15:8].
11. A[11:1] define the operand code to the register
12. Extended Mode Register is programmed by setting D-BA1=H and D-BA0=L. For Mode register programming, set D-BA1=D-BA0=L
13. All banks must be precharged before issuing an Auto-refresh command.
14. Clock suspend mode occurs when Column access or burst is in progress
15. Power-Down occurs when no accesses are in progress.
16. Data segment flash only operates in Asynchronous mode, F-CLK is ignored and WAIT is deasserted.

Table 17. LPSDRAM Functional Mode Description: Current State bank *n*, Command to Bank *n*

Current State	Dx-CS#	D-RAS#	D-CAS#	WE#	Command	Action	Notes
Any	H	X	X	X	No Operation	Continue previous Operation	
	L	H	H	H	No Operation	Continue previous Operation	
Idle	L	L	H	H	Active	Select and activate row	
	L	L	L	H	Auto refresh	Auto refresh	
	L	L	L	L	Load Mode register	Mode register set	
	L	L	H	L	Precharge	NOP	
Row Active	L	H	L	H	Read	Select Column & start read burst	
	L	H	L	L	Write	Select Column & start write burst	
	L	L	H	L	Precharge	Deactivate Row in bank (or banks)	3
Read (without Auto precharge)	L	H	L	H	READ	Truncate READ & start new READ burst	5
	L	H	L	L	WRITE	Truncate READ & start new WRITE burst	5
	L	L	H	L	PRECHARGE	Truncate READ, start PRECHARGE	
	L	H	H	L	Burst Terminate	Burst terminate	
Write (without Auto precharge)	L	H	L	H	READ	Truncate WRITE & start new READ burst	5
	L	H	L	L	WRITE	Truncate WRITE & start new WRITE burst	5
	L	L	H	L	PRECHARGE	Truncate WRITE, start PRECHARGE	
	L	H	H	L	Burst Terminate	Burst terminate	

NOTES:
1. The table applies when both $D\text{-}CKE_{n-1}$ and $D\text{-}CKE_n$ are high.
2. All states and sequences not shown are illegal or reserved.
3. This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for precharging.
4. A command other than No Operation (NOP), should not be issued to the same bank while a READ or WRITE Burst with auto precharge is enabled.
5. The new Read or Write command could be auto precharge enabled or auto precharge disabled.

Table 18. LPSDRAM Functional Mode: Current State bank *n*, Command to Bank *m*

Current State	Dx-CS#	D-RAS#	D-CAS#	WE#	Command	Action	Notes
Any	H	X	X	X	No Operation	Continue previous Operation	
	L	H	H	H	No Operation	Continue previous Operation	
Idle	X	X	X	X	Any	Any command allowed to bank m	
Row Activating, Active, or Precharging	L	L	H	H	Active	Activate Row	
	L	H	L	H	Read	Start READ burst	
	L	H	L	L	WRITE	Start WRITE burst	
	L	L	H	L	Precharge	Precharge	
Read with Auto Precharge disabled	L	L	H	H	Active	Activate Row	
	L	H	L	H	Read	Start READ burst	
	L	H	L	L	WRITE	Start WRITE burst	
	L	L	H	L	Precharge	Precharge	
Write with Auto precharge disabled	L	L	H	H	Active	Activate Row	
	L	H	L	H	Read	Start READ burst	
	L	H	L	L	WRITE	Start WRITE burst	
	L	L	H	L	Precharge	Precharge	
Read with Auto Precharge	L	L	H	H	Active	Activate Row	
	L	H	L	H	Read	Start READ burst	
	L	H	L	L	WRITE	Start WRITE burst	
	L	L	H	L	Precharge	Precharge	
Write with Auto precharge	L	L	H	H	Active	Activate Row	
	L	H	L	H	Read	Start READ burst	
	L	H	L	L	WRITE	Start WRITE burst	
	L	L	H	L	Precharge	Precharge	

NOTES:
1. The table applies when both $D\text{-}CKE_{n-1}$ and $D\text{-}CKE_n$ are high.
2. All states and sequences not shown are illegal or reserved.

10.0 Flash Read Operations

Refer to the Intel StrataFlash® Wireless Memory System datasheet (order number 253854) for information regarding flash read modes and operations.

11.0 Flash Program Operations

Refer to the *Intel StrataFlash® Wireless Memory System* datasheet (order number 253854) for information regarding flash program operations.

12.0 Flash Erase Operations

Refer to the *Intel StrataFlash® Wireless Memory System* datasheet (order number 253854) for information regarding flash erase operations.

13.0 Flash Suspend and Resume Operations

Refer to the *Intel StrataFlash® Wireless Memory System* datasheet (order number 253854) for information regarding flash security modes and operations.

14.0 Flash Block Locking and Unlocking Operations

Refer to the *Intel StrataFlash® Wireless Memory System* datasheet (order number 253854) for information regarding flash Read Configuration Register (RCR) functions and programming.

15.0 Flash Protection Register Operations

Refer to the *Intel StrataFlash® Wireless Memory System* datasheet (order number 253854) for information regarding flash power considerations and consumption.

16.0 Flash Configuration Operations

Refer to the *Intel StrataFlash® Wireless Memory System* datasheet (order number 253854) for information regarding flash Read Configuration Register (RCR) functions and programming.

17.0 Flash Dual Operation Considerations

Refer to the Intel StrataFlash® Wireless Memory System datasheet (order number 253854) for information regarding flash Read Configuration Register (RCR) functions and programming.

18.0 LPSDRAM Operations

18.1 LPSDRAM Power-up Sequence and Initialization

The LPSDRAM must be powered up and initialized in a predefined manner. Once power is applied to D-VCC and VCCQ simultaneously, and the clock is stable, the LPSDRAM requires a t_{INI} delay prior to issuing any command other than the NOP command. The NOP command should be applied at least once during the t_{INI} delay. After the t_{INI} delay, a Precharge command should be applied to precharge all banks. This must be followed by two back to back Auto Refresh cycles. After the Auto Refresh cycles are complete, the Mode registers must be programmed. The Mode Register will power up in an unknown state. The Mode Register and the Extended Mode Register should be loaded prior to issuing any operational commands.

18.2 LPSDRAM Mode Register

The Mode Register is used to define specific modes of operation of the LPSDRAM. This definition includes the selection of a burst length, burst type, a CAS latency, and a write burst mode. The Mode Register settings are illustrated in the Table below. The Mode Register is programmed by the Load Mode Register command and will retain the information until it is reprogrammed, the device loses power, or the device goes in Deep Power-Down mode. The register should be loaded when all banks are idle, and subsequent operation should only be initiated after t_{MRD}.

Addresses A[12:11, 9:8] must be set to 0 for all Mode Register programming. D-BA[1:0] should be set to (0,0) to differentiate from Extended Mode Register Programming.

Table 19. LPSDRAM Setting for Burst Length

Burst Length		A3	A2	A1
A4 = 0	A4 = 1			
1	1	0	0	0
2	2	0	0	1
4	4	0	1	0
8	8	0	1	1
Full Page	Reserved	1	1	1

NOTES:
1. States not mentioned are undefined.
2. The sequential burst will wrap on reaching the last column of the burst length.

Table 20. LPSDRAM Setting for Burst Type

A4	Burst Type
0	Sequential
1	Interleaved

Table 21. LPSDRAM Setting for CAS Latency

A7	A6	A5	CAS Latency
0	0	1	1
0	1	0	2
0	1	1	3

NOTE: States not mentioned are undefined.

Table 22. LPSDRAM Setting for Write Burst Mode

A10	Write Burst Mode
0	Programmed Burst
1	Single Word Burst

18.3 Extended Mode Register

The Extended Mode Register (EMR) controls two power saving functions:

- Temperature-Compensated Self Refresh (TCSR)
- Partial Array Self Refresh (PASR)

Both these features can only be used when the device is under Self Refresh. In addition the Configurable Output Driver Strength can be programmed through the EMR. The EMR is programmed by the Load Mode Register command and will retain the information until it is reprogrammed, the device loses power, or the device goes into Deep Power-Down mode. The register should be loaded when all banks are idle, and subsequent operation should only be initiated after t_{MRD}.

To program the EMR, bank addresses D-BA1 = 1, and D-BA0 = 0 should be used. Addresses A[12:6] should be set to '0'.

Table 23. LPSDRAM Setting for Partial Array Refresh

A3	A2	A1	Self-Refresh Coverage
0	0	0	Four Banks
0	0	1	Two Banks (Bank 0 & Bank 1)
0	1	0	One Bank (Bank 0)

Table 24. LPSDRAM Setting for Temperature-Compensated Self Refresh

A5	A4	Maximum Ambient Temperature
1	1	85 °C
0	0	70 °C
0	1	45 °C
1	0	15 °C

Table 25. Configurable Output Driver Strength

A7	A6	Strength	Output Load (pF)
0	0	Normal	30
0	1	Half	TBD
1	0	Reserved	NA
1	1	Reserved	NA

NOTE: LPSDRAM AC specs are guaranteed only when Normal Output Driver Strength is used.

18.4 LPSDRAM Commands and Operations

18.4.1 LPSDRAM No Operation / Device Deselect

The LPSDRAM device includes a Device Deselect (NOP) command and a No Operation (NOP) command.

18.4.1.1 Device Deselect (NOP)

The Device Deselect (NOP) command deselects the LPSDRAM by preventing new commands from being executed. Operations already in progress are not affected.

18.4.1.2 No Operation (NOP)

The No Operation (NOP) command is used on a LPSDRAM device that is selected (D-CS# / R-DS# is low). Operations already in progress are not affected.

18.4.2 LPSDRAM Active

The Active command is used to activate a row in particular bank for a subsequent read or write access. The value of the bank D-BA[1:0] and the row address needs to be provided. The row remains active until a precharge command is issued to the bank. A Precharge command must be issued before opening a different row in the same bank.

More than one bank can be active at any time. A Read or Write command could be issued to that row, subject to the t_{RCD} specification. t_{RCD} (min) should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the Active command on which the read/write can be entered. A subsequent Active command to another row in the same bank can be issued only after the previous row has been closed. The minimum time interval between two successive Active commands on the same bank is defined by t_{RC}. The minimum time interval between two successive Active commands on the different banks is defined by t_{RRD}. This is illustrated in Figure 11, "Active Command and Read Access Command Issued to 2 Different Banks" on page 47.

18.4.3 LPSDRAM Read

The Read command is used to initiate a burst read to an active row. The value of D-BA[1:0] selects the bank and address inputs select the starting column location. The value of A11 determines whether or not auto precharge is used. Output data appears on the data bus, subject to the logic level on the D-DM[1:0] inputs two clocks earlier. D-DM[1:0] latency for the Read command is 2 clock cycles.

The burst length is set in the Mode Register. The starting column and bank address is provided along with the auto precharge option. During read bursts, the starting valid data-out corresponding to the starting column address will be available after CAS latency cycles after the Read command. Each subsequent data-out will be valid by the next positive edge of the clock. This is shown in Figure 12, "Example of CAS Latency 2" on page 47 with a CAS latency of 2.

Data from a read burst may be truncated by a subsequent Read command. The first data from the new burst follows either the last element of a completed burst or the last desired element of a longer burst that is being truncated. The new Read command can be issued as early as CL-1 cycles before the last desired element. This is shown in Figure 13, "Consecutive Read Bursts with CL = 2" on page 48.

Figure 14, "Random Read Access with CL = 2" on page 48 shows random access reads. These can be issued to the same or different banks.

A read burst can be terminated by a subsequent Write command, and data from a fixed length read burst can be followed by a Write command. The Write command can be initiated on the clock edge immediately following the last data element from the read burst, provided I/O contention can be avoided. D-DM[1:0] can be used to control I/O contention as shown in Figure 15, "Read to Write Command" on page 48. D-DM[1:0] latency is 2 clocks for output buffers masking, so the D-DM[1:0] signal must be set high at least 2 clocks prior to the Write command. D-DM[1:0] latency for Write is zero clocks, so D-DM[1:0] must be set low before Write command to ensure data written is not masked.

A read burst may be followed by or truncated with a Precharge command, which could be issued CL-1 cycles before the last desired element. This is shown in Figure 16, "Read Command Followed by Precharge" on page 49.

Following a Precharge command, another command to the same bank cannot be issued until t_{RP} is met. Similarly a Burst Terminate command can be used to stop a burst as shown in Figure 17, "Read Followed by Burst Terminate" on page 49.

18.4.4 LPSDRAM Write

The Write command initiates a burst write access to an active row. The value of D-BA[1:0] selects the bank. Address inputs select the starting column location. The value of A11 determines whether or not auto precharge is used. Input data appearing on the data bus, is written to the memory array subject to the D-DM[1:0] input logic level appearing coincident with the data. D-DM[1:0] latency for Write command is 0 clock cycles.

The burst length is set in the Mode Register. The starting column and bank address is provided along with the auto precharge option. The first valid data-in is registered coincident with the Write command. Subsequent data elements will be registered on each successive positive clock edge. Figure 18, "Random Write to 4 Word Bursts" on page 49 shows 2 consecutive 4 word write bursts.

A write burst may be followed by or truncated with a Precharge command to the same bank. The Precharge should be issued t_{WR} after the clock edge after the last desired input data is entered. In addition, when truncating a Write burst, the D-DM[1:0] signal must be used to mask input data for the clock edge coincident with the Precharge command. This is shown in the following:

- Figure 19, "Write to Precharge Command Where Write Recovery Takes 1 Clock Cycle" on page 50
- Figure 20, "Write to Precharge Command Where Write Recovery Takes 2 Clock Cycles" on page 50

where t_{WR} corresponds to either 1 or 2 clock cycles, respectively.

Following the Precharge command, a subsequent command cannot be issued to the same bank until t_{RP} is met. Write Burst can be truncated with a Burst Terminate command. While truncating, the input data being applied coincident to the Burst Terminate will be ignored.

Data for any Writes may be truncated by a subsequent Read command as shown in Figure 21, "Write Command Followed by Read Command" on page 50. Once the Read command is registered, the data inputs will be ignored.

18.4.5 LPSDRAM Power-Down

Power-down occurs if D-CKE is set low coincident with Device Deselect or NOP command and when no accesses are in progress.

- If power-down occurs when all banks are idle, it is Precharge Power-Down.
- If power-down occurs when one or more banks are active, it is referred to as Active power-down. The device cannot stay in this mode for longer than the refresh period (64ms) without losing data.

The power-down state is exited by setting D-CKE high while issuing a Device Deselect or NOP command. This is shown in Figure 22, "Precharge Power-Down Mode" on page 51.

18.4.6 LPSDRAM Deep Power-Down

The Deep Power-Down (DPD) mode enables very low standby currents. All internal voltage generators inside the LPSDRAM are stopped and all memory data are lost in this mode. To enter the DPD mode, all banks must be precharged, prior to the DPD command. To exit this mode, the D-CKE is taken high after the clock is stable.

18.4.7 LPSDRAM Clock Suspend

This mode occurs when a column access or burst is in progress, and D-CKE is set low. The internal clock gets suspended freezing the LPSDRAM logic. Any command or data present on the input pins at the time of suspended internal clock is ignored. The output data on the pins stays frozen. This mode is exited by setting D-CKE high, which results in the operation being resumed. Figure

23, “Clock Suspend During Write Burst” on page 51 shows a clock suspend during a Write burst and Figure 24, “Clock Suspend During Read Burst (CL = 2)” on page 52 shows a clock suspend during a Read burst.

18.4.8 LPSDRAM Precharge

The Precharge is used to deactivate an active row in a particular bank or active row in all banks. The banks will be available for row access after a specified time (t_{RP}) after the Precharge command is issued. If one bank is to precharged, the particular bank address needs to be addressed. If all banks are to be precharged, A11 should be set high along with the Precharge command.

18.4.9 LPSDRAM Auto Precharge

Auto Precharge is accomplished when A11 is high, to enable auto precharge in conjunction with a specific read or write command. This precharges the row after the read or write burst is complete. Auto precharge ensures that a precharge is initiated at the earliest valid stage within a burst. Another command to the same bank must not be issued until the precharge time (t_{RP}) is completed. Auto precharge does not apply in full-page burst mode. Auto precharge is non- persistent.

18.4.10 LPSDRAM Concurrent Auto Precharge

If an access command with Auto Precharge enabled is being executed, it can be interrupted by another access command.

Figure 25, “Read with Auto Precharge to Bank n Interrupted by Read to Bank m” on page 52 shows a Read with Auto Precharge to Bank n, interrupted by a Read (with or without Auto precharge) to bank m. The Read to bank m will interrupt the Read to Bank n, CAS latency later. The precharge to bank n will begin when the Read to bank m is registered.

Figure 26, “Read with Auto Precharge to Bank n Interrupted by Write to Bank m” on page 53 shows a Read with Auto Precharge to Bank n, interrupted by a Write (with or without Auto precharge) to bank m. The precharge to bank n will begin when the Write to bank m is registered. D-DM[1:0] should be set high 2 clock before the Write command to prevent bus contention.

Figure 27, “Write with Auto Precharge to Bank n Interrupted by Read to Bank m” on page 53 shows a Write with Auto Precharge to Bank n, interrupted by a Read (with or without Auto precharge) to bank m. The new command initiates bank n Write recovery (t_{WR}) followed by precharge. The last valid data-in to bank n is 1 clock prior to the Read to bank m.

Figure 28, “Write with Auto Precharge to Bank n Interrupted by Write to Bank m” on page 53 shows a Write with Auto Precharge to Bank n, interrupted by a Write (with or without Auto precharge) to bank m. The new command initiates bank n Write recovery (t_{WR}) followed by precharge. The last valid data-in to bank n is 1 clock prior to the Write to bank m.

Figure 9. Auto Refresh Cycles with D-CKE High

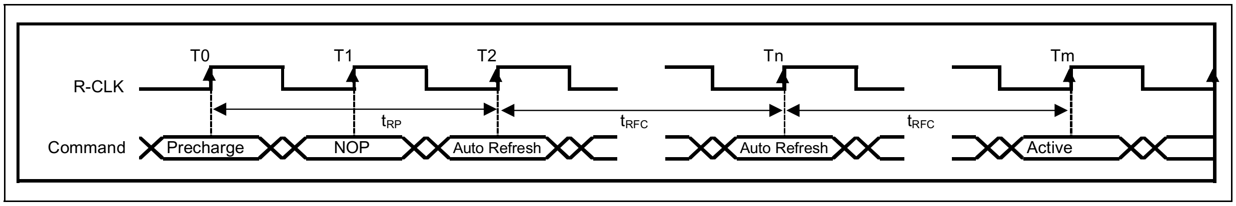


Figure 10. Self Refresh Entry and Exit Mode

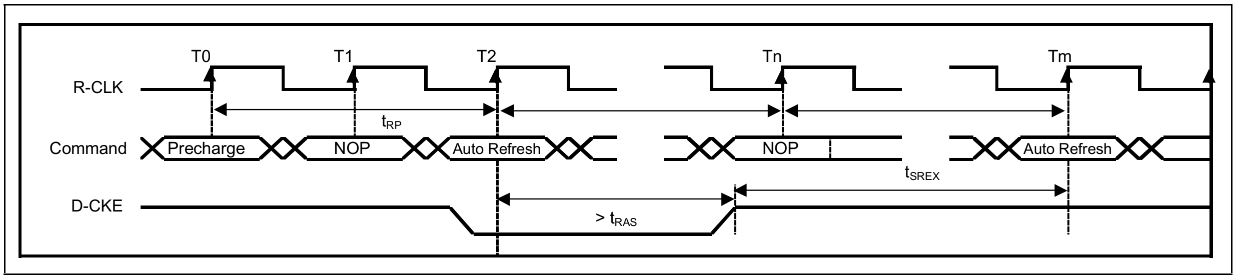


Figure 11. Active Command and Read Access Command Issued to 2 Different Banks

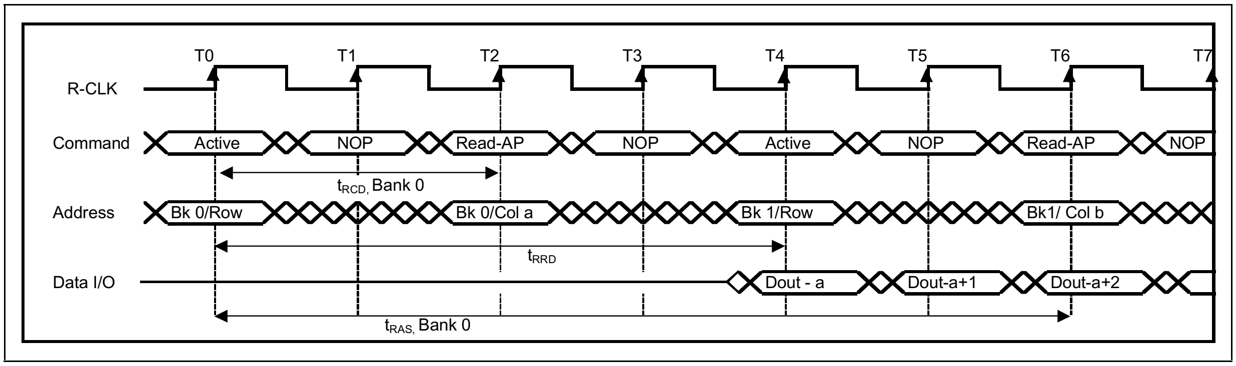


Figure 12. Example of CAS Latency 2

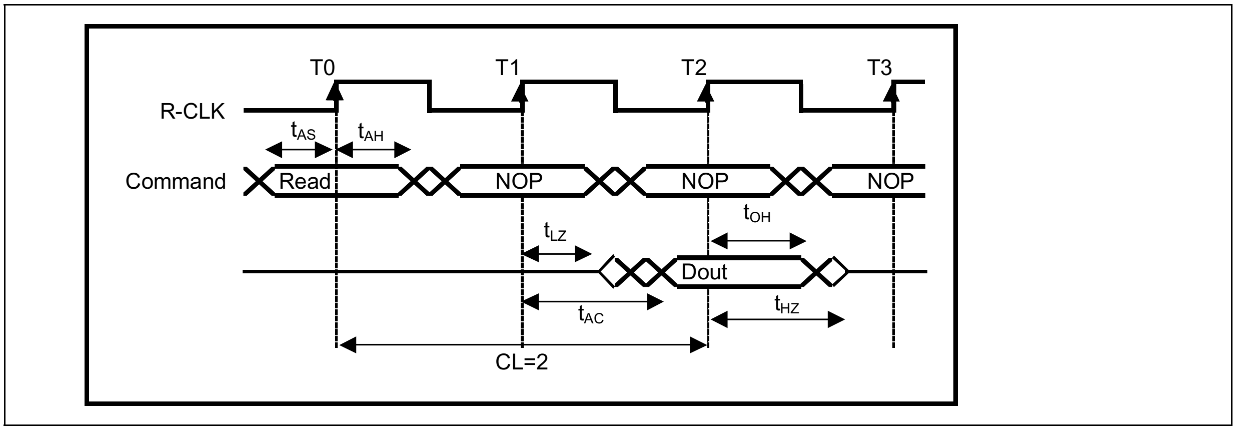
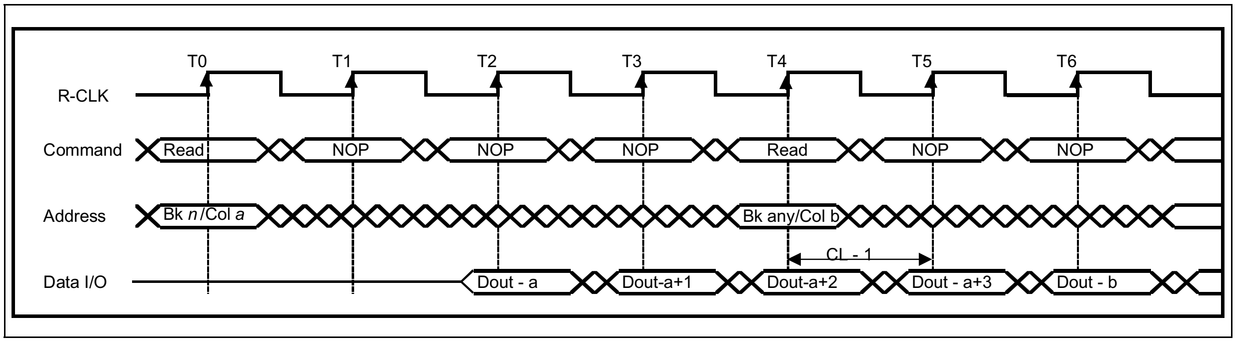


Figure 13. Consecutive Read Bursts with CL = 2



NOTE: A new command should be issued CL-1 clock cycles before the last desired data. The new command can be used to truncate the previous Read Burst.

Figure 14. Random Read Access with CL = 2

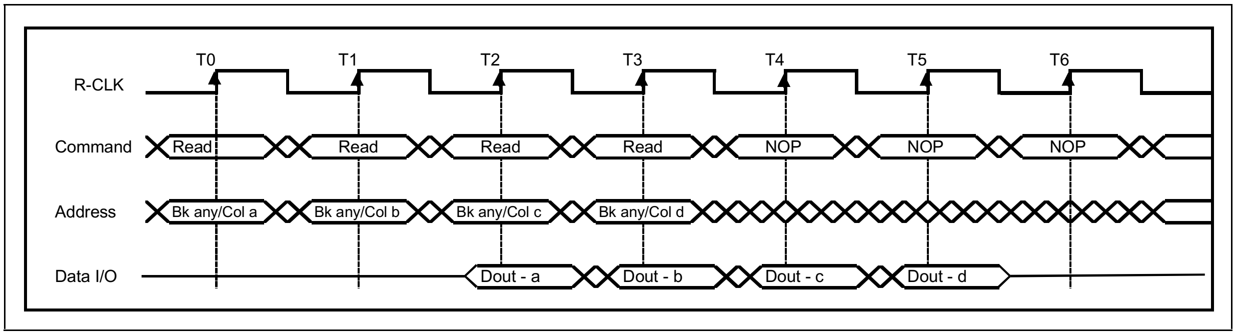
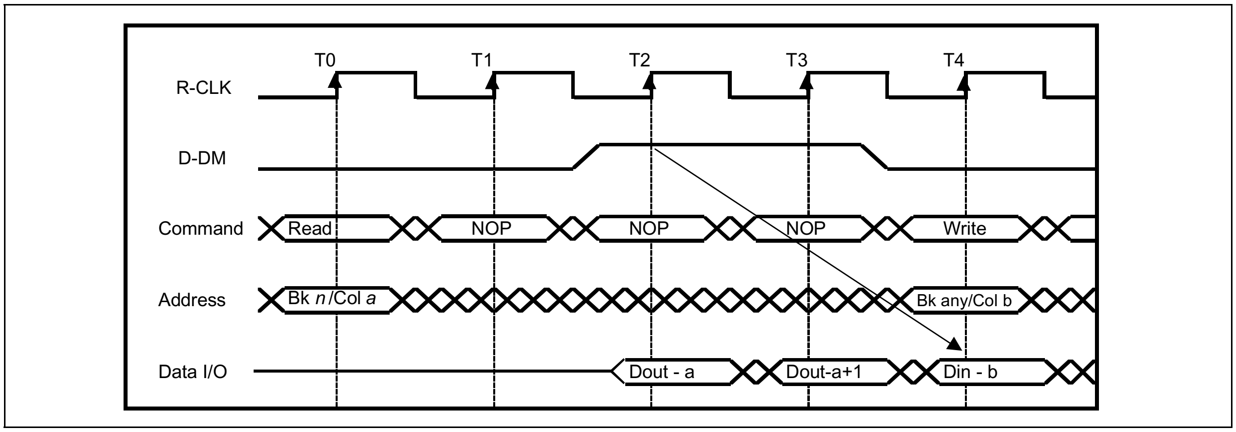
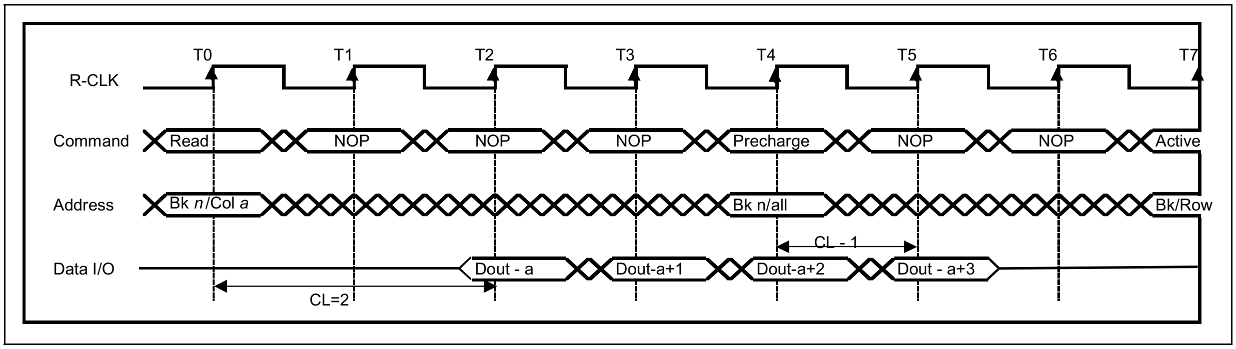


Figure 15. Read to Write Command



NOTE: Data masking used to prevent I/O contention.

Figure 16. Read Command Followed by Precharge



NOTE: Command issued CL-1 clocks before last desired data-out element.

Figure 17. Read Followed by Burst Terminate

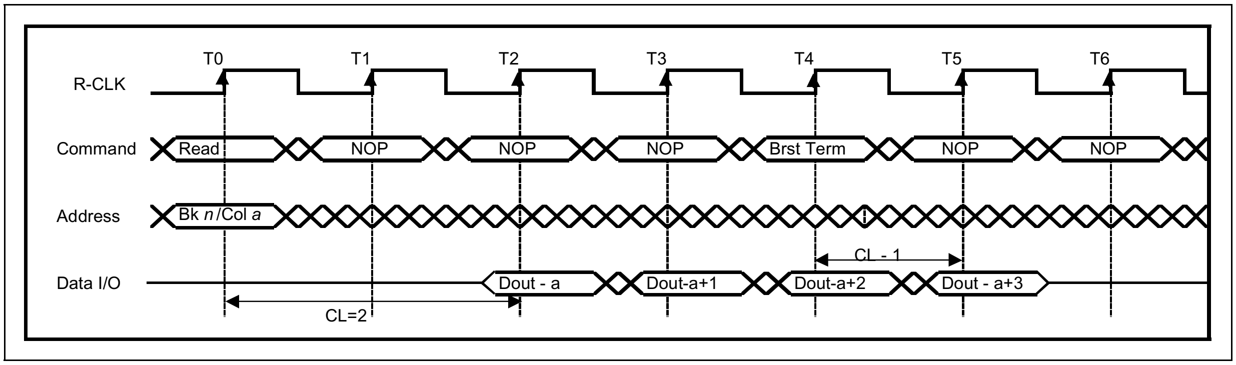
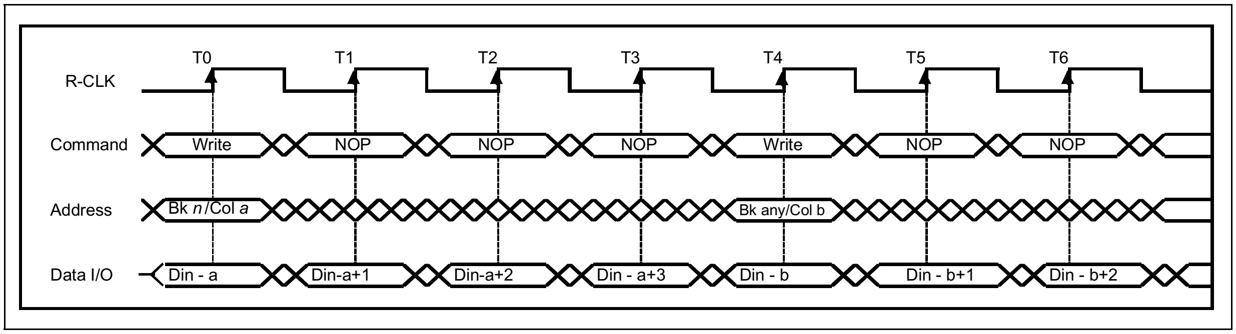


Figure 18. Random Write to 4 Word Bursts



NOTE: The commands can be to any active bank.

Figure 19. Write to Precharge Command Where Write Recovery Takes 1 Clock Cycle

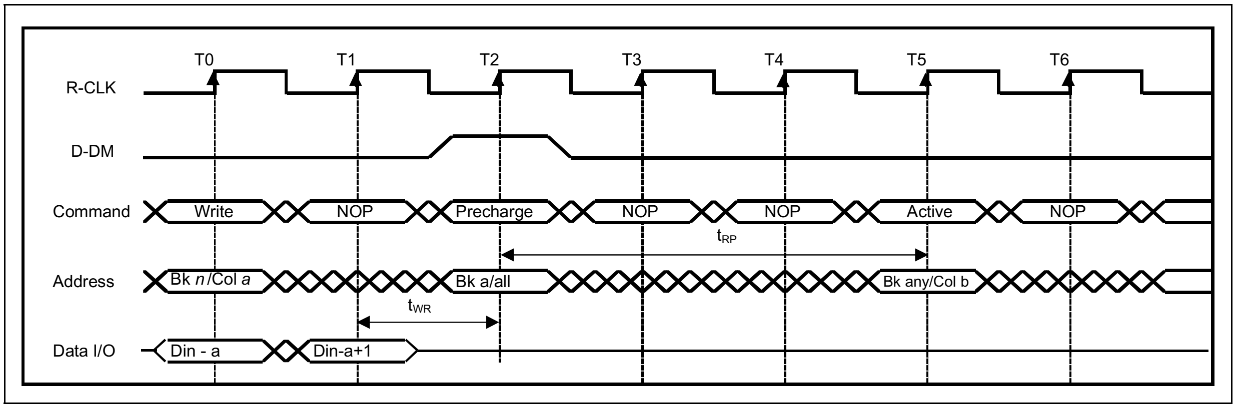


Figure 20. Write to Precharge Command Where Write Recovery Takes 2 Clock Cycles

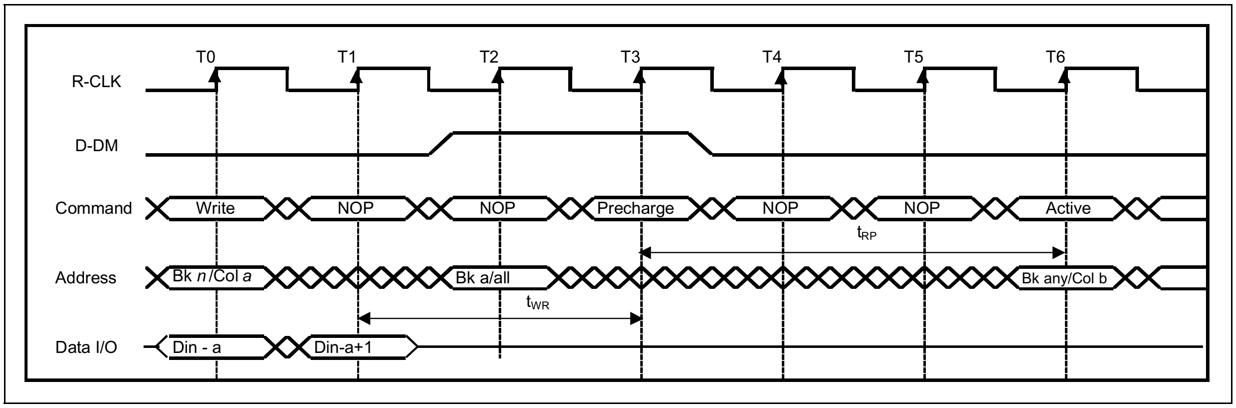
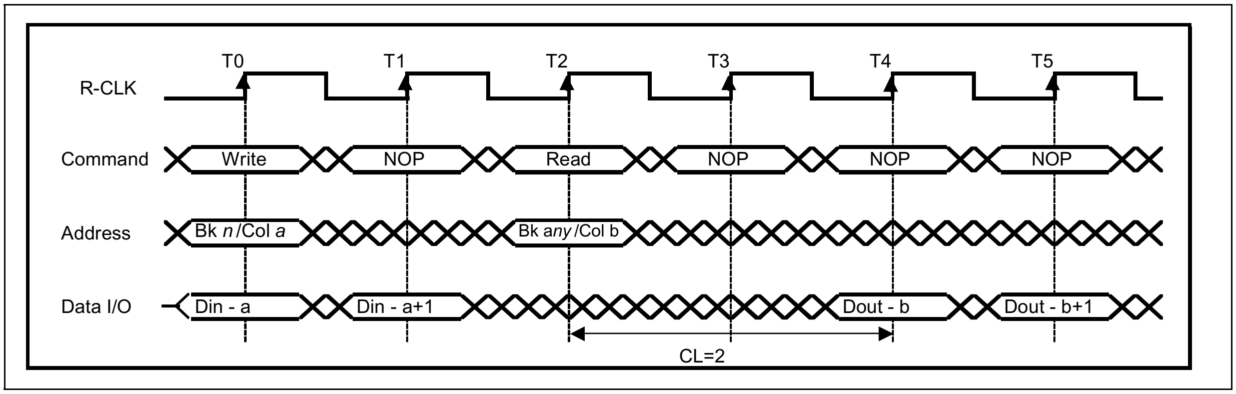
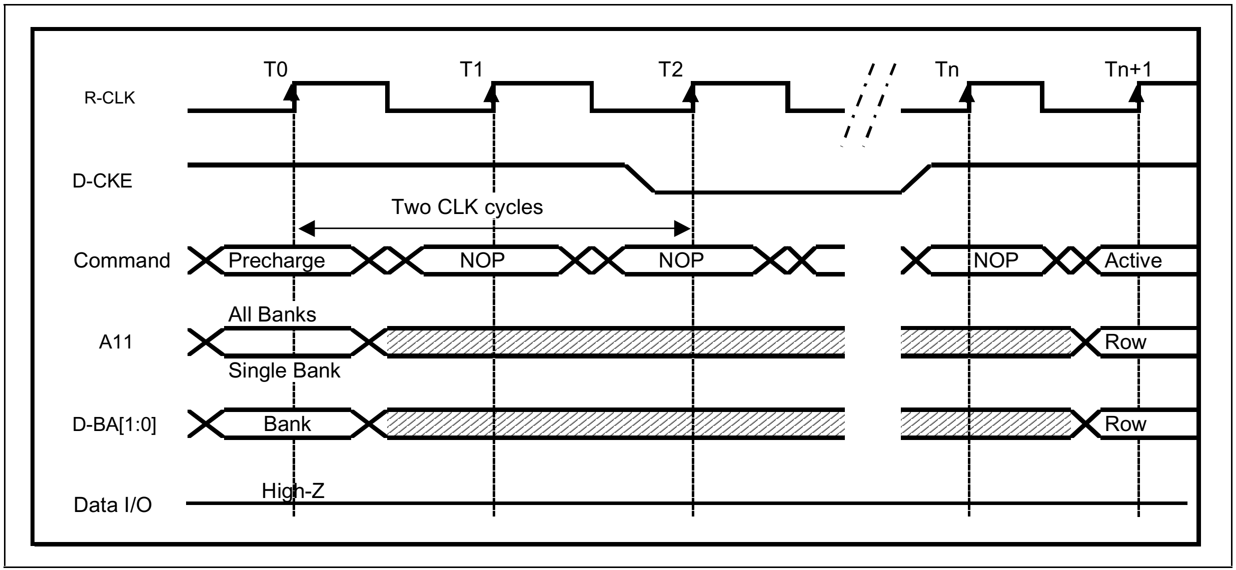


Figure 21. Write Command Followed by Read Command



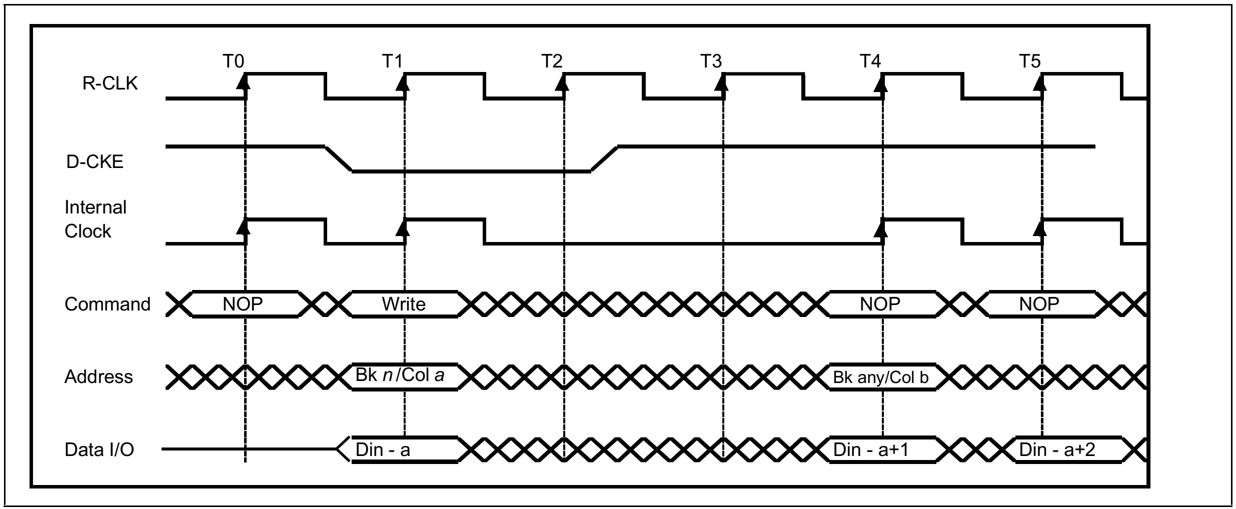
NOTE: The Read and Write commands can be done to any bank (CL = 2).

Figure 22. Precharge Power-Down Mode



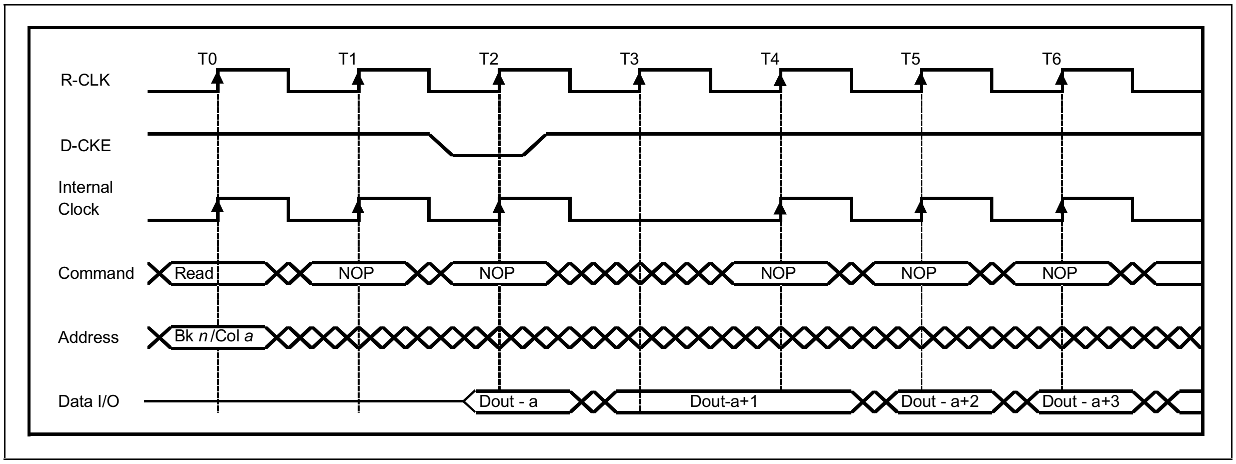
NOTE: All banks are idle with D-CKE low.

Figure 23. Clock Suspend During Write Burst



NOTE: Input data is ignored when internal clock is suspended.

Figure 24. Clock Suspend During Read Burst (CL = 2)



NOTE: Output data gets frozen while internal clock is suspended.

Figure 25. Read with Auto Precharge to Bank n Interrupted by Read to Bank m

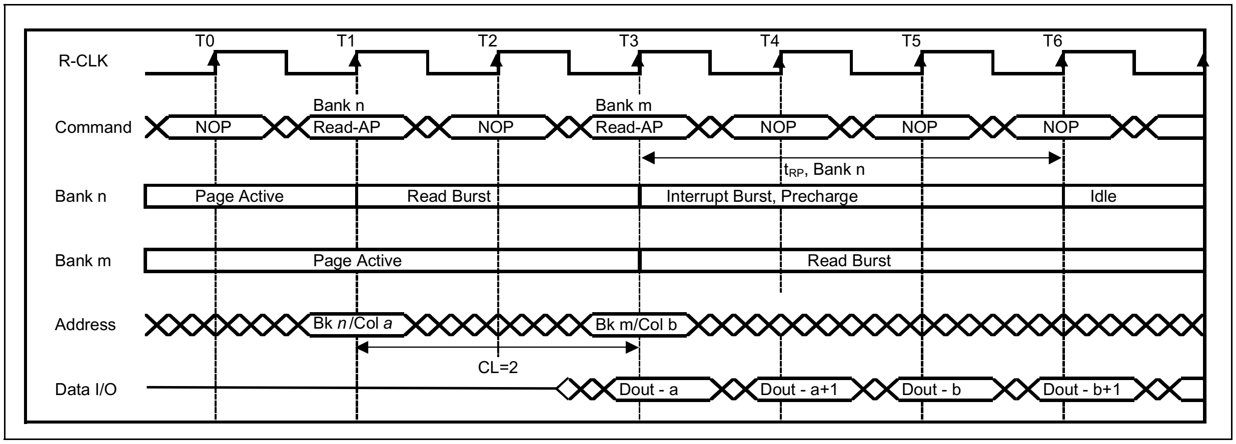


Figure 26. Read with Auto Precharge to Bank n Interrupted by Write to Bank m

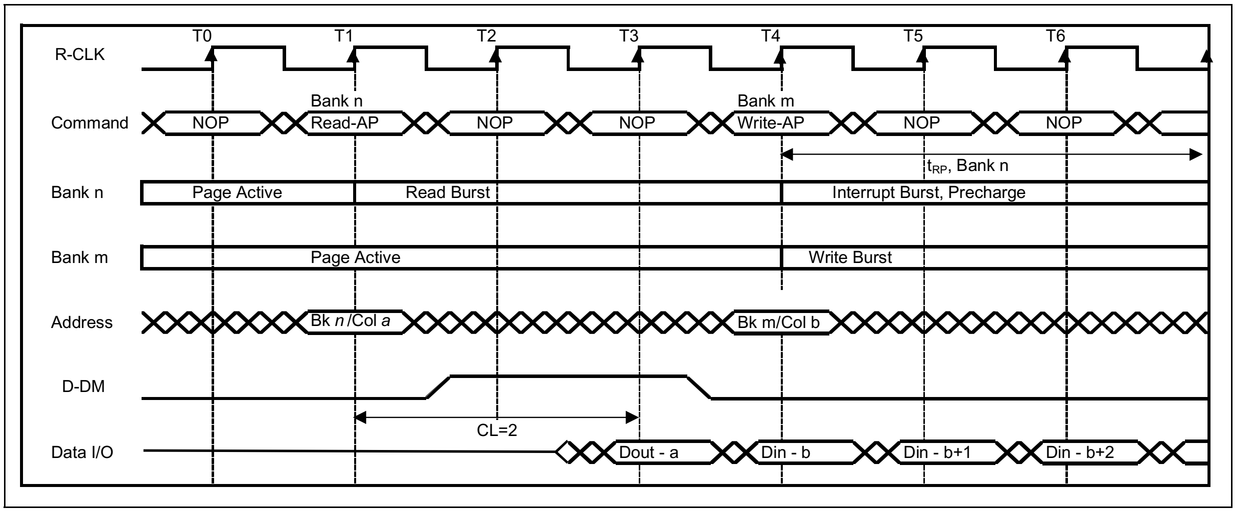


Figure 27. Write with Auto Precharge to Bank n Interrupted by Read to Bank m

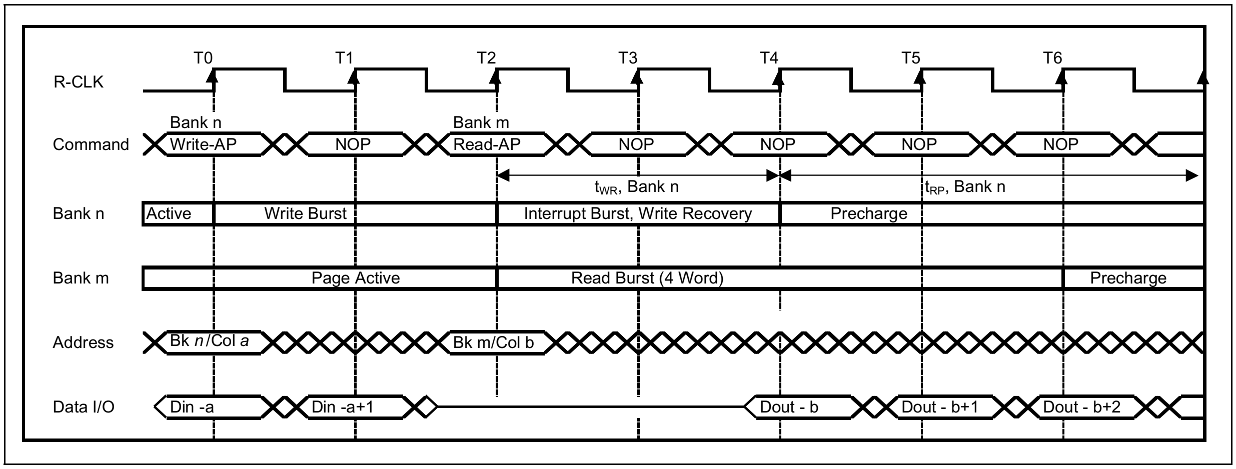
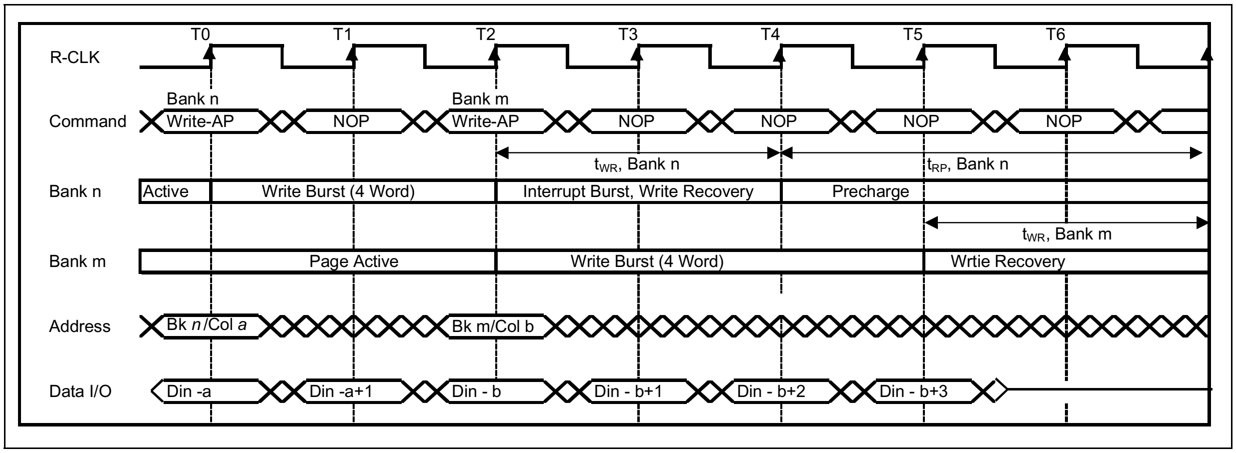


Figure 28. Write with Auto Precharge to Bank n Interrupted by Write to Bank m



18.4.11 LPSDRAM Burst Terminate

This command is used to truncate bursts. The most recent command prior to the burst terminate command will be truncated.

18.4.12 LPSDRAM Auto Refresh

This command is used during normal operation of the LPSDRAM. This command is non-persistent. All banks must be idle before issuing Auto Refresh command. This command can be issued after a minimum of t_{RP} after the precharge command. The address bits are "Do Not Care" during the Auto Refresh command. As an example, the 128-Mbit LPSDRAM requires 4096 auto refresh cycles (4096 rows/bank) every 64 ms (t_{REF}). Providing a distributed Auto Refresh command every 15.625 µs will meet the refresh requirement and ensure that each row is refreshed. Alternatively, 4096 auto refresh command cycles can be issued in a burst at a minimum cycle rate (t_{RFC}), once every 64 ms. Figure 9, "Auto Refresh Cycles with D-CKE High" on page 46 shows auto refresh cycles.

18.4.13 LPSDRAM Self Refresh

This state retains data in the LPSDRAM, even as the rest of the system is powered down. The Self Refresh command is initiated like the auto refresh command, except the D-CKE is disabled (low). All banks must be idle before this command is issued. Once the Self Refresh command is registered, all inputs become "Do Not Care" except D-CKE, which must remain low. The procedure for exiting Self Refresh mode requires a series of commands. The first clock must be stable before D-CKE going high. NOP commands should be issued (minimum of 2 clocks) to meet the refresh exit time (t_{SREX}) limitation. Figure 10, "Self Refresh Entry and Exit Mode" on page 47 shows Self Refresh Entry and Exit mode.

Appendix A Write State Machine

Refer to the *Intel StrataFlash® Wireless Memory System* datasheet (order number 253854) for the Write State Machine (WSM) details.

Appendix B Common Flash Interface

Refer to the *Intel StrataFlash® Wireless Memory System* datasheet (order number 253854) for the Common Flash Interface (CFI) details.

Appendix C Flash Flowcharts

Refer to the *Intel StrataFlash® Wireless Memory System* datasheet (order number 253854) for the flash flowchart details.

Appendix D Additional Information

Document Number	Datasheets
253854	*Intel StrataFlash® Wireless Memory System (LV18/LV30 SCSP) Datasheet*
	Application Notes
253856	Concurrent Program and Erase Using the Intel StrataFlash® Wireless Memory System (L18/L30 SCSP)
292221	AP-663 Using the Intel StrataFlash® memory write buffer®
292286	AP-738 Reduce Manufacturing Costs with Intel® Flash Memory Enhanced Factory Programming
251237	AP-759 Intel® Flash Memory Programming Algorithm Optimizations
297769	AP-678 Improving Programming Throughput of Automated Flash Memories
292186	AP-630 Designing for On-Board Programming Using IEEE1149.1 (JTAG) Access Port
292185	AP-629 Simplifying Manufacturing by Using Automatic Test Equipment for On-Board Programming
	Software Manuals
297833	Intel® Flash Data Integrator (FDI) User's Guide
298136	Intel® Persistent Storage Manager (PSM)
298132	Intel® Virtual Small Block File Manager (VFM)
	SCSP User Guide
298161	Intel® Flash Memory Chip Scale Package User's Guide

NOTES:
1. Call the Intel Literature Center at (800) 548-4725 to request Intel documentation. International customers must contact their local Intel or distribution sales office.
2. For the most current information on Intel® Flash memory products, software and tools, visit http://developer.intel.com/design/flash.

Appendix E Ordering Information

The following figures and tables provide ordering information for the LVX family with LPSDRAM device flash + RAM combinations:

- Table 26, "LVX Family with LPSDRAM: Available Product Ordering Information"
- Figure 29, "LVX Family with LPSDRAM: Ordering Information Decoder" on page 58
- Table 27, "38F and 48F Product Densities" on page 58

Table 26. LVX Family with LPSDRAM: Available Product Ordering Information

I/O Voltage (V)	Flash Density (Mbit) and Family	RAM Density (Mbit) and RAM Type	Package			Part Number	Notes
			Size (mm)	Ballout Name	Ball Type		
1.8	256 L18 + 256 L18 + 256 V18 + 256 V18	—	11x11x1.4	x16D (103 Ball)	SCSP Leaded	RD48F4444LVYBB0 RD48F4444LVYTB0	
	256 L18 + 256 V18	128 SDRAM	9x11x1.4	x16D (103 Ball)	SCSP Leaded	RD38F4460LVYBB0 RD38F4460LVYTB0 RD38F4460LVYGB0	1
	256 L18 + 256 L18 + 256 V18	128 SDRAM	9x11x1.4	x16D (103 Ball)	SCSP Leaded	RD58F0012LVYBB0 RD58F0012LVYTB0	2
	256 L18 + 256 V18 + 256 V18	128 SDRAM	9x11x1.4	x16D (103 Ball)	SCSP Leaded	RD58F0016LVYBB0 RD58F0016LVYTB0	2

NOTES:

1. For RD38F4460LVYGB0, the "G" designates a F-CE# parameter configuration where F1-CE# = Top parameter and F2-CE# = Top parameter.
2. The 58Fxxxx nomenclature indicates that more than three flash + RAM dies are used in the stacked device.

Figure 29. LVX Family with LPSDRAM: Ordering Information Decoder

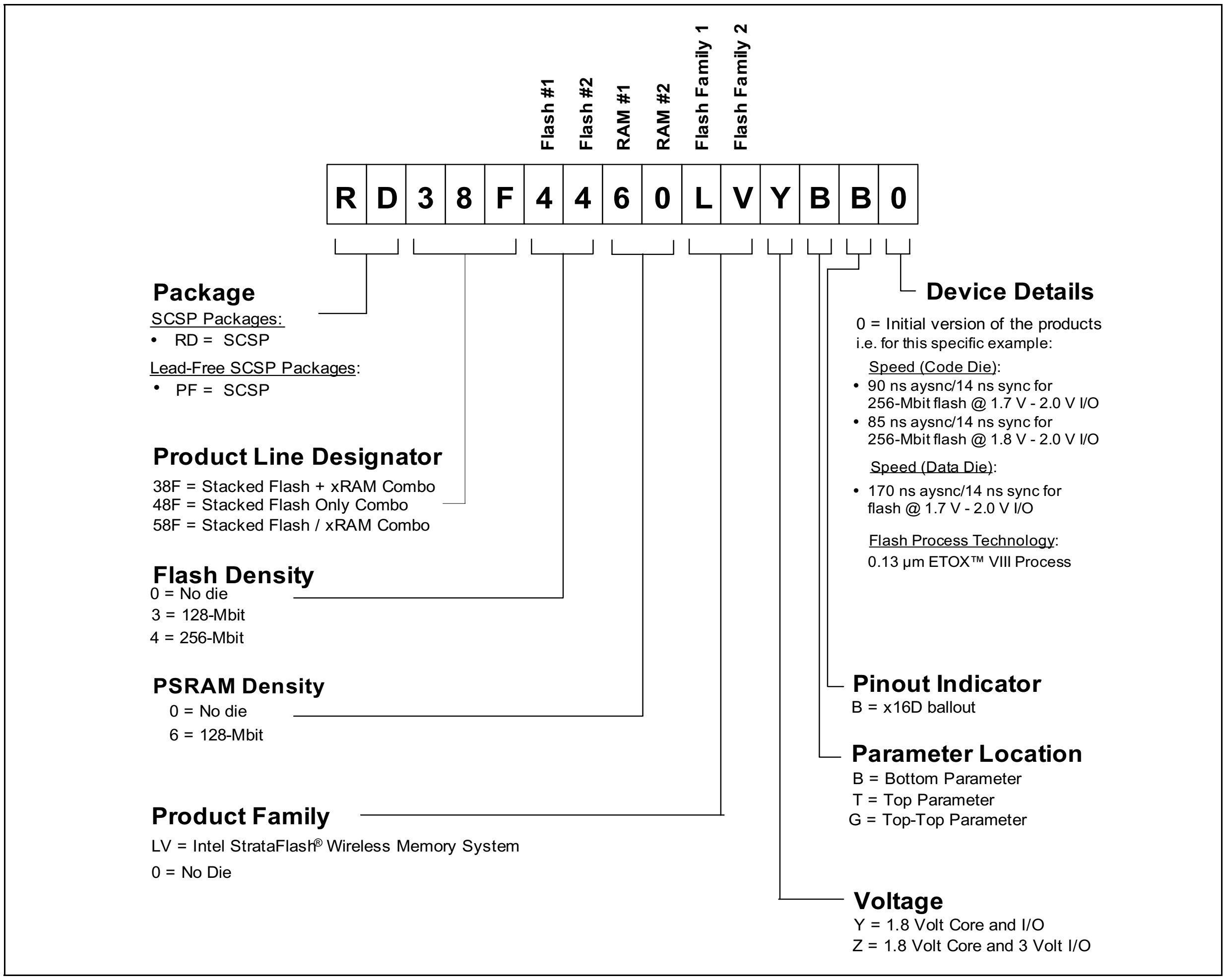


Table 27. 38F and 48F Product Densities

Code	Flash Die Density	RAM Die Density
0	No Die	No Die
1	32-Mbit	4-Mbit
2	64-Mbit	8-Mbit
3	128-Mbit	16-Mbit
4	256-Mbit	32-Mbit
5	512-Mbit	64-Mbit
6	1-Gbit	128-Mbit
7	2-Gbit	256-Mbit
8	4-Gbit	512-Mbit
9	8-Gbit	1-Gbit
A	16-Gbit	2-Gbit