RC4805 Precision High Speed Latching Comparator

Features

- 22 nS propagation delay
- Low offset voltage — 100 µA
- Low offset current — 15 nA
- TTL compatible latch
- TTL output

Description

The RC4805 is an ideal comparator for high speed, high precision applications. The input errors are factory trimmed to less than 1/10 LSB of a 12-bit, 10V system. The latch function allows the system designer additional flexibility. When the latch input is a TTL low, the comparator functions normally. When the input is raised to a TTL high, the comparator output is latched in its current state.

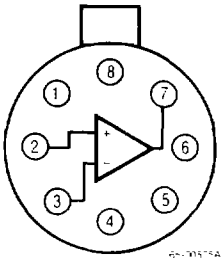
The RC4805 is ideal for ultra precise, very fast system designs. Typical applications include successive approximation A/D converters of 12 or more bits, zero crossing detectors, high speed sampling, or window detectors.

The RC4805 high speed comparator is functionally equivalent to the popular comparators HA-4950, AM686, SE527, CMP-05 and µA760. Propagation delay is 35 nS with a 1/2 LSB overdrive in a 12-bit, 10V system.

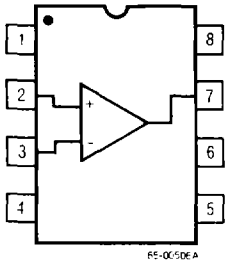
The RC4805 specifications and design have been upgraded since the last printing of this data sheet.

Connection Information

8-Lead
TO-99 Metal Can
(Top View)



8-Lead
Dual In-Line Package
(Top View)



Pin	Function
1	Ground
2	+ Input
3	-Input
4	$-V_S$
5	NC
6	Latch Enable
7	V_{OUT}
8	$+V_S$

Absolute Maximum Ratings

Supply Voltage ..... +5.5V/-16.5V
Differential Input Voltage 3V
Internal Power Dissipation* ..... 500 mW
Input Voltage ..... ±4V
Storage Temperature
Range ..... -65°C to +150°C
Operating Temperature Range
RM4805 ..... -55°C to +125°C
RC4805 ..... 0°C to +70°C
Lead Soldering Temperature
(60 sec) ..... +300°C

*See table of Thermal Characteristics for maximum ambient temperature derating factor.

Ordering Information

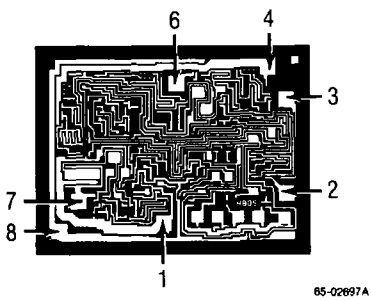
Part Number	Package	Operating Temperature Range
RC4805EN	N	0°C to +70°C
RC4805N	N	0°C to +70°C
RM4805D	D	-55°C to +125°C
RM4805D/883B	D	-55°C to +125°C
RM4805AD	D	-55°C to +125°C
RM4805AD/883B	D	-55°C to +125°C
RM4805T	T	-55°C to +125°C
RM4805T/883B	T	-55°C to +125°C
RM4805AT	T	-55°C to +125°C
RM4805AT/883B	T	-55°C to +125°C

Notes:
/883B suffix denotes Mil-Std-883, Level B processing
N = 8-lead plastic DIP
D = 8 lead ceramic DIP
T = 8-lead metal can (TO-99)
Contact a Raytheon sales office or representative for ordering information on special package/temperature range combinations.

Thermal Characteristics

	8- Lead Ceramic DIP	8- Lead TO-99 Metal Can	8- Lead Plastic DIP
Max. Junction Temp.	175°C	175°C	125°C
Max. P_D T_A <50°C	833mW	658mW	468mW
Therm. Res θ_{JC}	45°C/W	50°C/W	—
Therm. Res. θ_{JA}	150°C/W	190°C/W	160°C/W
For T_A >50°C Derate at	8.33mW per °C	5.26mW per °C	6.25 mW per °C

Mask Pattern



Die Size: 51 x 67 mils
Min. Pad Dimensions: 4 x 4 mils

Electrical Characteristics (V_S = ±5V, T_A = +25°C, Latch Enable = 0V unless otherwise noted)

Parameters	Test Conditions	RC4805E/ RM4805A			RC4805/ RM4805			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S \leq 50\Omega$		100	250		250	600	µV
Input Offset Current			10	80		25	150	nA
Input Bias Current			0.7	1.2		0.9	1.8	µA
Large Signal Voltage Gain		15	50		10	40		V/mV
Output Voltage Swing	V_{IN} > 10 mV, I_O = 200 µA	2.4	2.7		2.4	2.7		V
	V_{IN} < -10 mV, I_{SINK} = 8 mA		0.3	0.4		0.3	0.4	V
Input Voltage Range		±2.2	±2.7		±2.0	±2.7		V
Common Mode Rejection Ratio	$R_S \leq 50\Omega$, V_{CM} = Min Input Voltage Range	86			84			dB
Power Supply Rejection Ratio	$R_S \leq 50\Omega$, $+V_S$ = +5V, $-5.25V \leq -V_S \leq -4.75V$ and $-V_S$ = -5V, $+4.75V \leq +V_S \leq +5.25V$	86			84			dB
	$R_S \leq 50\Omega$ $+V_S$ = +5V, $-5V \leq -V_S \leq -15V$	86			84			dB
Supply Current (Positive)	$V_O \leq 0.4V$		11	16		13	18	mA
Supply Current (Negative)	$V_O \leq 0.4V$		12	16		13	18	mA
Power Consumption	$V_O \leq 0.4V$		115	160		130	180	mW
Propagation Delay*	100 mV Step, V_{OD} = 5 mV		22	35		22	35	nS
	100 mV Step, V_{OD} = 1.2 mV		35			35		nS
Latch Enable Time	V_{OD} = 5 mV		16			16		nS
Disable Time	V_{OD} = 5 mV		22			22		nS
Latch High Voltage		2.0			2.0			V
Low Voltage				0.8			0.8	V
Latch High Current	V_{LH} = 3.0V			40			75	µA
Low Current	V_{LL} = 0.8V			10			20	µA

*Minimize lead lengths by soldering directly to PC board. The use of sockets may cause oscillations from stray capacitive coupling.

Electrical Characteristics

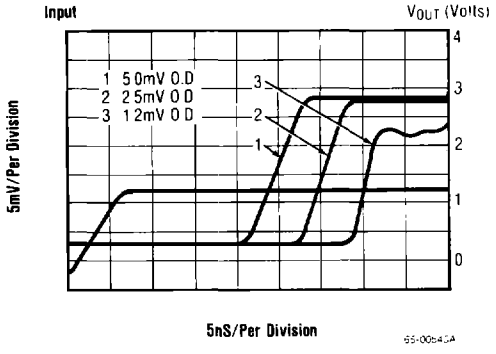
(V_S = ±5V, RM = -55°C ≤ TA ≤ +125°C; RC = 0°C ≤ T_A ≤ +70°C, Latch Enable = 0V unless otherwise noted)

Parameters	Test Conditions	RC4805E/ RM4805A			RC4805/ RM4805			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S \leq 50\Omega$		0.25	0.80		0.50	1.5	mV
Average Input Offset Voltage Drift	(Note 1)		1.5	5.0		2.5	7.5	µV/°C
Input Offset Current				200			400	nA
Input Bias Current				2.5			3.8	µA
Large Signal Voltage Gain			15			10		V/mV
Output Voltage Swing	V_{IN} > 10 mV, I_O = 200 µA	2.2	2.5		2.2			V
	V_{IN} < -10 mV, I_{SINK} = 6.4 mA		0.3	0.45		0.3	0.45	V
Input Voltage Range		±2.0			±2.0			V
Common Mode Rejection Ratio	$R_S \leq 50\Omega$, V_{CM} = ±2V Input Voltage Range	85			80			dB
Power Supply Rejection Ratio	$R_S \leq 50\Omega$, $+V_S$ = +5V, $-5.25V \leq -V_S \leq -4.75V$ and $-V_S$ = -5V, $+4.75V \leq +V_S \leq +5.25V$	75			72			dB
Supply Current (Positive)	$V_O \leq 0.4V$		13	18		15	20	mA
Supply Current (Negative)	$V_O \leq 0.4V$		15	20		15	20	mA
Power Consumption	$V_O \leq 0.4V$		140	190		150	200	mW
Propagation Delay[1]	100 mV Step, V_{OD} = 5 mV		30	50		35	55	nS
	100 mV Step, V_{OD} = 1.2 mV		50			50		nS

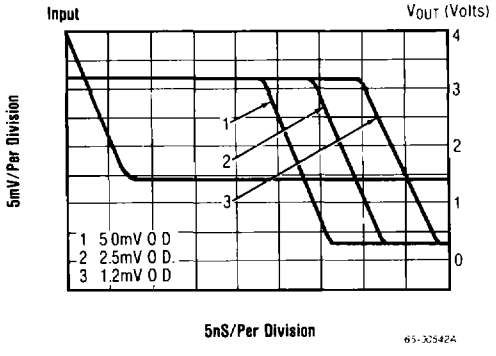
Notes:
1. Guaranteed but not tested.

Typical Performance Characteristics

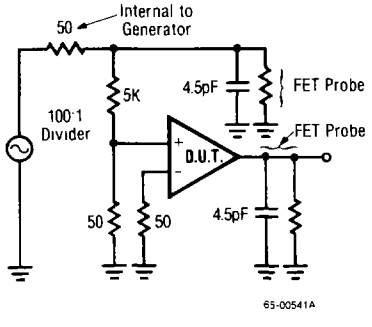
4805 Response Time Rising Edge



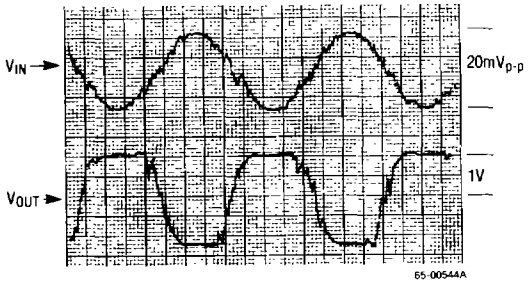
4805 Response Time Falling Edge



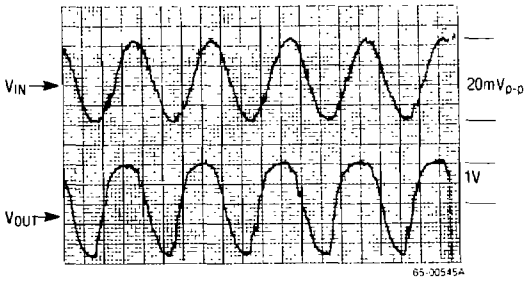
Response Photography Test Setup



Response to 25MHz Sine Wave

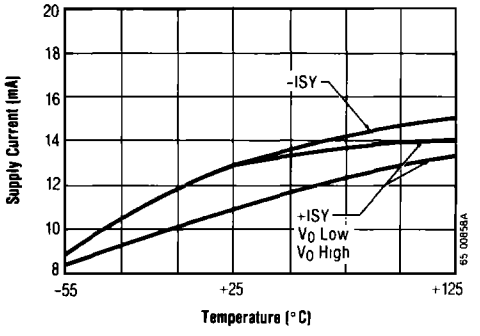


Response to 50MHz Sine Wave

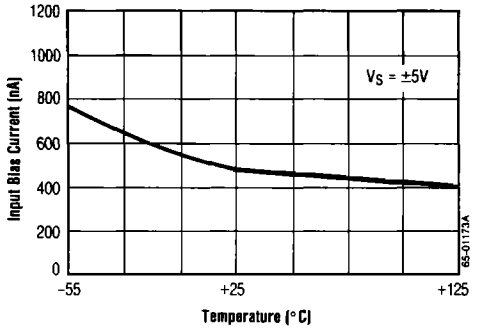


Typical Performance Characteristics (Continued)

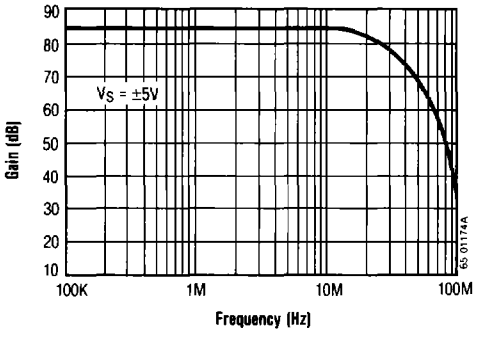
Supply Current vs. Temperature



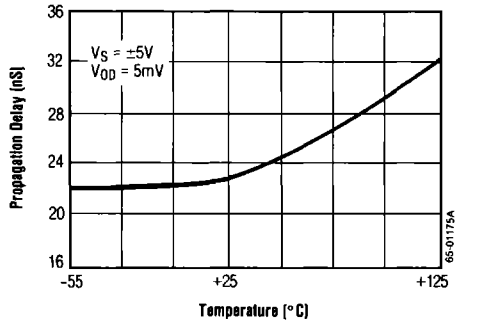
Input Bias Current vs. Temperature



Gain vs. Frequency



Propagation Delay vs. Temperature



Applications Information

Optimal performance of the 4805 in high speed applications circuits requires that careful layout and circuit design techniques are used. The use of good power supply bypass capacitors, minimum lead lengths, and a good ground plane are essential.

Bypass Capacitors

Tantalum electrolytics connected close to the power supply leads are usually sufficient; sometimes a smaller ceramic capacitor in parallel with the tantalum may improve high frequency response even further. Typical values would be 10μF in parallel with 0.01μF.

Minimize Lead Lengths

Short input leads are essential to eliminate stray capacitance that might otherwise induce oscillations. **Avoid the use of sockets;** solder the IC directly to the PC board. When laying out a PC board, position the signal source as close to the comparator inputs as is physically possible. Avoid stray capacitance from the inputs to ground, and route the output away from the inputs. Best response times will occur when the source impedance driving the inputs is kept low (<1kΩ). Avoid driving heavy capacitive loads with the output (example: coaxial cable, which has a parasitic capacitance of 50pF per foot).

Ground Plane

A ground plane reduces the parasitic inductance of PC traces. Current flow through the PC trace is mirrored by a return current flow that passes through the ground plane adjacent to the PC trace. This sets up a magnetic field that cancels the magnetic field in the PC trace, thus reducing parasitic inductance.

Use the component side of the board for the ground plane. Cover that side as completely as is practical, especially under traces carrying high frequency signals. Mount HF components close to the board.

Latch Enable

The effective gain at low levels of input overdrive can be increased by applying a carefully timed positive going step to the latch enable input. This technique is especially useful in successive approximation A/D converters, where the exact time of comparison is well defined. After the SAR changes the DAC output, a delayed pulse applied to pin 6 will increase the effective gain from about 5V/mV to 20V/mV, and therefore speeds up the response time for low levels input signals. In a 12-bit ±10V A/D system, the propagation delay for 1 LSB will decrease about 30%. Figure 1 shows the waveforms for this technique, and Figure 2 shows a one-shot time delay circuit using a TTL IC that can be used to create the pulse.

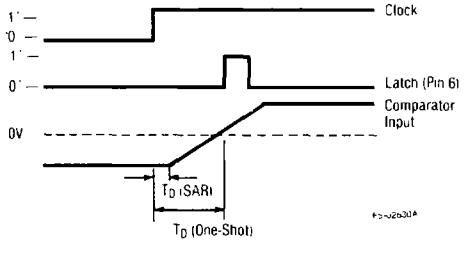


Figure 1. Gain Boost Waveforms

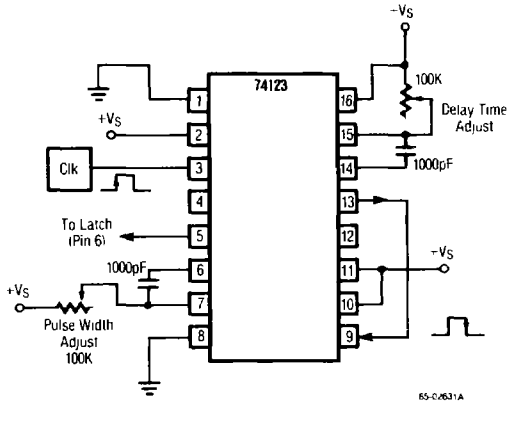
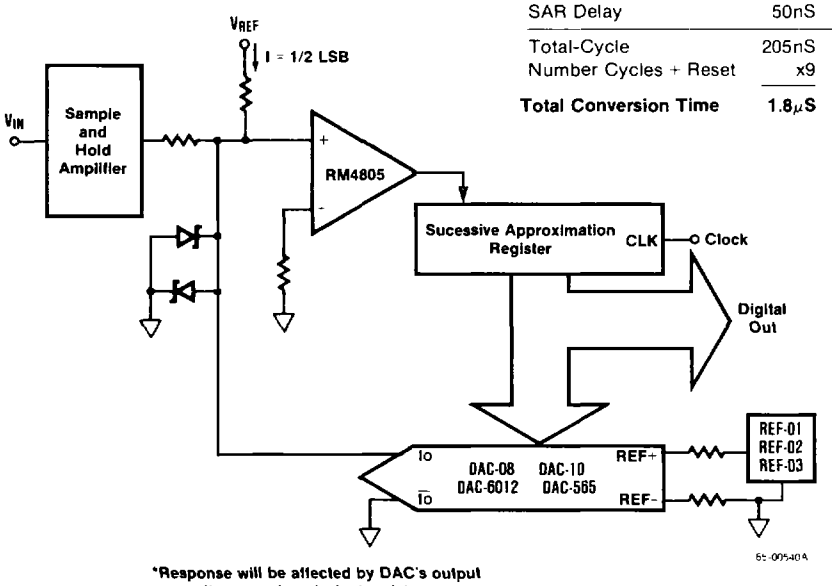


Figure 2. Delayed Pulse Circuit

Typical Applications

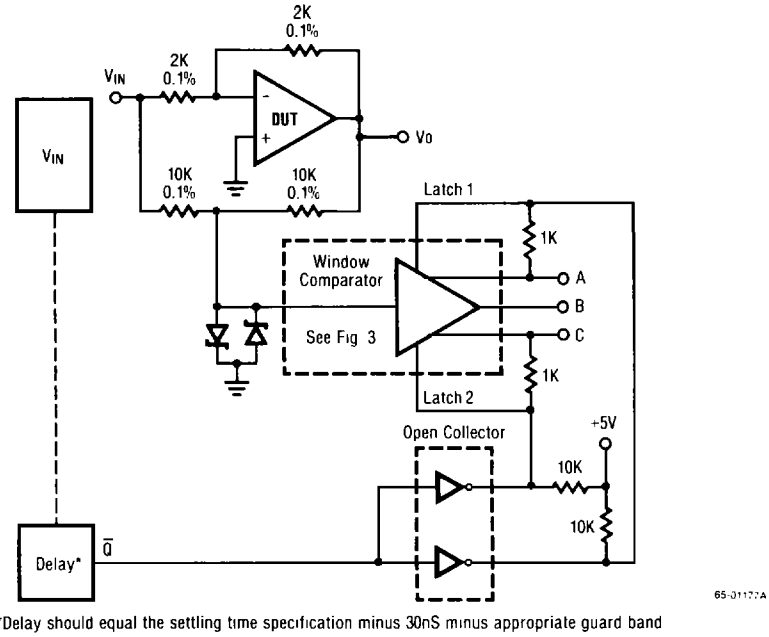
	Conversion Time		
	8-Bit	10-Bit	12-Bit
RM4805 Response	20nS	22nS	50nS
DAC Settling*	135nS	135nS	500nS
SAR Delay	50nS	50nS	50nS
Total-Cycle	205nS	207nS	600nS
Number Cycles + Reset	x9	x11	x13
Total Conversion Time	**1.8μS**	**2.3μS**	**7.8μS**



*Response will be affected by DAC's output capacitance and equivalent resistance.

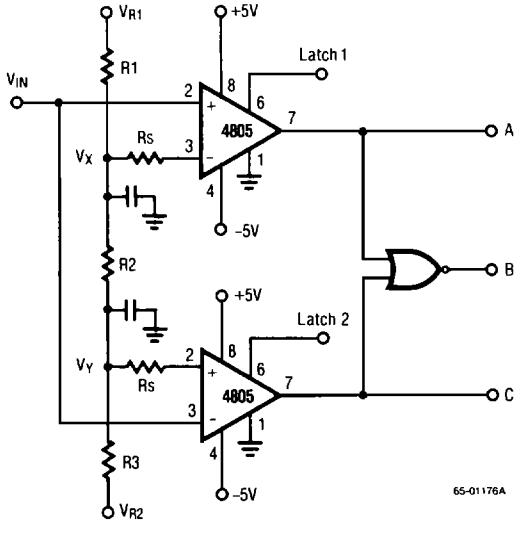
Figure 3. Successive Approximation 8, 10, or 12-bit Resolution

Typical Applications (Continued)



*Delay should equal the settling time specification minus 30nS minus appropriate guard band

Figure 4. Op Amp Settling Time Tester



The settling time tester uses the precision latching window comparator to automate op amp settling time testing. If the DUT is not settled by the end of the time delay, the A output is latched low.

V_{IN} ($V_X > V_Y$)*	A	B	C
$V_{IN} > V_X$	1	0	0
$V_X > V_{IN} > V_Y$	0	1	0
$V_Y > V_{IN}$	0	0	1

*Both latches low

Figure 5. Precision Latching Window Comparator (Detail)

Fast Latching ECL to TTL Line Translator, Up to 50MHz

The high speed differential input and the latched TTL output makes the RC4805 ideally suited for use as an ECL to TTL translator. Existing logic supplies of -5.2V and +5.0V are compatible with the RC4805 power supply requirements. With a TTL compatible latch input the RC4805 can be latched from the TTL subsystem or from the ECL subsystem, by using another RC4805 on the latch signal.

In ECL systems the termination resistors and pull-down resistors can be combined in a network as shown in Figure 6, a typical ECL to TTL translator. The configuration shown in Figure 8 has a common mode range of ±2.0V. But either input can swing as low as -5.0V below the input, providing one input stays in the ±2.0V common mode range. By using a -15V supply on the RC4805 the common mode range is extended to -8.0V, +2.0V as shown in Figure 7. The only caution is that the differential mode voltage must not exceed +5.0V.

Not all ECL families have the same logic levels, the same logic level V_S supply voltage, or the same temperature characteristics. By using the same logic type as a reference, a single-end ECL to TTL translator can be made to track changes in logic levels. A typical circuit is shown in Figure 8.

In system design one subsystem may in one configuration be driven with ECL line drivers, but in another configuration the same subsystem may be driven from a TTL gate.

High gain, low input bias current and ±2.0V common mode range on the RC4805 allow the easy design of an adaptive ECL-TTL to TTL translator. The ECL interface is the same as shown in Figure 6. By adding pull-up resistors and a bypassed level shifting resistor to the TTL outputs (see Figure 9), the same subsystem line receiver can interface with ECL or TTL with no hardware change in the receiver.

In summary, the RC4805 is a very flexible system element that allows the system designer to interface ECL to TTL in a number of easy to use configurations. The RC4805 can also be used in an adaptive ECL-TTL to TTL interface.

Typical Examples

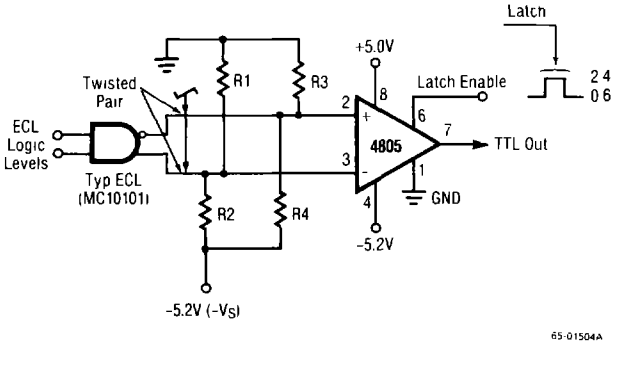
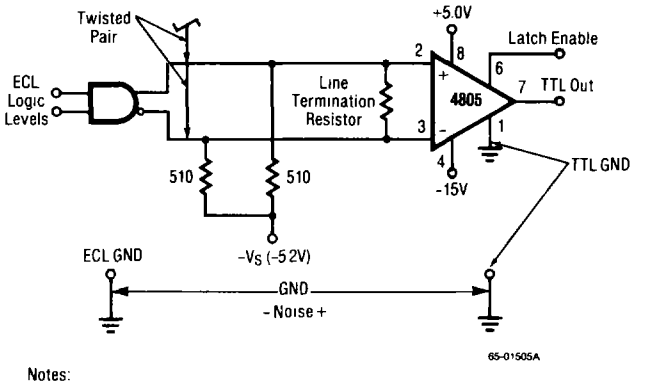


Figure 6. Typical ECL to TTL Translator

Typical Examples (Continued)



Notes:

1. Common mode range of 4805 is -8.0V to +2.0V.
2. The 4805 can stand -3.0V, +5.0V of GND noise from the ECL GND to the TTL GND.

Figure 7. ECL to TTL Translator With Extended Common Mode Range

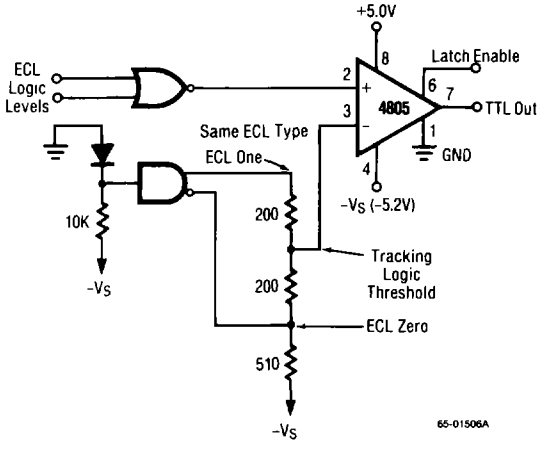


Figure 8. Single-Ended ECL to TTL Translator With Tracking ECL Reference

Typical Examples (Continued)

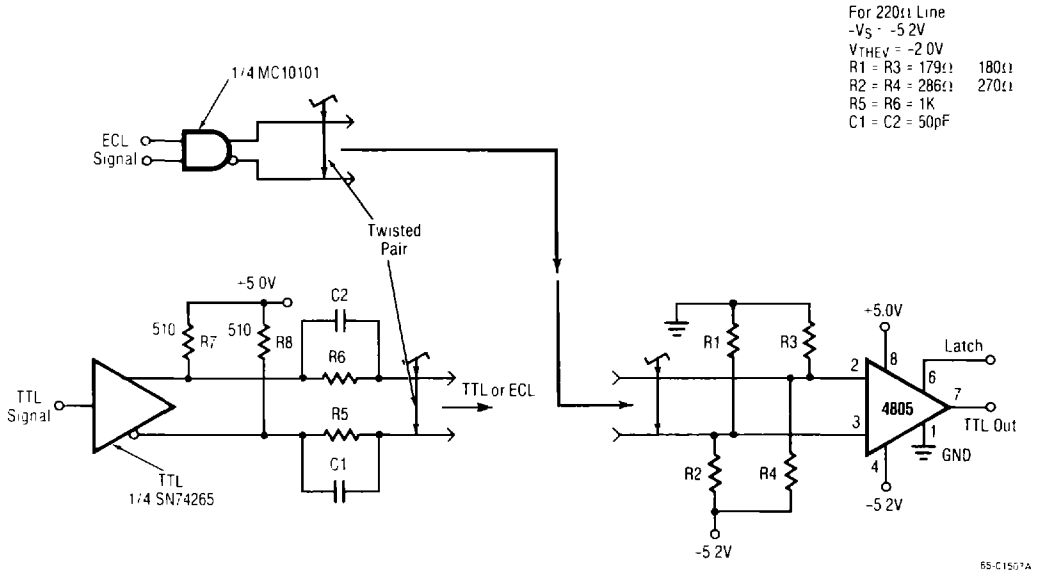


Figure 9. Adaptive ECL-TTL to TTL Translator

Schematic Diagram