RAA7884QR

Quad, ±16.5kV ESD Protected, 3.0V to 5.5V, RS-485/RS-422 Receiver

The RAA7884QR is a ±16.5kV IEC61000-4-2 ESD protected, 3.0V to 5.5V powered, quad receiver designed for balanced communication using the RS-485 and RS-422 standards. With low input currents (±200µA), the receiver presents a 1/4 unit load to the RS-485 bus and allows up to 128 receivers on the bus.

The RAA7884QR is a high data rate receiver that operates at data rates up to 80Mbps. With an 8ns maximum propagation delay skew (tolerance), it ensures excellent part-to-part matching.

The receiver outputs are tri-statable and include a hot plug feature to keep them disabled during power-up and power-down.

Related Literature

For a full list of related documents, visit our website:

- RAA7884QR device page

Applications

- Telecom equipment
- Motor controllers/encoders
- Programmable logic controllers
- Industrial/process control networks

Features

- IEC61000 ESD protection (RS-485 inputs): ±16.5kV
  - Class 3 ESD on all other pins: >8kV HBM
- Wide supply range: 3.0V to 5.5V
- Wide common-mode range: -7V to +12V
- Low part-to-part propagation delay tolerance: 8ns (maximum)
- Specified for +125°C operation
- Fail-safe open Rx inputs
- 1/4 unit load allows 128 devices on the bus
- Available in industry standard pinout
- High data rate of up to 80Mbps
- Low shutdown supply current: 15µA
- Tri-statable Rx outputs
- 5V tolerant logic inputs when V_{CC} = 3.3V
- RoHS Compliant

Table 1. Summary of Features

Part Number	Function	Data Rate (Mbps)	Hot Plug?	VL Supply Pin?	Rx Enable Type	Maximum Total Supply Current (mA)	Low Power Shutdown?	Pin Count
RAA7884QR	4 Rx	80	Yes	No	EN, $\overline{EN}$	15	Yes	16

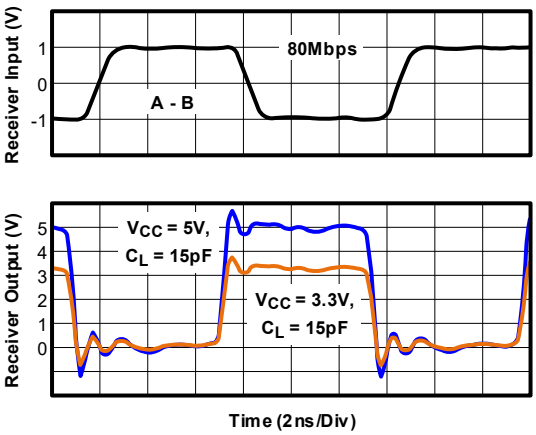


Figure 1. RAA7884QR Data Rate Performance

1. Overview

1.1 Typical Operating Circuits (1 of 4 Channels Shown)

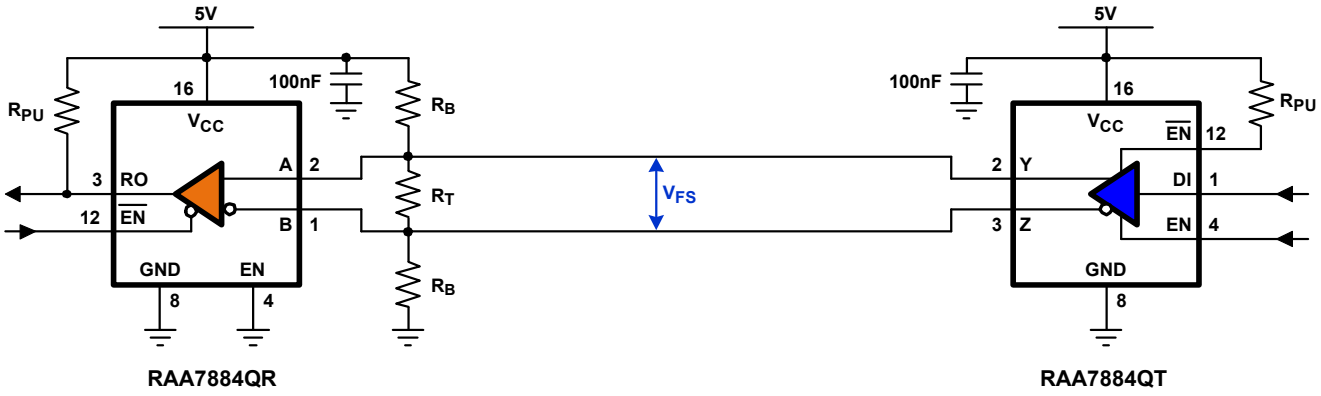


Figure 2. Network Using Group Enables

Note: To calculate the resistor values, see TB509.

1.2 Ordering Information

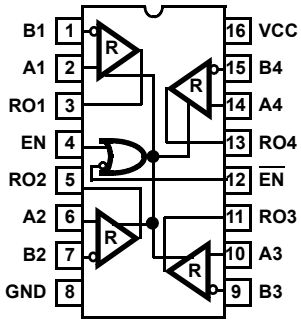
Part Number (Notes 2, 3)	Part Marking	Temp. Range (°C)	Tape and Reel (Units) (Note 1)	Package (RoHS Compliant)	Pkg. Dwg. #
RAA7884QR4GSP#AB0	RAA7884 QR4GSP	-40 to +125	-	16 Ld SOIC	M16.15
RAA7884QR4GSP#HB0	RAA7884 QR4GSP	-40 to +125	2.5k	16 Ld SOIC	M16.15

Notes:

1. See TB347 for details about reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
3. For Moisture Sensitivity Level (MSL), see RAA7884QR device page. For more information about MSL see TB363.

1.3 Pin Configuration

(16 Ld N-SOIC)
Top View



1.4 Pin Descriptions

Pin Number	Pin Name	Function
4, 12	EN, $\overline{EN}$	Group Driver Output Enables that are internally pulled high to VCC. All receiver outputs are enabled by driving EN high or $\overline{EN}$ low and the outputs are all high impedance when EN is low and $\overline{EN}$ is high (that is, if using only the active high EN, connect $\overline{EN}$ to VCC through a 1kΩ resistor; if using only the active low $\overline{EN}$, connect EN directly to GND). If the Group Enable function is not required, connect EN to VCC through a 1kΩ or greater resistor or connect $\overline{EN}$ directly to GND.
3, 5, 11, 13	RO1, RO2, RO3, RO4	Channel X receiver output: If A - B ≥ 200mV, RO is high; If A - B ≤ -200mV, RO is low. RO = High if A and B are unconnected (floating).
8	GND	Ground connection.
2, 6, 10, 14	A1, A2, A3, A4	±16.5kV IEC61000-4-2 ESD protected RS-485/422 level, Channel x non-inverting receiver input.
1, 7, 9, 15	B1, B2, B3, B4	±16.5kV IEC61000-4-2 ESD protected RS-485/422 level, Channel x inverting receiver input.
16	VCC	System power supply input (3.0V to 5.5V).

1.5 Truth Tables

Receiver Output (ROX Enabled)	
Inputs (A-B)	**Output (ROX)**
≥0.2V	1
≤-0.2V	0
Inputs Open (Floating)	1

Receiver Enable		
Inputs		**Outputs**
EN	$\overline{EN}$	ROX
X	0	ENABLED
1	X	ENABLED
0	1	DISABLED*

Note: *Low power Shutdown mode when disabled

2. Specifications

2.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
VCC to GND		7	V
Input Voltages			
EN (All varieties)	-0.3	7	V
A, B	-9	13	V
Output Voltages			
RO	-0.5	V_{CC} + 0.3	V
Short-Circuit Duration			
RO (One output at a time)		Indefinite	
ESD Rating	**See "ESD Performance" on page 5**		

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

2.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
16 Ld SOIC Package (Notes 4, 5)	70	30

Notes:

4. θ_{JA} is measured with the component mounted on a high-effective thermal conductivity test board in free air. See TB379 for details.
5. For θ_{JC}, the case temperature location is taken at the package top center.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature (Plastic Package)		+150	°C
Maximum Storage Temperature Range	-65	+150	°C
Pb-Free Reflow Profile	see TB493		

2.3 Recommended Operation Conditions

Parameter	Minimum	Maximum	Unit
Supply Voltage, V_{CC}	3.0	5.5	V
Ambient Temperature	-40	+125	°C
Bus Pin Common-Mode Voltage Range	-7	12	V
RO Output Current	-9	9	mA
RO Load Capacitance		≤15	pF

2.4 Electrical Specifications

Test Conditions: V_{CC} = 3.0V to 5.5V; T_A = +25°C; unless otherwise specified. **Boldface limits apply across the operating temperature range.** (Notes 6, 10)

Parameter	Symbol	Test Conditions		Temp (°C)	Min (Note 9)	Typ	Max (Note 9)	Unit
DC Characteristics								
Input High Voltage (Enable Pins)	V_{IH1}	3.0V ≤ V_{CC} ≤ 3.6V		Full	**2**			V
		4.5V ≤ V_{CC} ≤ 5.5V		Full	**2.2**			V
Input Low Voltage (Enable Pins)	V_{IL}	3.0V ≤ V_{CC} ≤ 5.5V		Full			**0.8**	V
Logic Input Current	I_{IN1}	EN, $\overline{EN}$		Full	**-15**		**15**	µA
Receiver Differential Threshold Voltage	V_{TH}	-7V ≤ V_{CM} ≤ 12V		Full	**-200**		**200**	mV
Receiver Input Hysteresis	ΔV_{TH}	V_{CM} = 0V		25		30		mV
Input Current (A, B)	I_{IN3}	V_{CC} = 0V or 5.5V	V_{IN} = 12V	Full			**0.2**	mA
			V_{IN} = -7V	Full	**-0.2**			mA
Receiver Input Resistance	R_{IN}	-7V ≤ V_{CM} ≤ 12V		Full	**48**			kΩ
Receiver Output Leakage Current	I_{OZ}	EN = 0V, 0V ≤ V_O ≤ V_{CC}		Full	**-10**		10	µA
Receiver Short-Circuit Current, V_O = High or Low	I_{OS}	EN = 1, 0V ≤ V_O ≤ V_{CC}		Full			**±165**	mA
Receiver Output High Voltage	V_{OH1}	3.0V ≤ V_{CC} ≤ 3.6V, I_O = -6mA, V_{ID} = 200mV		Full	**2.4**			V
		4.5V ≤ V_{CC} ≤ 5.5V, I_O = -8mA, V_{ID} = 200mV		Full	**V_{CC} - 1**			V
Receiver Output Low Voltage	V_{OL}	3.0V ≤ V_{CC} ≤ 5.5V, I_O = 8mA, V_{ID} = -200mV		Full			**0.4**	V
Supply Current								
No Load Supply Current	$80I_{CC}$	EN = 1, or $\overline{EN}$ = 0		Full			**15**	mA
Shutdown Supply Current	I_{SHDN}	All outputs disabled (Note 12)		Full			**15**	µA
ESD Performance								
RS-485 Pins (A, B)		IEC61000-4-2, from bus pins to GND	Air gap	25	-	±16.5		kV
			Contact	25	-	±8		kV
		Human Body Model, from bus pins to GND		25	-	±15		kV
All Pins		HBM		25	-	±8		kV
		Machine Model		25	-	500		V
Receiver Switching Characteristics								
Maximum Data Rate	f_{MAX}	V_{ID} = ±1.5V, C_L ≤ 15pF	V_{CC} ≤ 3.6V	Full	**80**			Mbps
			V_{CC} > 3.6V	Full	**50**			Mbps
Receiver Input to Output Delay	t_{PLH}, t_{PHL}			Full	**6**	11	**16**	ns
Receiver Skew | t_{PLH} - t_{PHL} |	t_{SKD}			Full		0.4	**2**	ns
Prop Delay Skew Channel-to-Channel	t_{SKC-C}	(Figure 3, Note 7)		Full		0.7	**4**	ns
Prop Delay Skew Part-to-Part	t_{SKP-P}	(Figure 3, Note 8)		Full		1.2	**8**	ns
Receiver Disable from Output High	t_{HZ}	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 4)		Full		18	**30**	ns
Receiver Disable from Output Low	t_{LZ}	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 4)		Full		19	**30**	ns
Receiver Enable from Shutdown to Output High	$t_{ZH(SHDN)}$	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 4, Note 13)		Full			**850**	ns
Receiver Enable from Shutdown to Output Low	$t_{ZL(SHDN)}$	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 4, Notes 13)		Full			**850**	ns

Test Conditions: V_{CC} = 3.0V to 5.5V; T_A = +25°C; unless otherwise specified. **Boldface limits apply across the operating temperature range.** (Notes 6, 10) **(Continued)**

Parameter	Symbol	Test Conditions	Temp (°C)	Min (Note 9)	Typ	Max (Note 9)	Unit

Notes:

6. All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.
7. Channel-to-channel skew is the magnitude of the worst case delta between any two propagation delays of any two outputs on the same IC, at the same test conditions.
8. t_{SKP-P} is the magnitude of the difference in propagation delays of the specified terminals of two units tested with identical test conditions (such as V_{CC} and temperature).
9. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
10. EN = 0 indicates that the output(s) under test are disabled using the appropriate logic pin settings. EN = 1 indicates that the logic pins are set to enable the output(s) under test.
11. Logic pins are the enable variants and SHDNEN.
12. EN low and $\overline{EN}$ high.
13. Shutdown is entered by simultaneously disabling all four outputs for at least 600ns.

2.5 Test Circuits and Waveforms

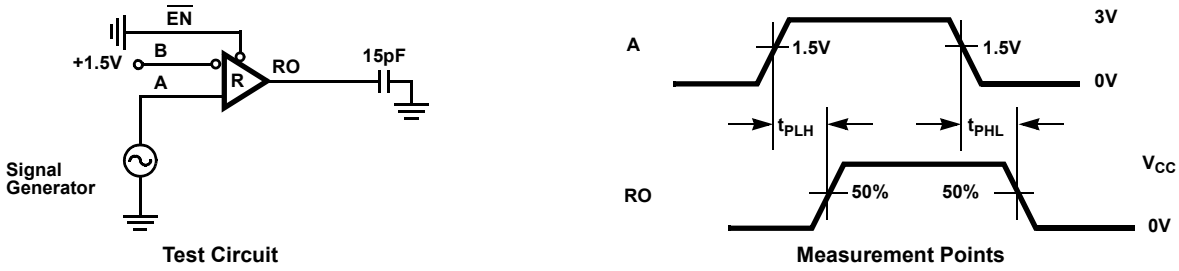
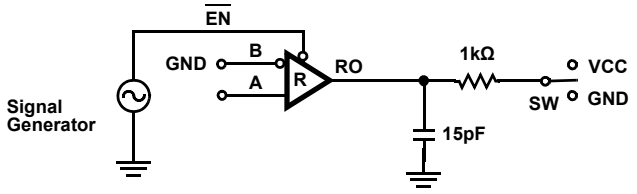
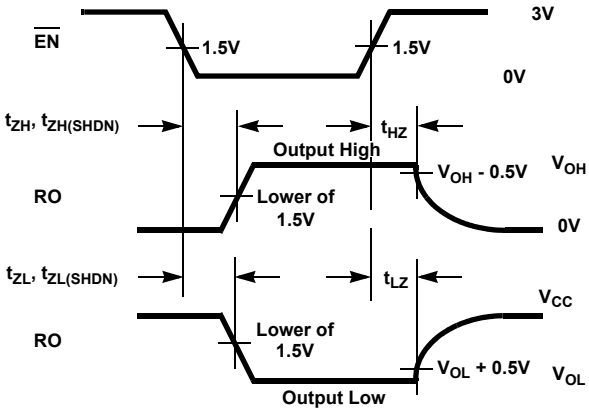


Figure 3. Receiver Propagation Delay



Parameter	A	SW
t_{HZ}	+1.5V	GND
t_{LZ}	-1.5V	VCC
$t_{ZH(SHDN)}$ (Note 13)	+1.5V	GND
$t_{ZL(SHDN)}$ (Note 13)	-1.5V	VCC

Test Circuit



Measurement Points

Figure 4. Receiver Enable and Disable Times

3. Typical Performance Curves

C_L = 15pF, V_{CC} = 5V, T_A = +25°C; unless otherwise specified.

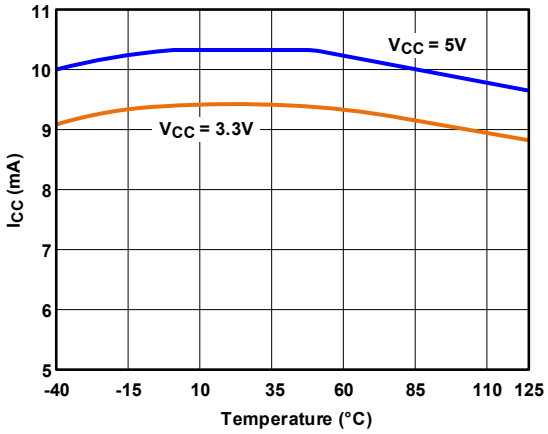


Figure 5. Supply Current vs Temperature

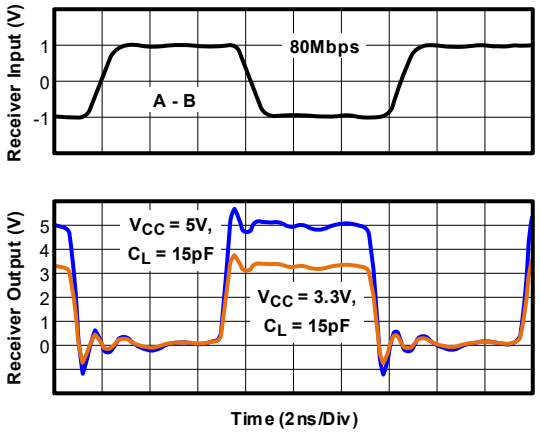


Figure 6. Receiver Waveforms

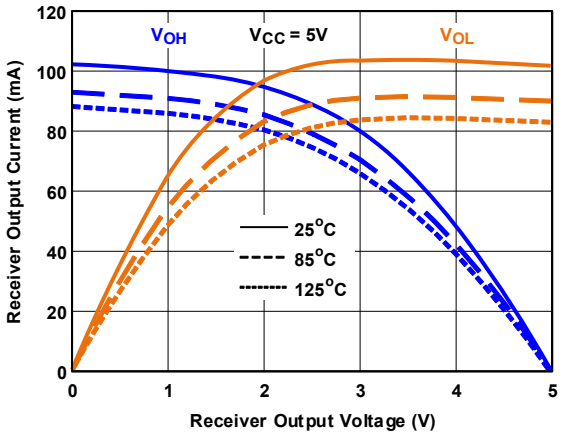


Figure 7. Receiver Output Current vs Receiver Output Voltage

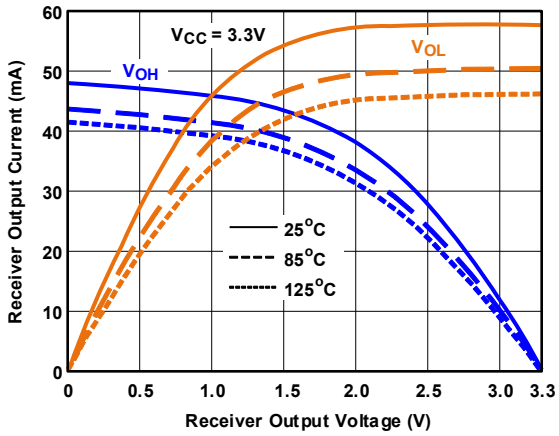


Figure 8. Receiver Output Current vs Receiver Output Voltage

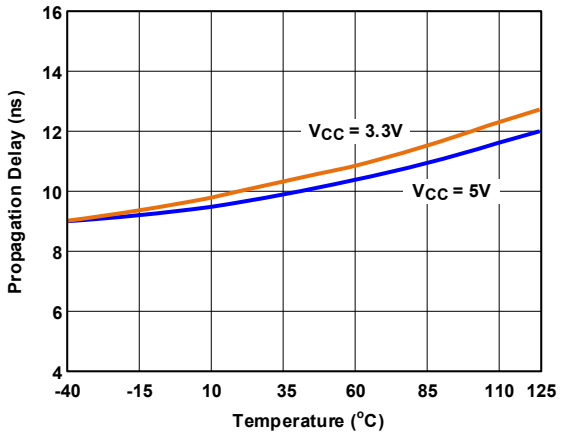


Figure 9. Receiver Propagation Delay vs Temperature

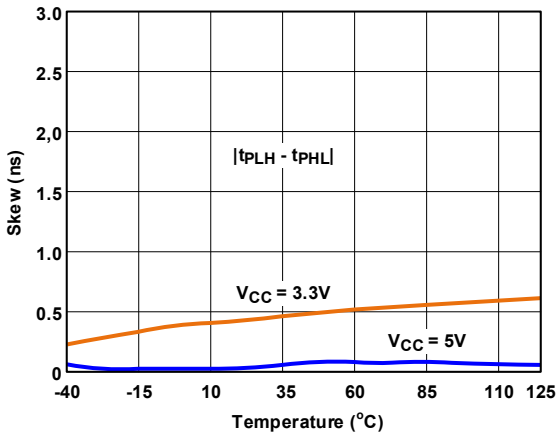


Figure 10. Receiver Skew vs Temperature

4. Application Information

RS-485 and RS-422 are differential (balanced) data transmission standards for use in long haul or noisy environments. RS-422 is a subset of RS-485, so RS-485 transceivers are also RS-422 compliant. RS-422 is a multidrop standard that allows only one driver and up to 10 one-unit load (1UL) receivers on each bus. 1 UL in RS-422 translates into a load resistance of 4kΩ. The RS-485 is a multipoint standard that allows up to 32 one-unit load devices (any combination of drivers and receivers) on each bus. 1UL in RS-485 translates into a load resistance of 12kΩ.

Another important advantage of RS-485 is the extended Common-Mode Range (CMR), which specifies that the driver outputs and receiver inputs withstand signals that range from +12V to -7V. RS-422 and RS-485 are intended for runs as long as 4000', so the wide CMR is necessary to handle ground potential differences, and voltages induced in the cable by external fields.

4.1 Receiver Features

The RAA7884QR uses differential receivers for maximum noise immunity and common-mode rejection. Input sensitivity is better than ±200mV, as required by the RS-422 and RS-485 specifications.

The receiver input resistance of 48kΩ surpasses the RS-422 specification of 4kΩ and is four times the RS-485 Unit Load (UL) requirement of 12kΩ minimum. Therefore, this device is known as a **one-quarter UL** receiver and there can be up to 128 of these devices on a network while still complying with the RS-485 loading specification.

Receiver inputs function with common-mode voltages as great as +9V/-7V outside the power supplies (for example, +12V and -7V with V_{CC} = 3.0V), making them ideal for long networks where induced voltages and ground potential differences are real concerns.

The receiver includes a "fail-safe open" function that ensures a high-level receiver output if the receiver inputs are unconnected (floating).

The RAA7884QR supports data rates up to 80Mbps. The receiver outputs are tri-statable.

4.2 Receiver Enable Functions

The RAA7884QR allows disabling of the Rx outputs. The RAA7884QR feature group (all four Rx) enables functions that are active high (EN) or active low ($\overline{EN}$). Receivers enable when EN = 1 or when $\overline{EN}$ = 0 and they disable only when EN = 0 and $\overline{EN}$ = 1. The Enable pins have internal pull-up resistors to VCC, but unused enable pins that need to be high (for example, $\overline{EN}$ when using the EN input for Enable control) should always be connected externally to VCC. If V_{CC} transients exceed 7V, insert a series resistor between the input(s) and VCC to limit the current that flows if the ESD protection of the input starts conducting.

4.3 Wide Supply Range

The RAA7884QR operates with a wide range of supply voltages from 3.0V to 5.5V and the receiver meets the RS-485 specs for that full supply voltage range.

4.4 Hot Plug Function

When a piece of equipment powers up, there is a time when the processor or ASIC driving the RS-485 control lines (EN, $\overline{EN}$) is unable to ensure that the RS-485 Rx outputs are kept disabled. If the equipment is connected to the bus, a receiver activating prematurely during power-up can generate RO transitions that can cause interrupts. To avoid this scenario, this device incorporates a hot plug function. During power-up, circuitry monitoring VCC ensures that the Rx outputs remain disabled for a while, regardless of the state of the enables. This gives the processor/ASIC a chance to stabilize and drive the RS-485 control lines to the proper states.

4.5 ESD Protection

The pins on this device include Class 3 (>8kV) Human Body Model (HBM) ESD protection structures, but the RS-485 pins (receiver inputs) incorporate advanced structures allowing them to survive ESD events above ±15kV HBM and ±16.5kV IEC 61000-4-2. The RS-485 pins are particularly vulnerable to ESD damage because they typically connect to an exposed port on the exterior of the finished product. Touching the port pins, or connecting a cable, can cause an ESD event that could destroy unprotected ICs. The new ESD structures protect the device whether powered up or not, without degrading the RS-485 common-mode range of -7V to +12V.

4.6 IEC 61000-4-2 Testing

The IEC 61000 test method applies to finished equipment, rather than to an individual IC, so the pins most likely to suffer an ESD event are those that are exposed to the outside world (the RS-485 pins in this case). Also, the IC is tested in its typical application configuration (power applied) rather than testing each pin-to-pin combination. The IEC61000 standard for the lower current limiting resistor coupled with the larger charge storage capacitor yields a test that is more severe than the HBM test. The extra ESD protection, built into the RS-485 pins of this device, allows for the design of equipment to meet a Level 4 criteria without the need for additional board-level protection on the RS-485 port.

4.6.1 Air-Gap Discharge Test Method

For the air-gap discharge test method, a charged probe tip moves toward the IC pin until the voltage arcs to it. The current waveform delivered to the IC pin depends on variables such as approach speed, humidity, and temperature, so it is difficult to obtain repeatable results. The A and B RS-485 pins withstand ±16.5kV air-gap discharges.

4.6.2 Contact Discharge Test Method

During the contact discharge test, the probe contacts the tested pin before the probe tip is energized, thereby eliminating the variables associated with the air-gap discharge. This quad receiver survives ±8kV contact discharges on the RS-485 pins.

4.7 Data Rate, Cables, and Terminations

The RS-485 and RS-422 are intended for network lengths up to 4000', but the maximum system data rate decreases as the transmission length increases. Networks operating at 80Mbps are limited to lengths much less than 100' (30m).

This device can be used at slower data rates, but there are some limitations. The RAA7884QR is optimized for high-speed operation, so its output may glitch if the Rx input differential transition times are too slow. Keeping the transition times below 500ns, which equates to a Tx driving a 1000' (305m) CAT 5 cable, yields excellent performance across the full operating temperature range.

Twisted pair is the cable of choice for RS-485 and RS-422 networks. Twisted pair cables tend to pick up noise and other electromagnetically induced voltages as common-mode signals, that are effectively rejected by the differential receivers in this device.

When using this receiver, proper termination is imperative to minimize reflections. Short networks using slew rate limited transmitters do not need to be terminated, but terminations are recommended unless power dissipation is an overriding concern.

In point-to-point or multidrop (single driver on a bus with multiple receivers) networks, terminate the main cable in its characteristic impedance (typically 120Ω) at the end farthest from the driver. In multireceiver applications, keep stubs connecting receivers to the main cable as short as possible. Multipoint (multidriver) systems requires that the main cable is terminated in its characteristic impedance at both ends. Keep stubs connecting a transmitter or receiver to the main cable as short as possible.

4.8 Low Power Shutdown Mode

This BiCMOS receiver uses a fraction of the power required by its bipolar counterparts, but it also includes a shutdown feature that reduces the already low quiescent I_{CC} to a microamp trickle. The RAA7884QR enters shutdown whenever EN is low and $\overline{EN}$ is high.

Remember that the Enable pins have pull-up resistors on them, so each pin that is low during shutdown adds up to 15µA to the SHDN supply current. The shutdown supply current entries in the Electrical Specifications table on page 5 include the resistor currents of the pins indicated to be in the low state.

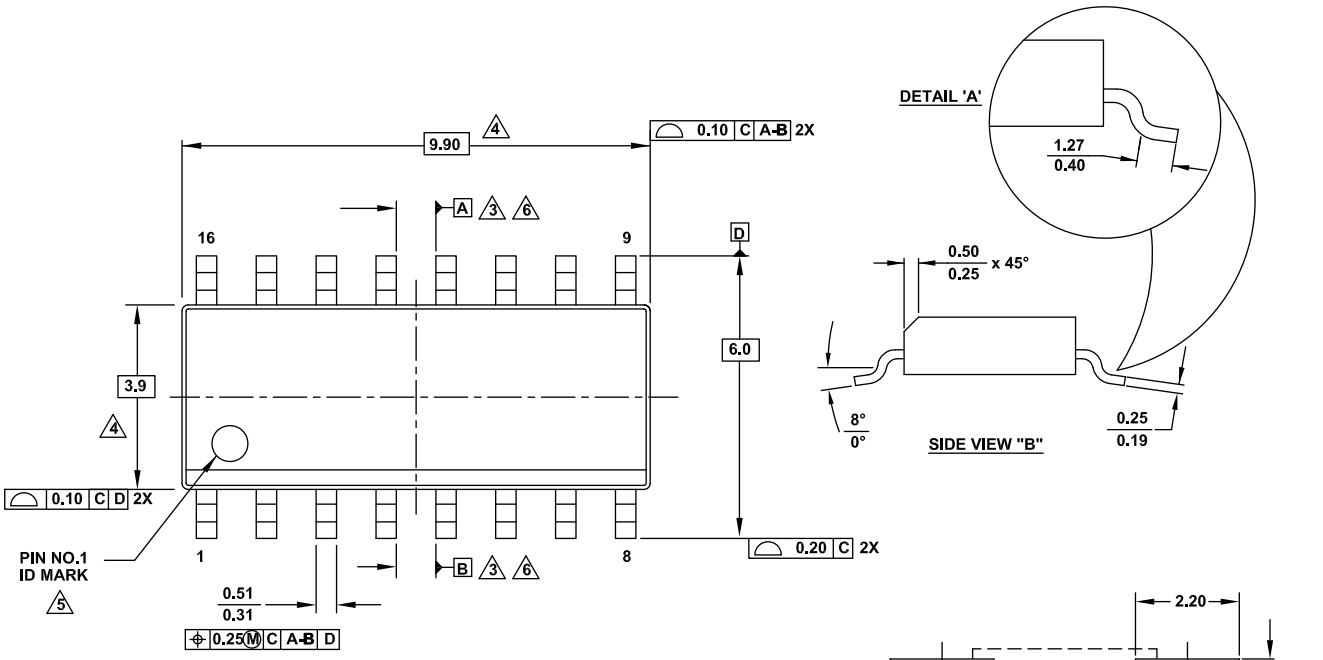
5. Revision History

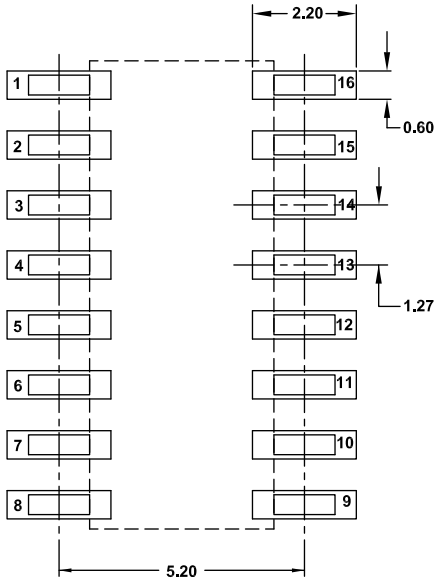
Rev.	Date	Description
2.00	Oct.14.20	Replaced Figure 1 and Figure 6. On page 5, updated Maximum Data Rate specifications for the Receiver Switching Characteristics by changing minimum spec for VCC > 3.6V from 20Mbps to 50Mbps and removing the third row.
1.01	Jul.10.20	Updated Low shutdown supply current Features bullet on page 1 to match the Electrical Specifications on page 5.
1.00	Apr.1.20	Initial release

6. Package Outline Drawing

For the most recent package outline drawing, see M16.15.

M16.15 (JEDEC MS-012-AC ISSUE C)
16 Lead Narrow Body Small Outline Plastic Package
Rev 2, 11/17





TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Datums A and B to be determined at Datum H.
4. Dimension does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 identifier may be either a mold or mark feature.
6. Does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm total in excess of lead width at maximum condition.
7. Reference to JEDEC MS-012-AC

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