RAA211412

45V 1A 630kHz DC/DC Step-Down Regulator

The RAA211412 is a DC/DC step-down (Buck) regulator that supports a wide operating input voltage range (from 5.8V to 45V) and adjustable output voltage. It can deliver up to continuous 1A output current with premium load regulation and line regulation performance.

The RAA211412 employs the PWM peak-current mode control architecture at a 630kHz switching frequency and provides fast transient response performance. In addition, with internal soft-start and loop compensation circuit, it can be easily used with minimum BOM.

The RAA211412 also offers protection features such as cycle-by-cycle current limit, input voltage UVLO, output voltage undervoltage protection, and thermal shutdown.

The RAA211412 is available in the TSOT23-6 package.

Features

- Wide input voltage range: 5.8V to 45V
- Adjustable output voltage
- Up to 1A output current
- Internal compensation
- Internal soft-start
- 600mΩ internal MOSFET
- 630kHz switching frequency
- Pulse skipping mode under light load condition
- Cycle-by-cycle current limit
- Input voltage UVLO and output voltage undervoltage protection
- Thermal shutdown
- Available in the TSOT23-6 package

Applications

- Power Meters
- Battery Powered Devices
- Distributed Power Systems
- Handheld Power Tools

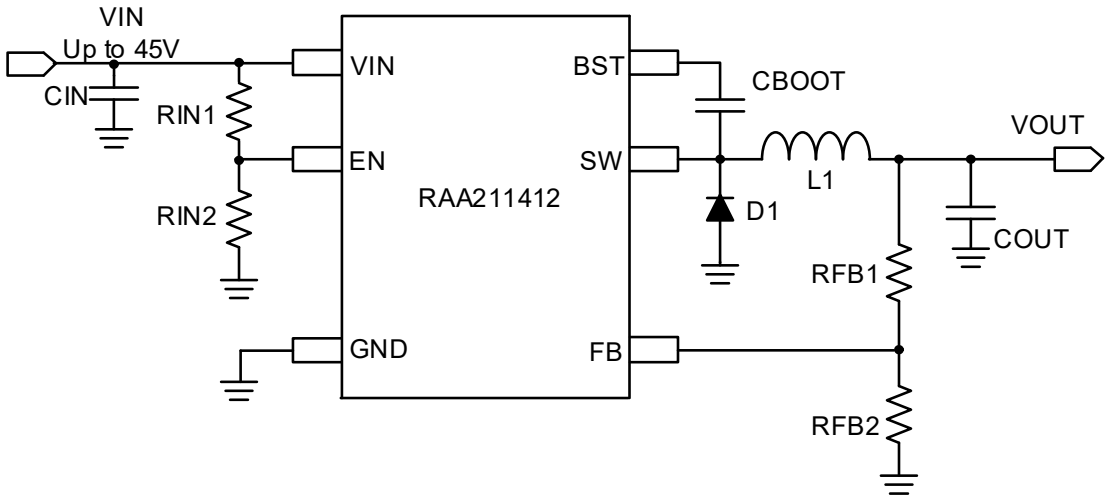


Figure 1. Typical Application Schematic

Contents

1. Overview

1.1 Block Diagram

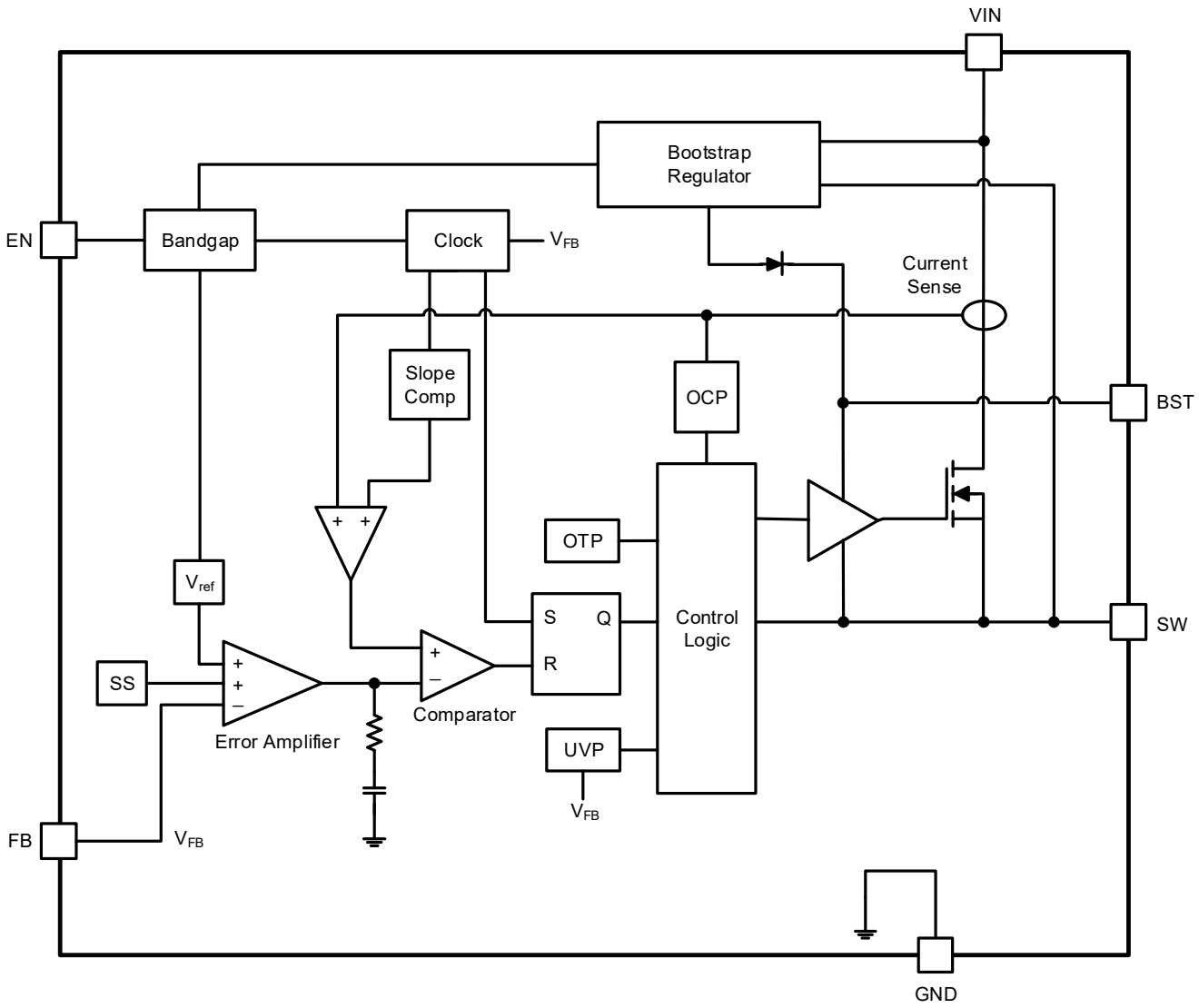
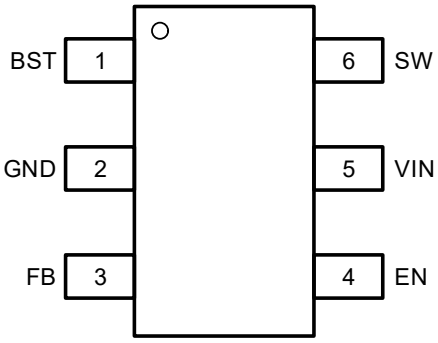


Figure 2. Block Diagram

2. Pin Information

2.1 Pin Assignments



Top View

2.2 Pin Descriptions

Pin #	Pin Name	Description
1	BST	This pin is the bootstrap circuit supply pin. Connect this pin to SW with a capacitor to provide bias voltage for the integrated MOSFET gate driver.
2	GND	This pin is the ground connection.
3	FB	This pin connects to the inverting input of the feedback error amplifier and should be connected to a properly selected resistor divider from VOUT to ground to set the output voltage.
4	EN	This pin is the enable pin. It is high voltage tolerant, therefore it can be directly connected to VIN.
5	VIN	This pin is connected to the drain of the integrated MOSFET. This pin is also connected to the input of internal linear regulator that provide bias for the IC. Connect this pin to the input rail.
6	SW	This pin is the phase node of the regulator and is connected to the source of the integrated MOSFET. This pin should be connected to the inductor, diode, and boot capacitor.

3. Specifications

3.1 Absolute Maximum Ratings

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter[1]	Min	Max	Unit
VIN	-0.3	55	V
EN	-0.3	55	V
SW	-0.7	V_{IN} + 0.3	V
BST		SW+4	V
BST to SW	-0.3	4	V
All other pins	-0.3	4	V
Operating junction temperature	-40	150	°C
Storage temperature range	-65	150	°C

1. All voltages referenced to VSS unless otherwise specified.

3.2 Recommended Operating Conditions

Parameter	Min	Max	Unit
Input Voltage (V_{IN})	5.8	45	V
Output Voltage (V_{OUT})	0.8	Vin × D_{MAX}[1]	V
Output Current (I_{OUT})	0	1	A
Junction Temperature (T_J)	-40	125	°C

1. D_{MAX} is 89% to 91%. Also, see the BST Refresh and BST Regulator section for refresh considerations.

3.3 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)[1]	θ_{JC} (°C/W)[2]
TSOT23	114	42

1. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.
2. For θ_{JC}, the case temperature location is on the top side of the package.

3.4 Electrical Specifications

Typical Values are at T_A = +25°C, V_{IN} = 24V unless otherwise noted. Min and Max values apply across the junction temperature range, -40°C to +125°C.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
V_{IN} Supply						
Input Voltage Range	V_{IN}		5.8		45	V
Shutdown Current		EN = 0V		2		µA
Quiescent Current	Iq	EN = 2V, V_{FB} = 0.825V, No Switching		300	450	µA

Typical Values are at T_A = +25°C, V_{IN} = 24V unless otherwise noted. Min and Max values apply across the junction temperature range, -40°C to +125°C. (Cont.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VIN/EN UVLO						
V_{IN} UVLO Threshold		Rising	5.1	5.4	5.7	V
V_{IN} UVLO Hysteresis		Falling		250		mV
EN UVLO		Rising	1	1.275	1.55	V
EN Hysteresis		Falling		125		mV
Feedback Voltage Reference						
Feedback Voltage Reference	V_{FB}	V_{IN} = 12V, 25°C	0.788	0.8	0.812	V
		V_{IN} = 12V, -40°C to 125°C	0.776	0.8	0.824	V
Feedback Voltage Line Regulation		5.8V < V_{IN} < 45V, -40°C to 125°C		0.5		µV/V
Integrated MOSFET						
High-Side FET On-Resistance	r_{DS_ONh}			600		mΩ
Soft Start						
Internal Soft-Start Time	t_{SS}			1		ms
Oscillator/PWM Comparator						
Switching Frequency	f_{SW}	V_{FB} = 0.8V	567	630	693	kHz
Minimum On-Time	t_{ON_MIN}	-40°C to 125°C			125	ns
Minimum Off-Time	t_{OFF_MIN}	25°C		162		ns
Over Current Protection (OCP)/VOUT Undervoltage Protection (UVP)						
Peak Current Limit	I_{HSOC}	Duty ratio = 0.9, 25°C		1.36	2.3	A
V_{FB} Undervoltage Threshold		V_{FB} falling, soft start completed		33		%
Foldback Frequency		V_{FB} = 0V		105		kHz
Hiccup Time	t_{HICCUP}			23		ms
Thermal Shutdown (OTP)						
Thermal Shutdown				158		°C
Thermal Shutdown Hysteresis				28		°C

4. Typical Performance Curves

Typical Values are at T_A = +25°C, V_{IN} = 24V, V_{OUT} = 3.3V, C_{OUT} = 10µF, unless otherwise noted.

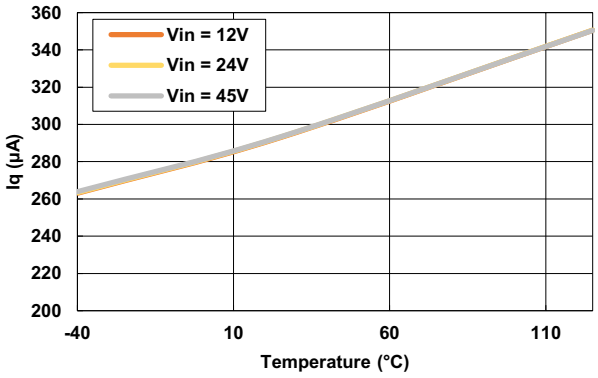


Figure 3. Quiescent Current vs Temperature

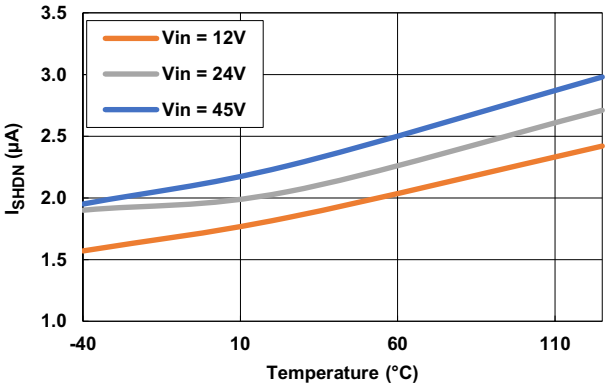


Figure 4. Shutdown Current vs Temperature

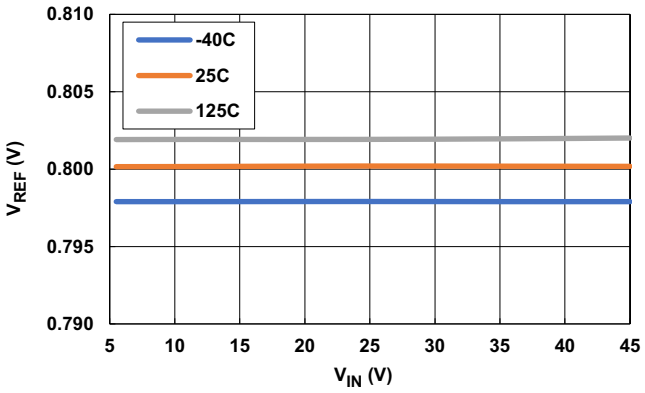


Figure 5. V_{REF} vs Temperature

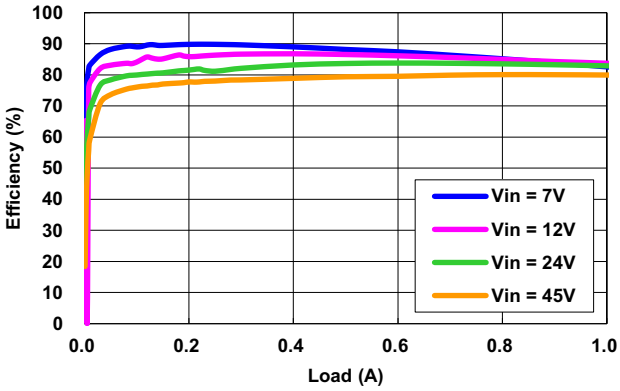


Figure 6. Efficiency

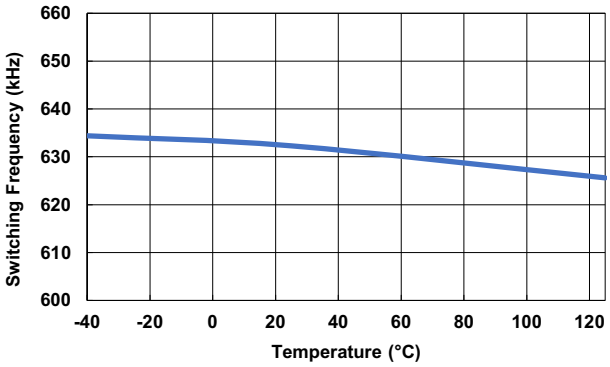


Figure 7. Switching Frequency vs Temperature

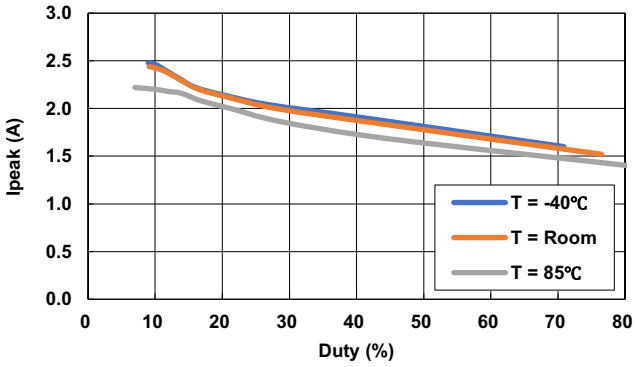


Figure 8. Peak Current vs Duty Cycle

Typical Values are at T_A = +25°C, V_{IN} = 24V, V_{OUT} = 3.3V, C_{OUT} = 10µF, unless otherwise noted. (Cont.)

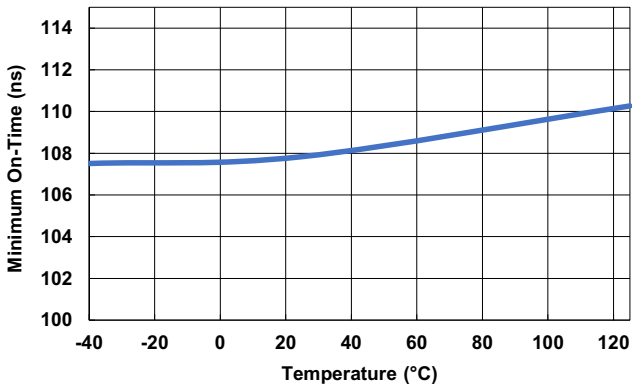


Figure 9. Minimum On-Time vs Temperature

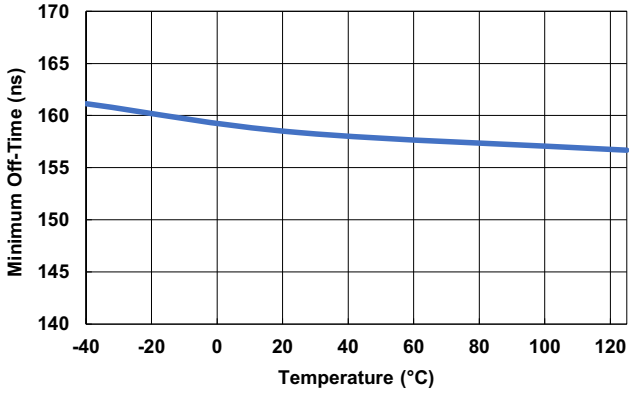


Figure 10. Minimum Off-Time vs Temperature

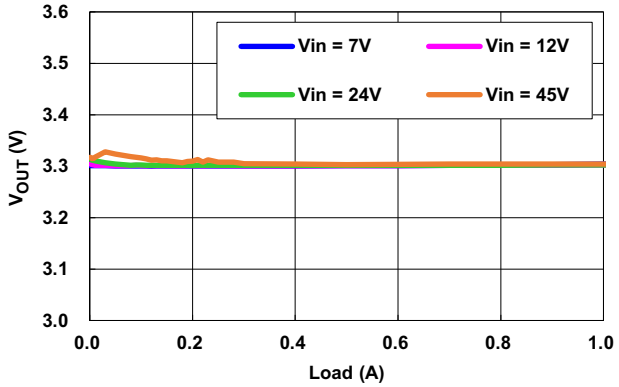


Figure 11. V_{OUT} vs Load

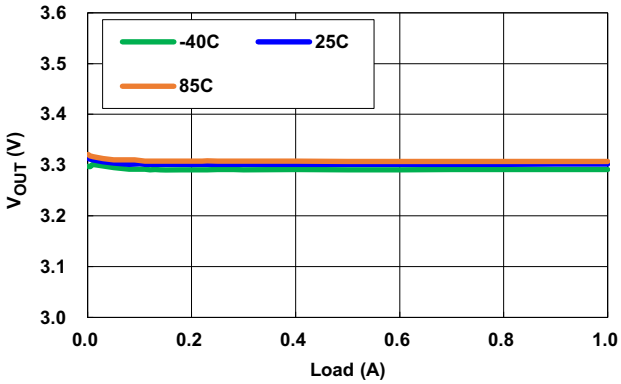


Figure 12. V_{OUT} vs Temperature (V_{IN} = 24V)

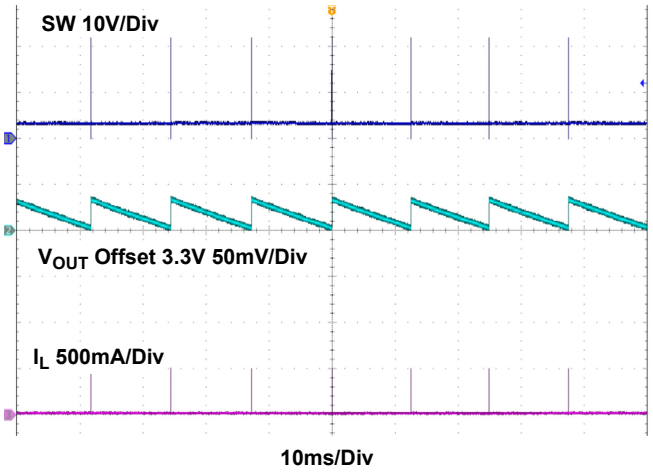


Figure 13. Typical Operation (No Load)

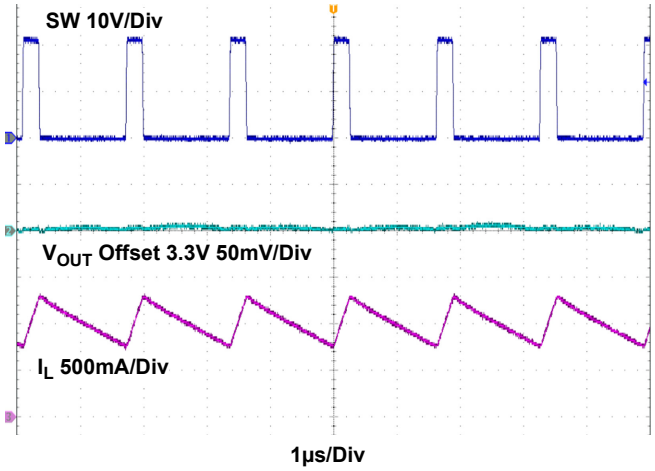


Figure 14. Typical Operation (Full Load)

Typical Values are at T_A = +25°C, V_{IN} = 24V, V_{OUT} = 3.3V, C_{OUT} = 10µF, unless otherwise noted. (Cont.)

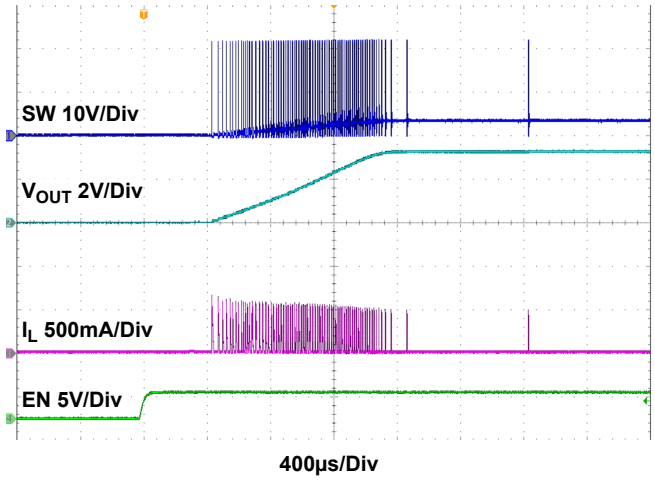


Figure 15. Startup by EN (No Load)

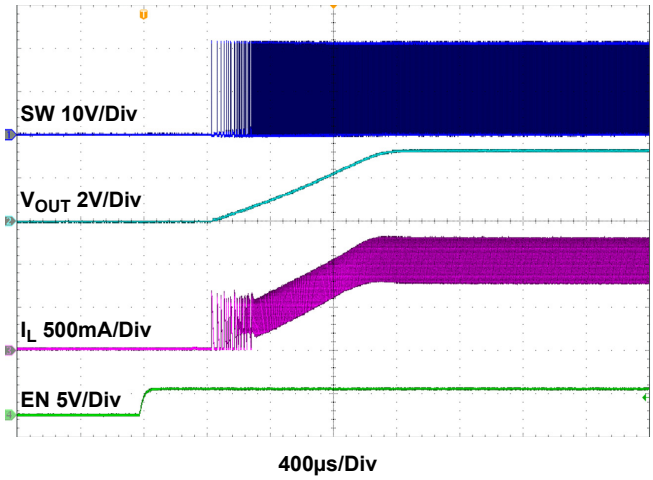


Figure 16. Startup by EN (Full Load)

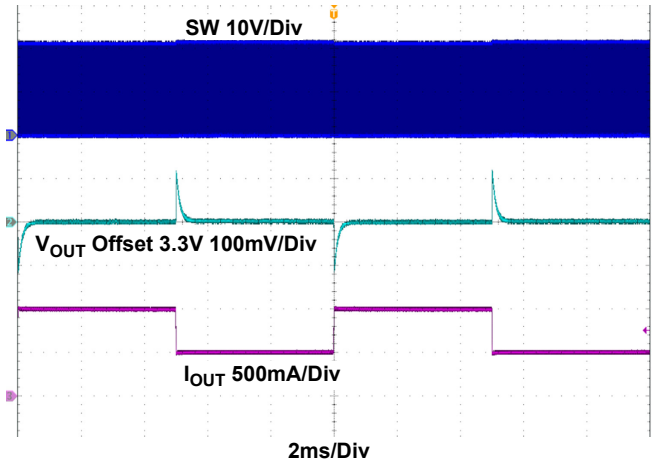


Figure 17. Load Transient Response (0.5A to 1A)

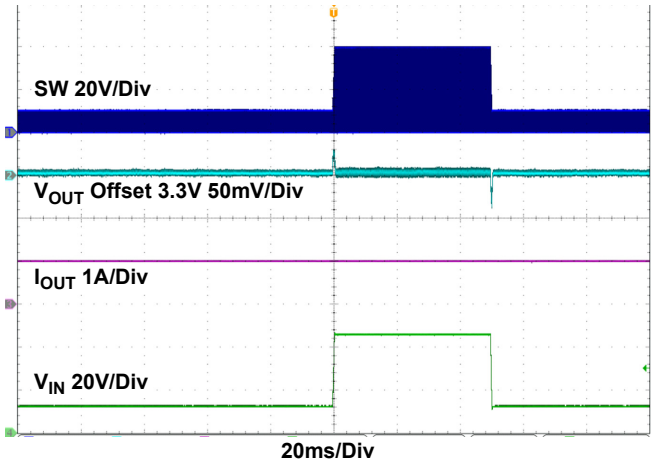


Figure 18. Line Transient Response at Full Load (12V to 45V)

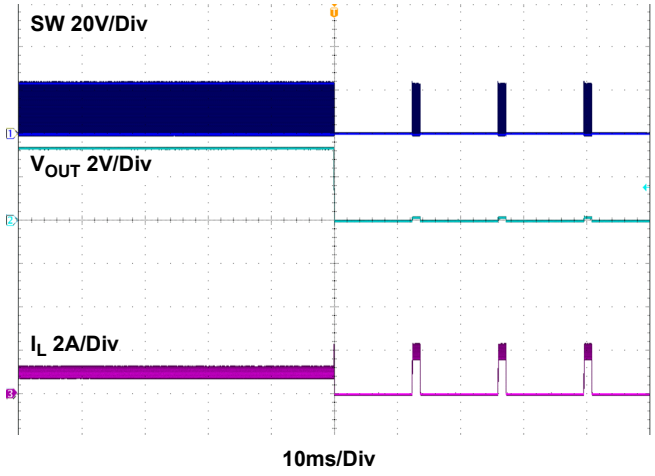


Figure 19. Overcurrent Protection (Full Load)

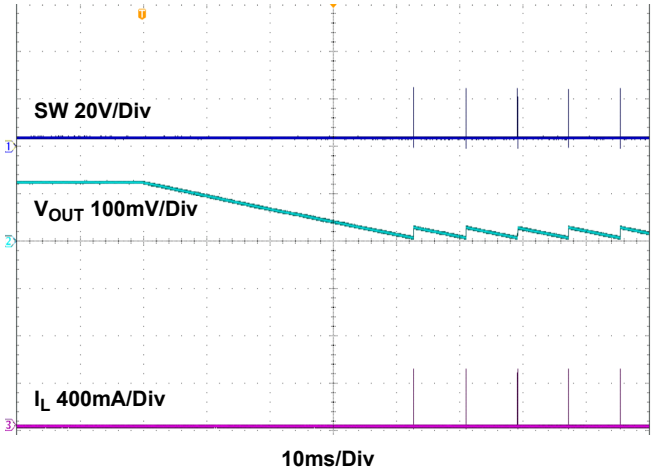


Figure 20. Overvoltage Protection (No Load)

5. Function Description

The RAA211412 is a peak current mode DC/DC step-down regulator with internal loop compensation. At light load or no load, it operates in pulse skipping mode. As the load increases and the regulator transitions from DCM to CCM, it operates at a fixed switching frequency of 630kHz.

5.1 Soft-Start

Soft-start forces the regulator output to ramp up in a controlled fashion, which helps reduce input inrush current into the buck output capacitors. During the soft-start period for the buck converter, the reference voltage of the error amplifier ramps from 0V to its nominal value of 0.8V in approximately 1ms.

5.2 Input Undervoltage Lockout

Input undervoltage lockout (UVLO) prevents the RAA211412 from operating until the input voltage exceeds 5.4V (typical). The UVLO threshold has approximately 250mV of hysteresis, so the device continues to operate when V_{IN} decreases until it drops below 5.15V (typical). Hysteresis prevents the part from turning off during power-up if V_{IN} is non-monotonic.

5.3 Current Limit

The RAA211412 uses cycle-by-cycle current limiting to protect the output switch. During each switching cycle, a current limit comparator detects if the output switch current exceeds 1.36A (typical) and turns off the switch until the next switching cycle begins. As the output voltage and the voltage on the FB pin decreases, the frequency fold-back function kicks in. When V_{FB} is 0, the fold-back frequency is around 105kHz.

5.4 Output Undervoltage Protection

The RAA211412 output undervoltage protection (UVP) is triggered if the FB pin voltage falls below 33% (typical) of nominal after the soft-start time completes. The response to UVP is to stop switching for the 23ms hiccup interval before retrying a new startup, which protects against both overcurrent faults and severe dropout conditions. In an overcurrent fault, the switch current is limited, and the output voltage falls. If FB voltage drops to the UVP threshold, the device enters the hiccup condition. In a severe overcurrent or a short on the output, the switching frequency folds back to 105kHz as secondary protection. When the input voltage is too low to maintain output voltage regulation, the RAA211412 operates in a dropout behavior where it switches at the maximum duty cycle. If the input voltage drops low enough to cause FB to fall to the UVP threshold, the device enters the hiccup condition.

5.5 Thermal Shutdown

Thermal shutdown limits total power dissipation by turning off the output switch when the IC junction temperature exceeds 158°C (typical). After thermal shutdown occurs, the output switch does not turn on until the junction temperature drops to approximately 130°C (typical).

6. Applications Information

6.1 Output Voltage Feedback Resistor Divider

The output voltage can be programmed down to 0.8V with a resistor divider from VOUT to FB pin to GND based on Equation 1. The recommended R_{FB2} (see Figure 1) resistance is 20kΩ. Table 1 can be referenced for R_{FB1} and R_{FB2} for typical V_{OUT} applications.

(EQ. 1) $$R_{FB1} = R_{FB2} \times \frac{V_{OUT} - 0.8}{0.8}$$

Table 1. Recommended Components Selection for Typical Applications

V_{OUT} (V)	R_{FB1} (kΩ)	R_{FB2} (kΩ)	L (µH)	C_{OUT}
0.8	0	20	3.3	56µF/10V/X7R/X5R
1.5	17.4	20	4.7	33µF/10V/X7R/X5R
3.3	61.9	20	10	22µF/10V/X7R/X5R
5	105	20	15	10µF/10V/X7R/X5R
12	280	20	33	4.7µF/50V/X7R/X5R
24	576	20	68	4.7µF/50V/X7R/X5R

6.2 Input Undervoltage Lockout

The input undervoltage lockout level can be set with a resistor divider from VIN to EN pin to GND based on Equation 2 (see Figure 1) where V_{INR} is the minimum input voltage for the part to turn on.

(EQ. 2) $$R_{IN1} = R_{IN2} \times \frac{V_{INR} - 1.275}{1.275}$$

The resulting input voltage V_{INF} for the part to be turned off is calculated using Equation 3 (see Figure 1).

(EQ. 3) $$V_{INF} = 1.15 \times \frac{R_{IN1} + R_{IN2}}{R_{IN2}}$$

6.3 Inductor Selection

The inductor of the buck converter determines its current ripple and factors such as inductance, saturation current, DC resistance should be considered when selecting it. Choosing the inductance requires the choice of inductor current ripple. Larger inductance results in less inductor current ripple and therefore less output voltage ripple. However, it may increase the response time and output voltage variance during a load transient. A reasonable starting point for inductor current ripple is 30% to 60% of the maximum output current. Considering the wide operating input voltage range of the part, Renesas recommends estimating the required inductance L using Equation 4 where V_{OUT} is the output voltage in V and the inductance L is in µH. Table 1 can be referenced for selecting the inductance for typical V_{OUT} applications.

(EQ. 4) $$L = 3 \times V_{OUT}$$

In addition, the saturation current rating of the inductor should be higher than the peak current under overload conditions. For lower loss and smaller output voltage ripple, the inductor with smallest possible DC resistance should be selected provided its mechanical dimensions meet application requirements.

6.4 Input Capacitor Selection

The input capacitor is used in Buck converter to maintain the input voltage by suppressing the voltage ripple induced by discontinuous switching current. The required RMS current rating $I_{IN(RMS)}$ of the input capacitor can be calculated using the following Equation 5 where $I_{OUT(MAX)}$ is the maximum average load current and D is the duty ratio. When D equals 0.5, $I_{IN(RMS)}$ has the maximum value which is $I_{OUT(MAX)}/2$.

(EQ. 5) $$I_{IN(RMS)} = I_{OUT(MAX)} \times \sqrt{D \times (1 - D)}$$

The voltage rating of the input capacitor should be higher than the maximum input voltage. The required capacitance (C_{IN}) of the input capacitor to ensure the expected peak-to-peak input voltage ripple ΔV_{IN} is calculated using Equation 6 where f_{SW} is the switching frequency.

(EQ. 6) $$C_{IN} = I_{OUT(MAX)} \times \frac{D \times (1 - D)}{f_{SW} \times \Delta V_{IN}}$$

The required capacitance also has the maximum value when D equals 0.5. Renesas recommends using ceramic capacitors as input capacitor, which has low ESR and low ESL. When selecting the ceramic capacitor, it should be considered that the effective capacitance reduces with DC bias voltage across it. Also, Renesas recommends using X7R ceramic capacitors because of their small temperature coefficient.

If the part is connected to the power source through a high-impedance path, Renesas recommends adding an electrolytic capacitor in addition to the ceramic capacitor to damp the input voltage oscillation.

6.5 Output Capacitor Selection

The output capacitor determines both steady state performance and transient performance of the Buck converter. Factors such as output voltage ripple, output voltage variation during transients, and control loop stability should be considered when selecting the output capacitor. For this part, X7R ceramic capacitors are recommended to be used as the output capacitor. When selecting the ceramic capacitor, it should be considered that the effective capacitance reduces with DC bias voltage across it.

For the ceramic capacitor, its capacitance is dominating the voltage ripple. Therefore, the required capacitance $C_{OUT(RIPPLE)}$ for the expected peak-to-peak output voltage ripple $\Delta V_{OUT(RIPPLE)}$ is calculated using Equation 7 where ΔI_L is the inductor the inductor peak-to-peak current ripple and f_{SW} is the switching frequency.

(EQ. 7) $$C_{OUT(RIPPLE)} = \frac{\Delta I_L}{8 \times f_{SW} \times \Delta V_{OUT(RIPPLE)}}$$

To meet the output voltage variation requirements during load step up and load step down transients, the required capacitance $C_{OUT(STEPUP)}$ is calculated using Equation 8 and $C_{OUT(STEPDOWN)}$ is calculated using Equation 9 where I_{STEP} is the transient load step and ΔV_{OUT} is the expected voltage variation during the transient.

(EQ. 8) $$C_{OUT(STEPUP)} = \frac{L \times \left(I_{STEP} + \frac{\Delta I_L}{2}\right)^2}{2 \times (V_{IN} - V_{OUT}) \times \Delta V_{OUT}}$$

(EQ. 9) $$C_{OUT(STEPDOWN)} = \frac{L \times \left(I_{STEP} + \frac{\Delta I_L}{2}\right)^2}{2 \times V_{OUT} \times \Delta V_{OUT}}$$

For the control loop to be stable with gain and phase margin as well as sufficient bandwidth, the required capacitance COUT(LOOP) can be estimated using Equation 10 where $C_{OUT(LOOP)}$ is in µF and V_{OUT} is in V.

(EQ. 10) $$C_{OUT(LOOP)} = \frac{22}{V_{OUT}}$$

The output capacitors should be selected such that aforementioned requirements are met which means the total output capacitance should be higher than the maximum value of the above calculated capacitance.

For convenience, Table 1 can be referenced when selecting output capacitors for typical V_{OUT} applications.

6.6 Diode Selection

The RAA211412 requires a freewheeling diode for inductor current to flow when the internal high-side MOSFET is turned off. Renesas recommends choosing a diode with reverse voltage rating at least 20% higher than the maximum input voltage. The continuous current rating of the diode should be greater than the highest output current. Ideally, the selected diode should have minimum forward voltage and reverse recovery time. Therefore, Schottky diodes are recommended. However, bigger sized diodes with higher current rating can be selected as well for thermal and efficiency considerations.

6.7 BST Refresh and BST Regulator

BST voltage is generated by an internal 3V regulator and acts as the power supply for the high-side MOSFET gate driver. The internal regulator charges the boot capacitor when the SW node is pulled low during the switching cycle, as well as any time VIN-SW is greater than 3V. For the typical case of high V_{IN} voltage and low V_{OUT} voltage ($V_{IN} – V_{OUT} > 3V$), no switching is needed to keep BST refreshed and the device can skip cycles for an unlimited duration in light load for improved efficiency. If an application runs in the dropout mode of the BST regulator ($V_{IN} – V_{OUT} < 3V$), a minimum load of 5mA to 10mA is recommended to ensure some occasional switching will keep BST refreshed.

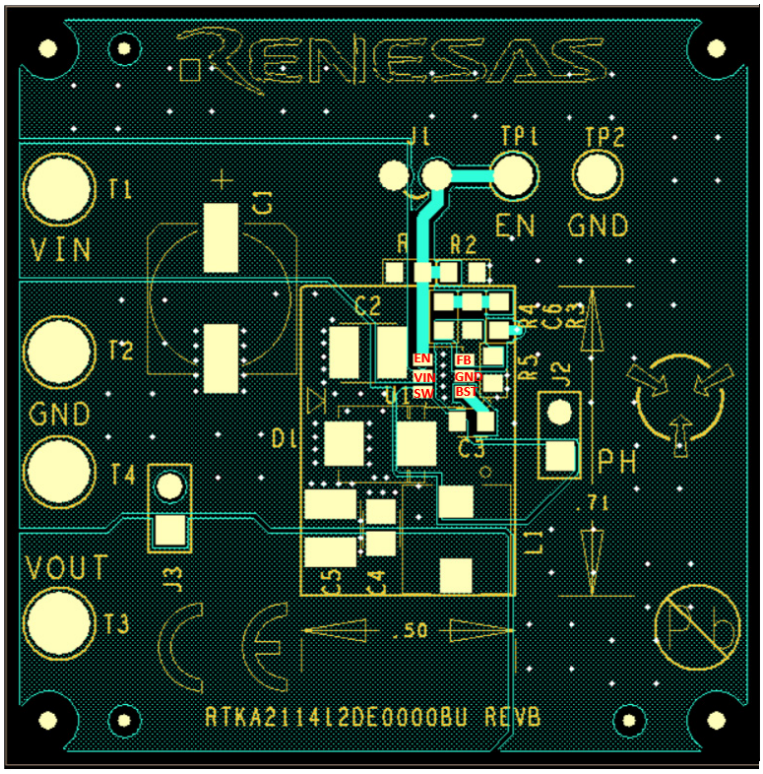
6.8 Boot Capacitor Selection

A capacitor is needed between BST pin and SW pin to provide gate voltage for the high-side internal MOSFET. Renesas recommends using a 16V X7R 0.1µF ceramic capacitor as the bootstrap capacitor for most applications.

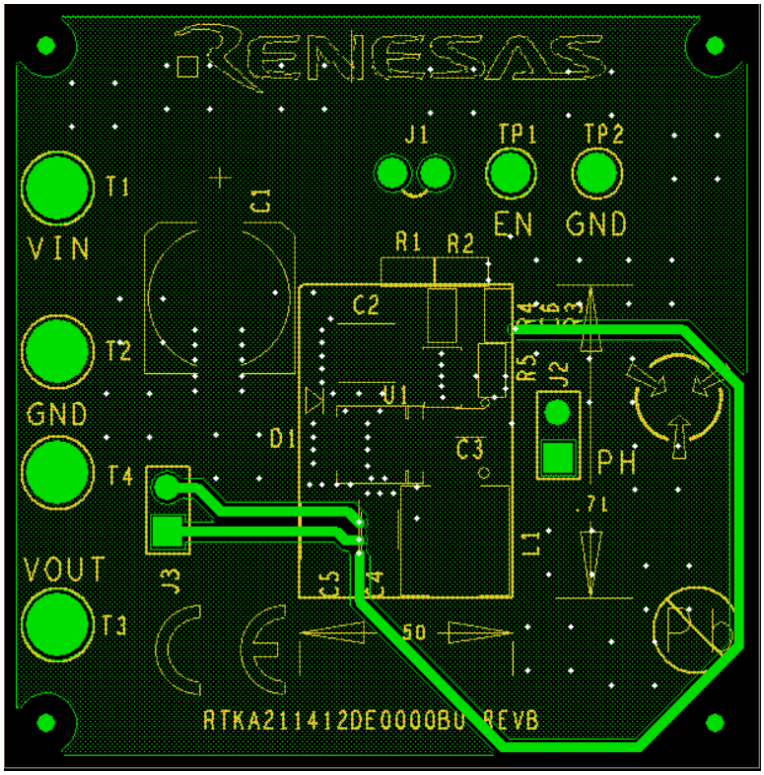
7. Layout Suggestions

1. Place the input ceramic capacitor(s) as close as possible to the IC VIN PIN and the diode. Keep the power loop (input ceramic capacitor, IC VIN pin, and diode) as small as possible for less phase voltage ring induced by trace parasitic inductance as well as better EMI performance.
2. If the aluminum electrolytic capacitor is used, place it as close as possible to the IC VIN pin.
3. Keep the phase node copper area small for less parasitic capacitance but large enough to handle the load current.
4. Place the output capacitor(s) close to the inductor and diode.
5. Connect the power ground (CIN, diode, and COUT ground) to the analog ground plain, which connects to GND pin, in only one spot.
6. Place feedback resistors close to the FB and GND pin and away from phase node.
7. Allocate adequate copper area for GND to dissipate heat. Apply ground vias near the input and output capacitors and freewheeling diode, as well as underneath the IC.

An example of layout can be seen in Figure 21, where C2 is the input ceramic capacitor, U1 is the IC, D1 is the freewheeling diode, L1 is the inductor, and C4 and C5 are output capacitors.



Top Layer



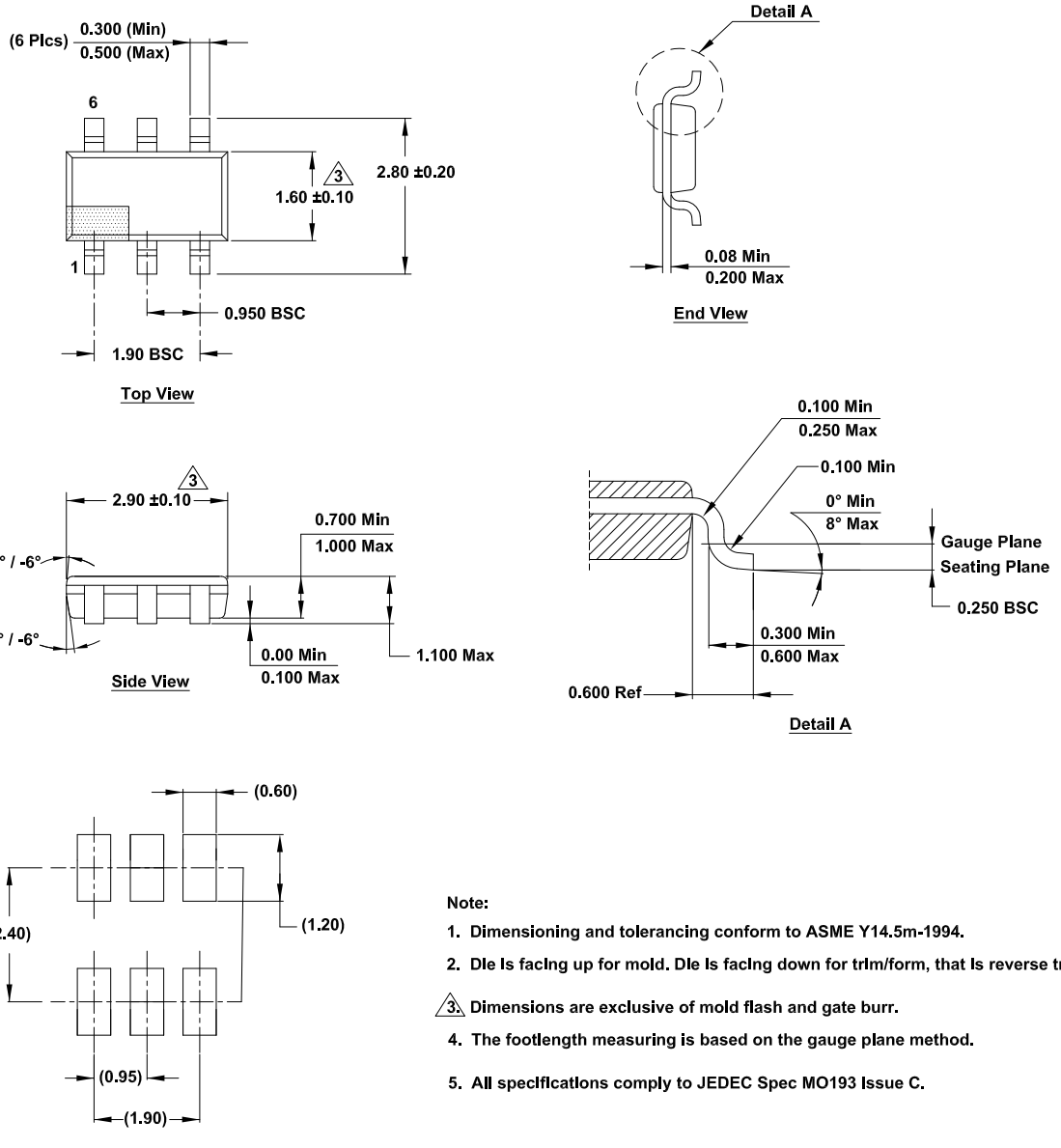
Bottom Layer

Figure 21. Example Layout

8. Package Outline Drawing

For the most recent package outline drawing, see P6.064C.

P6.064C
6 Lead Thin Small Outline Transistor (TSOT) Plastic Package
Rev 2, 12/20



Typical Recommended Land Pattern

Note:

1. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
2. Die is facing up for mold. Die is facing down for trim/form, that is reverse trim/form.
3. Dimensions are exclusive of mold flash and gate burr.
4. The footlength measuring is based on the gauge plane method.
5. All specifications comply to JEDEC Spec MO193 Issue C.

9. Ordering Information

Part Number[1][2]	Part Marking[3]	Package Description (RoHS Compliant)	Pkg. Dwg. #	Carrier Type[4]	Temp Range
RAA211412GP3#JA0	412	6 Ld TSOT	P6.064C	Reel, 3k	-40 to 125°C

1. These Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate -e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
2. For Moisture Sensitivity Level (MSL), see the Product Options on the RAA211412 product page (click the packaging icon). For more information about MSL, see TB363.
3. Part marking is located on the bottom of the part.
4. See TB347 for details about reel specifications.

10. Revision History

Revision	Date	Description
1.03	Mar 24, 2023	Updated Max for Output Voltage, VOUT in Recommended Operating Conditions.
1.02	Jun 24, 2022	Updated the Output Undervoltage Protection section. Updated Figure 21. Corrected part number.
1.01	Feb 10, 2022	Removed RAA2114124GP3#NA0 from Ordering Information.
1.00	Jan 12, 2022	Initial release.

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