



# **RA8815**

## **128x33 Character/Graphic LCD Driver Specification**

Version 2.2  
July 1, 2006

| Update History |                   |                                                                                                                                                                                                                                                                                               |
|----------------|-------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Version        | Date              | Description                                                                                                                                                                                                                                                                                   |
| 1.0            | November 26, 2004 | First Release                                                                                                                                                                                                                                                                                 |
| 1.5            | June 23, 2005     | Modify the sequence of signals EL_CHRG and EL_DCHG.<br>Add Table 8-1: Bump Size and Pitch                                                                                                                                                                                                     |
| 1.7            | September 1, 2005 | Update the Power Range and Table 9-2.<br>Modify the description of PBK_EN of REG[13h]BLTR.<br>Modify the description of AUTO)SCR of REG[0Eh]SCCR.<br>Modify Section 9-3-2 Serial Interface, the unit of Access Time should be $\mu$ s.<br>Modify the Figure A-7 and A-8 : ITO Layout Example. |
| 2.0            | November 11, 2005 | Update Figure 6-29                                                                                                                                                                                                                                                                            |
| 2.1            | January 10, 2006  | Modify Figure 6-15 and Figure 6-16: Memory Write/Read on 6800(8-Bit) I/F.<br>Modify Table 6-2: Power Circuit Setup                                                                                                                                                                            |
| 2.2            | July 1, 2006      | Modify Table 8-1: Bump Size and Pitch<br>Modify Figure 8-2 : Gold Bump PAD Dimension<br>Modify Figure 6-27: 4x5 Key Matrix Circuit                                                                                                                                                            |

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## 1. General Description

The RA8815 is a Dot-Matrix LCD Driver that supports both character and graphic mode. It built-in a 256Kbyte character ROM that consists of Chinese, English and ASCII fonts. The embedded 528Byte display RAM supports up to 128x33 dots LCD panel. The RA8815 also provides a scrolling buffer memory for scrolling functions. It supports up, down, left and right scrolling features, and all of the scrolling is execute by hardware.

In character mode, the RA8815 supports Chinese BIG5 code or GB code. The system(MPU) does not need take a lot of time to show the Chinese font in graphic mode. It also provides small ASCII(8x8) and big ASCII(8x16) font for English character, Japanese, European and Latin. The RA8815 integrates much powerful hardware that including Contrast adjustment, 4x5 Key-Scan, eight General Purpose I/O and EL Backlight signals for EL driver.

The RA8815 is a high integration chip of LCD Controller. It reduce a lot of time for system develop, and save much cost for hardware system that due to it provides many features for related LCD display application.

## 2. Feature

- Support both Character and Graphic Mode
- Support 8080/6800 8/4-bit Parallel Interface and 3-Wire/4-Wire Serial Interface
- Built-in 256KB Font ROM: Chinese, English, ASCII, Japanese, Latin, Latin-ext A, Latin-ext B
- Support ASCII 8x8/8x16 Half Size Font, 16x16 Full Size Chinese Font
- Support Maximum 128Seg x 33Com LCD Panel. 2 x 8 Chinese Fonts(16x16), or 4 x 16 English Fonts(8x8)
- Built-in 528 Bytes Display RAM and 354Byte Scrolling Buffer
- Built-in 2X~3X(Voltage Booster), Voltage Regulator, Voltage Follower
- Support 1/33 Duty, 1/6~1/4 Bias Panel
- Eight General Purpose I/O
- Built-in 4x5 Key-scan Circuit
- Support Horizontal/Vertical Scrolling Functions
- Built-in 256Byte SRAM for Create Font
- Provide Signals for EL Driver
- Provide 32-Steps Contrast Adjust
- Build-in RC Oscillator
- Voltage Operation: Chip → 2.5~3.6V · COG  
Module → 2.7~3.8V
- Package: Gold Bump Die

## 3. Block Diagram

The RA8815 is consist of Display RAM, 256Kbyte Font ROM, Command Registers, LCD Controller, LCD Driver, Voltage Booster, Voltage Regulator, MPU Interface and Key-Scan circuit.

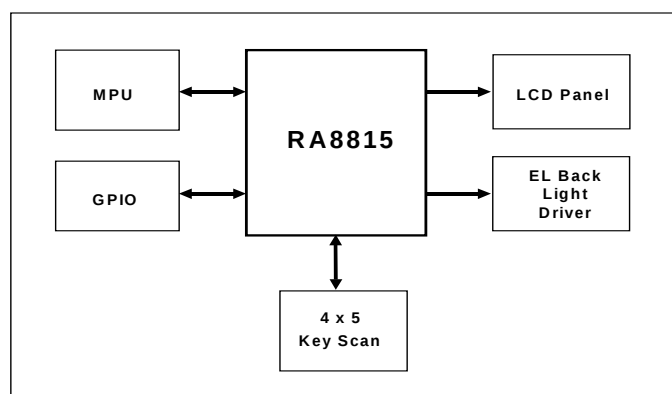


Figure 3-1: System Block

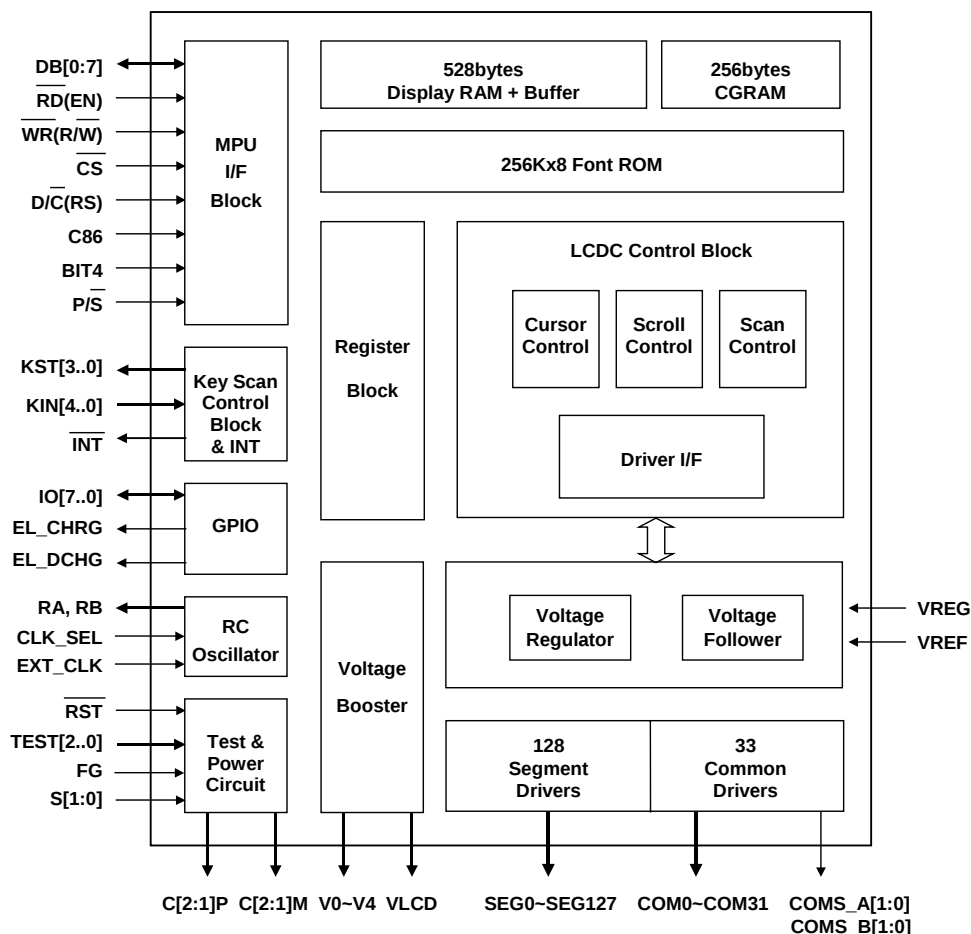


Figure 3-2: Internal Block

## 4. Pin Definition

### 4-1 MPU Interface

| Pin Name             | I/O | Description                                                                                                                                                 |
|----------------------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DB[7..0]             | I/O | <b>Data Bus</b>                                                                                                                                             |
| DB0: SCK             |     | When the MPU uses parallel mode and 8-bit then all of the DB[7:0] are valid. When use 4-bit then only DB[4:0] are valid, and DB[7:4] have to keep floating. |
| DB1: SDA/SDO         |     | When P/ $\overline{S}$ is "0", then the interface between MPU and RA8815 is Serial Mode. The pins DB[7:6](SMOD[1:0]) are used to select which serial mode:  |
| DB2: RS/SDI          |     | <b>SMOD:                      Serial Mode</b>                                                                                                               |
| DB3: $\overline{CS}$ |     | -----                                                                                                                                                       |
| DB[7:6]: SMOD        |     | 0 X : 3-Wire, SCK, SDA, $\overline{CS}$ are used.                                                                                                           |
|                      |     | 1 0 : 4-Wire, SCK, SDA, RS, $\overline{CS}$ are used.                                                                                                       |
|                      |     | 1 1 : 4-Wire, SCK, SDO, SDI, $\overline{CS}$ are used.                                                                                                      |

|                                                    |   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|----------------------------------------------------|---|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                                    |   | <p>In serial mode, all of the related signals are defined by DB[3:0]:</p> <p>SCK(DB0) : Serial Clock.<br/> SDA(DB1) : Bi-direction Mode Serial Data.<br/> SDO(DB1) : Data Out.<br/> RS(DB2) : Memory/Register Cycle Select.<br/> SDI(DB2) : Serial Data In.<br/> <math>\overline{\text{CS}}</math>(DB3) : Chip Select, active low.</p> <p>The unused pin must keep NC for serial mode.</p>                                                                                              |
| $\overline{\text{RD}}$<br>EN                       | I | <p><b>Read Control or Enable</b></p> <p>When use 8080 series interface, <math>\overline{\text{RD}}</math> is the read signal and active low.<br/> When use 6800 series interface, EN is the Enable signal and active high.<br/> This pin must keep NC for serial mode.</p>                                                                                                                                                                                                              |
| $\overline{\text{WR}}$<br>R/ $\overline{\text{W}}$ | I | <p><b>Write Control or Read-Write Control</b></p> <p>When use 8080 series interface, <math>\overline{\text{WR}}</math> is the write signal and active low.<br/> When use 6800 series interface, this pin is R/<math>\overline{\text{W}}</math>, active high for read cycle and active low for write cycle.<br/> This pin must keep NC for serial mode.</p>                                                                                                                              |
| D/ $\overline{\text{C}}$<br>RS                     | I | <p><b>Data/Command Select or Register Select)</b></p> <p>When use 8080 series interface, this is Data or Command signal. When D/<math>\overline{\text{C}}</math> is "0", means Register Cycle(or Command Cycle). When D/<math>\overline{\text{C}}</math> is "1", means Data Access Cycle(Data Cycle).<br/> When use 6800 series interface, this is the RS signal. When RS is "0", means Register Cycle and "1" means Data Access Cycle.<br/> This pin must keep NC for serial mode.</p> |
| $\overline{\text{CS}}$                             | I | <p><b>Chip Select</b></p> <p>This is a chip enable for RA8815.<br/> This pin must keep NC for serial mode.</p>                                                                                                                                                                                                                                                                                                                                                                          |
| $\overline{\text{INT}}$                            | O | <p><b>Interrupt Signal</b></p> <p>This is an interrupt output for MPU. Active low ◦</p>                                                                                                                                                                                                                                                                                                                                                                                                 |
| C86                                                | I | <p><b>MPU Select</b></p> <p>C86 = 0 → The MPU interface is 8080 series.<br/> C86 = 1 → The MPU interface is 6800 series(Default).<br/> This pin must keep NC for serial mode.</p>                                                                                                                                                                                                                                                                                                       |
| BIT4                                               | I | <p><b>Data Bit Select</b></p> <p>BIT4 = 0 → The parallel mode is use 8-bit data bus.<br/> BIT4 = 1 → The parallel mode is use 4-bit data bus(Default).<br/> This pin must keep NC for serial mode.</p>                                                                                                                                                                                                                                                                                  |
| P/ $\overline{\text{S}}$                           | I | <p><b>Parallel/Serial Select</b></p> <p>P/<math>\overline{\text{S}}</math> = 0 → The MPU interface is serial mode(Default). See the setting of DB[7:6].<br/> P/<math>\overline{\text{S}}</math> = 1 → The MPU interface is parallel mode.</p>                                                                                                                                                                                                                                           |

## 4-2 LCD Panel Interface

| Pin Name      | I/O | Description               |
|---------------|-----|---------------------------|
| SEG0 ~ SEG127 | O   | Segment Signals for Panel |
| COM0 ~ COM31  | O   | Common Signals for Panel  |

|                            |   |                               |
|----------------------------|---|-------------------------------|
| COMS_A[1:0]<br>COMS_B[1:0] | O | Icon Common Signals for Panel |
| DUM_L<br>DUM_R             | O | Dummy PAD                     |

### 4-3 Clock and Power

| Pin Name    | I/O | Description                                                                                                                                                                                                                                                        |
|-------------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RA, RB      | I   | <b>Resister Input</b><br>These are used to connect a resistor for internal oscillator.                                                                                                                                                                             |
| V0~V4       | O   | <b>Voltage Source of LCD Driver</b><br>The relationship of the power is $VLCD > VREG \geq V0 \geq V1 \geq V2 \geq V3 \geq V4 \geq VSS$ .                                                                                                                           |
| C1P, C1M    | I   | <b>Capacitor Input</b><br>These are used to connect a capacitor for internal Booster.                                                                                                                                                                              |
| C2P, C2M    | I   | <b>Capacitor Input</b><br>These are used to connect a capacitor for internal Booster.                                                                                                                                                                              |
| VLCD        | O   | <b>Booster Output</b>                                                                                                                                                                                                                                              |
| VREF        | I   | <b>Reference Voltage Input</b><br>This is the reference voltage input when use an external regulator.                                                                                                                                                              |
| VREG        | I   | <b>Voltage Regulator Output</b><br>When the internal voltage regulator is disable, this pin is connect to VLCD and used to generate V0~V4.                                                                                                                         |
| CLK_SEL     | I   | <b>Clock Select</b><br>This pin is used to select the clock source. When CLK_SEL "1", the clock is generated by internal oscillator and the external resistor that connect on RA and RB. When CLK_SEL is "0", the system clock is drive by external pin - EXT_CLK. |
| EXT_CLK     | I   | <b>External Clock</b><br>When CLK_SEL is "0", this pin is the external clock input. When CLK_SEL is "1", this pin do not used and has to connect VDD or GND.                                                                                                       |
| VDD<br>VDDP | P   | <b>VDD Power</b>                                                                                                                                                                                                                                                   |
| GND<br>GNDP | P   | <b>Ground</b>                                                                                                                                                                                                                                                      |

### 4-4 Misc.

| Pin Name                | I/O | Description                                                  |
|-------------------------|-----|--------------------------------------------------------------|
| KST[3..0]               | O   | <b>Key Strobe Output</b>                                     |
| KIN[4..0]               | I   | <b>Key Data Input</b><br>The unused pins keep floating(NC).  |
| IO[7..0]                | I/O | <b>General Purpose I/O</b>                                   |
| EL_CHRG                 | O   | <b>EL Charge Signal</b>                                      |
| EL_DCHG                 | O   | <b>EL Discharge Signal</b>                                   |
| $\overline{RST}$        | I   | <b>Reset</b>                                                 |
| TEST[2:0]<br>S[1:0], FG | I   | <b>Test Pins</b><br>These pins must keep NC for normal mode. |

Table 4-1: Pin Definition of Parallel/Serial Mode of MPU

| Pin Name                                          | I/O | Parallel Mode            |                          |                          |                          | Serial Mode            |                        |                        |
|---------------------------------------------------|-----|--------------------------|--------------------------|--------------------------|--------------------------|------------------------|------------------------|------------------------|
|                                                   |     | 8080                     |                          | 6800                     |                          | 3-Wire                 | 4-Wire<br>(A-Typ)      | 4-Wire<br>(B-Typ)      |
|                                                   |     | 8Bit                     | 4Bit                     | 8Bit                     | 4Bit                     |                        |                        |                        |
| DB7                                               | I/O | DB7                      | --                       | DB7                      | --                       | 0                      | 1                      | 1                      |
| DB6                                               | I/O | DB6                      | --                       | DB6                      | --                       | X                      | 0                      | 1                      |
| DB5                                               | I/O | DB5                      | --                       | DB5                      | --                       | --                     | --                     | --                     |
| DB4                                               | I/O | DB4                      | --                       | DB4                      | --                       | --                     | --                     | --                     |
| DB3                                               | I/O | DB3                      | DB3                      | DB3                      | DB3                      | $\overline{\text{CS}}$ | $\overline{\text{CS}}$ | $\overline{\text{CS}}$ |
| DB2                                               | I/O | DB2                      | DB2                      | DB2                      | DB2                      | --                     | RS                     | SDI                    |
| DB1                                               | I/O | DB1                      | DB1                      | DB1                      | DB1                      | SDA                    | SDA                    | SDO                    |
| DB0                                               | I/O | DB0                      | DB0                      | DB0                      | DB0                      | SCK                    | SCK                    | SCK                    |
| $\overline{\text{RD}}$ , EN                       | I   | $\overline{\text{RD}}$   | $\overline{\text{RD}}$   | EN                       | EN                       | --                     | --                     | --                     |
| $\overline{\text{WR}}$ , R/ $\overline{\text{W}}$ | I   | $\overline{\text{WR}}$   | $\overline{\text{WR}}$   | R/ $\overline{\text{W}}$ | R/ $\overline{\text{W}}$ | --                     | --                     | --                     |
| D/ $\overline{\text{C}}$ , RS                     | I   | D/ $\overline{\text{C}}$ | D/ $\overline{\text{C}}$ | RS                       | RS                       | --                     | --                     | --                     |
| $\overline{\text{CS}}$                            | I   | $\overline{\text{CS}}$   | $\overline{\text{CS}}$   | $\overline{\text{CS}}$   | $\overline{\text{CS}}$   | --                     | --                     | --                     |
| C86                                               | I   | 0                        | 0                        | 1                        | 1                        | --                     | --                     | --                     |
| BIT4                                              | I   | 0                        | 1                        | 0                        | 1                        | --                     | --                     | --                     |
| P/ $\overline{\text{S}}$                          | I   | 1                        | 1                        | 1                        | 1                        | 0                      | 0                      | 0                      |

"X" : 0 or 1(Do not care).

"--" : Not used, keep floating(NC).

## 5. Registers Description

### 5-1 Register Table

Table 5-1: Register Table

| ID | Name   | D7           | D6           | D5         | D4           | D3           | D2           | D1            | D0            | Description         |
|----|--------|--------------|--------------|------------|--------------|--------------|--------------|---------------|---------------|---------------------|
| 0  | DWFR   | B/C          | --           | NW5        | NW4          | NW3          | NW2          | NW1           | NW0           | Wave Form Select    |
| 1  | PWRR   | SRST         | MCLR         | --         | --           | KWK          | IOWK         | DOFF_Z        | SLP           | Power Control       |
| 2  | SYSR   | LS3          | LS2          | LS1        | LS0          | GB_EN        | --           | RS1           | RS0           | System Setting      |
| 3  | MWMR   | BMOD1        | BMOD0        | BIEN       | ASCS         | BOLD         | INV          | MD1           | MD0           | Memory Mode         |
| 4  | CURCR  | H3           | H2           | H1         | H0           | --           | BLK          | CR            | CUR_E<br>N    | Cursor Control      |
| 5  | X-CUR  | --           | --           | X5         | X4           | X3           | X2           | X1            | X0            | Cursor X Position   |
| 6  | Y-CUR  | --           | Y6           | Y5         | Y4           | Y3           | Y2           | Y1            | Y0            | Cursor Y Position   |
| 7  | KEYR   | KSB          | KDB1         | KDB0       | KSTB_S<br>EL | K_AUTO       | IRE          | KF1/<br>KSTB1 | KF0/<br>KSTB0 | Key-scan Control    |
|    | KSDR   | SIRQ         | KSTB1        | KSTB0      | KSD4         | KSD3         | KSD2         | KSD1          | KSD0          | Key-scan Data       |
|    |        | SIRQ         | AKD6         | AKD5       | AKD4         | AKD3         | AKD2         | AKD1          | AKD0          |                     |
| 8  | SWSXR  | --           | --           | --         | SSX4         | SSX3         | SSX2         | SSX1          | SSX0          | X-Scroll Start      |
| 9  | SWSYR  | --           | --           | SSY5       | SSY4         | SSY3         | SSY2         | SSY1          | SSY0          | Y-Scroll Start      |
| A  | SWRXR  | --           | --           | --         | SRX4         | SRX3         | SRX2         | SRX1          | SRX0          | X-Scroll Range      |
| B  | SWRYR  | --           | --           | SRY5       | SRY4         | SRY3         | SRY2         | SRY1          | SRY0          | Y-Scroll Range      |
| C  | SCOR   | SL7          | SL6          | SL5/SR5    | SL4/SR4      | SL3/SR3      | SL2/SR2      | SL1/SR1       | SL0/SR0       | Scroll Unit         |
| D  | ASCR   | SPD3         | SPD2         | SPD1       | SPD0         | STP3         | STP2         | STP1          | STP0          | Auto Scroll Control |
| E  | SCCR   | SCR_IM<br>D1 | SCR_IM<br>D0 | SCR_M<br>D | SBUF         | SCR_DI<br>R1 | SCR_DI<br>R0 | SCR_IN<br>TEN | AUTO_S<br>CR  | Scroll Control      |
| F  | ISR    | BF           | --           | --         | --           | --           | SCR_I        | KI            | BI            | Interrupt Status    |
| 10 | CSTR   | BR2          | BR1          | BR0        | CT4          | CT3          | CT2          | CT1           | CT0           | Contrast            |
| 11 | DRCR_A | BOFF         | EN_R         | EN_G       | ROFF         | --           | TMPS         | CDIR          | SDIR          | Driver Control      |
| 12 | DRCR_B | CK_BS1       | CK_BS0       | RR2        | RR1          | RR0          | HD2          | HD1           | HD0           | Driver Control      |
| 13 | BLTR   | BLK_EN       | PBK_EN       | --         | GINV         | BLT3         | BLT2         | BLT1          | BLT0          | Blink Setting       |
| 14 | IODR   | OE7          | OE6          | OE5        | OE4          | OE3          | OE2          | OE1           | OE0           | IO Port Direction   |
| 15 | IODAR  | IOD7         | IOD6         | IOD5       | IOD4         | IOD3         | IOD2         | IOD1          | IOD0          | IO Port Data        |
| 16 | ELCR   | EL_EN        | --           | --         | --           | ELT3         | ELT2         | ELT1          | ELT0          | EL Control          |
| 17 | CGMI   | --           | --           | --         | --           | --           | UMI2         | UMI1          | UMI0          | Create Font Select  |
| 18 | CGMD   | CGMD7        | CGMD6        | CGMD5      | CGMD4        | CGMD3        | CGMD2        | CGMD1         | CGMD0         | Create Font Data    |

### 5-2 Register Contents

The RA8815 accept two Command Cycle from MPU. One is Register Cycle(RS = 0) and the other is Memory Cycle(RS = 1). The MPU has to assign the register number of RA8815 that before access these registers. Therefore, the first byte that MPU pass to RA8815 will be store into Index Register. And RA8815 will assume the next byte is read from or write into the register which Index Register assigned.

**IR (Index Register)**

| RW | RS | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0  | 0   | 0   | 0   | ID4 | ID3 | ID2 | ID1 | ID0 |

**ID[4:0]:** These bits are used to store the register number that MPU want to access on next cycle.

The ID[[4:0] provide 32 register number(00h~1Fh). But currently the RA8815 only used 25 registers (00h~18h). All of these registers are be initially to "00h" after RESET.

**Memory Data (RAMD)**

| RW  | RS | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|-----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0/1 | 1  | D7  | D6  | D5  | D4  | D3  | D2  | D1  | D0  |

If RS is "1", It means MPU execute the Memory Cycle for RA8815. When RW is "0", MPU will write data to Display RAM or ICON RAM that according the setting of MD[1:0](REG[03h] bit1-0). For example, MPU write Big5/CG code to memory in Text Mode, or write bitmap data to display memory in Graphic mode. When RW is "1", the MPU read data from different paths of RA8815. It depend on the operation mode as following:

1. Full Size Text Mode: From up to down of Left side(16-Bytes), and then up to down of Right side(16-Bytes), total is 32-Bytes.
2. Half Size Text Mode: From up to down, total 16-Bytes data.
3. Small ASCII Text Mode: From up to down, total 8-Bytes data.
4. Graphics Mode: From left to right, each reading is one byte(8-Pixels).

**[00h] Driver Waveform Register (DWFR)**

| RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | B/C | --  | NW5 | NW4 | NW3 | NW2 | NW1 | NW0 |

**B/C:** Select waveform of drive. 0 → B-Type waveform. 1 → C-Type waveform.

**NW[5:0]:** These bits are used to assign the Segment/Row number that when internal Frame signals can to it and want to change the state. This function support only when B/C is "1" (C-Type wave form).

**[01h] Power Control Register (PWRR)**

| RW | DB7  | DB6  | DB5 | DB4 | DB3 | DB2  | DB1    | DB0 |
|----|------|------|-----|-----|-----|------|--------|-----|
| 0  | SRST | MCLR | --  | --  | KWK | IOWK | DOFF_Z | SLP |

**SRST:** S/W reset. 1 → All of the register will be initialed again except the display memory. 0 → No action.

**MCLR:** Clear memory. 1 → Clear the Display RAM data to "00h". 0 → No action. If both MCLR and SRST set to "1" then RA8815 will clear the display RAM and then Reset.

**KWK:** Key-scan wake up Setting. 0 → Key-scan Wake up function off. 1 → Key-scan wake up function on.

**IOWK:** I/O wake up Setting. 0 → IO port wake up function off. 1 → IO port wake up function on.

**DOFF\_Z:** Display off. 0 → LCD driver and display off. 1 → LCD driver and display on.

**SLP:** Sleep mode setting. 1 → Enter sleep mode, and turn off the clock. 0 → RA8815 wake up. This bit was clear to "0" when wake up from I/O port or Key-scan.

**[02h] System Register (SYSR)**

| RW | DB7 | DB6 | DB5 | DB4 | DB3   | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-------|-----|-----|-----|
| 0  | LS3 | LS2 | LS1 | LS0 | GB_EN | --  | RS1 | RS0 |

**LS[3:0]:** Setup the segment number. The maximum segment of RA8815 is 128.

| LS3 | LS2 | LS1 | LS0 | Line No. |
|-----|-----|-----|-----|----------|
| 0   | 0   | 0   | 0   | 16       |
| 0   | 0   | 0   | 1   | 32       |
| 0   | 0   | 1   | 0   | 48       |
| 0   | 0   | 1   | 1   | 64       |
| 0   | 1   | 0   | 0   | 80       |
| 0   | 1   | 0   | 1   | 96       |
| 0   | 1   | 1   | 0   | 112      |
| 0   | 1   | 1   | 1   | 128      |
| 1   | 0   | 0   | 0   | Reserved |
| :   |     |     |     | Reserved |
| 1   | 1   | 1   | 1   | Reserved |

**GB\_EN:** Setup the GB code or BIG5 code. 1 → GB Code. 0 → BIG5 Code.

**RS[1:0]:** Setup the common number. The maximum common of RA8815 is 32(Not including Icon).

| RS1 | RS0 | Row No.  |
|-----|-----|----------|
| 0   | 0   | 16       |
| 0   | 1   | 32       |
| 1   | 0   | Reserved |
| 1   | 1   | Reserved |

**[03h] Memory Write Mode Register (MWMR)**

| RW | DB7   | DB6   | DB5  | DB4  | DB3  | DB2 | DB1 | DB0 |
|----|-------|-------|------|------|------|-----|-----|-----|
| 0  | BMOD1 | BMOD0 | BIEN | ASCS | BOLD | INV | MD1 | MD0 |

**BMOD[1:0]:** Setup the range for memory written.

| BMOD1 | BMOD0 | Memory Range of Write         |
|-------|-------|-------------------------------|
| 0     | 0     | Normal Display Range          |
| 0     | 1     | Display Range + Scroll-Buffer |
| 1     | x     | Scroll-Buffer                 |

**BIEN:** Busy interrupt control. 1 → Busy interrupt enable (After write data to memory). 0 → Busy interrupt disable.

**ASCS:** Select ASCII Table. 0 → Select ASCII Table-1. 1 → Select ASCII Table-2. Refer Chapter 6-9.

**BOLD:** Select Bold Font to write Display RAM. 0 → Normal font. 1 → Bold font.

**INV:** Select reverse font to write Display RAM. 0 → Normal font. 1 → Reverse font.

**MD[1:0]:** Select operation mode for Display RAM.

| MD1 | MD0 | Operation Mode    |
|-----|-----|-------------------|
| 0   | 0   | Graphic Mode      |
| 0   | 1   | Small ASCII (8X8) |
| 1   | 0   | Big ASCII(8X16)   |

|   |   |                  |
|---|---|------------------|
| 1 | 1 | Full Size(16X16) |
|---|---|------------------|

When Full-Size mode(MD[1:0] = 11), if the first byte data is less than 80h, RA8815 will assume it's an ASCII code and show the Big ASCII font. But if want to show the Big ASCII font that code is large than 80h, then the operation mode has to change to Big ASCII mode(MD[1:0] = 10).

**[04h] Cursor Control Register (CURCR)**

| RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0    |
|----|-----|-----|-----|-----|-----|-----|-----|--------|
| 0  | H3  | H2  | H1  | H0  | --  | BLK | CR  | CUR_EN |

**H[3:0]: Setup the cursor height.**

| H3 | H2 | H1 | H0 | Height (Pixel) |
|----|----|----|----|----------------|
| 0  | 0  | 0  | 0  | 1              |
| 0  | 0  | 0  | 1  | 2              |
| 0  | 0  | 1  | 0  | 3              |
| 0  | 0  | 1  | 1  | 4              |
| 0  | 1  | 0  | 0  | 5              |
| 0  | 1  | 0  | 1  | 6              |
| 0  | 1  | 1  | 0  | 7              |
| 0  | 1  | 1  | 1  | 8              |
| 1  | 0  | 0  | 0  | 9              |
| 1  | 0  | 0  | 1  | 10             |
| 1  | 0  | 1  | 0  | 11             |
| 1  | 0  | 1  | 1  | 12             |
| 1  | 1  | 0  | 0  | 13             |
| 1  | 1  | 0  | 1  | 14             |
| 1  | 1  | 1  | 0  | 15             |
| 1  | 1  | 1  | 1  | 16             |

In Small ASCII mode(8X8), the H3 is reserved. The setting of cursor height is only form 1~8pixels(H[3:0] = x000b~x111b).

**BLK:** Cursor blink select. 0 → No Blinking. 1 → Cursor Blinking.

**CR:** Cursor return. 0 → No action. 1 → Cursor return. Cursor will return to the left of panel.

**CUR\_EN:** Cursor display select. 0 → Cursor hides. 1 → Cursor Display.

**[05h] Cursor Position Register of X (X-CUR)**

| RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | --  | --  | X5  | X4  | X3  | X2  | X1  | X0  |

**X[5:0]:** Setup the cursor position on segment. The unit is 8-pixels. Because maximum segment of RA8815 is 128-pixels, therefore the range of X[5:0] is 0~Fh. When the X[5:0] is 20h or 21h, then the cursor position is assign to horizontal Scroll-Buffer.

**[06h] Cursor Position Register of Y (Y-CUR)**

| RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | --  | Y6  | Y5  | Y4  | Y3  | Y2  | Y1  | Y0  |

**Y[6:0]:** Setup the cursor position on common. The unit is 1-pixels. Because maximum common of RA8815 is 32-pixels, therefore the range of Y[6:0] is 0~1Fh. When the Y[6:0] is 40h~4Fh, then the cursor position is assign to vertical Scroll-Buffer. When Y[6:0] is 50h then cursor is located at COMS(lcon).

**[07h] Key-scan Control Register (KEYR) (Write Only)**

| RW | DB7 | DB6  | DB5  | DB4      | DB3    | DB2 | DB1           | DB0           |
|----|-----|------|------|----------|--------|-----|---------------|---------------|
| 0  | KSB | KDB1 | KDB0 | KSTB_SEL | K_AUTO | IRE | KF1/<br>KSTB1 | KF0/<br>KSTB0 |

**KSB:** Key-scan control. 0 → Key-scan disable. 1 → Key-scan enable.

**KDB[1:0]:** Setup the de-bounce times of Key-scan in Auto-Mode. The one time means the time that Key-scan for one loop.

| KDB1 | KDB0 | Times |
|------|------|-------|
| 0    | 0    | 8     |
| 0    | 1    | 16    |
| 1    | 0    | 32    |
| 1    | 1    | 64    |

**KSTB\_SEL:** In non-Auto-mode, 0 → the DB[1:0] are defined as KF[1:0]. 1 → The DB[1:0] are defined as KSTB[1:0]. In Auto-Mode, the DB[1:0] is also defined as KF[1:0].

**K\_AUTO:** Setup the scan mode. 1 → Auto-Mode. The RA8815 will auto detect the key and store the code into AKD[6:0] for MPU reading. 0 → Non-Auto-Mode. The RA8815 will not store the code to AKD[6:0]. The MPU has to read data from KSTB[1:0] and KSD[4:0] to make sure which key was pressed. Of course, MPU could know if not only one key pressed at the same time In Non-Auto-Mode.

**IRE:** Setup the Interrupt of Key-scan. 0 → Hardware Interrupt disable while key was pressed. 1 → Generate hardware interrupt while key was pressed.

**KF[1:0]:** Setup the frequency of Key-scan.

| KF1 | KF0 | Pulse Width | Key-scan Cycle Time<br>(4x5) |
|-----|-----|-------------|------------------------------|
| 0   | 0   | 256us       | 1.024ms                      |
| 0   | 1   | 512us       | 2.048ms                      |
| 1   | 0   | 1.024ms     | 4.096ms                      |
| 1   | 1   | 2.048ms     | 9.182ms                      |

**KSTB[1:0]:** In Non-Auto-Mode, These two bits are used to setup the strobe for the Row of key matrix. If any key pressed, the MPU can read data from KSTB[1:0] and KSD[4:0] to make sure which key was pressed. The strobe data are also readable from Bit[6:5] of register KSDR.

**[07h] Key-scan Data Register (KSDR) (Read Only)**

If K\_AUTO = 0:

| RW | DB7  | DB6   | DB5   | DB4  | DB3  | DB2  | DB1  | DB0  |
|----|------|-------|-------|------|------|------|------|------|
| 1  | SIRQ | KSTB1 | KSTB0 | KSD4 | KSD3 | KSD2 | KSD1 | KSD0 |

**SIRQ:** Indicate the interrupt of Key-scan. This bit was clear when REG[0Fh] bit 1 write "0".

**KSTB[1:0]:** These two bit show which pin of KST[3:0] active.

**KSD[4:0]:** KIN Return Data. These bits are used in Non-Auto-Mode. The MPU can read data from KSTB[1:0] and KSD[4:0] to make sure which key was pressed.

If K\_AUTO = 1:

| RW | DB7  | DB6  | DB5  | DB4  | DB3  | DB2  | DB1  | DB0  |
|----|------|------|------|------|------|------|------|------|
| 1  | SIRQ | AKD6 | AKD5 | AKD4 | AKD3 | AKD2 | AKD1 | AKD0 |

**SIRQ:** Indicate the interrupt of Key-scan. This bit was clear when REG[0Fh] bit 1 write "0".

**AKD[6:0]:** Scan Data(Code). In Auto-Mode, the MPU read data from this register to know the status of key matrix. The RA8815 supports 4x5 key matrix -- total 20Keys. The BCD number of 0~19h are mapping to these keys.

| AKD[6:0] | Scan Data          |
|----------|--------------------|
| 0~19h    | Key No. Input      |
| 20~39h   | Long Key No. Input |
| 42       | Key Release        |
| Other    | Reserved           |

#### [08h] Scroll Window Start X Register (SWSXR)

| RW | DB7 | DB6 | DB5 | DB4  | DB3  | DB2  | DB1  | DB0  |
|----|-----|-----|-----|------|------|------|------|------|
| 0  | --  | --  | --  | SSX4 | SSX3 | SSX2 | SSX1 | SSX0 |

**SSX[4:0]:** When the shift direction is from right to left, then these bits are used to setup Segment (X) start point of scroll window. The unit is half size width(8-Pixels).

**Note:** When the shift direction is from left to right, these bits have to set 0.

#### [09h] Scroll Window Start Y Register (SWSYR)

| RW | DB7 | DB6 | DB5  | DB4  | DB3  | DB2  | DB1  | DB0  |
|----|-----|-----|------|------|------|------|------|------|
| 0  | --  | --  | SSY5 | SSY4 | SSY3 | SSY2 | SSY1 | SSY0 |

**SSY[5:0]:** Setup the Common (Y) start point of scroll window. The unit is pixel.

#### [0Ah] Scroll Window Rang X Register (SWRXR)

| RW | DB7 | DB6 | DB5 | DB4  | DB3  | DB2  | DB1  | DB0  |
|----|-----|-----|-----|------|------|------|------|------|
| 0  | --  | --  | --  | SRX4 | SRX3 | SRX2 | SRX1 | SRX0 |

**SRX[4:0]:** Setup Segment (X) offset of scroll window. The unit is half size width(8-Pixels).

Note:

1. SRX must large or equal than 1, that means the minimum scroll range of X is 16 pixels.
2. The "SSX+SRX" can not exceed the range of Segment (X) of LCD panel. For example, if the panel resolution is 96x32, then SSX+SRX must less than 96/8=12. That means the maximum of "SSX+SRX" is 11.

**[0Bh] Scroll Window Rang Y Register (SWRYR)**

| RW | DB7 | DB6 | DB5  | DB4  | DB3  | DB2  | DB1  | DB0  |
|----|-----|-----|------|------|------|------|------|------|
| 0  | --  | --  | SRY5 | SRY4 | SRY3 | SRY2 | SRY1 | SRY0 |

**SRY[5:0]:** Setup the Common (Y) offset of scroll window. The unit is pixel.

Note:

1. SRY must large or equal than 1, that means the minimum scroll range of Y is 2 pixels.
2. The "SSY+SRY" can not exceed the range of Common (Y) of LCD panel. For example, if the panel resolution is 96x32, then SSY+SRY must less than 32. That means the maximum of "SSY+SRY" is 31.

**[0Ch] Scroll Offset Register (SCOR)**

| RW | DB7 | DB6 | DB5     | DB4     | DB3     | DB2     | DB1     | DB0     |
|----|-----|-----|---------|---------|---------|---------|---------|---------|
| 0  | SL7 | SL6 | SL5/SR5 | SL4/SR4 | SL3/SR3 | SL2/SR2 | SL1/SR1 | SL0/SR0 |

**SL[7:0]:** Setup the shift unit of horizontal scroll. The unit is pixel and active when register SCR\_MD1 (REG[0Eh]bit 3) is clear to "0".

**SR[5:0]:** Setup the shift unit of vertical scroll. The unit is pixel and active when register SCR\_MD1 (REG[0Eh]bit 3) is set to "1".

In auto scroll mode, this register is also used to setup the start position of scroll of Common or Segment.

**[0Dh] Auto-Scroll Control Register (ASCR)**

| RW | DB7  | DB6  | DB5  | DB4  | DB3  | DB2  | DB1  | DB0  |
|----|------|------|------|------|------|------|------|------|
| 0  | SPD3 | SPD2 | SPD1 | SPD0 | STP3 | STP2 | STP1 | STP0 |

**SPD[3:0]:** Setup the speed of auto scroll.

| SPD3 | SPD2 | SPD1 | SPD0 | Scroll Time |
|------|------|------|------|-------------|
| 0    | 0    | 0    | 0    | 1 Unit      |
| 0    | 0    | 0    | 1    | 3 Units     |
| 0    | 0    | 1    | 0    | 5 Units     |
| 0    | 0    | 1    | 1    | 7 Units     |
| 0    | 1    | 0    | 0    | 17 Units    |
| 0    | 1    | 0    | 1    | 19 Units    |
| 0    | 1    | 1    | 0    | 21 Units    |
| 0    | 1    | 1    | 1    | 23 Units    |
| 1    | 0    | 0    | 0    | 129 Units   |
| 1    | 0    | 0    | 1    | 131 Units   |
| 1    | 0    | 1    | 0    | 133 Units   |
| 1    | 0    | 1    | 1    | 135 Units   |
| 1    | 1    | 0    | 0    | 145 Units   |
| 1    | 1    | 0    | 1    | 147 Units   |
| 1    | 1    | 1    | 0    | 149 Units   |
| 1    | 1    | 1    | 1    | 151 Units   |

1 Unit = 1 Frame Times

**STP[3:0]:** Setup the shift unit on auto scroll mode.

| STP3 | STP2 | STP1 | STP0 | Shift Pixel |
|------|------|------|------|-------------|
| 0    | 0    | 0    | 0    | 1           |
| 0    | 0    | 0    | 1    | 2           |
| 0    | 0    | 1    | 0    | 3           |
| 0    | 0    | 1    | 1    | 4           |
| 0    | 1    | 0    | 0    | 5           |
| 0    | 1    | 0    | 1    | 6           |
| 0    | 1    | 1    | 0    | 7           |
| 0    | 1    | 1    | 1    | 8           |
| 1    | 0    | 0    | 0    | 9           |
| 1    | 0    | 0    | 1    | 10          |
| 1    | 0    | 1    | 0    | 11          |
| 1    | 0    | 1    | 1    | 12          |
| 1    | 1    | 0    | 0    | 13          |
| 1    | 1    | 0    | 1    | 14          |
| 1    | 1    | 1    | 0    | 15          |
| 1    | 1    | 1    | 1    | 16          |

**[0Eh] Scroll Control Register (SCCR)**

| RW | DB7          | DB6          | DB5    | DB4  | DB3          | DB2          | DB1           | DB0          |
|----|--------------|--------------|--------|------|--------------|--------------|---------------|--------------|
| 0  | SCR_IM<br>D1 | SCR_IM<br>D0 | SCR_MD | SBUF | SCR_DI<br>R1 | SCR_DI<br>R0 | SCR_INT<br>EN | AUTO_S<br>CR |

**SCR\_IMD[1:0]:** The definition is as following and they are available at Auto-Scroll-Mode.

0X: Setup 1-pixel shift to caused interrupt(SCR\_INTEN must be 1).

10: Setup 8-pixel shift to caused interrupt(SCR\_INTEN must be 1)

11: Setup 16-pixel shift to caused interrupt(SCR\_INTEN must be 1)

**SCR\_MD:** Scroll Mode Select. 0 → Non-Auto-Scroll, the scroll offset clear to "0". 1 → Auto-Scroll Mode.

**SBUF:** Scroll-Buffer Control. 0 → Scroll-Buffer disable. The scroll will not including the Scroll-Buffer, only for display area. 1 → Scroll-Buffer enable. The scroll area is including the display and Scroll-Buffer.

**SCR\_DIR[1:0]:** Select the direction of scroll.

| SCR_DIR1 | SCR_DIR0 | Direction of Scroll       |
|----------|----------|---------------------------|
| 0        | 0        | Left to Right(Horizontal) |
| 0        | 1        | Right to Left(Horizontal) |
| 1        | 0        | Up to Down(Vertical)      |
| 1        | 1        | Down to Up(Vertical)      |

**SCR\_INTEN:** Setup the scroll interrupt. 0 → Scroll interrupt disable. 1 → In auto scroll mode, when scroll 1, 8 or 16-pixels generate an interrupt to MPU.

**AUTO\_SCR:** Auto-Scroll control. 0 → Stop the Auto-Scroll. If want to close the Auto-Scroll mode or display new data on the screen, then the Bit5 - SCR\_MD must clear to 0 first. 1 → Auto-Scroll going.

**[0Fh] Interrupt Status Register (ISR)**

| RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2   | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-------|-----|-----|
| 1  | BF  | --  | --  | --  | --  | SCR_I | KI  | BI  |

**BF:** Busy Flag. 1 → Display RAM is in busy(Data Write). 0 → Display RAM is idle(Write complete).

**SCR\_I:** Scroll interrupt. 1 → Interrupt for scroll complete. 0 → No scroll Interrupt.

**KI:** Key-scan interrupt. 1 → Interrupt for key pressed. 0 → No Key pressed Interrupt.

**BI:** Busy Interrupt. 1 → Interrupt for the activity of writing data to display RAM completed. 0 → No busy Interrupt

**[10h] Contrast Adjust Register (CSTR)**

| RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | BR2 | BR1 | BR0 | CT4 | CT3 | CT2 | CT1 | CT0 |

**BR[2:0]:** Setup the LCD Bias(Base on 128x33).

| BR2 | BR1 | BR0 | Bias  |
|-----|-----|-----|-------|
| 0   | 0   | 0   | 1/4   |
| 0   | 0   | 1   | 1/4.5 |
| 0   | 1   | 0   | 1/5   |
| 0   | 1   | 1   | 1/5.5 |
| 1   | 0   | 0   | 1/6   |
| 1   | 0   | 1   | 1/6.5 |
| 1   | 1   | X   | 1/7   |

**CT[4:0]:** Setup the Contrast(32 Level). Normally depend on the liquid, power and panel size to adjust the best display quality.

| CT4 | CT3 | CT2 | CT1 | CT0 | Contrast     |
|-----|-----|-----|-----|-----|--------------|
| 0   | 0   | 0   | 0   | 0   | Light        |
| 0   | 0   | 0   | 0   | 1   | <div>↓</div> |
| ⋮   |     |     |     |     |              |
| ⋮   |     |     |     |     |              |
| 1   | 1   | 1   | 1   | 1   | Dark         |

**[11h] Driver Control Register1 (DRCR\_A)**

| RW | DB7  | DB6  | DB5  | DB4  | DB3 | DB2 | DB1  | DB0  |
|----|------|------|------|------|-----|-----|------|------|
| 0  | BOFF | EN_R | EN_G | ROFF | --  | --  | CDIR | SDIR |

**BOFF:** Booster control. 1 → Internal Booster enable. 0 → Internal Booster disabled and used external voltage.

**EN\_R:** Reference voltage control. 1 → Internal reference voltage enable for Regulator. 0 → Disable the internal reference voltage. The Regulator use external reference voltage.

**EN\_G:** VREG control. 1 → The VREG is generated by internal Regulator. 0 → Use external VREG, and the EN\_R and BOFF have to clear "0"(Off) to reduce power consumption.

**ROFF:** Voltage Follower control. 1 → Internal Voltage Follower enable for LCD Bias voltage. 0 → Disable

internal Voltage Follower, and use external voltage to generate LCD Bias voltage. If use external Voltage Follower, then EN\_G, EN\_R and BOFF have to clear "0"(Off) to reduce power consumption.

**CDIR:** Common sequency select. 0 → Pins COM0~31 are mapping to Common 0~31. 1 → Pins COM0~31 are mapping to Common 31~0.

**SDIR:** Segment sequency select. 0 → Pins SEG0~127 are mapping to Segment 0~127. 1 → Pins SEG0~127 are mapping to Segment 127~0.

**[12h] Driver Control Register (DRCR\_B)**

| RW | DB7    | DB6    | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|--------|--------|-----|-----|-----|-----|-----|-----|
| 0  | CK_BS1 | CK_BS0 | RR2 | RR1 | RR0 | HD2 | HD1 | HD0 |

**CK\_BS[1:0]:** Select the clock of Booster. Assume the RC oscillator clock is 45KHz.

| CK_BS1 | CK_BS0 | Clock of Booster     |
|--------|--------|----------------------|
| 0      | 0      | SYS_CLK/2 → 22.5KHz  |
| 0      | 1      | SYS_CLK/4 → 11.25KHz |
| 1      | 0      | SYS_CLK/6 → 7.5KHz   |
| 1      | 1      | SYS_CLK/8 → 5.625KHz |

**RR[2:0]:** Setup the Resistor Ratio of Regulator. The ratio is  $V_{REF} : V_{REG}$ .

| RR2 | RR1 | RR0 | Resistor Ratio |
|-----|-----|-----|----------------|
| 0   | 0   | 0   | X2             |
| 0   | 0   | 1   | X2.5           |
| 0   | 1   | 0   | X3             |
| 0   | 1   | 1   | X3.5           |
| 1   | 0   | 0   | X4             |
| 1   | 0   | 1   | X4.5           |
| 1   | 1   | 0   | X5             |
| 1   | 1   | 1   | --             |

Note: The VREF is 1.6V.

**HD[2:0]:** Setup the LCD driving current. Normally big panel use bigger driving current to void bad display quality.

| HD2 | HD1 | HD0 | Driving Current                                              |
|-----|-----|-----|--------------------------------------------------------------|
| 0   | 0   | 0   | <div style="text-align: center;"> Min<br/> ↓<br/> Max </div> |
| 0   | 0   | 1   |                                                              |
| 0   | 1   | 0   |                                                              |
| 0   | 1   | 1   |                                                              |
| 1   | 0   | 0   |                                                              |
| 1   | 0   | 1   |                                                              |
| 1   | 1   | 0   |                                                              |
| 1   | 1   | 1   |                                                              |

**[13h] Blink Timer Register (BLTR)**

| RW | DB7    | DB6    | DB5 | DB4  | DB3  | DB2  | DB1  | DB0  |
|----|--------|--------|-----|------|------|------|------|------|
| 0  | BLK_EN | PBK_EN | --  | GINV | BLT3 | BLT2 | BLT1 | BLT0 |

**BLK\_EN:** Blinking. 0 → Blinking off. 1 → Blinking on.

**PBK\_EN:** Whole or Partial Blinking selection. 0 → Whole screen Blinking. 1 → Partial screen Blinking. The blinking area is depending on the scroll window. That means the partial area is setting by register SWSXR, SWSYR, SWRXR and SWRYR. When the Partial Blinking off, the above four registers had better clear to 0. Note, only BLK\_EN set to "1" when blink is active.

**GINV:** Setup display reverse. 0 → Normal display. 1 → Display reverse.

**BLT[3:0]:** Setup blinking time.

| BLT3 | BLT2 | BLT1 | BLT0 | Blink Time<br>(Unit: Frames) |
|------|------|------|------|------------------------------|
| 0    | 0    | 0    | 0    | 8                            |
| 0    | 0    | 0    | 1    | 16                           |
| 0    | 0    | 1    | 0    | 24                           |
| 0    | 0    | 1    | 1    | 32                           |
| 0    | 1    | 0    | 0    | 40                           |
| 0    | 1    | 0    | 1    | 48                           |
| 0    | 1    | 1    | 0    | 56                           |
| 0    | 1    | 1    | 1    | 64                           |
| 1    | 0    | 0    | 0    | 72                           |
| 1    | 0    | 0    | 1    | 80                           |
| 1    | 0    | 1    | 0    | 88                           |
| 1    | 0    | 1    | 1    | 96                           |
| 1    | 1    | 0    | 0    | 104                          |
| 1    | 1    | 0    | 1    | 112                          |
| 1    | 1    | 1    | 0    | 120                          |
| 1    | 1    | 1    | 1    | 128                          |

**[14h] IO Direction Control Register (IODR)**

| RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | OE7 | OE6 | OE5 | OE4 | OE3 | OE2 | OE1 | OE0 |

**OE[7:0]:** Select the I/O port direction. 0 → Input. 1 → Output.

**[15h] IO Data Register (IODAR)**

| RW | DB7  | DB6  | DB5  | DB4  | DB3  | DB2  | DB1  | DB0  |
|----|------|------|------|------|------|------|------|------|
| 0  | IOD7 | IOD6 | IOD5 | IOD4 | IOD3 | IOD2 | IOD1 | IOD0 |

**IO[7:0]:** This register stores the input data of I/O port when I/O port is input mode.

**[16h] EL Control Register (ELCR)**

| RW | DB7   | DB6 | DB5 | DB4 | DB3  | DB2  | DB1  | DB0  |
|----|-------|-----|-----|-----|------|------|------|------|
| 0  | EL_EN | --  | --  | --  | ELT3 | ELT2 | ELT1 | ELT0 |

**EL\_EN:** EL signals output . 0 → Off. 1 → On.

**ELT[3:0]:** Setup the output time of EL signals. The following table is base on the RC oscillator fix at 45KHz.  
The output time is longer when RC oscillator clock is slower.

| ELT3 | ELT2 | ELT1 | ELT0 | Output Time(Sec) |
|------|------|------|------|------------------|
| 0    | 0    | 0    | 0    | 1                |
| 0    | 0    | 0    | 1    | 2                |
| 0    | 0    | 1    | 0    | 4                |
| 0    | 0    | 1    | 1    | 6                |
| 0    | 1    | 0    | 0    | 8                |
| 0    | 1    | 0    | 1    | 10               |
| 0    | 1    | 1    | 0    | 12               |
| 0    | 1    | 1    | 1    | 14               |
| 1    | 0    | 0    | 0    | 16               |
| 1    | 0    | 0    | 1    | 18               |
| 1    | 0    | 1    | 0    | 20               |
| 1    | 0    | 1    | 1    | 22               |
| 1    | 1    | 0    | 0    | 24               |
| 1    | 1    | 0    | 1    | 26               |
| 1    | 1    | 1    | 0    | 28               |
| 1    | 1    | 1    | 1    | 30               |

**[17h] CGRAM Register (CGMI)**

| RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2  | DB1  | DB0  |
|----|-----|-----|-----|-----|-----|------|------|------|
| 0  | --  | --  | --  | --  | --  | UMI2 | UMI1 | UMI0 |

**UMI[2:0]:** Select the create font number. The RA8815 allow user create eight 16x16 full size font. The mapping font code is FFF0h~FFF7h.

| UMI2 | UMI1 | UMI0 | Font Code |
|------|------|------|-----------|
| 0    | 0    | 0    | FFF0h     |
| 0    | 0    | 1    | FFF1h     |
| 0    | 1    | 0    | FFF2h     |
| 0    | 1    | 1    | FFF3h     |
| 1    | 0    | 0    | FFF4h     |
| 1    | 0    | 1    | FFF5h     |
| 1    | 1    | 0    | FFF6h     |
| 1    | 1    | 1    | FFF7h     |

**[18h] CGRAM Data Register (CGMD)**

| RW | DB7   | DB6   | DB5   | DB4   | DB3   | DB2   | DB1   | DB0   |
|----|-------|-------|-------|-------|-------|-------|-------|-------|
| 0  | CGMD7 | CGMD6 | CGMD5 | CGMD4 | CGMD3 | CGMD2 | CGMD1 | CGMD0 |

**CGMD[7:0]:** This register is used to transfer or read the data of 16x16 full size font. The MPU write

continuous 32-bytes data of bit-map of 16x16 full size font into this register that after program the REG[17h]. If user want to show the self-create font, just write the two bytes font code to RA8815.

## 6. Function Description

### 6-1 MPU Interface

#### 6-1-1 Parallel Interface

The MPU interface of RA8815 supports both 8080 and 6800 series with in 4-Bit or 8-bit bus width. If the “C86” connects to GND, then the MPU is defined as 8080 type interface. If pin “C86” connects to VDD, then it’s defined as 6800 type interface. Refer to the Figure 6-2.

If the pin “BIT4” connects to GND, then the bus width of MPU interface is 8-Bit. If the pin “BIT4” connects to VDD, then the bus width is 4-Bit. And only the DB[3:0] of data bus are available.

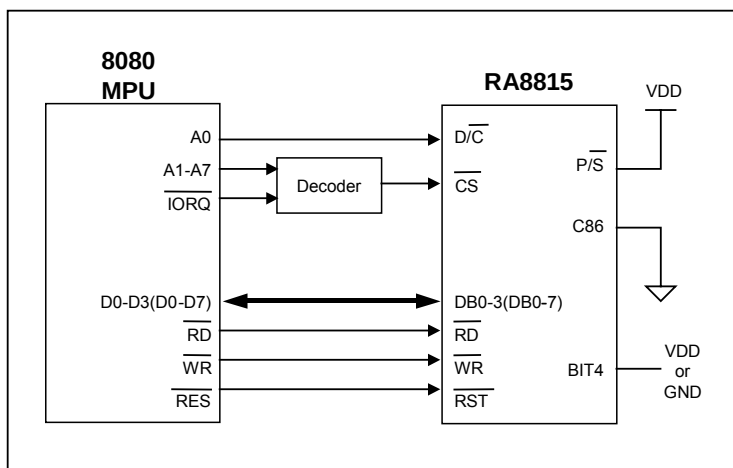


Figure 6-1: 8080 (4/8-Bit) MPU Interface

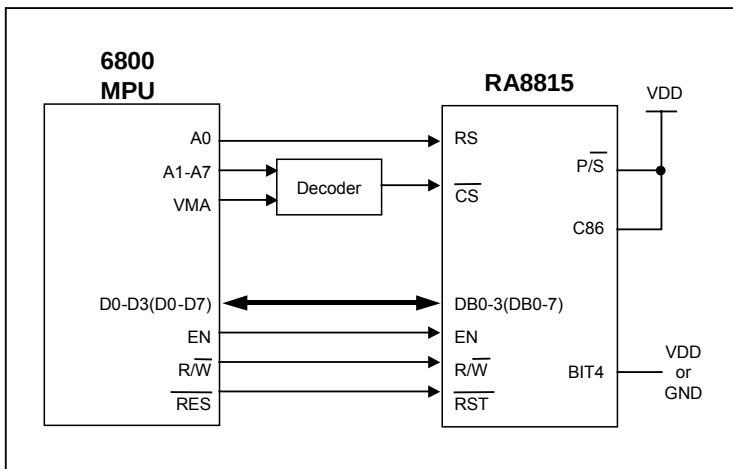


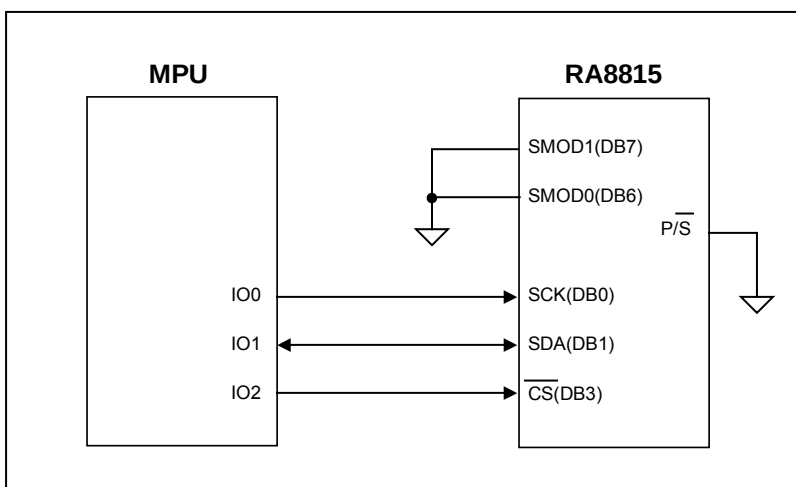
Figure 6-2: 6800 (4/8-Bit) MPU Interface

### 6-1-2 Serial Interface

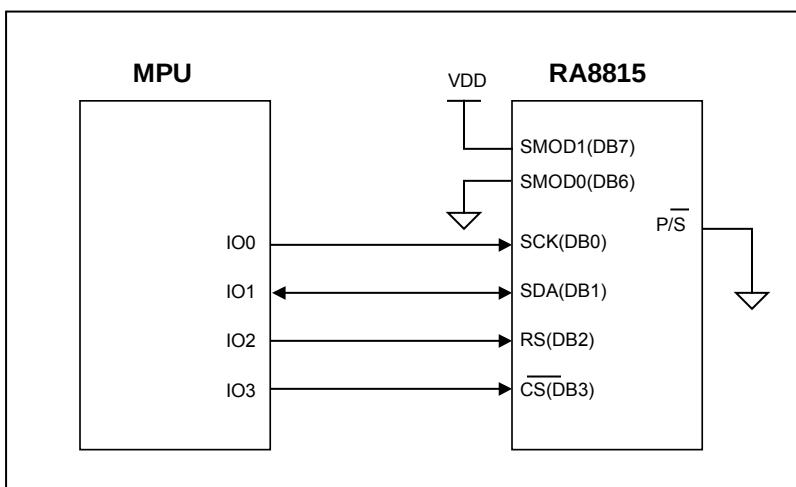
The RA8815 also support three type serial interface. One is 3-Wires and the others are 4-Wires(A-Type, B-Type). This feature is control by the pin "P/ $\overline{S}$ " and DB[7:6]. Refer to Table 4-1. In serial mode the DB[7:6] are used as SMOD[1:0] to select the different serial mode. Please also refer to Table 6-1. The Figure 6-3 to 6-5 are the interface diagram of MPU and RA8815 which in serial mode.

**Table 6-1**

| SMOD | Serial Mode Interface                                             |
|------|-------------------------------------------------------------------|
| 0 X  | 3-Wires. Use signals SCK, SDA and $\overline{CS}$ .               |
| 1 0  | 4-Wires (A-Type). Use signals SCK, SDA, RS and $\overline{CS}$ .  |
| 1 1  | 4-Wires (B-Type). Use signals SCK, SDO, SDI and $\overline{CS}$ . |



**Figure 6-3: 3-Wires MPU interface**



**Figure 6-4: 4-Wires(A-Type) MPU interface**

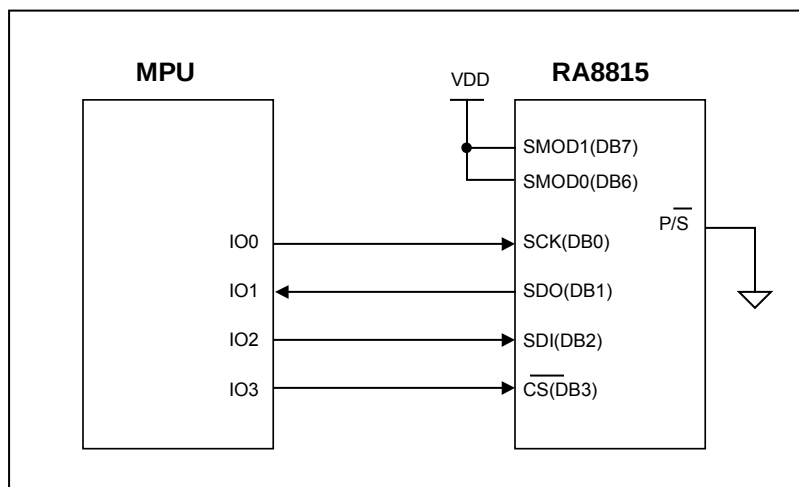


Figure 6-5: 4-Wires(B-Type) MPU interface

### 6-1-3 Register Read/Write

The RA8815 accepts two access cycles from MPU. One is read data from register or write data to register. Another is read data from memory or write data to memory. As description of Chapter 5-2, MPU must tell the RA8815 that which register will be access. Therefore the first data that write to RA8815 is to select the register number. And the second data is the exact data that writing into or reading from this register.

Because the features of RA8815 are controlled by the contents of internal registers, so if we write data to register is like to give a command to RA8815. Therefore we can say that the Register Access Cycle is same as Command Cycle.

The Figure 6-6 and 6-7 show the register access timing of 8080 MPU(8-Bit) with RA8815. Figure 6-8 and 6-9 show the register access timing of 6800MPU(8-Bit) interface. Figure 6-10 to 6-12 show the register access timing of serial interface.

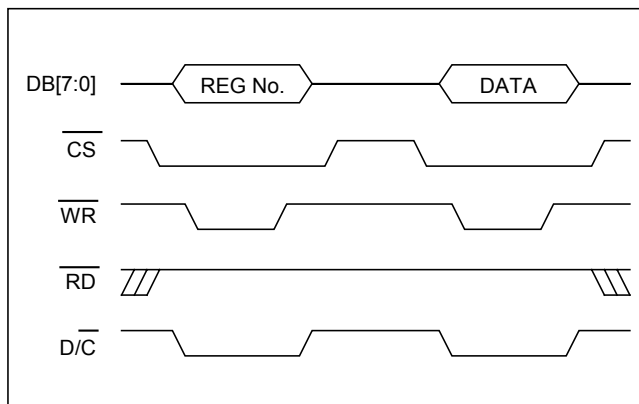


Figure 6-6: Register Wrie on 8080(8-Bit) I/F

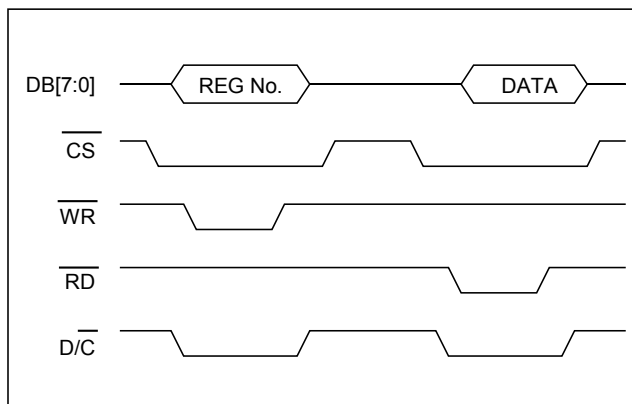


Figure 6-7: Register Read on 8080(8-Bit) I/F

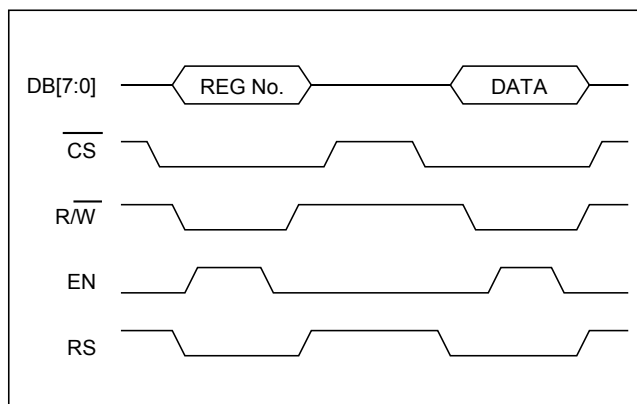


Figure 6-8: Register Write on 6800(8-Bit) I/F

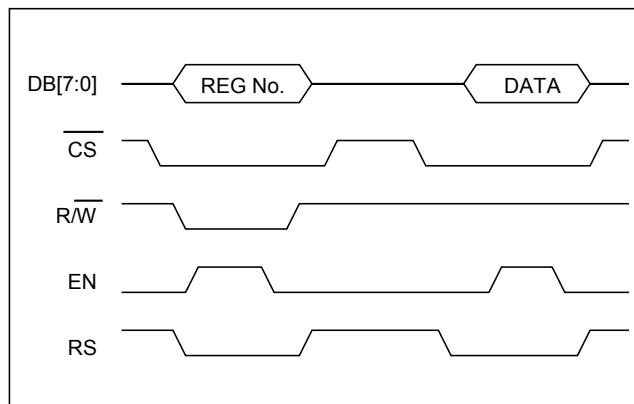


Figure 6-9: Register Read on 6800(8-Bit) I/F

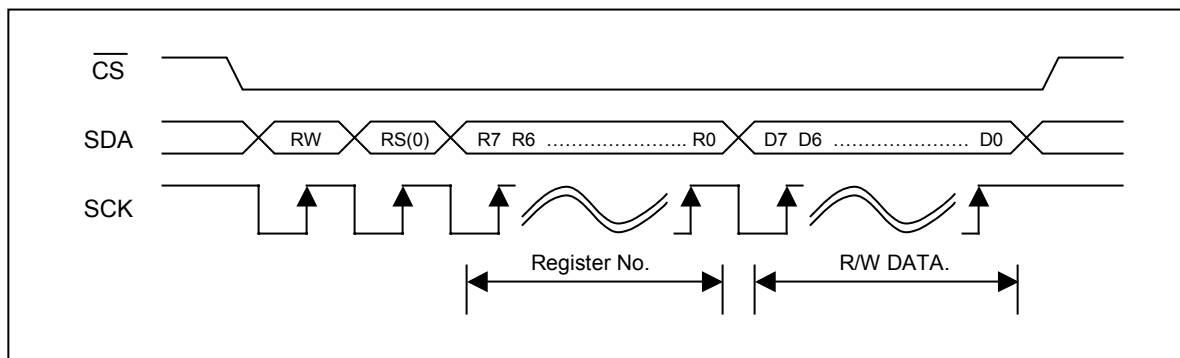


Figure 6-10: Register Read/Write Access on 3-Wires I/F

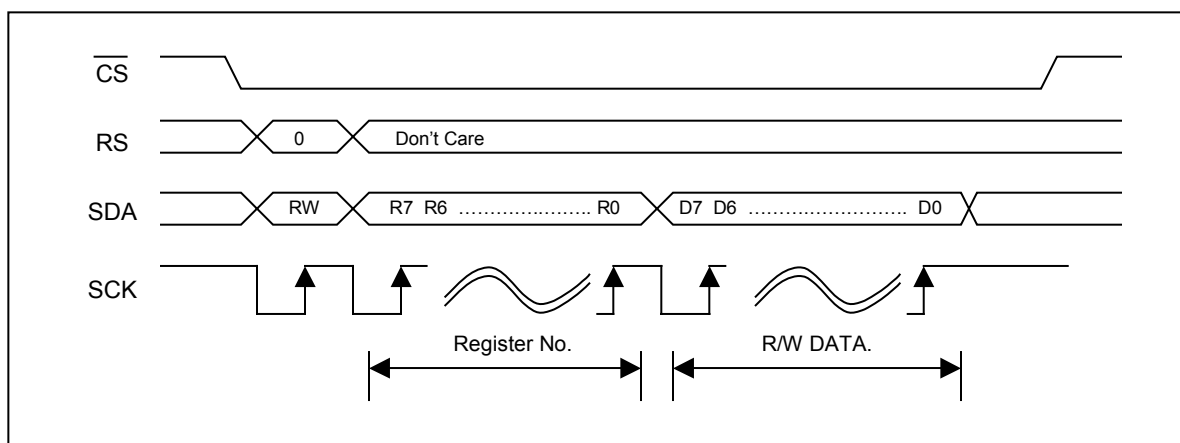
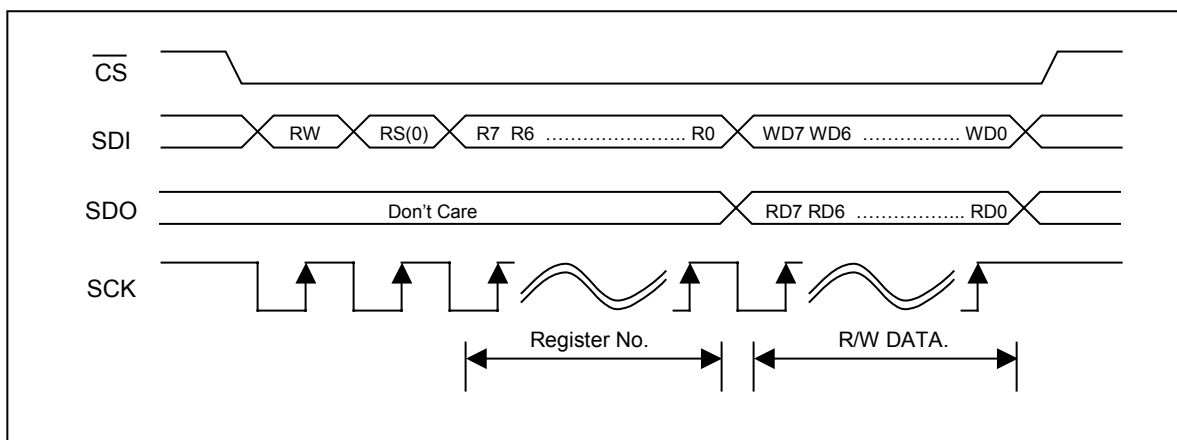


Figure 6-11: Register Read/Write Access on 4-Wires(A-Type) I/F

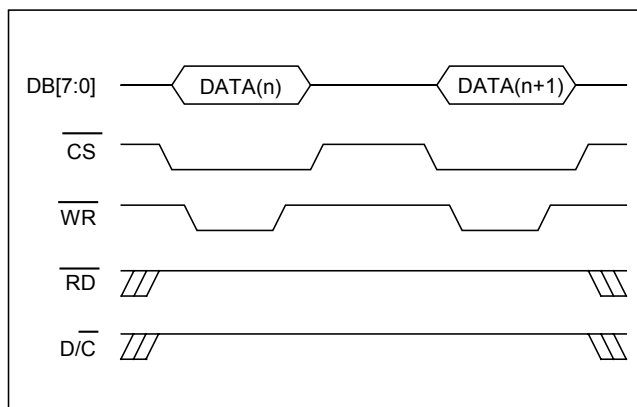


**Figure 6-12: Register Read/Write Access on 4-Wires(B-Type) I/F**

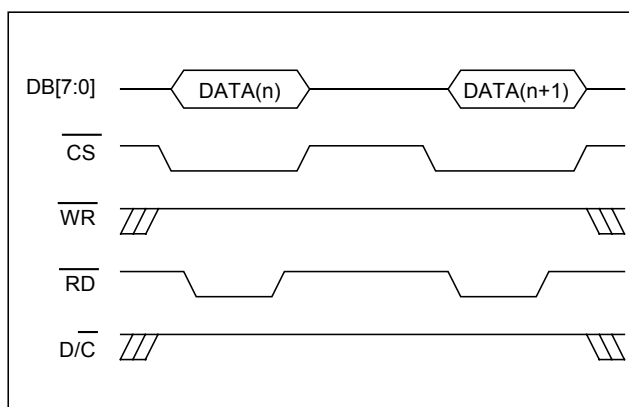
#### 6-1-4 Memory Read/Write

Another cycle for MPU to RA8815 is memory Read/Write cycle. Normally it used to show information on the LCD screen. A memory writes means write a data into the mapping address that cursor located. After a memory write complete, the cursor will auto increase. And the data of next memory write will fill into the new memory address that new cursor position located. Because all of the memory read/write cycles are transfer the display data, so we can abbreviate the name of Memory Access Cycle to Data Cycle.

The Figure 6-13 and 6-14 show the memory access timing of 8080 MPU(8-Bit) with RA8815. Figure 6-15 and 6-16 show the memory access timing of 6800MPU(8-Bit) interface. Figure 6-17 to 6-19 show the memory access timing of serial interface.



**Figure 6-13: Memory Write on 8080(8-Bit) I/F**



**Figure 6-14: Memory Read on 8080(8-Bit) I/F**

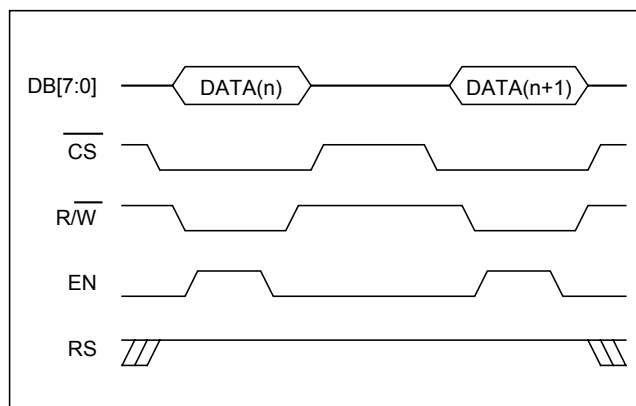


Figure 6-15: Memory Write on 6800(8-Bit) I/F

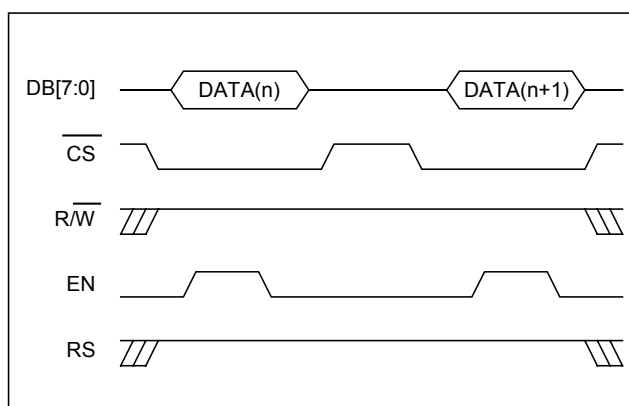


Figure 6-16: Memory Read on 6800(8-Bit) I/F

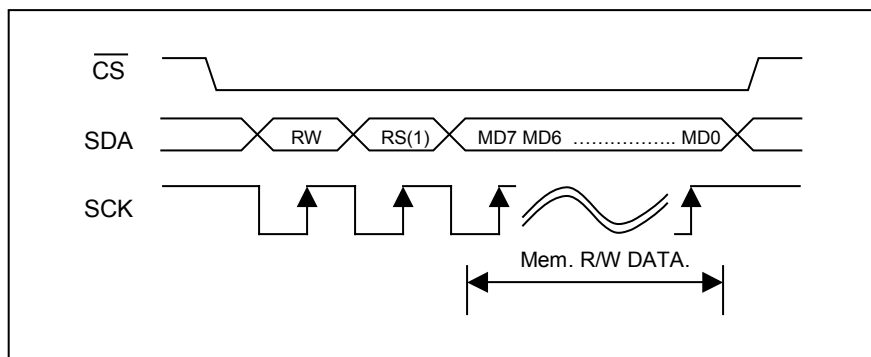


Figure 6-17: Memory Read/Write Access on 3-Wires I/F

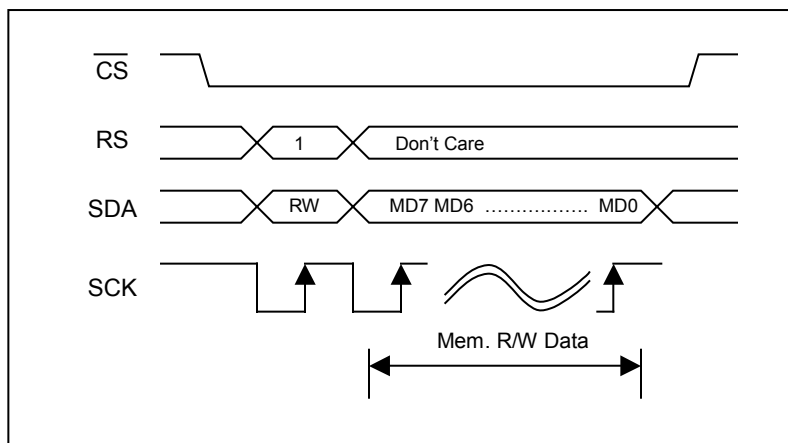
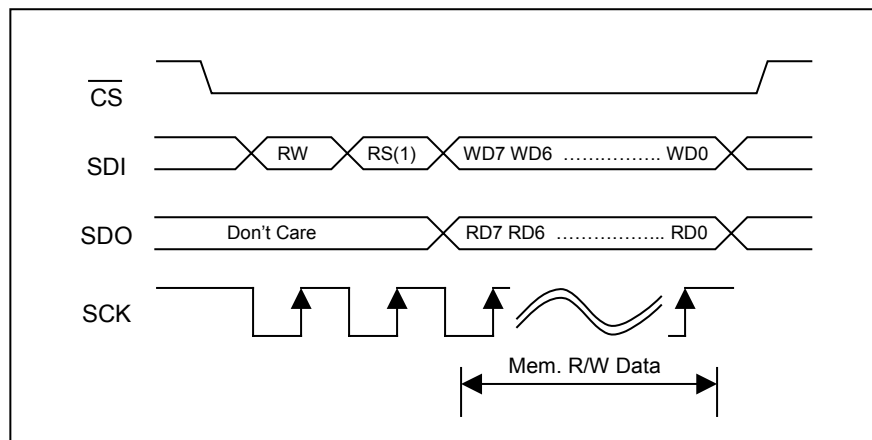


Figure 6-18: Memory Read/Write Access on 4-Wires(A-Type) I/F



**Figure 6-19: Memory Read/Write Access on 4-Wires(B-Type) I/F**

## 6-2 Memory

The RA8815 built-in three memory:

1. 256Kbyte Font ROM
2. 528Byte Display RAM
3. Character Generator RAM(CGRAM)

The 256Kbyte Font ROM stores bit map data of Chinese font. It also including English, Japanese, European, Latin(Latin-ext A, Latin-ext B) and ASCII. In text mode, RA8815 will read the bit map data from Font ROM and pass to display RAM that when RA8815 received the standard code from MPU. The LCD control circuit will read data of display RAM continuous and send to driver circuit. So the text will show on the LCD screen. Therefore, the MPU will save a lot of time to calculate the position of cursor and read map bit map data from font ROM then write to display RAM. The MPU will promote the display efficiency to handle Chinese text display. And it will reduce the system develop time.

The display range of RA8815 is 128x33 dots. So it needs 528Byte(128\*33/8) display RAM. In addition, RA8815 also built-in a scroll buffer to provide the scrolling and shifting functions.

The Character Generator RAM(CGRAM) is used for user to create special fonts. There are eight space of full size font to reserved for user. Their codes are fixed from FFF0h to FFF7h. The MPU could write the mapping code to RA8815 and show the bit map font on screen that after the user font(writing 32 byte to CGRAM) was created.

## 6-3 System Clock

The clock of RA8815 is generated by the internal circuit and resistor that between pin RA and RB. Normally the resistor is value is 270Kohm and the clock frequency is around 55KHz. When the bit0(SLP) of register PWRR set to "1", then the clock will be stop.

When the input pin "CLK\_SEL" set to "0", then system clock can also input from external clock through pin "EXT\_CLK".

## 6-4 LCD Driver and Power Circuit

The driver circuit of RA8815 is a low power design. The power supply circuit is consist of Booster, Voltage Regulator and Voltage Follower. For different requirement of power, the Driver Control Register(REG[11h]) is used to enable or disaable for related circuit.

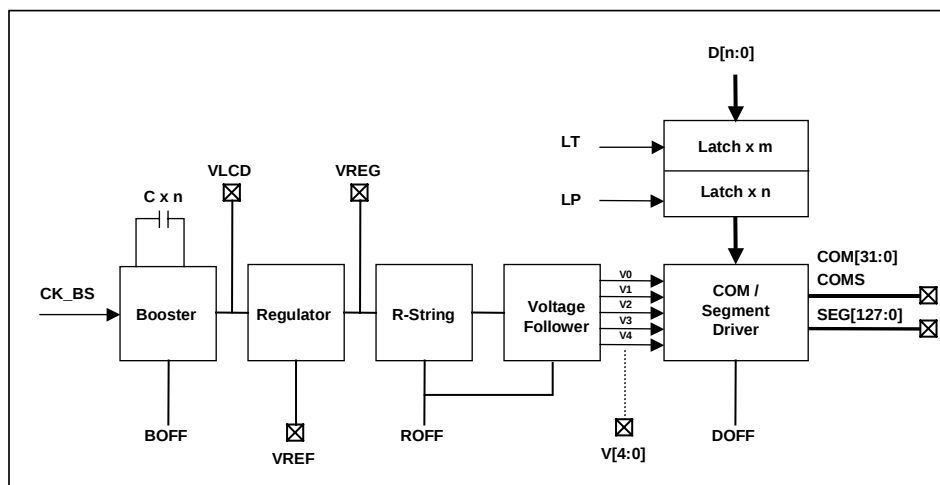


Figure 6-20: LCD Driver and Power Supply Circuit Block

The user could use the setting of register REG[11h] to select the internal or external power. Please refer to the following of Table 6-2 and Table 6-3.

Table 6-2: Power Circuit Setup

| Driver Control Register (DRCR_A) | Functions                             | State '1' '0' |
|----------------------------------|---------------------------------------|---------------|
| Bit7                             | Booster Circuit Control Bit           | ON OFF        |
| Bit6                             | Reference Voltage Circuit Control Bit | ON OFF        |
| Bit5                             | Voltage Regulator Circuit Control Bit | ON OFF        |
| Bit4                             | Voltage Follower Circuit Control Bit  | ON OFF        |

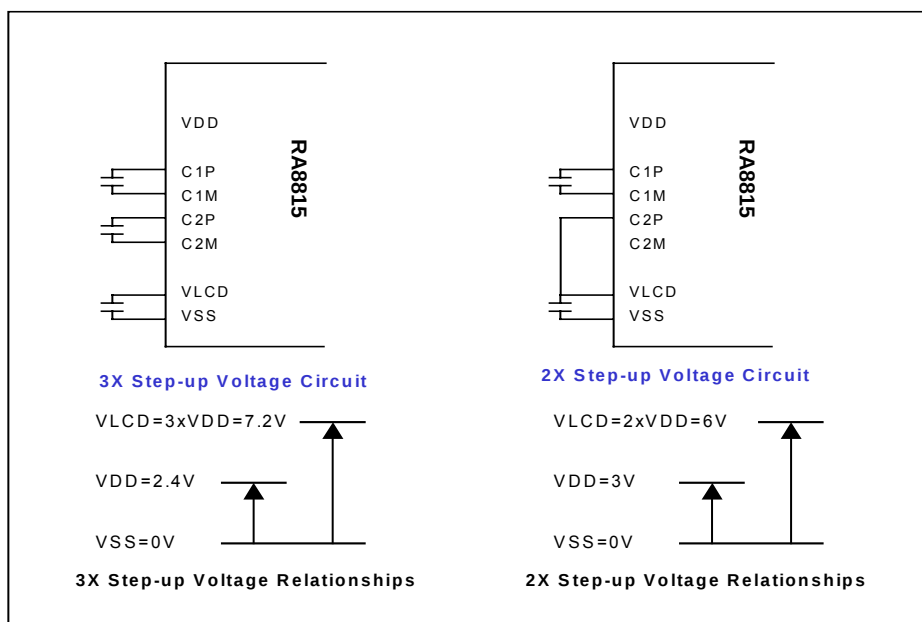
Table 6-3: Setting Table of Power Circuit

| Driver Control Register (DRCR_A)<br>D7 D6 D5 D4 | Booster | Voltage Regulator | Reference Voltage(VREF) of Voltage Regulator | Voltage Follower | External Power  |
|-------------------------------------------------|---------|-------------------|----------------------------------------------|------------------|-----------------|
| 1 1 1 1                                         | ON      | ON                | Internal                                     | ON               | VDD             |
| 0 1 1 1                                         | OFF     | ON                | Internal                                     | ON               | VLCD, VDD       |
| 1 0 1 1                                         | ON      | ON                | External                                     | ON               | VREF, VDD       |
| 0 0 1 1                                         | OFF     | ON                | External                                     | ON               | VLCD, VREF, VDD |
| 0 0 0 1                                         | OFF     | OFF               | Don't Need                                   | ON               | VREG, VDD       |
| 0 0 0 0                                         | OFF     | OFF               | Don't Need                                   | OFF              | V0~V4, VDD      |

#### 6-4-1 Booster Circuit

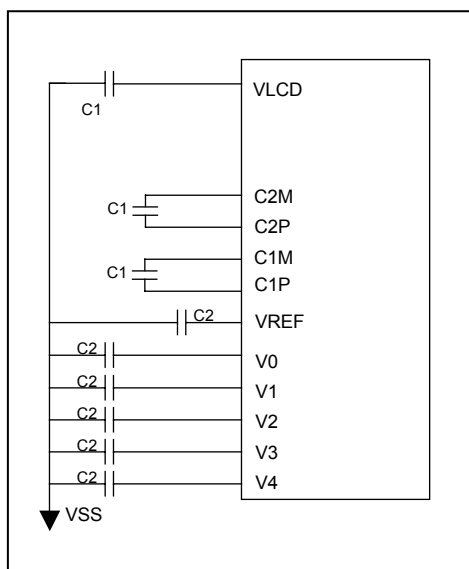
The RA8815 built-in a Booster which create 3-times or 2-times of " $V_{DD}-V_{SS}$ " that we called "VLCD". The VLCD is supply the power for next stage curcuit – Voltage Regulator and internal Driver cuicuit. If connect an 1uF capacitor on pin C1P and C1M, then the VLCD is eaul to 2\*VDD. If the pin C2P and C2Malso connect n 1uF capacitor then the VLCD is 3\*VDD. Refer to the following description of Figure 6-21.

Because the RA8815 supports maximumn LCD panel is 128x33. Therefore sometimes you can get the good display quality that base on lower power such as 5V only. In that case, user only need to connect 5V to VDD, VLCD, C1P and C2P. And you do not need to add capacitor on C1P/C1M and C2P/C2M.

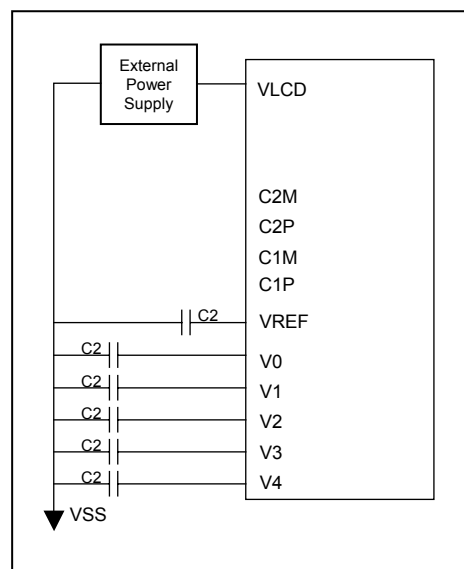


**Figure 6-21: Application Circuit of Booster**

The clock source of Booster is also control by register DRCR\_B. Please refer to the description of REG[12h] in Chapter 5-2. Normally, if use the internal Driver Power, then the application circuit is follow Figure 6-22. If use external VLCD, that means do not use the internal Booster, then the connection is show as Figure 6-23.



**Figure 6-22: Internal VLCD(3\*VDD)**



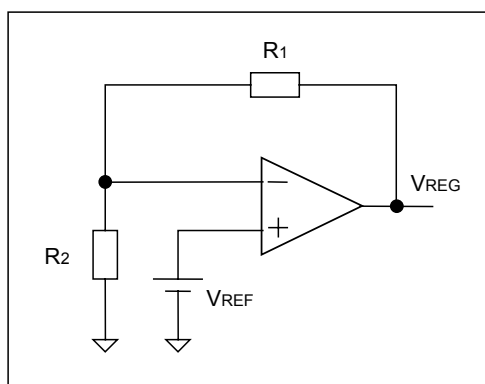
**Figure 6-23: External VLCD**

Note: The capacitor value of C1 is 1uF and C2 is 0.1uF.

#### 6-4-2 Voltage Regulator

The Voltage Regulator is consists of Band-Gap and OP-Amp. The purpose is used to generated a stable power -  $V_{REG}$  for Voltage Follower. The RA8815 also built-in a fixed reference power -  $V_{REF}$  for Voltage Regulator to generated  $V_{REG}$ . The basic formula is as following:

$$V_{REG} = (1 + R_1/R_2) \times V_{REF}$$



**Figure 6-24: Voltage Regulator**

The resistor ratio( $V_{REF}$  and  $V_{REG}$ ) of Voltage Regulator is adjustable by register DRCR\_B. There are total seven cases - 2/2.5/3/3.5/4/4.5/5X. Refer to the description of Bit[5:3] of register RCR\_B on Chapter 5-2. The Voltage Regulator also provide -0.05% auto adjust for temperature compensation.

The internal  $V_{REF}$  of RA8815 value is 1.6V. It's also could supply from external circuit. Please refer to Table 6-3 and Table 6-4:

Table 6-4: Select  $V_{REF}$

| Register DRCR_A<br>Bit6(EN_R) | $V_{REF}$       |
|-------------------------------|-----------------|
| 0                             | 1.60V (Ta=25°C) |
| 1                             | External        |

### 6-4-3 Voltage Follower

The internal Voltage Follower provides V0~V4 power for LCD Driver circuit. Of course, the user could select internal or external Voltage Follower. The relationship of V0~V4 and LVLCD is as following:

$$VLCD > V0 > V1 > V2 > V3 > V4 > GND$$

Figure 6-25A shows the circuit of using internal Voltage Follower. For external V0~V4, the connection is show as Figure 6-25B.

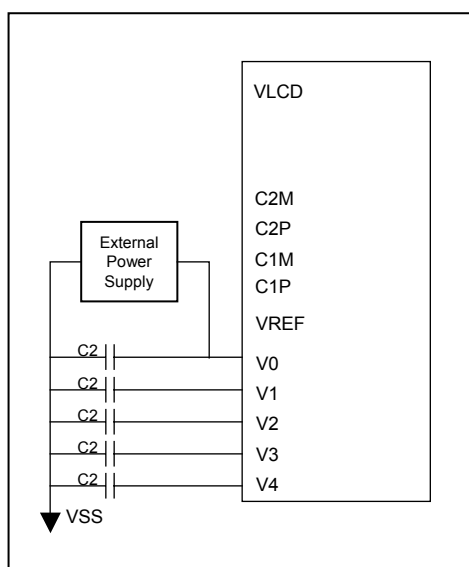


Figure 6-25A: Use Internal Voltage Follower

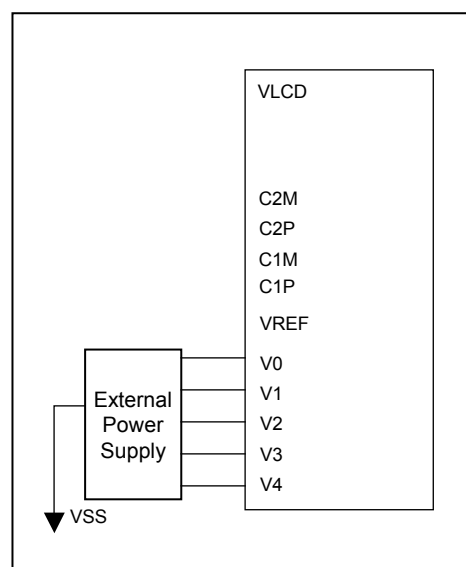


Figure 6-25B Use External Voltage Follower

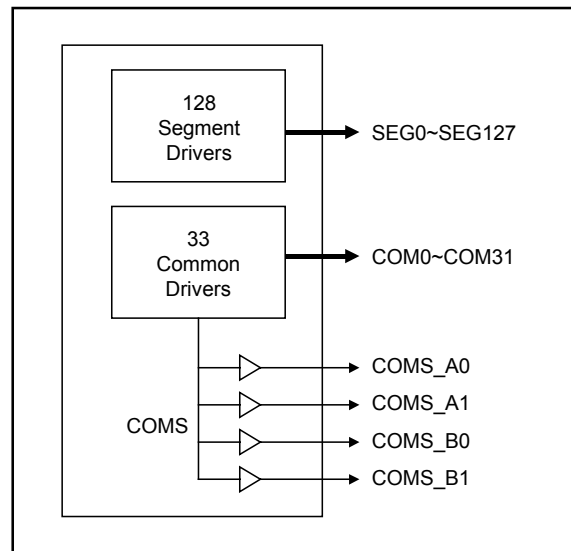
### 6-4-4 LCD Driver

The Segment/Common Driver of RA8815 is used to latch the data of pre-stage, then send to Level Shifter for combination. The combined data will follow the Timing Generator to control the switches then pass the V0~V4 to Common and Segment.

The LCD Bias of RA8815 is adjustable by register CSTR that from 1/4 to 1/7. The user can also adjust the display quality from this register. Meanwhile, the driving current is also adjustable by register DRCR\_B that in order to meet different panel.

As Figure 6-26, the RA8815 provides 128 Segment and 33 Common signals. One of the Common signal – COMS is provide for the Icon of LCD Panel. The COMS\_A[1:0] and COMS\_B[1:0] are located on the both side of RA8815 that in order to easier layout for COG panel. The COMS\_A[1:0]

and COMS\_B[1:0] have independent buffers, so if the area of Icon is bigger, then you can connect the COMS\_A0 and COMS\_A1 together. Or connect COMS\_B0 and COMS\_B1 together.



**Figure 6-26: The Driver of Segment and Common**

The DOFF\_Z of register PWRR is used to control the On/Off of LCD Panel. When DOFF\_Z is set to "0" then LCD Driver was closed. At this state, the driver output signals COM0~COM31 and SEG0~SEG127 are connect to GND, and the screen of LCD Panel was Off.

## 6-5 Interrupt

The RA8815 provide a interrupt signal( $\overline{INT}$ ) to response three possible interrupt:

- ◆ Busy Interrupt– When the data write to display RAM was complete.
- ◆ Scroll Interrupt - When the scroll window shifted 1, 8 or 16-pixels.
- ◆ Key-scan Interrupt - When a key was pressed.

The interrupt of above can be enabled or disable by register. The MPU can read the interrupt message form interrupt status register. The  $\overline{INT}$  is active low, so when MPU detect the interrupt happen then must clear interrupt status for  $\overline{INT}$  return to high. If user do not use the hardware interrupt( $\overline{INT}$ ), then MPU can get the interrupt message by reading the status register.

## 6-6 Key-Scan

The RA8815 built-in 4x5 key-scan circuit for extra key board function to help user integrate a key matrix application. In auto-mode, MPU can read the key code from register to know the key was short-press, long-press or key released. User can also adjust the cycle time of key-scan. Figure 6-27 is the simple application circuit. Table 6-5 is the mapping keyboard code of key matrix as Figure 6-27. So MPU knows which key be pressed by reading register – KSDR.

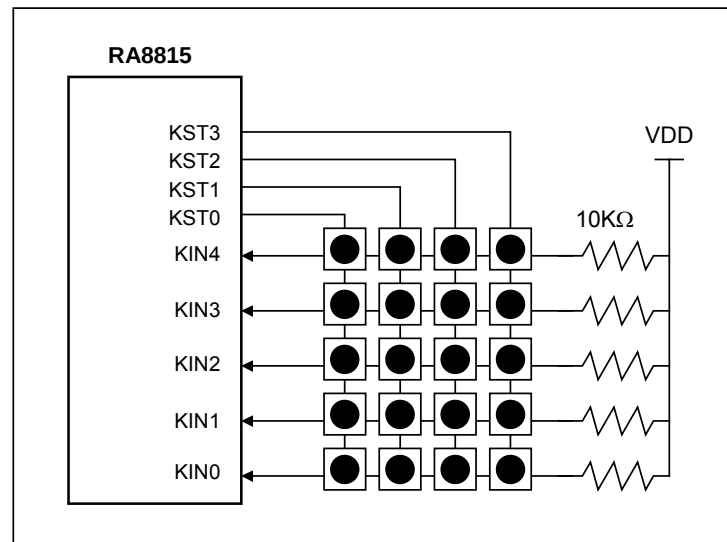


Figure 6-27: 4x5 Key Matrix Curcuit

Table 6-5: Keyboard Code of Auto-Mode

|      | Short-Press |      |      |      | Long-Press |      |      |      |
|------|-------------|------|------|------|------------|------|------|------|
|      | KST3        | KST2 | KST1 | KST0 | KST3       | KST2 | KST1 | KST0 |
| KIN0 | 15h         | 10h  | 05h  | 00h  | 35h        | 30h  | 25h  | 20h  |
| KIN1 | 16h         | 11h  | 06h  | 01h  | 36h        | 31h  | 26h  | 21h  |
| KIN2 | 17h         | 12h  | 07h  | 02h  | 37h        | 32h  | 27h  | 22h  |
| KIN3 | 18h         | 13h  | 08h  | 03h  | 38h        | 33h  | 28h  | 23h  |
| KIN4 | 19h         | 14h  | 09h  | 04h  | 39h        | 34h  | 29h  | 24h  |

In Auto-Mode of Key-Scan function, if the key pressed over one second, then the RA8815 will cause interrupt and change the data of register – KSDR to a long-press code. Therefore MPU knows which key was pressed ove one second.

## 6-7 I/O Port

The RA8815 provide eight lgeneral purpose I/O pins. Each I/O pin is easy to setup as input or output. They can use to drive LED, wakeup the RA8815 or provide information for whole system.

## 6-8 EL Signals

The RA8815 provide two special signals for EL driver circuit. The signals active time can also setup by register ELCR. The waveform and application are show as Figure 6-28 and 6-29.

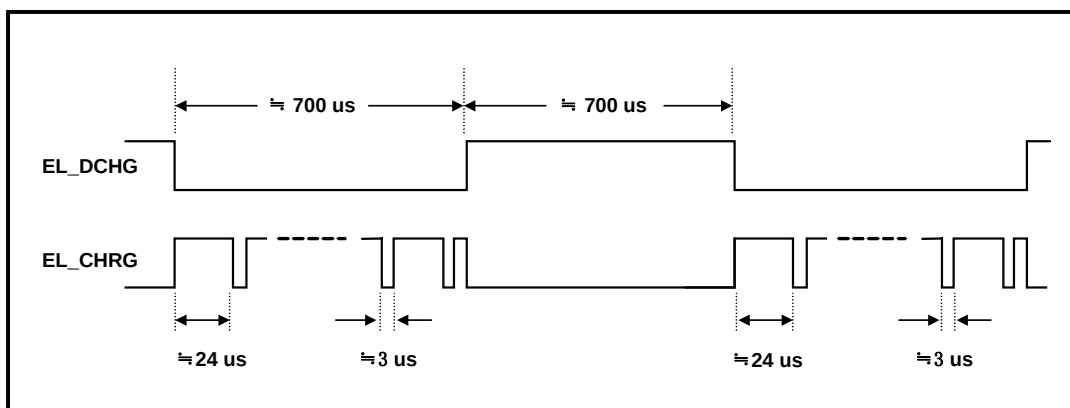


Figure 6-28: Control Signals for EL Driver

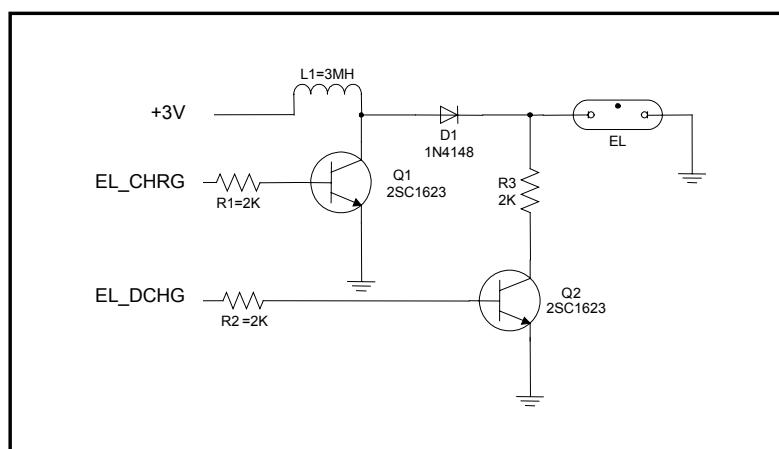


Figure 6-29: EL Driver Circuit

## 6-9 ASCII Block

|   | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 1 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 2 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 3 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 4 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 5 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 6 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 7 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 8 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 9 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| B |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| C |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| D |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| E |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| F |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

Figure 6-30: SamII ASCII(Table 0)

The RA8815 built-in three ASCII block which contains ASCII and special symbol for user to show on display directly in text mode. Actually these three ASCII block are stored in 256Kbyte Font ROM(see

Chapter 6-2). As the Figures 6-30~6-32, the left of each table is the High Nibble, and the right is the Low Nibble. The selection of these block is by MD0 and MD1 of register MWMR.

The Figure 6-30 is the table of small ASCII. Each character size is 8x8 dots. Therefore if the LCD panel size is 128Segx33Com then it can show four rows, and each row has 16 samll ASCII font. Figure 6-31 and 6-32 are the table of big ASCII. For the same panel size, it can show two row, and each row has 16 character.

|   | 0 | 1 | 2 | 3  | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
|---|---|---|---|----|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | ☺ | ☻ | ♥ | ♠  | ♣ | ♦ | ♠ | ♣ | ♦ | ♠ | ♣ | ♠ | ♣ | ♠ | ♣ | ♠ |
| 1 | ▶ | ◀ | ⬆ | ⬇  | ⬇ | ⬆ | ⬆ | ⬆ | ⬆ | ⬆ | ⬆ | ⬆ | ⬆ | ⬆ | ⬆ | ⬆ |
| 2 | ! | " | # | \$ | % | & | ' | ( | ) | * | + | , | - | . | / |   |
| 3 | 0 | 1 | 2 | 3  | 4 | 5 | 6 | 7 | 8 | 9 | : | ; | < | = | > | ? |
| 4 | @ | A | B | C  | D | E | F | G | H | I | J | K | L | M | N | O |
| 5 | P | Q | R | S  | T | U | V | W | X | Y | Z | [ | \ | ] | ^ | _ |
| 6 | ' | a | b | c  | d | e | f | g | h | i | j | k | l | m | n | o |
| 7 | p | q | r | s  | t | u | v | w | x | y | z | { |   | } | ~ |   |
| 8 | ™ | ⌂ | ⌂ | ⌂  | ⌂ | ⌂ | ⌂ | ⌂ | ⌂ | ⌂ | ⌂ | ⌂ | ⌂ | ⌂ | ⌂ | ⌂ |
| 9 | É | æ | œ | ô  | ö | û | ü | ÿ | ö | ü | ÿ | ö | ü | ÿ | ö | ü |
| A | á | í | ó | ú  | ñ | ñ | ñ | ñ | ñ | ñ | ñ | ñ | ñ | ñ | ñ | ñ |
| B | ⌂ | ⌂ | ⌂ | ⌂  | ⌂ | ⌂ | ⌂ | ⌂ | ⌂ | ⌂ | ⌂ | ⌂ | ⌂ | ⌂ | ⌂ | ⌂ |
| C | ⌂ | ⌂ | ⌂ | ⌂  | ⌂ | ⌂ | ⌂ | ⌂ | ⌂ | ⌂ | ⌂ | ⌂ | ⌂ | ⌂ | ⌂ | ⌂ |
| D | ⌂ | ⌂ | ⌂ | ⌂  | ⌂ | ⌂ | ⌂ | ⌂ | ⌂ | ⌂ | ⌂ | ⌂ | ⌂ | ⌂ | ⌂ | ⌂ |
| E | α | β | γ | π  | σ | μ | τ | ϕ | θ | ω | δ | ∞ | ∅ | ∈ | ∩ |   |
| F | ≡ | ± | ± | ±  | ± | ± | ± | ± | ± | ± | ± | ± | ± | ± | ± | ± |

Figure 6-31: Big ASCII (Table 1)

|   | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | Ä | ä | Å | å | Ä | ä | Å | å | Ä | ä | Å | å | Ä | ä | Å | å |
| 1 | Ð | ð | È | è | Ê | ê | Ê | ê | Ê | ê | Ê | ê | Ê | ê | Ê | ê |
| 2 | Ġ | ġ | Ġ | ġ | Ġ | ġ | Ġ | ġ | Ġ | ġ | Ġ | ġ | Ġ | ġ | Ġ | ġ |
| 3 | İ | ı | İ | ı | İ | ı | İ | ı | İ | ı | İ | ı | İ | ı | İ | ı |
| 4 | İ | ı | İ | ı | İ | ı | İ | ı | İ | ı | İ | ı | İ | ı | İ | ı |
| 5 | Ö | ö | œ | œ | œ | œ | œ | œ | œ | œ | œ | œ | œ | œ | œ | œ |
| 6 | Š | š | Š | š | Š | š | Š | š | Š | š | Š | š | Š | š | Š | š |
| 7 | Ů | ů | Ů | ů | Ů | ů | Ů | ů | Ů | ů | Ů | ů | Ů | ů | Ů | ů |
| 8 | Ĥ | ĥ | Ĥ | ĥ | Ĥ | ĥ | Ĥ | ĥ | Ĥ | ĥ | Ĥ | ĥ | Ĥ | ĥ | Ĥ | ĥ |
| 9 | Ɔ | Ɔ | Ɔ | Ɔ | Ɔ | Ɔ | Ɔ | Ɔ | Ɔ | Ɔ | Ɔ | Ɔ | Ɔ | Ɔ | Ɔ | Ɔ |
| A | Œ | œ | Œ | œ | Œ | œ | Œ | œ | Œ | œ | Œ | œ | Œ | œ | Œ | œ |
| B | Ů | ů | Ů | ů | Ů | ů | Ů | ů | Ů | ů | Ů | ů | Ů | ů | Ů | ů |
| C | İ | ı | İ | ı | İ | ı | İ | ı | İ | ı | İ | ı | İ | ı | İ | ı |
| D | İ | ı | İ | ı | İ | ı | İ | ı | İ | ı | İ | ı | İ | ı | İ | ı |
| E | Ä | ä | Ä | ä | Ä | ä | Ä | ä | Ä | ä | Ä | ä | Ä | ä | Ä | ä |
| F | İ | ı | İ | ı | İ | ı | İ | ı | İ | ı | İ | ı | İ | ı | İ | ı |

Figure 6-32: Big ASCII (Table 2)

## 6-10 Power Control

The RA8815 supports Normal Mode and Sleep Mode for operation. If write "0" to bit0 of register PWRR, then RA8815 will enter sleep mode. The functions of LCD display and driver will stop. All of the signals of COM and SEG will keep low, Key Strobe signals will keep high, and I/O keep the original state. Because the RC clock was stop, so the power consumption is very samll.

The RA8815 provide three way to wake up the system:

1. Write "1" to the bit0 of register PWRR.
2. Key-scan to wake up
3. I/O wake up

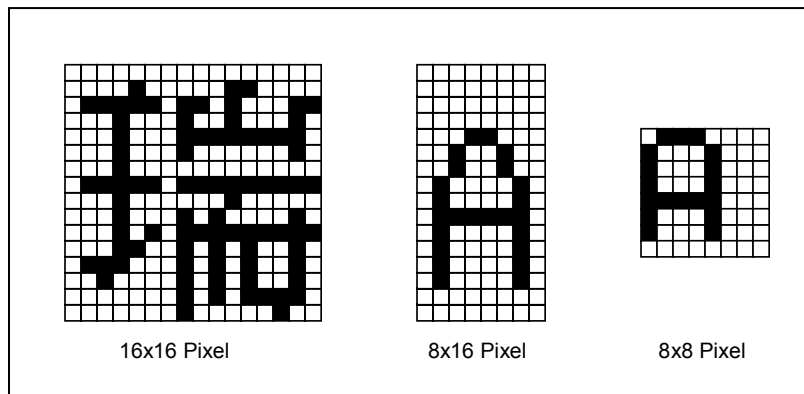
In wake up phase, the RA8815 will wake up the RC oscillator first, and it will take around 250ms. Then the RA8815 is enable to accept the command from MPU and LCD driver wake up for activity.

The VDD power operation range of RA8815 is 2.5~3.6V. But on the COG module, some power consumption will lose on the connection of FPC and chip that due to the ITO layout issue. So normally the VDD power range of COG module on the FPC side is around V2.7~3.8V.

## 7. Display Functions

### 7-1 Text Mode

The RA8815 built-in a 256KB Font ROM that including Traditional Chinese or Simplified Chinese, English, Japanese, ASCII, European and Latin(Latin-ext A, Latin-ext B). In text mode, it supports full-size font(Chinese or English) display or half-size(English) display. The full-size font is consist of 16x16 bit map. And half-size is consist of 8x16 or 8x8. Refer to the following Figure 7-1:



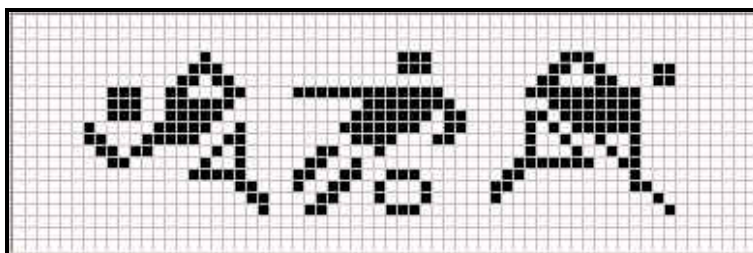
**Figure 7-1: Full-Size and Half-Size Font**

The Chinese display is operating at text mode. So if the RA8815 received two Chinese codes(BIG5 or GB) then the mapped font will show on the cursor position. Because each Chinese code including two bytes data, therefore the MPU has to send the code twice – High byte and Low byte. For English or Numeric, only one byte is need. The maximum supports panel size of RA8815 is 128x33dots. So in text mode it could show 2x8 Chinese fonts and 4x16 English fonts.

The register MWMR is used to setup the font size for display. The user can also select the different display mode such as bold, inverse or normal mode in this register.

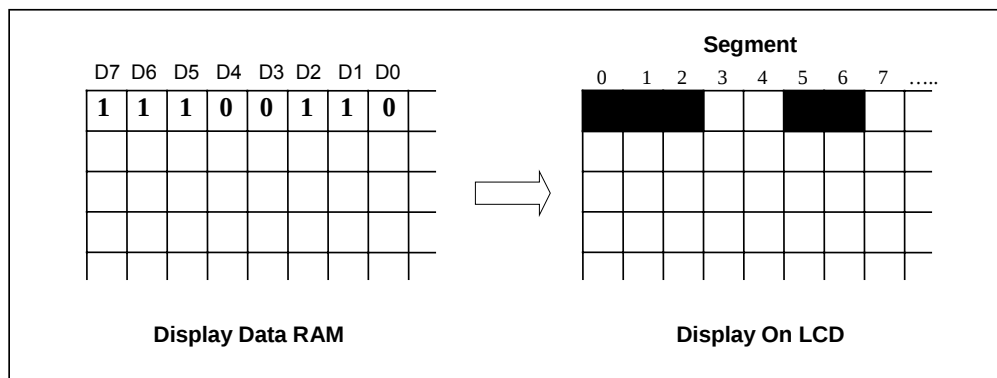
### 7-2 Graphic Mode

In the graphics mode, the RA8815 is fill the bit map data into display memory directly. So if the [MD1, MD0] of register is set to "00" (Graphics Mode), then write the data into memory, the data will show on the screen that cursor pointed.



**Figure 7-2: Graphics Mode Display**

The display RAM size of RA8815 is 528Byte(128\*33/8). Each memory bit is mapping to the LCD panel. If the data is “1” then the mapped dot is turn on. Please refer the Figure 7-3.



**Figure 7-3: Display Data Mapping to the Screen**

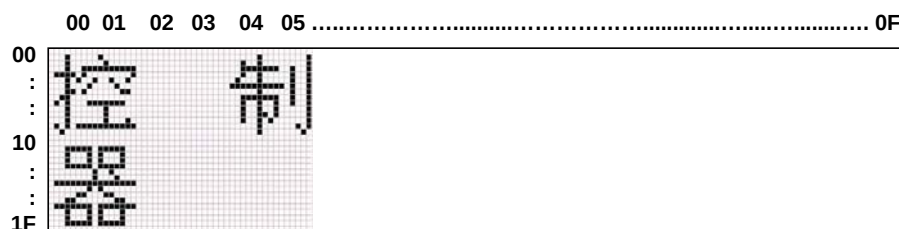
The RA8815 also provide a clean feature to clear all of the display RAM. If the “MCLR” of register PWRR is set to “1”, then all of contents of Display RAM will be clear to “0”. In the graphics mode, the user could select the blinking or inverse through register BLTR. The blinking are is assigned by the size of Scroll Window.

## 7-3 Cursor Setting

### 7-3-1 Cursor Position and Shift

The unit of Segment Address is 8-Bit, Commom is 1-Bit. For example, if user want to show a font “制” on the third position(full-size) of top, then the register X-CUR has to set 04h and Y-CUR set to 00h. If the second row wan to show “器” as Figure 7-4, then the X-CUR set to 00h and Y-CUR set to 10h.

Both of text mode and graphics mode, the cursor position are use the same resgidter - X-CUR and Y-CUR. If fill data to display RAM or show a Chinese font on the screen, the cursor will auto increase, and the boundry is the display window.



128(Segment) x 32(Common)

**Figure 7-4: An Example for Cursor Setting**

### 7-3-2 Cursor Display and Blink

The RA8815 provide cursor On/Off and blinking features. These functions are control by register CURCR. The cycle time of blinking is depend on the setting of register BLTR. The range is from 8 to 128 frames.

### 7-3-3 Cursor Height

The cursor height is also setting by register CURCR. For full-size mode the cursor height is adjustable from 1 to 16 pixels, and half size is form 1 to 8 pixels. Please refer to Figure 7-5.

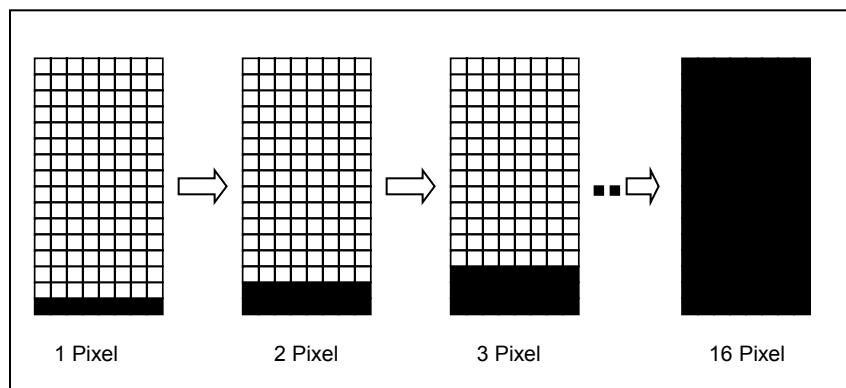


Figure 7-5: Cursor Height

### 7-4 Display Window

Normally, the Display Window size is same as LCD panel. It's setting by register SYSR. The maximum range is 128(Segment)x32(Common). The RA8815 provide a extran Common(Com-S) as the selection of Icon. Therefore the total 128 Icon for usage. Before access the Com-S, the register Y-CUR has set to 50h, then program the X-CUR to select Icon.

The RA8815 provides two positions for the panel layout of COM-S. It's convenient for user to design the position of Icon from their application. Refer to the Figure 7-6.

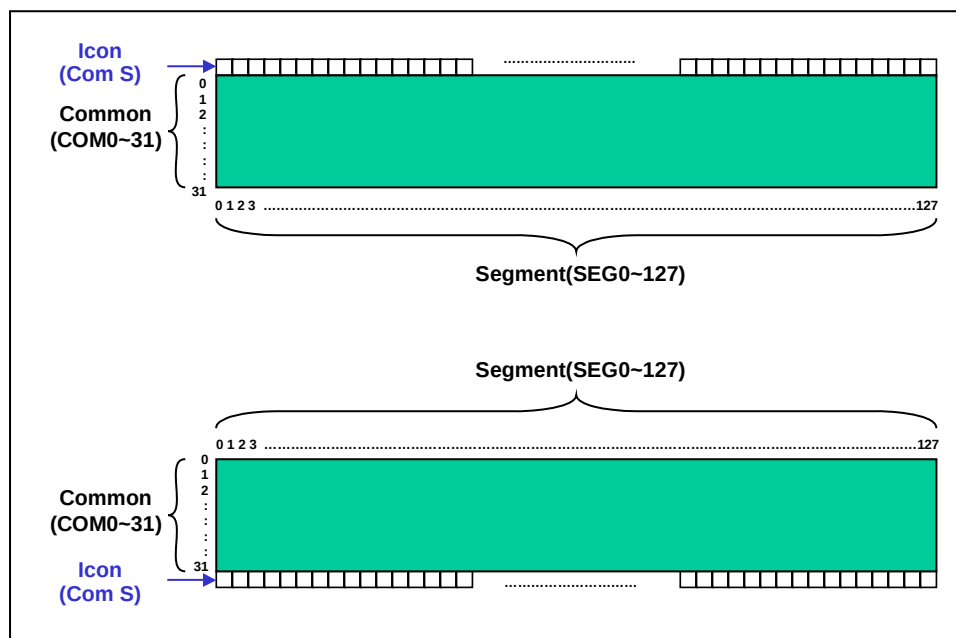
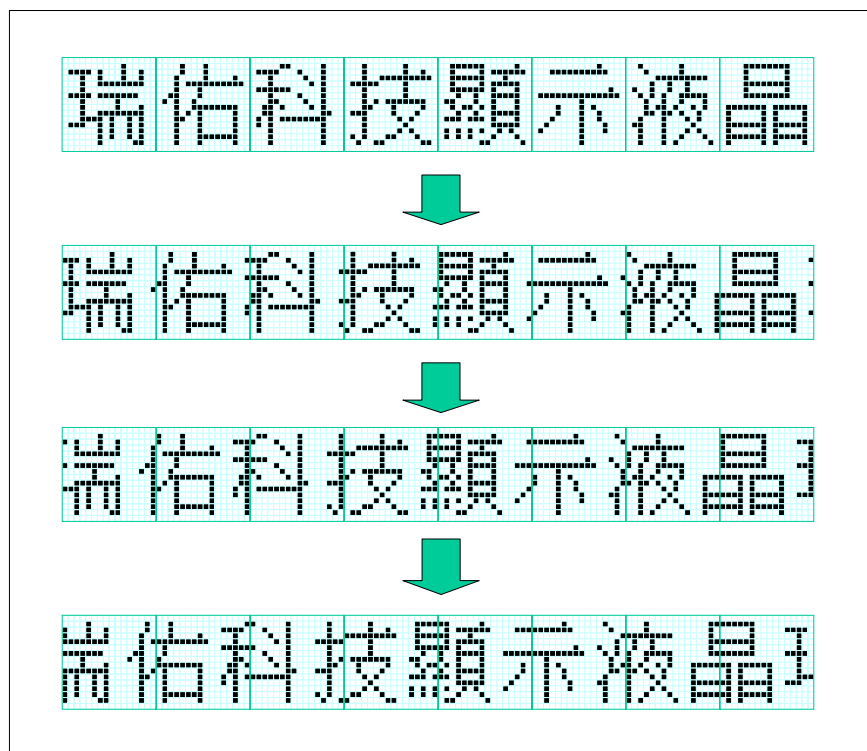


Figure 7-6: Display Window and Icon

## 7-5 Horizontal Scroll

The RA8815 provide Horizontal Scroll feature. User could assign the range of scrolling, scroll unit and speed. Refer to the following example as Figure 7-7. The scroll unit is set to 2 pixels.



**Figure 7-7: Horizontal Scroll**

The RA8815 allows horizontal scroll for right or left way. The user could use the scrolling buffer to show the Shift function. For example, store the data or text on the Horizontal Scroll Buffer first, then fill the new data/text into the buffer that after the screen shift 16pixels. You can repeat these action and find the screen is shift like caption of advertisement. The Figure 7-8 is an example to show the Horizontal Shift. The shift unit is 8pixels and the gray area is the scroll buffer. The display data will not show on the screen.

Please refer to application note for the related horizontal scroll feature.

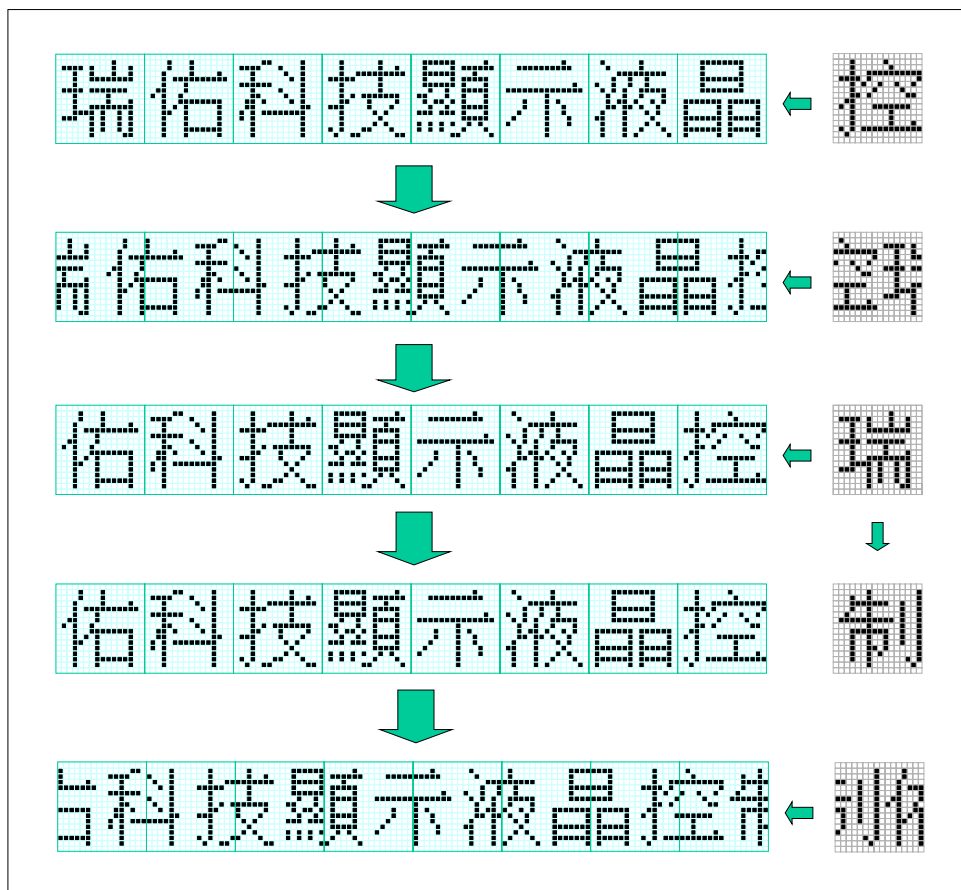


Figure 7-8: Horizontal Shift

## 7-6 Vertical Scroll

The RA8815 also provides the Vertical Scroll and Shift features that like horizontal function. User could assign the range of scrolling, scroll unit and speed. Refer to the following example as Figure 7-9. The vertical scroll unit is set to 2 pixels.

The RA8815 allows vertical scroll for up or down way. The user could use the scrolling buffer to show the Shift function. For example, store the data or text on the Vertical Scroll Buffer first, then fill the new data/text into the buffer that after the screen shift 16pixels. Please refer to application note for the related vertical scroll features.

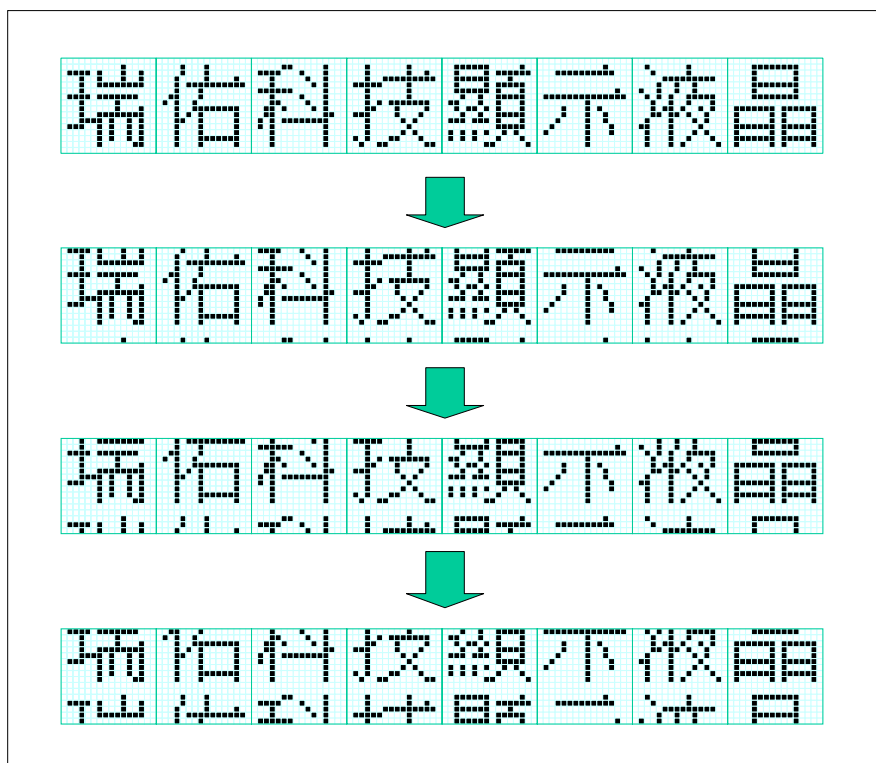


Figure 7-9: Vertical Scroll

## 8. Pin Diagram

### 8-1 COG Pad

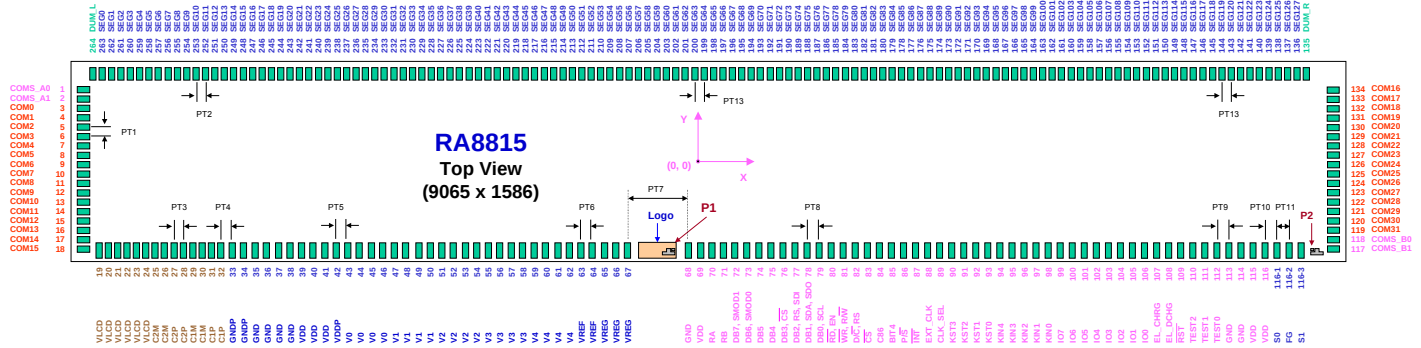
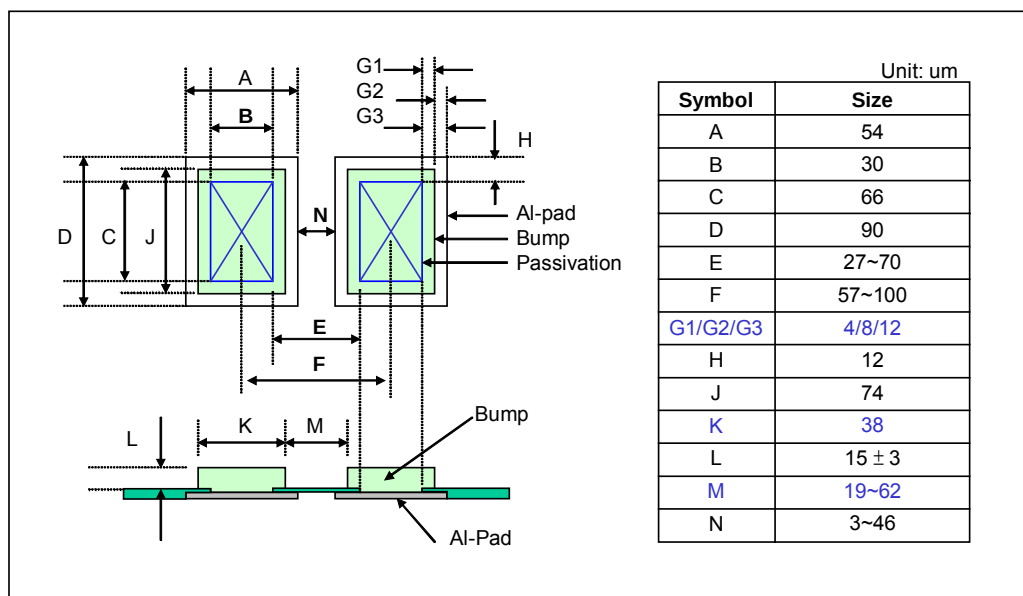


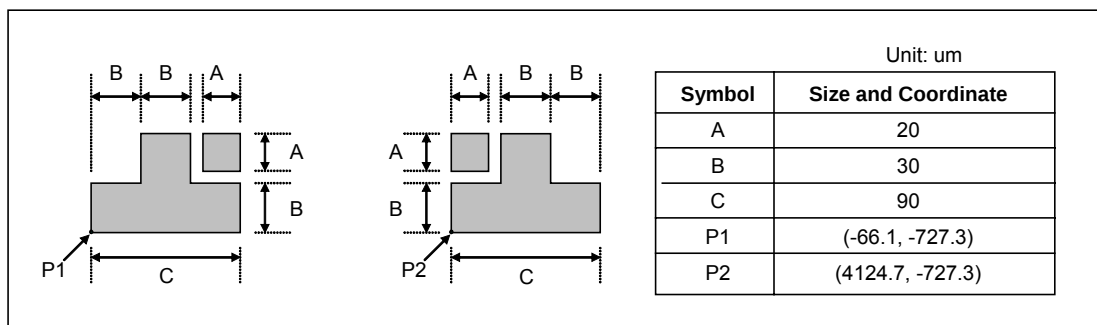
Figure 8-1 : Pin Diagram

Table 8-1: Bump Size and Pitch

|             |                                                                                                                      |                                     |
|-------------|----------------------------------------------------------------------------------------------------------------------|-------------------------------------|
| Chip Size   | 9065 $\mu\text{m}$ x 1586 $\mu\text{m}$                                                                              |                                     |
| Bump Size   | PAD 1~18, PAD 117~134 (COM Pads)                                                                                     | 74 $\mu\text{m}$ x 38 $\mu\text{m}$ |
|             | PAD 135~264 (SEG Pads),                                                                                              |                                     |
|             | PAD 19~116 (MCU/Power Pads)                                                                                          | 38 $\mu\text{m}$ x 74 $\mu\text{m}$ |
|             | PAD 161-1 ~ 161-3 (S0, FG, S1)                                                                                       |                                     |
| Bump Pitch  | PT1: PAD 1~18, PAD 117~134                                                                                           | 57 $\mu\text{m}$                    |
|             | PT2: PAD 135~143, 144~159, 160~175, 176~191, 192~199, 200~207, 208~223, 224~239, 240~255, 256~264                    | 64.8 $\mu\text{m}$                  |
|             | PT3: PAD 19~32, PAD 33~42                                                                                            | 57 $\mu\text{m}$                    |
|             | PT4: PAD 32 to 33                                                                                                    | 63.3 $\mu\text{m}$                  |
|             | PT5: PAD 42 to 43                                                                                                    | 84.2 $\mu\text{m}$                  |
|             | PT6: PAD 43 to 67, PAD 68 to 70                                                                                      | 100 $\mu\text{m}$                   |
|             | PT7: PAD 67 to 68                                                                                                    | 500 $\mu\text{m}$                   |
|             | PT8: PAD 70 to 112                                                                                                   | 80 $\mu\text{m}$                    |
|             | PT9: PAD 112 to 116                                                                                                  | 60 $\mu\text{m}$                    |
|             | PT10: PAD 116 to 116-1                                                                                               | 63.2 $\mu\text{m}$                  |
|             | PT11: PAD 116-1 to 116-3                                                                                             | 55 $\mu\text{m}$                    |
|             | PT12: PAD 143 to 144, 159 to 160, 175 to 176, 191 to 192, 199 to 200, 207 to 208, 223 to 224, 239 to 240, 255 to 256 | 74.6 $\mu\text{m}$                  |
|             | PT13: 199 to 200                                                                                                     | 89 $\mu\text{m}$                    |
| Bump Height | 15 $\pm$ 3 $\mu\text{m}$                                                                                             |                                     |



**Figure 8-2 : Gold Bump PAD Dimension**



**Figure 8-3 : Fixed Point Dimension**

## 8-2 Pad X/Y Coordinate

| Pad No. | Pad Name | X       | Y      |
|---------|----------|---------|--------|
| 1       | COMS_A0  | -4437.9 | 491.3  |
| 2       | COMS_A1  | -4437.9 | 434.3  |
| 3       | COM0     | -4437.9 | 377.3  |
| 4       | COM1     | -4437.9 | 320.3  |
| 5       | COM2     | -4437.9 | 263.3  |
| 6       | COM3     | -4437.9 | 206.3  |
| 7       | COM4     | -4437.9 | 149.3  |
| 8       | COM5     | -4437.9 | 92.3   |
| 9       | COM6     | -4437.9 | 35.3   |
| 10      | COM7     | -4437.9 | -35.3  |
| 11      | COM8     | -4437.9 | -92.3  |
| 12      | COM9     | -4437.9 | -149.3 |
| 13      | COM10    | -4437.9 | -206.3 |
| 14      | COM11    | -4437.9 | -263.3 |
| 15      | COM12    | -4437.9 | -320.3 |
| 16      | COM13    | -4437.9 | -377.3 |
| 17      | COM14    | -4437.9 | -434.3 |
| 18      | COM15    | -4437.9 | -491.3 |
| 19      | VLCD     | -4212.9 | -698.3 |
| 20      | VLCD     | -4155.9 | -698.3 |
| 21      | VLCD     | -4098.9 | -698.3 |
| 22      | VLCD     | -4041.9 | -698.3 |
| 23      | VLCD     | -3984.9 | -698.3 |
| 24      | VLCD     | -3927.9 | -698.3 |
| 25      | C2M      | -3870.9 | -698.3 |
| 26      | C2M      | -3813.9 | -698.3 |
| 27      | C2P      | -3756.9 | -698.3 |
| 28      | C2P      | -3699.9 | -698.3 |
| 29      | C1M      | -3642.9 | -698.3 |
| 30      | C1M      | -3585.9 | -698.3 |
| 31      | C1P      | -3528.9 | -698.3 |
| 32      | C1P      | -3471.9 | -698.3 |
| 33      | GNDP     | -3408.6 | -698.3 |
| 34      | GNDP     | -3351.6 | -698.3 |
| 35      | GND      | -3294.6 | -698.3 |

| Pad No. | Pad Name | X       | Y      |
|---------|----------|---------|--------|
| 36      | GND      | -3237.6 | -698.3 |
| 37      | GND      | -3180.6 | -698.3 |
| 38      | GND      | -3123.6 | -698.3 |
| 39      | VDD      | -3066.6 | -698.3 |
| 40      | VDD      | -3009.6 | -698.3 |
| 41      | VDD      | -2952.6 | -698.3 |
| 42      | VDDP     | -2895.6 | -698.3 |
| 43      | V0       | -2811.4 | -698.3 |
| 44      | V0       | -2711.4 | -698.3 |
| 45      | V0       | -2611.4 | -698.3 |
| 46      | V0       | -2511.4 | -698.3 |
| 47      | V1       | -2411.4 | -698.3 |
| 48      | V1       | -2311.4 | -698.3 |
| 49      | V1       | -2211.4 | -698.3 |
| 50      | V1       | -2111.4 | -698.3 |
| 51      | V2       | -2011.4 | -698.3 |
| 52      | V2       | -1911.4 | -698.3 |
| 53      | V2       | -1811.4 | -698.3 |
| 54      | V2       | -1711.4 | -698.3 |
| 55      | V3       | -1611.4 | -698.3 |
| 56      | V3       | -1511.4 | -698.3 |
| 57      | V3       | -1411.4 | -698.3 |
| 58      | V3       | -1311.4 | -698.3 |
| 59      | V4       | -1211.4 | -698.3 |
| 60      | V4       | -1111.4 | -698.3 |
| 61      | V4       | -1011.4 | -698.3 |
| 62      | V4       | -911.4  | -698.3 |
| 63      | VREF     | -811.4  | -698.3 |
| 64      | VREF     | -711.4  | -698.3 |
| 65      | VREG     | -611.4  | -698.3 |
| 66      | VREG     | -511.4  | -698.3 |
| 67      | VREG     | -411.4  | -698.3 |
| 68      | GND      | 88.6    | -698.3 |
| 69      | VDD      | 188.6   | -698.3 |
| 70      | RA       | 288.6   | -698.3 |

| Pad No. | Pad Name                       | X      | Y      |
|---------|--------------------------------|--------|--------|
| 71      | RB                             | 368.6  | -698.3 |
| 72      | DB7                            | 448.6  | -698.3 |
| 73      | DB6                            | 528.6  | -698.3 |
| 74      | DB5                            | 608.6  | -698.3 |
| 75      | DB4                            | 688.6  | -698.3 |
| 76      | DB3                            | 768.6  | -698.3 |
| 77      | DB2                            | 848.6  | -698.3 |
| 78      | DB1                            | 928.6  | -698.3 |
| 79      | DB0                            | 1008.6 | -698.3 |
| 80      | $\overline{\text{RD}}$         | 1088.6 | -698.3 |
| 81      | $\overline{\text{WR}}$         | 1168.6 | -698.3 |
| 82      | $\text{D}/\overline{\text{C}}$ | 1248.6 | -698.3 |
| 83      | $\overline{\text{CS}}$         | 1328.6 | -698.3 |
| 84      | C86                            | 1408.6 | -698.3 |
| 85      | BIT4                           | 1488.6 | -698.3 |
| 86      | $\text{P}/\overline{\text{S}}$ | 1568.6 | -698.3 |
| 87      | $\overline{\text{INT}}$        | 1648.6 | -698.3 |
| 88      | EXT_CLK                        | 1728.6 | -698.3 |
| 89      | CLK_SEL                        | 1808.6 | -698.3 |
| 90      | KST3                           | 1888.6 | -698.3 |
| 91      | KST2                           | 1968.6 | -698.3 |
| 92      | KST1                           | 2048.6 | -698.3 |
| 93      | KST0                           | 2128.6 | -698.3 |
| 94      | KIN4                           | 2208.6 | -698.3 |
| 95      | KIN3                           | 2288.6 | -698.3 |
| 96      | KIN2                           | 2368.6 | -698.3 |
| 97      | KIN1                           | 2448.6 | -698.3 |
| 98      | KIN0                           | 2528.6 | -698.3 |
| 99      | IO7                            | 2608.6 | -698.3 |
| 100     | IO6                            | 2688.6 | -698.3 |
| 101     | IO5                            | 2768.6 | -698.3 |
| 102     | IO4                            | 2848.6 | -698.3 |
| 103     | IO3                            | 2928.6 | -698.3 |
| 104     | IO2                            | 3008.6 | -698.3 |
| 105     | IO1                            | 3088.6 | -698.3 |
| 106     | IO0                            | 3168.6 | -698.3 |
| 107     | EL_CHRG                        | 3248.6 | -698.3 |

| Pad No. | Pad Name                | X      | Y      |
|---------|-------------------------|--------|--------|
| 108     | EL_DCHG                 | 3328.6 | -698.3 |
| 109     | $\overline{\text{RST}}$ | 3408.6 | -698.3 |
| 110     | TEST2                   | 3488.6 | -698.3 |
| 111     | TEST1                   | 3568.6 | -698.3 |
| 112     | TEST0                   | 3648.6 | -698.3 |
| 113     | GND                     | 3708.6 | -698.3 |
| 114     | GND                     | 3768.6 | -698.3 |
| 115     | VDD                     | 3828.6 | -698.3 |
| 116     | VDD                     | 3888.6 | -698.3 |
| 116-1   | S0                      | 3951.8 | -698.3 |
| 116-2   | FG                      | 4006.8 | -698.3 |
| 116-3   | S1                      | 4061.8 | -693.3 |
| 117     | COMS_B1                 | 4437.9 | -491.3 |
| 118     | COMS_B0                 | 4437.9 | -434.3 |
| 119     | COM31                   | 4437.9 | -377.3 |
| 120     | COM30                   | 4437.9 | -320.3 |
| 121     | COM29                   | 4437.9 | -263.3 |
| 122     | COM28                   | 4437.9 | -206.3 |
| 123     | COM27                   | 4437.9 | -149.3 |
| 124     | COM26                   | 4437.9 | -92.3  |
| 125     | COM25                   | 4437.9 | -35.3  |
| 126     | COM24                   | 4437.9 | 35.3   |
| 127     | COM23                   | 4437.9 | 92.3   |
| 128     | COM22                   | 4437.9 | 149.3  |
| 129     | COM21                   | 4437.9 | 206.3  |
| 130     | COM20                   | 4437.9 | 263.3  |
| 131     | COM19                   | 4437.9 | 320.3  |
| 132     | COM18                   | 4437.9 | 377.3  |
| 133     | COM17                   | 4437.9 | 434.3  |
| 134     | COM16                   | 4437.9 | 491.3  |
| 135     | DUM_R                   | 4230.9 | 698.3  |
| 136     | SEG127                  | 4166.1 | 698.3  |
| 137     | SEG126                  | 4101.3 | 698.3  |
| 138     | SEG125                  | 4036.5 | 698.3  |
| 139     | SEG124                  | 3971.7 | 698.3  |
| 140     | SEG123                  | 3906.9 | 698.3  |
| 141     | SEG122                  | 3842.1 | 698.3  |

| Pad No. | Pad Name | X      | Y     |
|---------|----------|--------|-------|
| 142     | SEG121   | 3777.3 | 698.3 |
| 143     | SEG120   | 3712.5 | 698.3 |
| 144     | SEG119   | 3637.9 | 698.3 |
| 145     | SEG118   | 3573.1 | 698.3 |
| 146     | SEG117   | 3508.3 | 698.3 |
| 147     | SEG116   | 3443.5 | 698.3 |
| 148     | SEG115   | 3378.7 | 698.3 |
| 149     | SEG114   | 3313.9 | 698.3 |
| 150     | SEG113   | 3249.1 | 698.3 |
| 151     | SEG112   | 3184.3 | 698.3 |
| 152     | SEG111   | 3119.5 | 698.3 |
| 153     | SEG110   | 3054.7 | 698.3 |
| 154     | SEG109   | 2989.9 | 698.3 |
| 155     | SEG108   | 2925.1 | 698.3 |
| 156     | SEG107   | 2860.3 | 698.3 |
| 157     | SEG106   | 2795.5 | 698.3 |
| 158     | SEG105   | 2730.7 | 698.3 |
| 159     | SEG104   | 2665.9 | 698.3 |
| 160     | SEG103   | 2591.3 | 698.3 |
| 161     | SEG102   | 2526.5 | 698.3 |
| 162     | SEG101   | 2461.7 | 698.3 |
| 163     | SEG100   | 2396.9 | 698.3 |
| 164     | SEG99    | 2332.1 | 698.3 |
| 165     | SEG98    | 2267.3 | 698.3 |
| 166     | SEG97    | 2202.5 | 698.3 |
| 167     | SEG96    | 2137.7 | 698.3 |
| 168     | SEG95    | 2072.9 | 698.3 |
| 169     | SEG94    | 2008.1 | 698.3 |
| 170     | SEG93    | 1943.3 | 698.3 |
| 171     | SEG92    | 1878.5 | 698.3 |
| 172     | SEG91    | 1813.7 | 698.3 |
| 173     | SEG90    | 1748.9 | 698.3 |
| 174     | SEG89    | 1684.1 | 698.3 |
| 175     | SEG88    | 1619.3 | 698.3 |
| 176     | SEG87    | 1544.7 | 698.3 |
| 177     | SEG86    | 1479.9 | 698.3 |
| 178     | SEG85    | 1415.1 | 698.3 |

| Pad No. | Pad Name | X       | Y     |
|---------|----------|---------|-------|
| 179     | SEG84    | 1350.3  | 698.3 |
| 180     | SEG83    | 1285.5  | 698.3 |
| 181     | SEG82    | 1220.7  | 698.3 |
| 182     | SEG81    | 1155.9  | 698.3 |
| 183     | SEG80    | 1091.1  | 698.3 |
| 184     | SEG79    | 1026.3  | 698.3 |
| 185     | SEG78    | 961.5   | 698.3 |
| 186     | SEG77    | 896.7   | 698.3 |
| 187     | SEG76    | 831.9   | 698.3 |
| 188     | SEG75    | 767.1   | 698.3 |
| 189     | SEG74    | 702.3   | 698.3 |
| 190     | SEG73    | 637.5   | 698.3 |
| 191     | SEG72    | 572.7   | 698.3 |
| 192     | SEG71    | 498.1   | 698.3 |
| 193     | SEG70    | 433.3   | 698.3 |
| 194     | SEG69    | 368.5   | 698.3 |
| 195     | SEG68    | 303.7   | 698.3 |
| 196     | SEG67    | 238.9   | 698.3 |
| 197     | SEG66    | 174.1   | 698.3 |
| 198     | SEG65    | 109.3   | 698.3 |
| 199     | SEG64    | 44.5    | 698.3 |
| 200     | SEG63    | -44.5   | 698.3 |
| 201     | SEG62    | -109.3  | 698.3 |
| 202     | SEG61    | -174.1  | 698.3 |
| 203     | SEG60    | -238.9  | 698.3 |
| 204     | SEG59    | -303.7  | 698.3 |
| 205     | SEG58    | -368.5  | 698.3 |
| 206     | SEG57    | -433.3  | 698.3 |
| 207     | SEG56    | -498.1  | 698.3 |
| 208     | SEG55    | -572.7  | 698.3 |
| 209     | SEG54    | -637.5  | 698.3 |
| 210     | SEG53    | -702.3  | 698.3 |
| 211     | SEG52    | -767.1  | 698.3 |
| 212     | SEG51    | -831.9  | 698.3 |
| 213     | SEG50    | -896.7  | 698.3 |
| 214     | SEG49    | -961.5  | 698.3 |
| 215     | SEG48    | -1026.3 | 698.3 |

| Pad No. | Pad Name | X       | Y     |
|---------|----------|---------|-------|
| 216     | SEG47    | -1091.1 | 698.3 |
| 217     | SEG46    | -1155.9 | 698.3 |
| 218     | SEG45    | -1220.7 | 698.3 |
| 219     | SEG44    | -1285.5 | 698.3 |
| 220     | SEG43    | -1350.3 | 698.3 |
| 221     | SEG42    | -1415.1 | 698.3 |
| 222     | SEG41    | -1479.9 | 698.3 |
| 223     | SEG40    | -1544.7 | 698.3 |
| 224     | SEG39    | -1619.3 | 698.3 |
| 225     | SEG38    | -1684.1 | 698.3 |
| 226     | SEG37    | -1748.9 | 698.3 |
| 227     | SEG36    | -1813.7 | 698.3 |
| 228     | SEG35    | -1878.5 | 698.3 |
| 229     | SEG34    | -1943.3 | 698.3 |
| 230     | SEG33    | -2008.1 | 698.3 |
| 231     | SEG32    | -2072.9 | 698.3 |
| 232     | SEG31    | -2137.7 | 698.3 |
| 233     | SEG30    | -2202.5 | 698.3 |
| 234     | SEG29    | -2267.3 | 698.3 |
| 235     | SEG28    | -2332.1 | 698.3 |
| 236     | SEG27    | -2396.9 | 698.3 |
| 237     | SEG26    | -2461.7 | 698.3 |
| 238     | SEG25    | -2526.5 | 698.3 |
| 239     | SEG24    | -2591.3 | 698.3 |
| 240     | SEG23    | -2665.9 | 698.3 |
| 241     | SEG22    | -2730.7 | 698.3 |
| 242     | SEG21    | -2795.5 | 698.3 |
| 243     | SEG20    | -2860.3 | 698.3 |
| 244     | SEG19    | -2925.1 | 698.3 |
| 245     | SEG18    | -2989.9 | 698.3 |
| 246     | SEG17    | -3054.7 | 698.3 |
| 247     | SEG16    | -3119.5 | 698.3 |
| 248     | SEG15    | -3184.3 | 698.3 |
| 249     | SEG14    | -3249.1 | 698.3 |
| 250     | SEG13    | -3313.9 | 698.3 |
| 251     | SEG12    | -3378.7 | 698.3 |
| 252     | SEG11    | -3443.5 | 698.3 |

| Pad No. | Pad Name | X       | Y     |
|---------|----------|---------|-------|
| 253     | SEG10    | -3508.3 | 698.3 |
| 254     | SEG9     | -3573.1 | 698.3 |
| 255     | SEG8     | -3637.9 | 698.3 |
| 256     | SEG7     | -3712.5 | 698.3 |
| 257     | SEG6     | -3777.3 | 698.3 |
| 258     | SEG5     | -3842.1 | 698.3 |
| 259     | SEG4     | -3906.9 | 698.3 |
| 260     | SEG3     | -3971.7 | 698.3 |
| 261     | SEG2     | -4036.5 | 698.3 |
| 262     | SEG1     | -4101.3 | 698.3 |
| 263     | SEG0     | -4166.1 | 698.3 |
| 264     | DUM_L    | -4230.9 | 698.3 |

## 9. Electrical Characteristic

### 9-1 Absolute Maximum Ratings

Table 9-1

| Parameter                   | Symbol    | Rating               | Unit |
|-----------------------------|-----------|----------------------|------|
| Supply Voltage Range        | $V_{DD}$  | -0.3 to 6.5          | V    |
| Input Voltage Range         | $V_{IN}$  | -0.3 to $V_{DD}+0.3$ | V    |
| External VLCD Voltage Range | $V_{LCD}$ | -0.3 to 8.0          | V    |
| Operation Temperature Range | $T_{OPR}$ | -20 to 80            | °C   |
| Storage Temperature Range   | $T_{ST}$  | -45 to 125           | °C   |

### 9-2 DC Characteristic

Table 9-2

| Parameter                                     | Symbol        | Min.                | Typ. | Max.                | Unit | Condition                                                                                                                   |
|-----------------------------------------------|---------------|---------------------|------|---------------------|------|-----------------------------------------------------------------------------------------------------------------------------|
| Operating Voltage                             | $V_{DD}$      | 2.5                 | 3.3  | 3.6                 | V    | Bare Die                                                                                                                    |
| Operating Voltage                             | $V_{DD}$      | 2.7                 | 3.3  | 3.8                 | V    | COG Module                                                                                                                  |
| VLCD Voltage                                  | $V_{LCD}$     | --                  | 5~7  | 7.8                 | V    |                                                                                                                             |
| Input High Voltage                            | $V_{IH}$      | $0.8 \times V_{DD}$ | --   | $V_{DD}$            | V    |                                                                                                                             |
| Input Low Voltage                             | $V_{IL}$      | Gnd                 | --   | $0.2 \times V_{DD}$ | V    |                                                                                                                             |
| Output High Voltage                           | $V_{OH}$      | $0.8 \times V_{DD}$ | --   | $V_{DD}$            | V    |                                                                                                                             |
| Output Low Voltage                            | $V_{OL}$      | Gnd                 | --   | $0.2 \times V_{DD}$ | V    |                                                                                                                             |
| Input Leakage Current                         | $I_{IL}$      | -1                  | --   | +1                  | μA   | $V_{IN} = V_{DD}$ to $V_{SS}$                                                                                               |
| Output Leakage Current                        | $I_{OL}$      | -3                  | --   | +2                  | μA   | $V_{IN} = V_{DD}$ to $V_{SS}$                                                                                               |
| Oscillator Frequency                          | $F_{CL}$      | --                  | 56   | --                  | KHz  | $V_{DD}=3.3V$ , R = 270K                                                                                                    |
|                                               |               | --                  | 55   | --                  |      | $V_{DD}=3.0V$ , R = 270K                                                                                                    |
|                                               |               | --                  | 47   | --                  |      | $V_{DD}=2.4V$ , R = 270K                                                                                                    |
| Standby Mode Current<br>(Normal Mode Current) | $I_{SB}$      | --                  | 70   | --                  | μA   | <b>No MPU I/F Access</b><br>$V_{DD}=3.3V$ , $F_{CL} = 55KHz$<br>Segment=128,<br>Common=32<br>FRM = 60Hz<br>$T_A=25^\circ C$ |
| Display Off Current                           | $I_{DISPLAY}$ | --                  | 25   | --                  | μA   | The same as above                                                                                                           |
| Sleep Mode Current                            | $I_{SLEEP}$   | --                  | 0.2  | 0.5                 | μA   | The same as above                                                                                                           |

$V_{DD} = 2.4$  to  $3.6V$ , Gnd = 0V,  $T_a = -20$  to  $80^\circ C$

## 9-3 Timing Characteristic

### 9-3-1 Parallel Interface

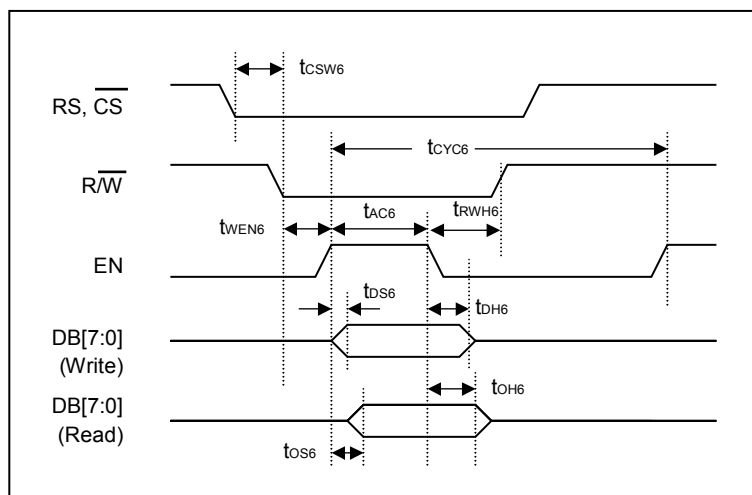


Figure 9-1 : 6800 MPU Timing

#### 6800 MPU Interface

| Item                  | Signal              | Symbol            | Condition     | Rating |      | Unit |
|-----------------------|---------------------|-------------------|---------------|--------|------|------|
|                       |                     |                   |               | Min.   | Max. |      |
| Address Setup Time    | RS, $\overline{CS}$ | t <sub>CSW6</sub> |               | 0      | --   | ns   |
| Read/Write Setup Time | R/ $\overline{W}$   | t <sub>WEN6</sub> |               | 10     | --   |      |
| Read/Write Hold Time  |                     | t <sub>RWH6</sub> |               | 10     | --   |      |
| Enable Access Time    | EN                  | t <sub>AC6</sub>  |               | 90     | --   |      |
| Access Cycle Time     |                     | t <sub>CYC6</sub> | Command Cycle | 200    | --   |      |
|                       |                     |                   | Data Cycle    | 400    | --   |      |
| Write Data Setup Time | DB[7:0]             | t <sub>DS6</sub>  |               | 0      | --   |      |
| Write Data Hold Time  |                     | t <sub>DH6</sub>  |               | 10     | --   |      |
| Read Data Access Time |                     | t <sub>OS6</sub>  |               | --     | 0    |      |
| Read Data Hold Time   |                     | t <sub>OH6</sub>  |               | 10     | --   |      |

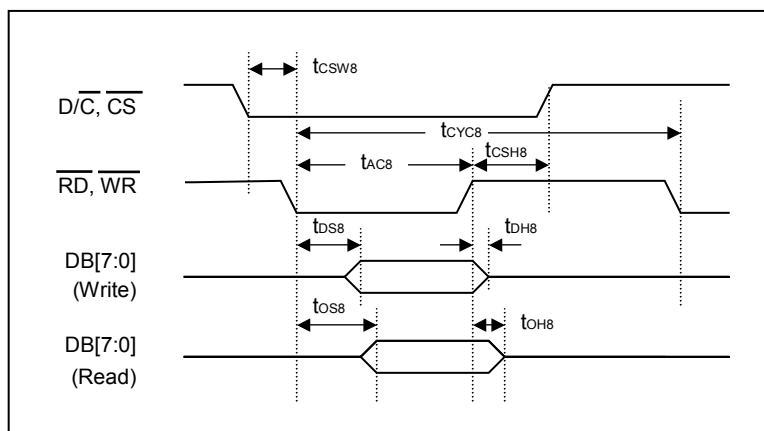


Figure 9-2 : 8080 MPU Timing

#### 8080 MPU Interface

| Item                   | Signal                                          | Symbol            | Condition     | Rating |      | Unit |
|------------------------|-------------------------------------------------|-------------------|---------------|--------|------|------|
|                        |                                                 |                   |               | Min.   | Max. |      |
| Address Setup Time     | RS, $\overline{\text{CS}}$                      | $T_{\text{CSW8}}$ |               | 10     | --   | ns   |
| Address Hold Time      |                                                 | $T_{\text{CSH8}}$ |               | 10     | --   |      |
| Read/Write Access Time | $\overline{\text{RD}}$ , $\overline{\text{WR}}$ | $t_{\text{AC8}}$  |               | 90     | --   |      |
| Access Cycle Time      |                                                 | $T_{\text{CYC8}}$ | Command Cycle | 200    | --   |      |
|                        |                                                 |                   | Data Cycle    | 400    | --   |      |
| Write Data Setup Time  | DB[7:0]                                         | $t_{\text{DS6}}$  |               | 0      | --   |      |
| Write Data Hold Time   |                                                 | $t_{\text{DH6}}$  |               | 10     | --   |      |
| Read Data Setup Time   |                                                 | $t_{\text{OS6}}$  |               | --     | 0    |      |
| Read Data Setup Time   |                                                 | $t_{\text{OH6}}$  |               | 10     | --   |      |

#### 9-3-2 Serial Interface

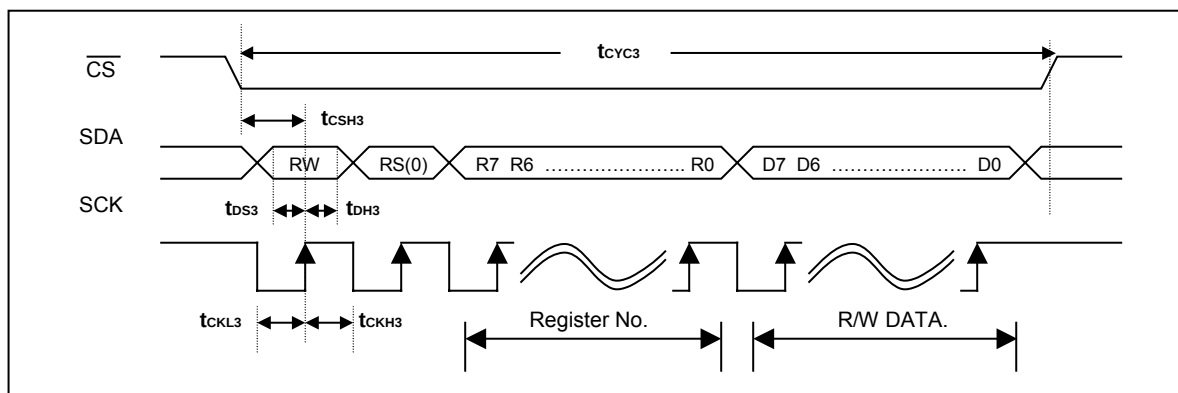


Figure 9-3 : 3-Wire Timing

### 3-Wire Serial Interface

| Item                       | Signal          | Symbol     | Condition | Rating |      | Unit    |
|----------------------------|-----------------|------------|-----------|--------|------|---------|
|                            |                 |            |           | Min.   | Max. |         |
| Access Time                | $\overline{CS}$ | $t_{CYC3}$ |           | 3.6    | --   | $\mu s$ |
| $\overline{CS}$ Setup Time |                 | $t_{CSH3}$ |           | 20     | --   | ns      |
| Clock Low Pulse Width      | SCK             | $t_{CKL3}$ |           | 100    | --   |         |
| Clock High Pulse Width     |                 | $t_{CKH3}$ |           | 100    | --   |         |
| Data Setup Time            | SDA             | $t_{DS3}$  |           | 20     | --   |         |
| Data Hold Time             |                 | $t_{DH3}$  |           | 10     | --   |         |

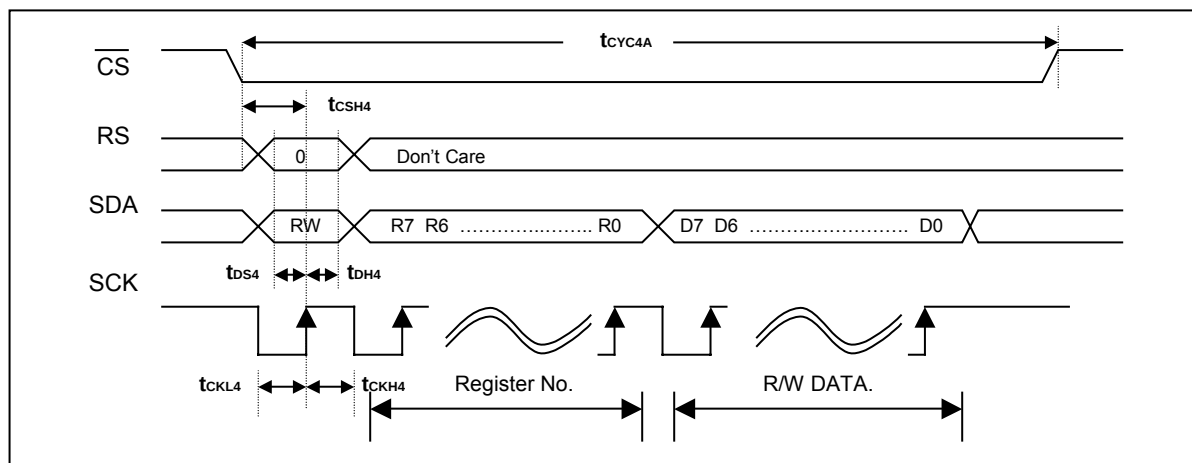


Figure 9-4 : 4-Wire(A-Type) Timing

### 4-Wire(A-Type) Serial Interface

| Item                       | Signal          | Symbol      | Condition | Rating |      | Unit    |
|----------------------------|-----------------|-------------|-----------|--------|------|---------|
|                            |                 |             |           | Min.   | Max. |         |
| Access Time                | $\overline{CS}$ | $t_{CYC4A}$ |           | 3.4    | --   | $\mu s$ |
| $\overline{CS}$ Setup Time |                 | $t_{CSH4}$  |           | 20     | --   | ns      |
| Clock Low Pulse Width      | SCK             | $t_{CKL4}$  |           | 100    | --   |         |
| Clock High Pulse Width     |                 | $t_{CKH4}$  |           | 100    | --   |         |
| Data Setup Time            | SDA, RS         | $t_{DS4}$   |           | 20     | --   |         |
| Data Hold Time             |                 | $t_{DH4}$   |           | 10     | --   |         |

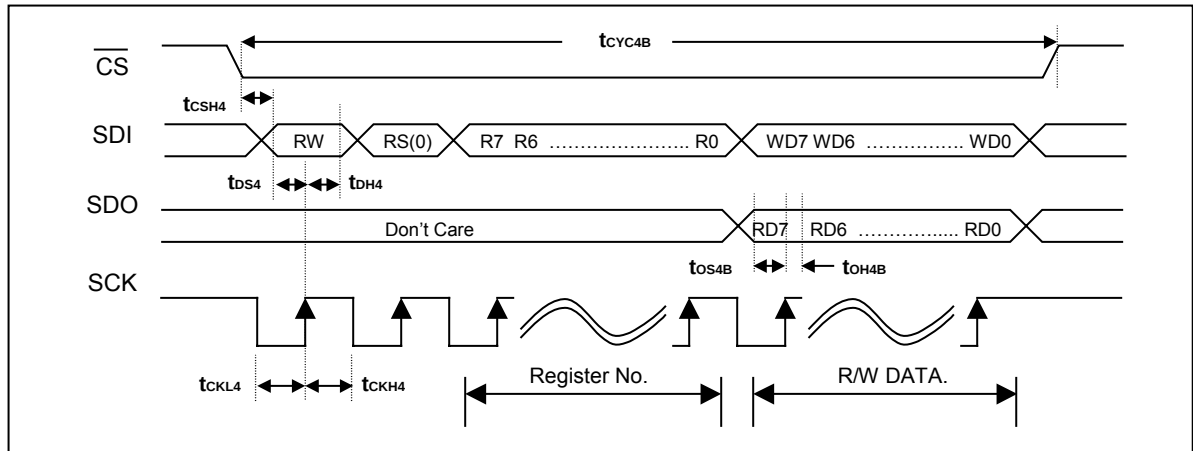


Figure 9-5 : 4-Wire(B Type) Timing

#### 4-Wire(B-Type) Serial Interface

| Item                       | Signal          | Symbol      | Condition | Rating |      | Unit    |
|----------------------------|-----------------|-------------|-----------|--------|------|---------|
|                            |                 |             |           | Min.   | Max. |         |
| Access Time                | $\overline{CS}$ | $t_{CYC4A}$ |           | 3.6    | --   | $\mu s$ |
| $\overline{CS}$ Setup Time |                 | $t_{CSH4}$  |           | 20     | --   | ns      |
| Clock Low Pulse Width      | SCK             | $t_{CKL4}$  |           | 100    | --   |         |
| Clock High Pulse Width     |                 | $t_{CKH4}$  |           | 100    | --   |         |
| Data Write Setup Time      | SDI             | $t_{DS4}$   |           | 20     | --   |         |
| Data Write Hold Time       |                 | $t_{DH4}$   |           | 10     | --   |         |
| Data Read Setup Time       | SDO             | $t_{OS4B}$  |           | 20     | --   |         |
| Data Read Hold Time        |                 | $t_{OH4B}$  |           | 10     | --   |         |

#### 9-3-3 Reset Interface

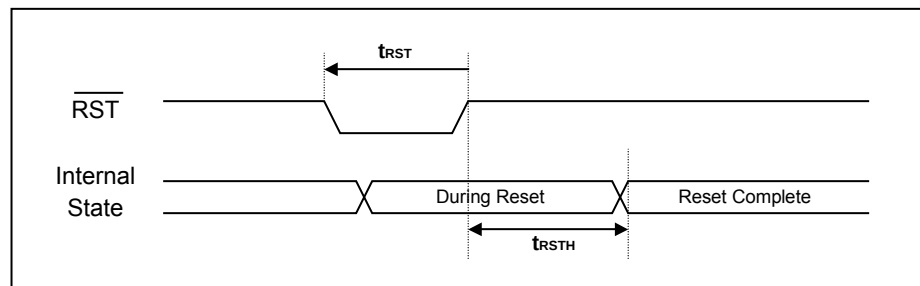


Figure 9-6: Reset Timing

| Item                     | Signal                  | Symbol            | Condition                      | Rating |      | Unit |
|--------------------------|-------------------------|-------------------|--------------------------------|--------|------|------|
|                          |                         |                   |                                | Min.   | Max. |      |
| Reset Pulse Width        | $\overline{\text{RST}}$ | $t_{\text{RST}}$  |                                | 100    | --   | ms   |
| Reset Complete Hold Time | $\overline{\text{RST}}$ | $t_{\text{RSTH}}$ | $F_{\text{CL}} = 55\text{KHz}$ | 150    | 250  | ms   |

## Appendix A.

### A-1 COG Application

#### A-1-1 Basic Connection of Serial I/F

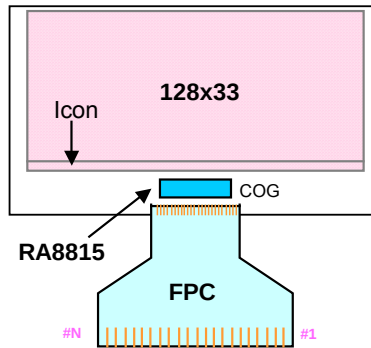


Figure A-1 : COG Module

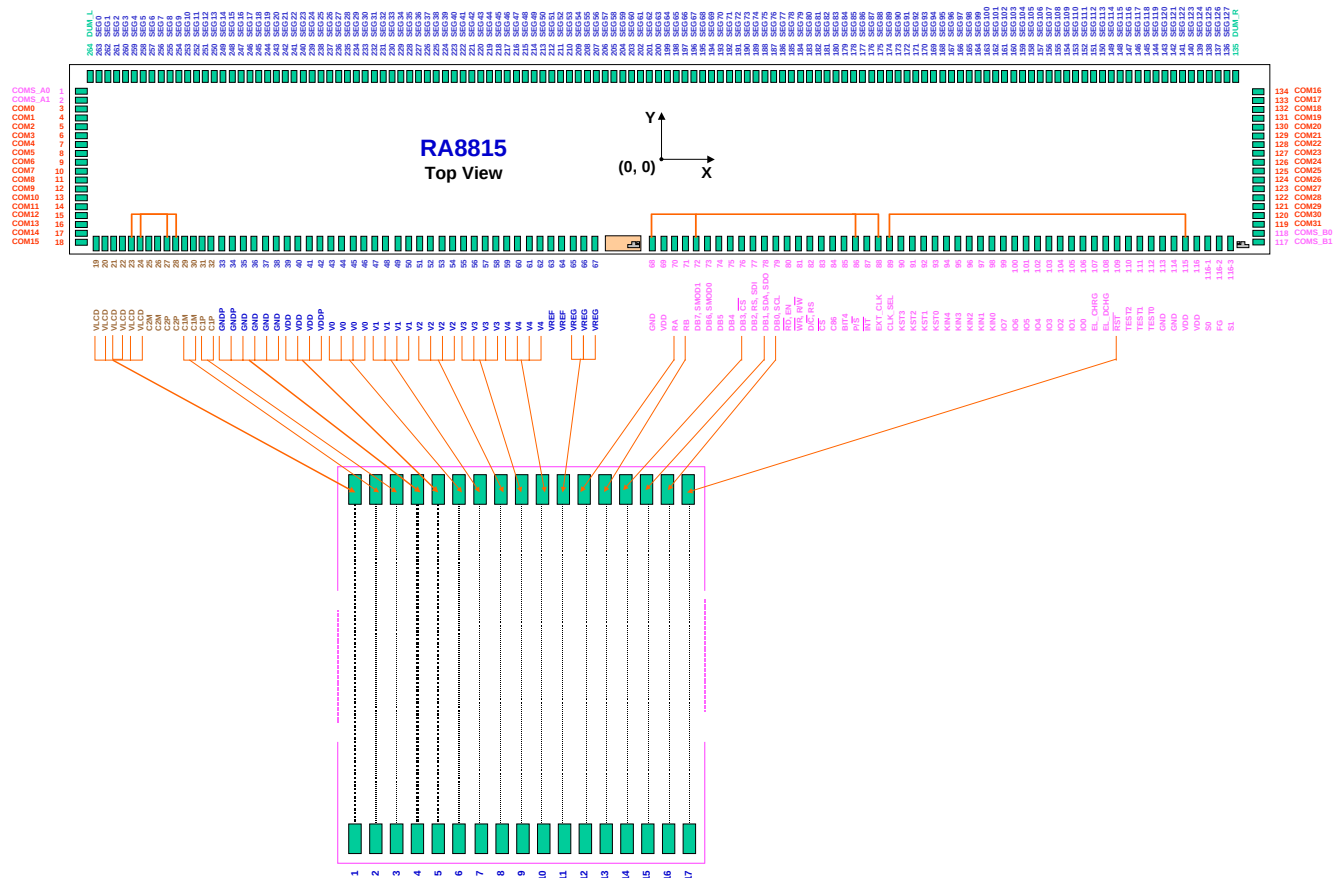
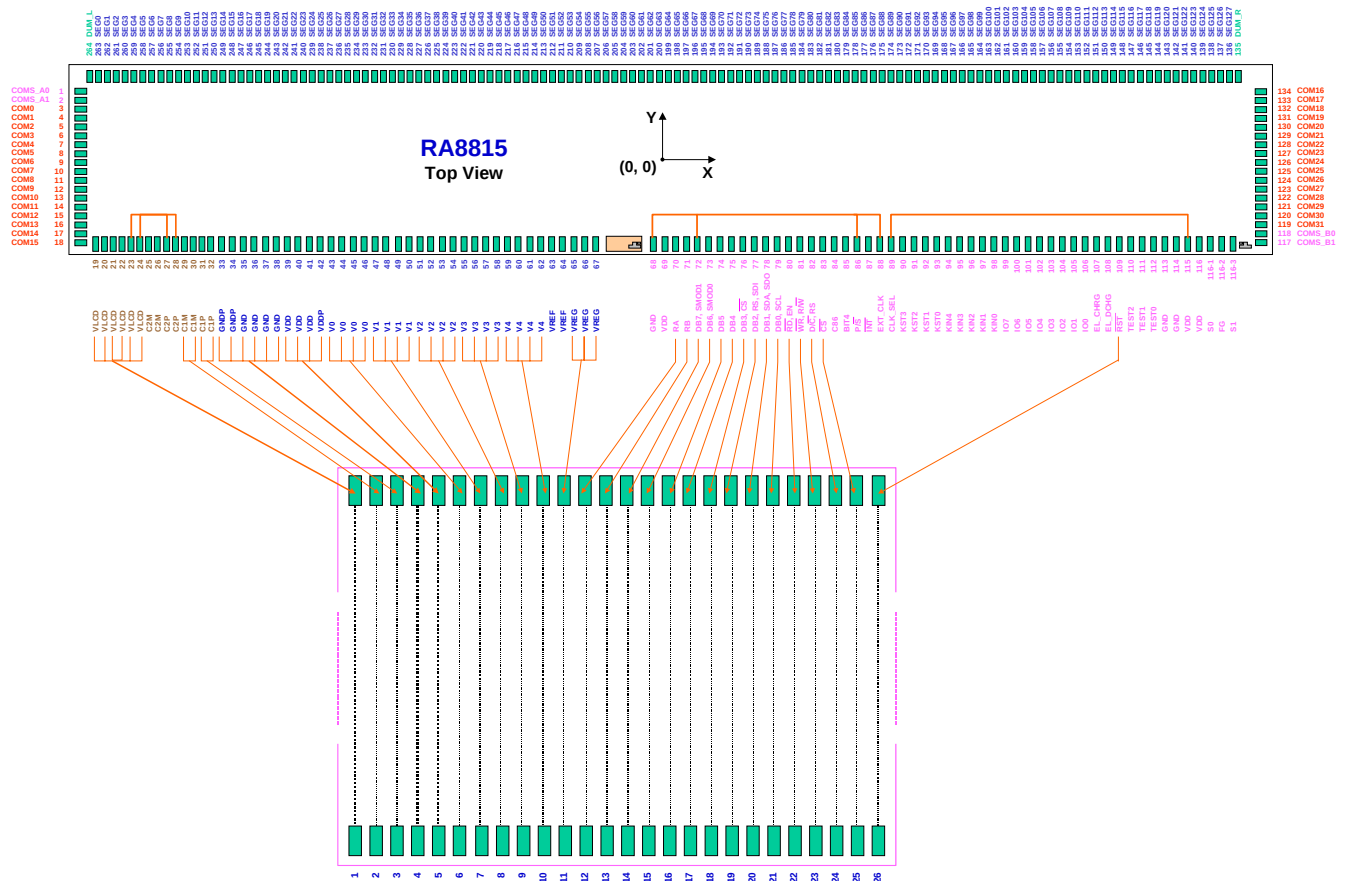


Figure A-1b: Basic Connection of Serial I/F

The RA8815 provide many interfaces for MPU that including parallel, 3-Wire serial and 4-Wire serial, and some useful I/O interface like I/O and Key-scan. Therefore there are many options for user to connect the COG die to FPC. The Figure A-1b is the basic connection of serial mode in COG module. If the MPC interface is serial mode, then these signals are necessary for FPC.

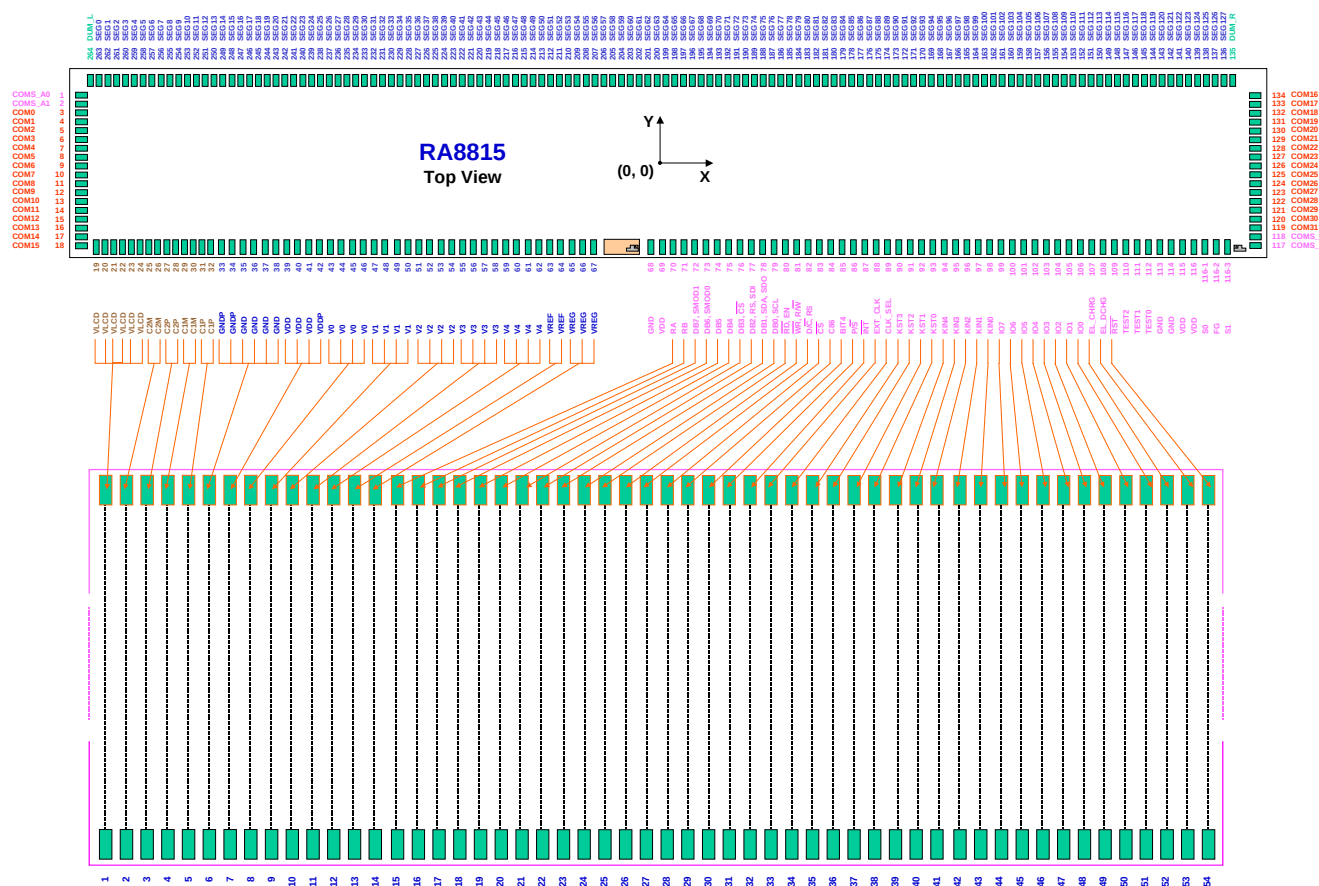
### A-1-2 Basic Connection of Parallel I/F



**Figure A-1c: Basic Connection of Parallel I/F**

The figure A-1c is the basic connection of parallel mode in COG module. If the MPC interface is parallel mode, then these signals are necessary for FPC.

### A-1-3 EPC Connection for Other Functions



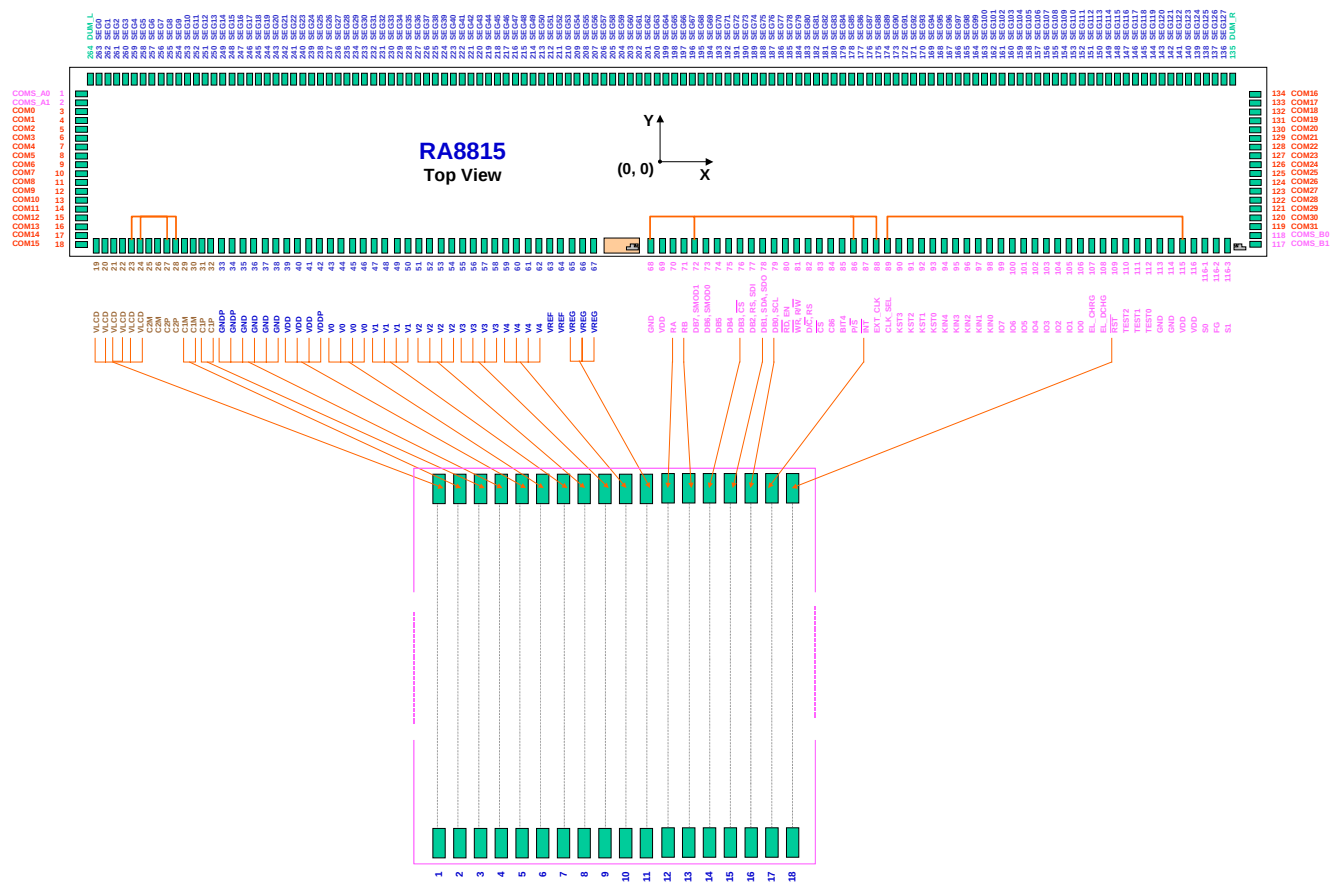
**Figure A-2 : Example(A) of FPC Connection**

As previous mention, the RA8815 provides many interfaces for MPU that including parallel, 3-Wire serial and 4-Wire serial, and some useful I/O interface like I/O and Key-scan. The Figure A-2 is an example for RA8815 COG die that connect all of the signals to FPC.

The RA8815 also provides two common outputs for Icon that let the panel layout easier to meet their application.

The Figure A-3 is a simple example that use serial 3-Wires, 2 times VDD, internal RC oscillator and interrupt signal. Therefore only 18pins used. But in this case, some signals(P/ $\overline{S}$ 、CLK\_SEL、EXT\_CLK) have to connect to VDD or GND directly through ITO resistance. If the system wants to use another features such as Key-scan, then the user have to connect the KIN[4:0] and KST[3:0] to FPC.

The pad number 68, 69, 113, 114, 115, 116 are VDD or GND. Their purposes are used to pull-up or pull-down for some signals on panel. They do not need to connect to FPC.



**Figure A-3 : Example(B) of COG Module**

The Figure A-4 is another example that uses 8080/8bit MPU, 2-times VDD, internal RC Oscillator, EL driver and interrupt signal. In this case, the FPC only uses 29pins. Some configure pin are connect to VDD or GND through ITO resistance, such as C86, BIT4, P/ $\overline{S}$ , CLK\_SEL and EXT\_CLK.

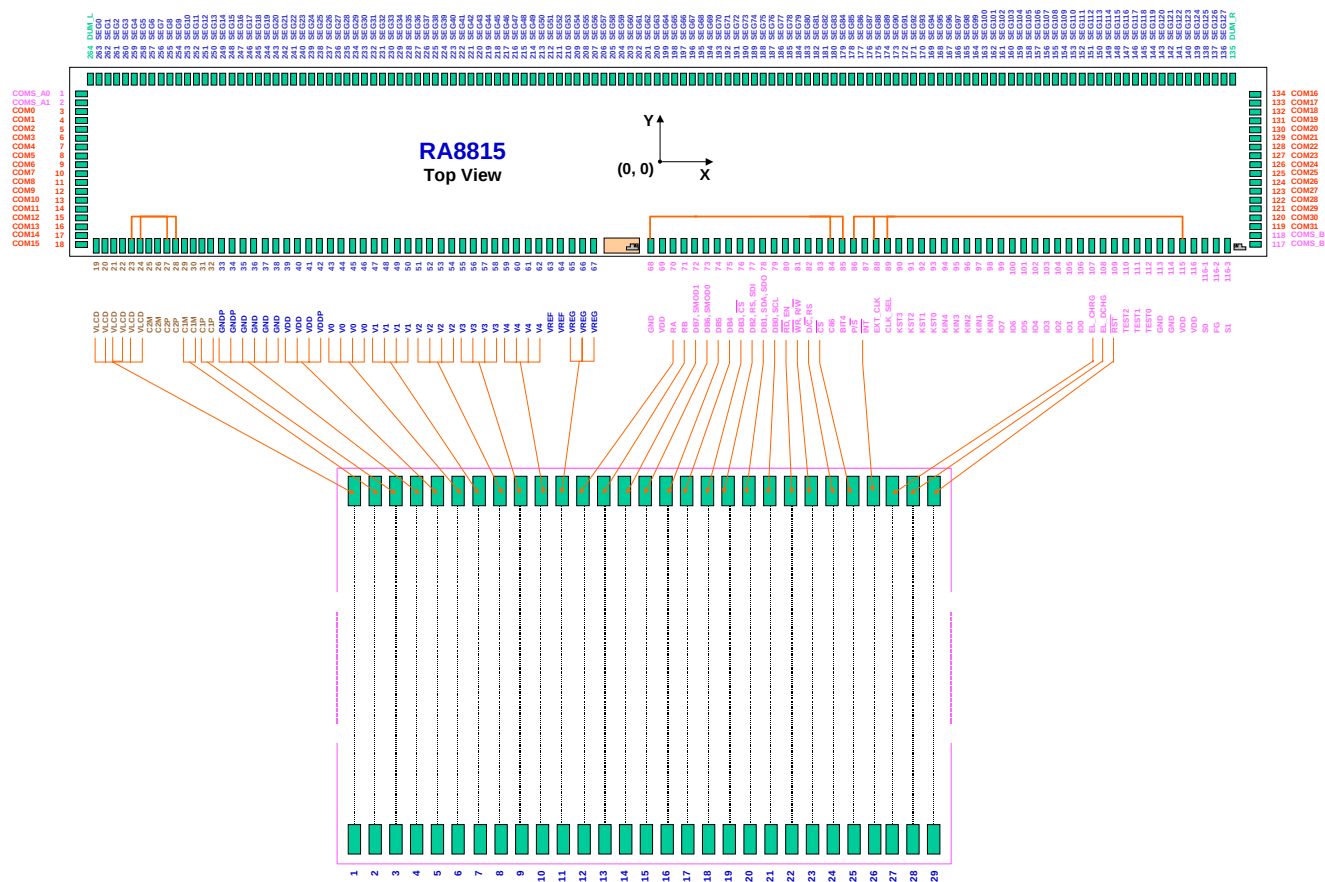
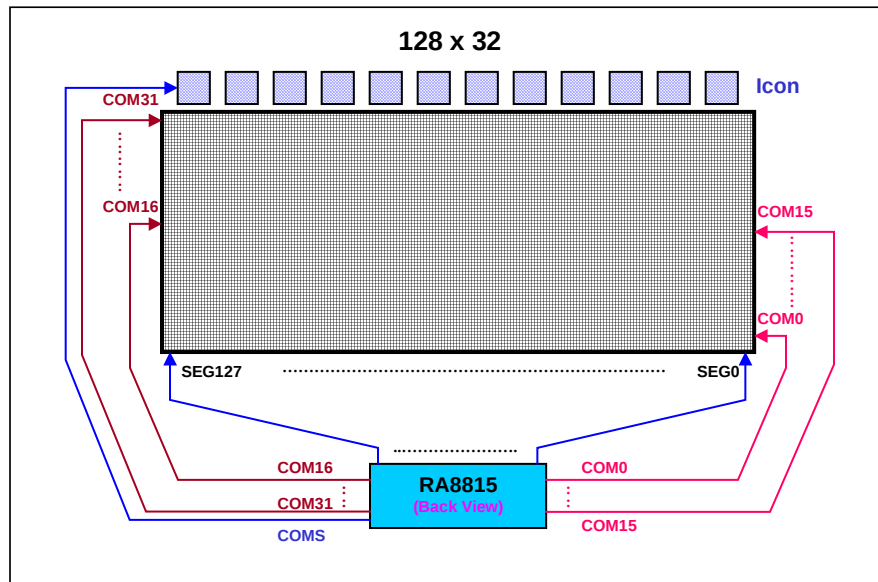


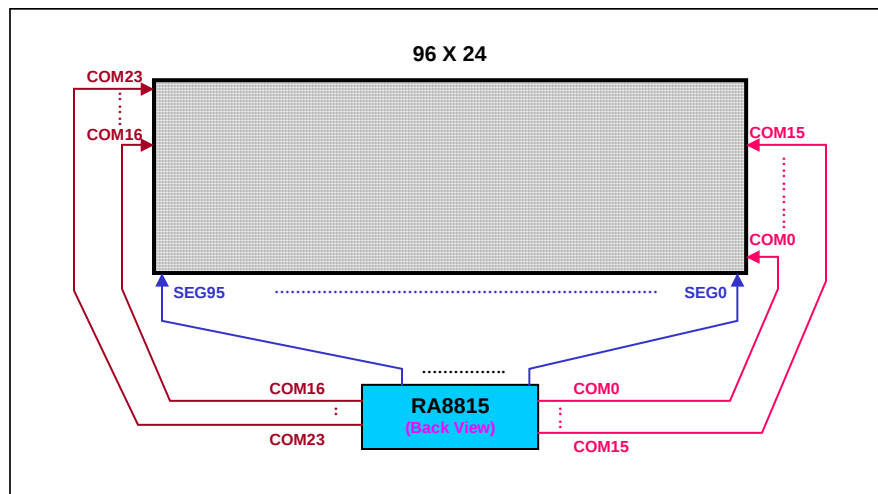
Figure A-4 : Example(C) of COG Module

The Figure A-5 is an example for RA8815 to connect the driver signals(COM/SEG) to LCD panel. In this case, the panel size is 128x32. If the Common of panel is less than 32, then care for the selection of Common. Because RA8815 supports text mode, so the user cannot separate the common willfully and connect them to panel.

Please note the COG is reverse and stamp on the glass, so the point of COM0/SEG0 is on the right-bottom corner. Refer to Figure A-5.



**Figure A-5: The Connection of RA8815 with LCD Panel(128x32)**



**Figure A-6: The Connection of RA8815 with LCD Panel(96x24)**

The Figure A-6 is an example of connection that use 96x24 panel. In this case, it supports one row for full size(16x16) and half-size(8x8) font. Or three rows for half-size(8x8) fonts. If the application of user is on graphics mode, then separate the common signal for same number and each size is 13 common signals.

## A-2 ITO

Table A-1: ITO Resistance of COG

| PAD Name   | ITO(Ohm) | PAD Name                            | ITO(Ohm) | PAD Name         | ITO(Ohm) |
|------------|----------|-------------------------------------|----------|------------------|----------|
| VDD , VDDP | 150      | C2P                                 | 200      | P/ $\bar{S}$     | 600      |
| GND , GNDP | 150      | C2M                                 | 200      | CLK_SEL          | 600      |
| VREF       | 200      | RA                                  | 200      | EXT_CLK          | 600      |
| VLCD       | 200      | RB                                  | 200      | KST[3..0]        | 600      |
| VREG       | 200      | DB[7:0]                             | 600      | KIN[4..0]        | 600      |
| V4         | 200      | $\overline{RD}$ , EN                | 600      | IO[7:0]          | 600      |
| V3         | 200      | $\overline{WR}$ , R/ $\overline{W}$ | 600      | EL_CHRG          | 600      |
| V2         | 200      | D/ $\overline{C}$ , RS              | 600      | EL_DCHG          | 600      |
| V1         | 200      | $\overline{CS}$                     | 600      | $\overline{RST}$ | 600      |
| V0         | 200      | $\overline{INT}$                    | 600      | TEST[2..0]       | 600      |
| C1P        | 200      | C86                                 | 600      |                  |          |
| C1M        | 200      | BIT4                                | 600      |                  |          |

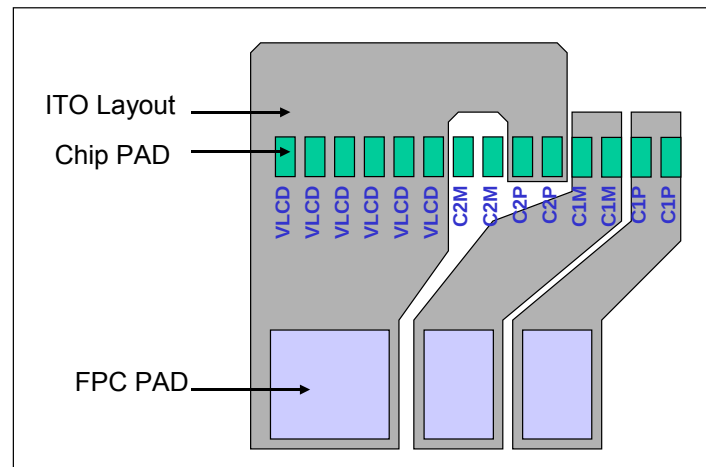
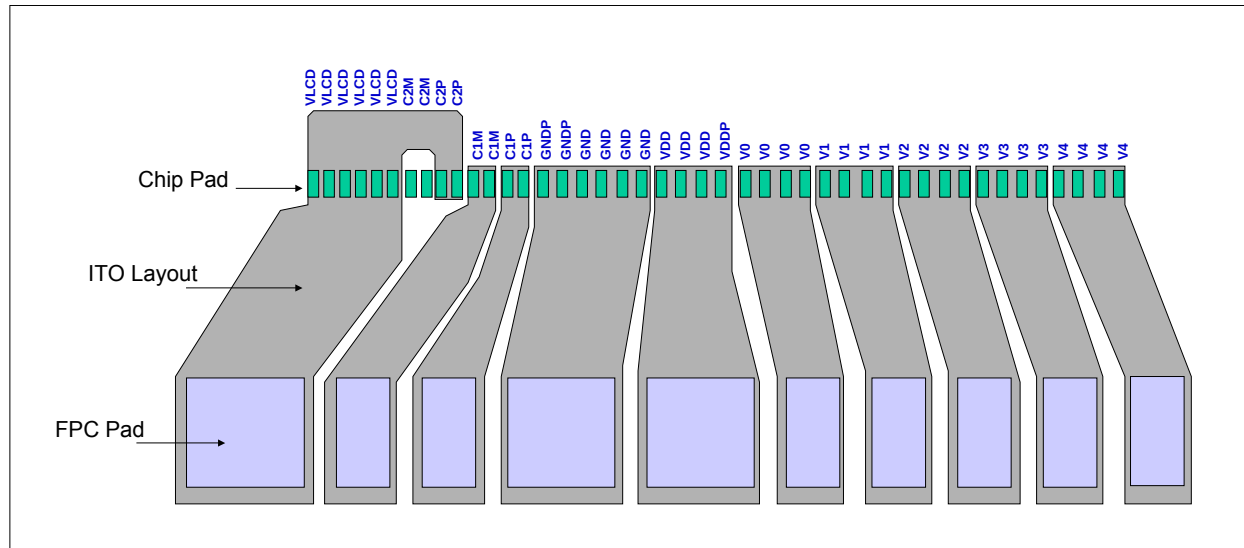


Figure A-7 : ITO Layout Example - VLCD(2\*VDD)

The RA8815 power signals (such as VDD, GND, VLCD, V[4:0], C1P, C1M) have to keep the smaller ITO resistance for panel layout. So the wires of layout need to keep as thick as possible to reduce the ITO resistance. The Figure A-7 is an example for VLCD layout of panel. Because the RA8815 provide six pads for VLCD, therefore the layout engineer has to connect all of these pads to FPC. In this case, the VLCD is two times of VDD, so the C2P have to connect to VLCD and do not forget keep the wire thicker.

The Figure A-8 is a layout example of RA8815 to FPC on COG module. The VDD and GND of RA8815 should as close as possible to FPC. The RA8815 provide six GND pad, user have to connect these six

pad to FPC with a thick wire. For the design of FPC, the related power signals(VDD, GND, VLCD) of layout need to keep as thick as possible to reduce the wire resistance. And the VDD, GND pad of FPC keep double width than other signals.



**Figure A-8 : ITO Layout Example**