Rockwell

R65/11EB and R65/11EAB Backpack Emulator

INTRODUCTION

The Rockwell R65/11EB and R65/11EAB Backpack Emulator are PROM prototyping versions of the 8-bit, masked-ROM R6500/11 and R6500/15 one-chip microcomputers. Like the R6500/11, the backpack device is totally upward/downward compatible with all members of the R6500/11 family. It is designed to accept standard 5-volt, 24-pin EPROMs or ROMs directly, in a socket on top of the Emulator. This packaging concept allows a standard EPROM to be easily removed, re-programmed, then reinserted as often as desired.

The backpack devices have the same pinouts as the masked-ROM R6500/11 and R6500/15 microcomputers. These 40 pins are functionally and operationally identical to the pins on the R6500/11. The R6500/11 Microcomputer Product Description (Order No. 2119) includes a description of the interface signals and their functions. Whereas the masked-ROM R6500/11 provides 3K bytes of read-only memory, the R65/11EB will address 4K bytes of external program memory. This extra memory accommodates program patches, test programs or optional programs during breadboard and prototype development states.

FEATURES

- PROM version of the R6500/11 and R6500/15
- Completely pin compatible with R6500/11 single-chip microcomputers
- Profile approaches 40-pin DIP of R6500/11
- Accepts 5 volt, 24-pin industry-standard EMPROMS—4K memories—2732, 2732A (4K bytes addressable)
- Use as prototyping tool or for low volume production
- 4K bytes of memory capacity
- 192 x 8 static RAM
- Separate power pin for 32 bytes of RAM
- Software compatibility with the R6500 family
- 32 bi-directional TTL compatible I/O lines (4 ports)
- Two 16-bit programmable counter/latches with six modes (interval timer, pulse generator, event counter, pulse width measurement, asymmetrical pulse generator, and retriggerable interval timer)
- 10 interrupts (reset, non-maskable, four external edge sensitive, 2 counters, serial data received, serial data transmitted)
- Crystal or external time base
- Single +5V power supply

Note: R6500/11 describes both R6500/11 and R6500/15.

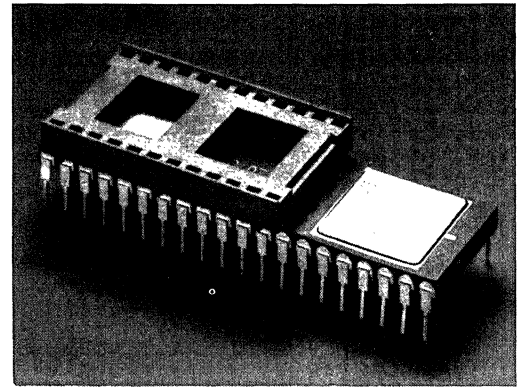
ORDERING INFORMATION

BACKPACK EMULATOR

Part Number	Memory Capacity	Compatible Memories	Temperature Range and Speed
R65/11EB	4K x 8	2732	0°C to 70°C 1 MHz
R65/11EAB	4K x 8	2732A	0°C to 70°C 2 MHz

SUPPORT PRODUCTS

Part Number	Description
RDC-3101	Low Cost Emulator (LCE) Development System
RDC-3030	LCE PROM Programmer Module
RDC-309	1 or 2-MHz R6500/11 Personality Module



R65/11EB Backpack Emulator

CONFIGURATIONS

The Backpack Emulator is available in two different versions, to accommodate 1 MHz and 2 MHz speeds. Both versions provide 192 bytes of RAM and I/O, as well as 24 signals to support the external memory "backpack" socket.

The emulator will relocate the EPROM address space to FXXX (see Memory Map). EPROM addresses FFA through FFF must contain the interrupt vectors.

EXTERNAL FREQUENCY REFERENCE

The external frequency reference may be a crystal or a clock. The R65/11EB and R65/11EAB divide the input clock by two regardless of the source.

I/O PORT PULLUPS

The devices have internal I/O port pull-up resistors on ports A, B, & C. Port D has push-pull drivers.

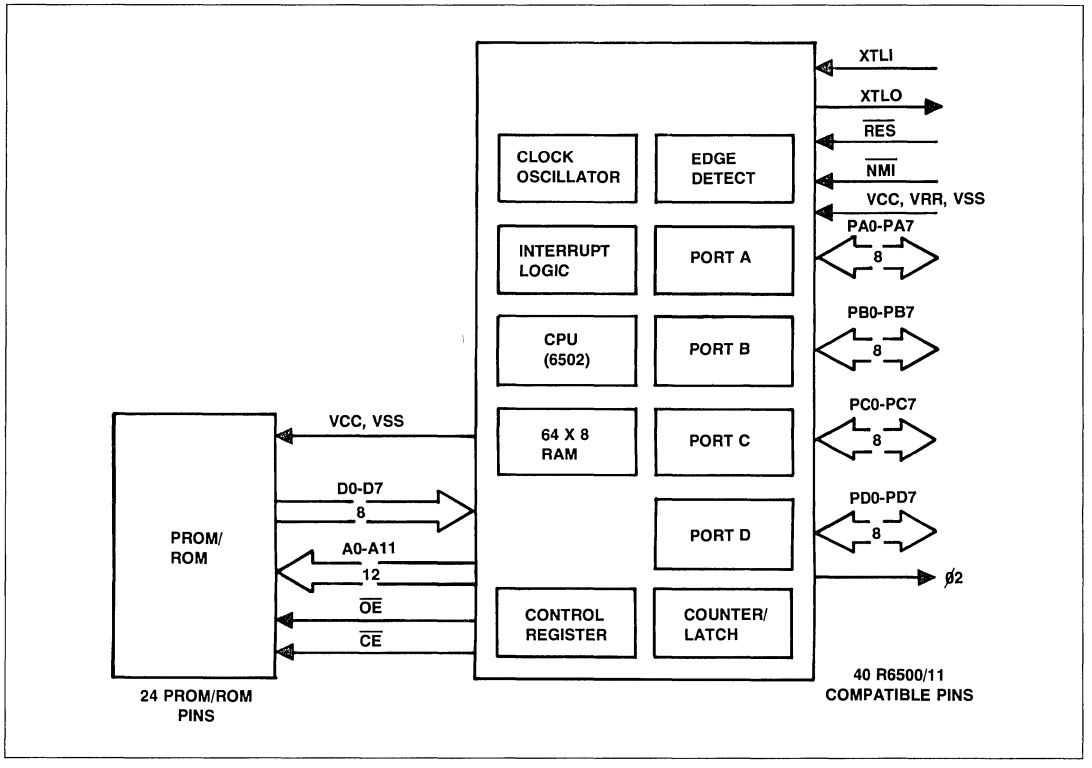
MODE CONTROL REGISTER

Bit 6 of the MODE CONTROL REGISTER (MCR6) must be set to 1 if Bit 7 (MCR7) is set to ϕ. (R65/11EB and R65/11EAB only).

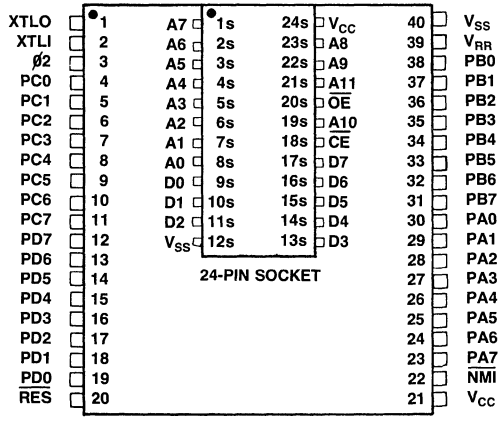
PRODUCT SUPPORT

The Backpack Emulator is just one of the products that Rockwell offers to facilitate system and program development for the R6500/11.

The Low Cost Emulator (LCE) Development System with R6500/11 Personality Module supports both hardware and software development. Complete in-circuit user emulation with the R6500/11 Personality Module allows total system test and evaluation. With the optional PROM Programmer, the LCE can also be used to program EPROMs for the development activity. When PROM programs have been finalized, the PROM device can be sent to Rockwell for masking into the 3K ROM of the R6500/11 or the 4K ROM of the R6500/15.



R65/11EB Interface Diagram



Pin Configuration

BACKPACK MEMORY SIGNAL DESCRIPTION

Signal Name	Pin No.	Description
D0–D7	9S–11S, 13S–17S	Data Bus Lines. All instruction and data transfers take place on the data bus lines. The buffers driving the data bus lines have full three-state capability. Each data bus pin is connected to an input and an output buffer, with the output buffer remaining in the floating condition.
A0–A7 A8, A9 A10 A11	1S–8A, 23S, 24S 19S 21S	Address Bus Lines. The address bus lines are buffered by push/pull type drivers that can drive one standard TTL load.
$\overline{CE}$	18S	Chip Enable. $\overline{CE}$ is active when the address is 8000-FFFF. This line can drive one TTL load.
$\overline{OE}$	20S	Memory Enable Line. This signal provides the output enable for the memory to place information on the data bus lines. This signal is driven by an inverted R/$\overline{W}$ signal from the CPU. It can drive 1 TTL load.
V_{CC}	24S	Main Power Supply +5V. This pin is tied directly to pin 21 (V_{CC}).
V_{SS}	12S	Signal and Power Ground (zero volts). This pin is tied directly to pin 40 (V_{SS}).

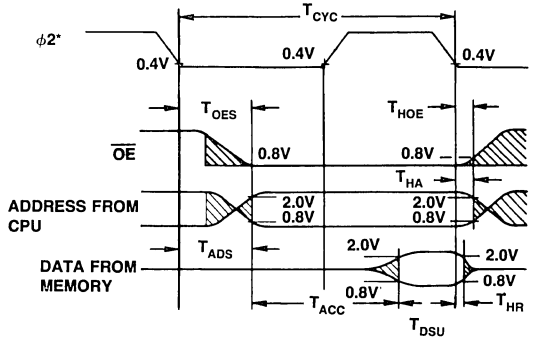
I/O AND INTERNAL REGISTER ADDRESSES

Address (Hex)	Read	Write
001F	— —	— —
1E	Lower Counter B	Upper Latch B, Cntr B←Latch B, CLR Flag
1D	Upper Counter B	Upper Latch B, Latch C←Latch B
1C	Lower Counter B, CLR Flag	Lower Latch B
1B	— —	— —
1A	Lower Counter A	Upper Latch A, Cntr A←Latch A, CLR Flag
19	Upper Counter A	Upper Latch A
18	Lower Conter A, CLR Flag	Lower Latch A
17	Serial Receiver Data Register	Serial Transmitter Data Register
16	Serial Comm. Status Register	Serial Comm. Status Reg. Bits 4 & 5 only
15	Serial Comm. Control Register	Serial Comm. Control Register
14	Mode Control Register	Mode Control Register
13	— —	— —
12	Interrupt Enable Register	Interrupt Enable Register
11	Interrupt Flag Register	— —
0010	Read FF	Clear Int Flag (Bits 0-3 only, Write 0's only)
04 thru 0F	— —	— —
03	Port D	Port D
02	Port C	Port C
01	Port B	Port B
0000	Port A	Port A

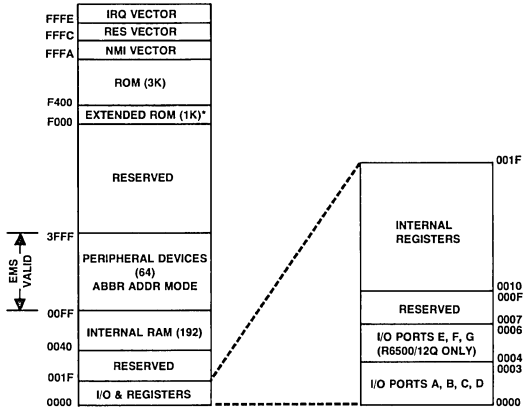
READ TIMING CHARACTERISTICS

Signal	Symbol	1 MHz		2 MHz		Unit
		Min.	Max.	Min.	Max.	
$\overline{OE}$ and $\overline{CE}$ setup time from CPU	T_{OES}	—	225	—	140	ns
Address setup time from CPU	T_{ADS}	—	150	—	75	ns
Memory read access time	T_{ACC}	—	700	—	315	ns
Data set up time	T_{DSU}	50	—	35	—	ns
Data hold time—Read	T_{HR}	10	—	10	—	ns
Address hold time	T_{HA}	30	—	30	—	ns
$\overline{OE}$ and $\overline{CE}$ hold time	T_{HOE}	30	—	30	—	ns
Cycle Time	T_{CYC}	1.0	10.0	0.5	10.0	μs

READ TIMING WAVEFORMS

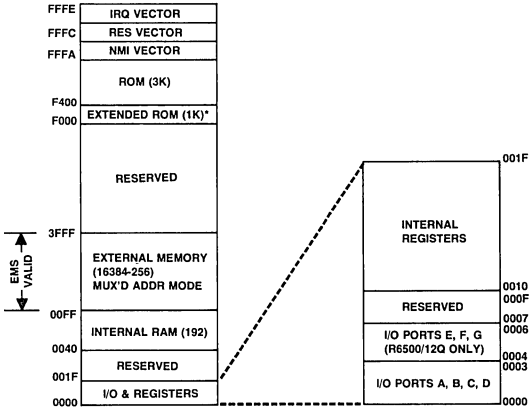


ABBREVIATED MODE MEMORY MAP



*NOT AVAILABLE FOR MASKED ROM R6500/11.

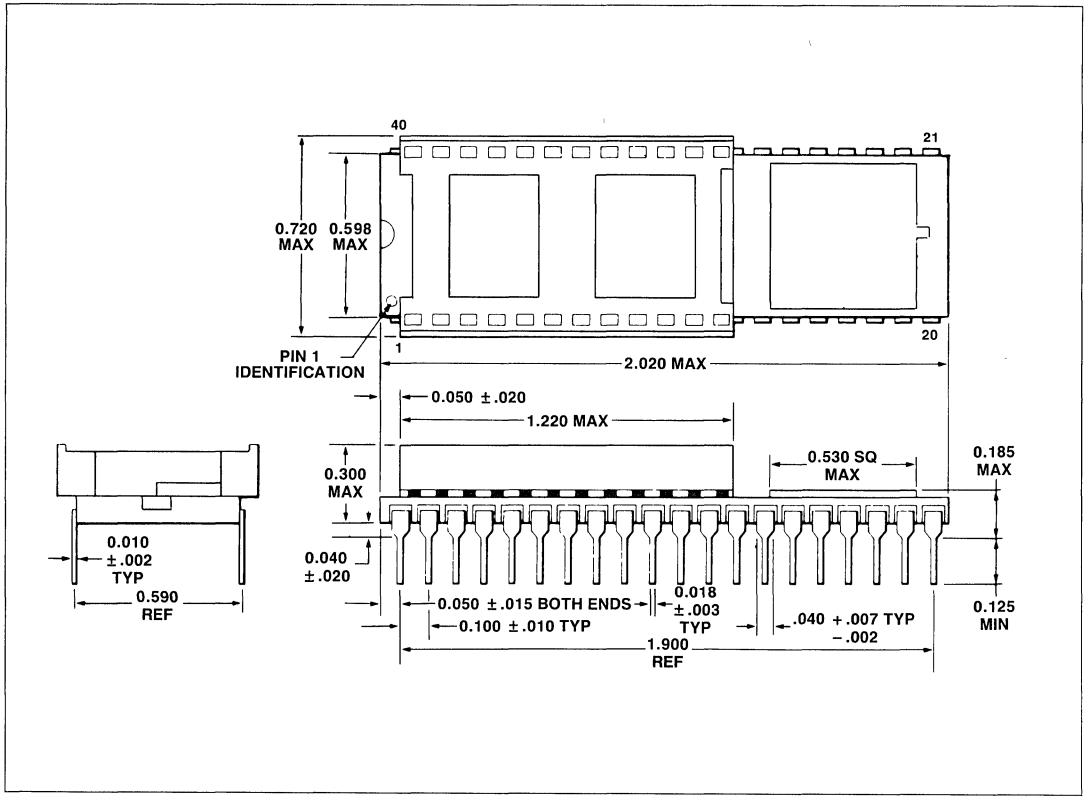
MULTIPLEXED MODE MEMORY MAP



ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = 0°C to 70°C, unless otherwise stated)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Conditions
Input High Threshold Voltage D0-D7	V_{IHT}	+2.0	—	—	Vdc	
Input Low Threshold Voltage D0-D7	V_{ILT}	—	—	+0.8	Vdc	
Three-State (Off State) Input Current D0-D7	I_{TSI}	—	—	±10	μA	V_{CC} = 5.25V V_{IN} = 0.4V to 2.4V
Output High Voltage D0-D7, A0-A11, $\overline{OE}$, $\overline{CE}$	V_{OH}	+2.4	—	—	Vdc	V_{CC} = 4.75V I_{LOAD} = 100μA
Output Low Voltage D0-D7, A0-A11 $\overline{OE}$, $\overline{CE}$	V_{OL}	—	—	+0.4	Vdc	V_{CC} = 4.75V I_{LOAD} = 1.6mA
Power Dissipation (less EPROM)	P_D	—	0.80	1.20	W	
Output Capacitance (High Impendance State) D0-D7	C_{OUT}	—	—	10	pF	T_A = 25°C V_{IN} = 0V f = 1 MHz
Input Capacitance	C_{IN}	—	—	10	pF	
I/O Port Pull-up Resistance	R_L	3.0	6.0	11.5	kohm	



40-Pin Backpack Package