RENESAS

RL78/L1A

RENESAS MCU

Integrated LCD controller/driver, 12-bit resolution A/D Converter, 12-bit resolution D/A Converter, Operational amplifier, Internal reference voltage for A/D and D/A converters. True Low Power Platform (as low as 70.8 µA/MHz, and 0.68 µA in Halt mode(RTC2 + LVD)), 1.8 V to 3.6 V operation, 48 to 128 Kbyte Flash, 33 DMIPS at 24 MHz, for All LCD Based Applications.

1. OUTLINE

1.1 Features

○ Ultra-low power consumption technology
- V_{DD} = single power supply voltage of 1.8 to 3.6 V
- HALT mode
- STOP mode
- SNOOZE mode

○ RL78 CPU core
- CISC architecture with 3-stage pipeline
- Minimum instruction execution time: Can be changed from high speed (0.04167 µs: @ 24 MHz operation with high-speed on-chip oscillator clock) to ultra-low speed (30.5 µs: @ 32.768 kHz operation with subsystem clock)
- Multiply/divide and multiply/accumulate instructions are supported.
- Address space: 1 MB
- General-purpose registers: (8-bit register × 8) × 4 banks
- On-chip RAM: 5.5 KB

○ Code flash memory
- Code flash memory: 48 to 128 KB
- Block size: 1 KB
- Prohibition of block erase and rewriting (security function)
- On-chip debug function
- Self-programming (with boot swap function/flash shield window function)

○ Data flash memory
- Data flash memory: 8 KB
- Background operation (BGO): Instructions can be executed from the program memory while rewriting the data flash memory.
- Number of rewrites: 1,000,000 times (TYP.)
- Voltage of rewrites: V_{DD} = 1.8 to 3.6 V

○ High-speed on-chip oscillator
- Select from 24 MHz, 16 MHz, 12 MHz, 8 MHz, 6 MHz, 4 MHz, 3 MHz, 2 MHz, and 1 MHz
- High accuracy: ±1.0% (V_{DD} = 1.8 to 3.6 V, T_A = -20 to +85°C)

○ Operating ambient temperature
- T_A = -40 to +85°C (A: Consumer applications)

○ Power management and reset function
- On-chip power-on-reset (POR) circuit
- On-chip voltage detector (LVD) (Select interrupt and reset from 10 levels)

○ Data transfer controller (DTC)
- Transfer modes: Normal transfer mode, repeat transfer mode, block transfer mode
- Activation sources: Activated by interrupt sources (30 sources).
- Chain transfer function

○ Event link controller (ELC)
- Event signals of 22 types can be linked to the specified peripheral function.

○ Serial interfaces
- CSI/CSI (SPI supported): 4 channels
- UART: 4 channels
- I^2C/simplified I^2C: 5 channels

○ Timers
- 16-bit timer: 8 channels
- 8-bit timer: 2 channels
- 12-bit interval timer: 1 channel
- Real-time clock 2: 1 channel (calendar for 99 years, alarm function, and clock correction function)
- Watchdog timer: 1 channel (operable with the dedicated low-speed on-chip oscillator)

○ LCD controller/driver
- Internal voltage boosting method, capacitor split method, and external resistance division method are switchable.
- Segment signal output: 32 (28) to 45 (41) [Note 1]
- Common signal output: 4 (8) [Note 1]

○ A/D converter
- 12-bit resolution A/D converter (1.8 V ≤ AV_{DD} ≤ V_{DD} ≤ 3.6 V)
- Analog input: 10 to 15 channels (including a dedicated one for internal 1/2 AV_{DD})
- Internal reference voltage (TYP. 1.45 V) and temperature sensor [Note 2]

○ D/A converter
- 12-bit resolution D/A converter (1.8 V ≤ AV_{DD} ≤ V_{DD} ≤ 3.6 V)
- Analog output: 2 channels
- Output voltage: 0.35 V to AV_{DD} − 0.47 V

○ Voltage reference
- The output voltage can be selected from among 1.5 V (typ.), 1.8 V (typ.), 2.048 V (typ.), and 2.5 V (typ.).
- Can be used as the internal reference voltage for A/D and D/A converters.

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○ Comparator
- 1 channel
- Operating modes: Comparator high-speed mode, comparator low-speed mode, window mode
- The external reference voltage or internal reference voltage can be selected as the reference voltage.

○ Operational amplifier
- General-purpose operational amplifier: 1 channel
- Rail-to-rail operational amplifier with analog MUX: 2 channels

○ I/O ports
- I/O ports: 59 to 79 (N-ch open drain I/O [withstand voltage of 6 V]: 2)
- Can be set to N-ch open drain, TTL input buffer, and on-chip pull-up resistor
- On-chip key interrupt function
- On-chip clock output/buzzer output controller

○ Others
- On-chip BCD (binary-coded decimal) correction circuit

Note 1. The number in parentheses indicates the number of signal outputs when 8 coms are used.

Note 2. Selectable only in HS (high-speed main) mode.

Remark The functions mounted depend on the product. See **1.6 Outline of Functions**.

○ ROM, RAM capacities

Flash ROM	Data Flash	RAM	RL78/L1A	
			80 pins	100 pins
128 KB	8 KB	5.5 KB	—	R5F11MPG
96 KB	8 KB	5.5 KB	R5F11MMF	R5F11MPF
64 KB	8 KB	5.5 KB	R5F11MME	R5F11MPE
48 KB	8 KB	5.5 KB	R5F11MMD	—

1.2   Ordering Information

Pin Count	Package	Fields of Application	Orderable Part Number
80 pins	80-pin plastic LFQFP (12 × 12 mm, 0.5 mm pitch)	A	R5F11MMDAFB#30, R5F11MMEAFB#30, R5F111MFAFB#30 R5F11MMDAFB#50, R5F11MMEAFB#50, R5F11MMFAFB#50
100 pins	100-pin plastic LFQFP (14 × 14 mm, 0.5 mm pitch)	A	R5F11MPEAFB#30, R5F11MPFAFB#30, R5F11MPGAFB#30 R5F11MPEAFB#50, R5F11MPFAFB#50, R5F11MPGAFB#50

Figure 1 - 1 Part Number, Memory Size, and Package of RL78/L1A

Part No. R 5 F 1 1 M P E A x x x F B # 3 0

Packaging specification:
    #30: Tray
    #50: Embossed Tape

Package type:
    FB: LFQFP, 0.50 mm pitch

ROM number (Omitted with blank products)

Fields of application:
    A: Consumer applications, T_A = -40 to +85°C

ROM capacity:
    D: 48 KB
    E: 64 KB
    F: 96 KB
    G: 128 KB

Pin count:
    M: 80-pin
    P: 100-pin

RL78/L1A Group
    11M: RL78/L1A

Memory type:
    F: Flash memory

Renesas MCU

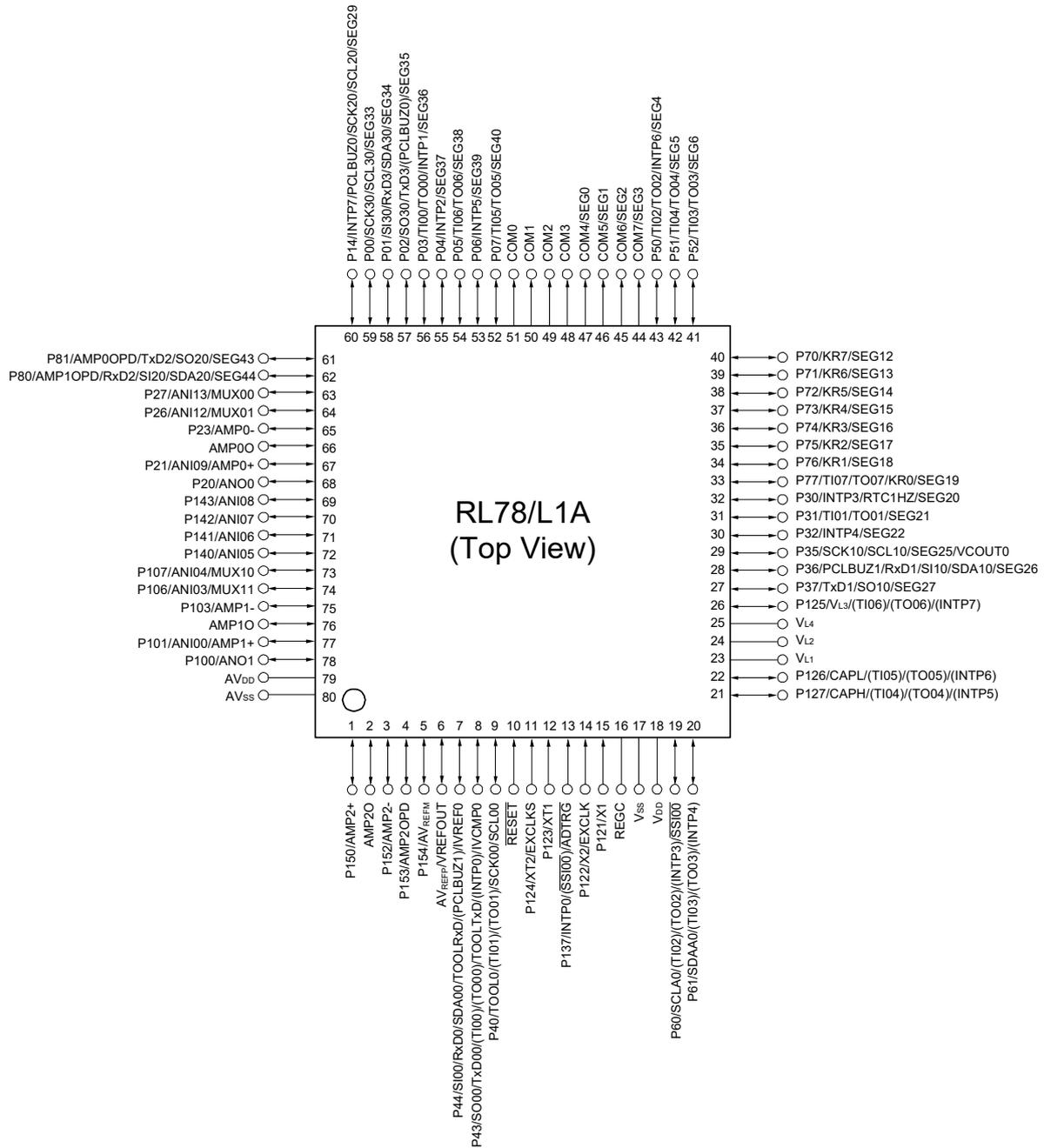Renesas semiconductor product

Caution   Orderable part numbers are current as of when this manual was published.
                Please make sure to refer to the relevant product page on the Renesas website for the latest part numbers.

1.3   Pin Configuration (Top View)

1.3.1   80-pin products

• 80-pin plastic LFQFP (fine pitch) (12 × 12 mm, 0.5 mm pitch)

Caution   Connect the REGC pin to VSS pin via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see **1.4 Pin Identification**.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.3.2   100-pin products

• 100-pin plastic LFQFP (fine pitch) (14 × 14 mm, 0.5 mm pitch)
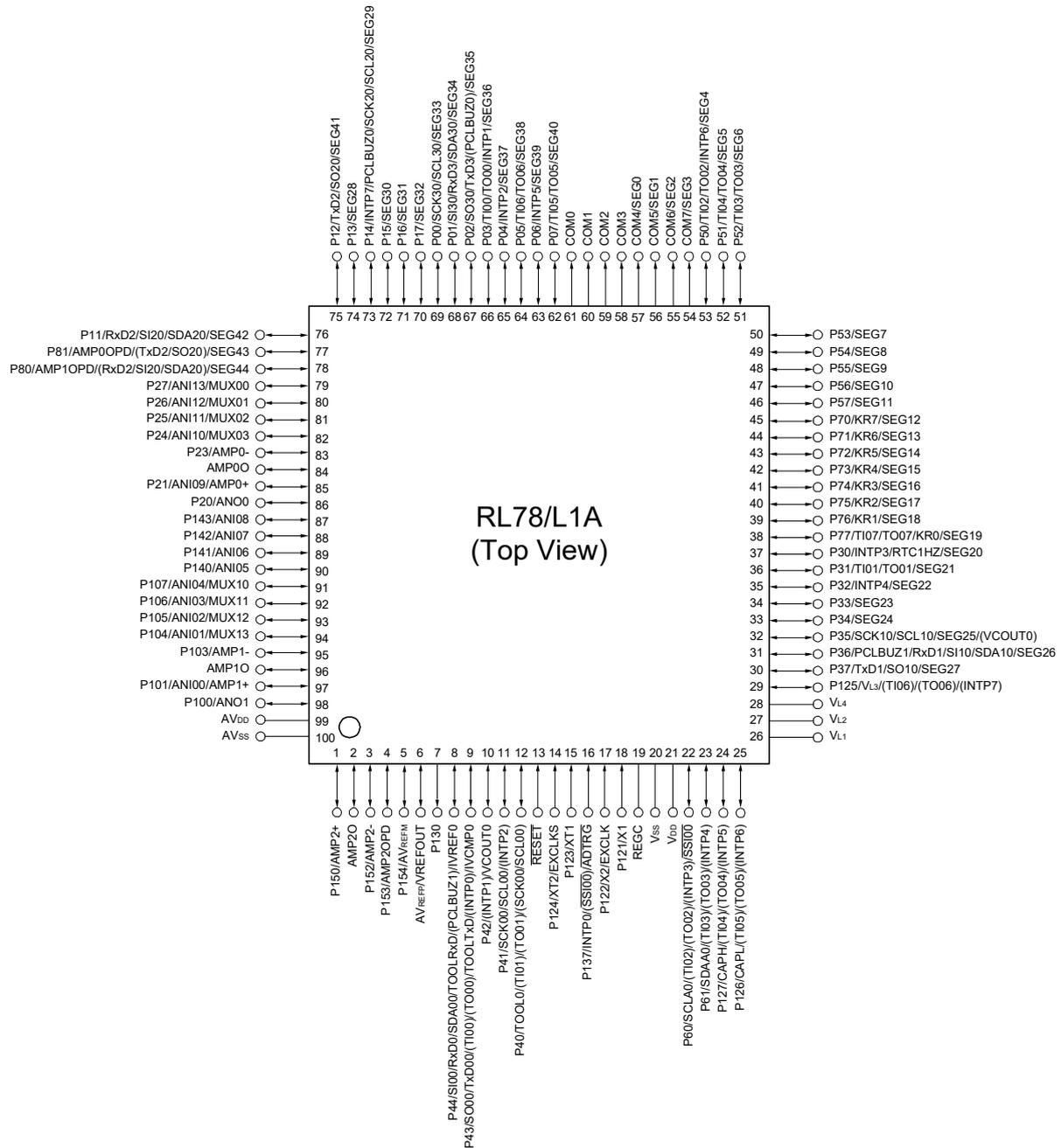

RL78/L1A
(Top View)

Caution   Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see **1.4 Pin Identification**.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).
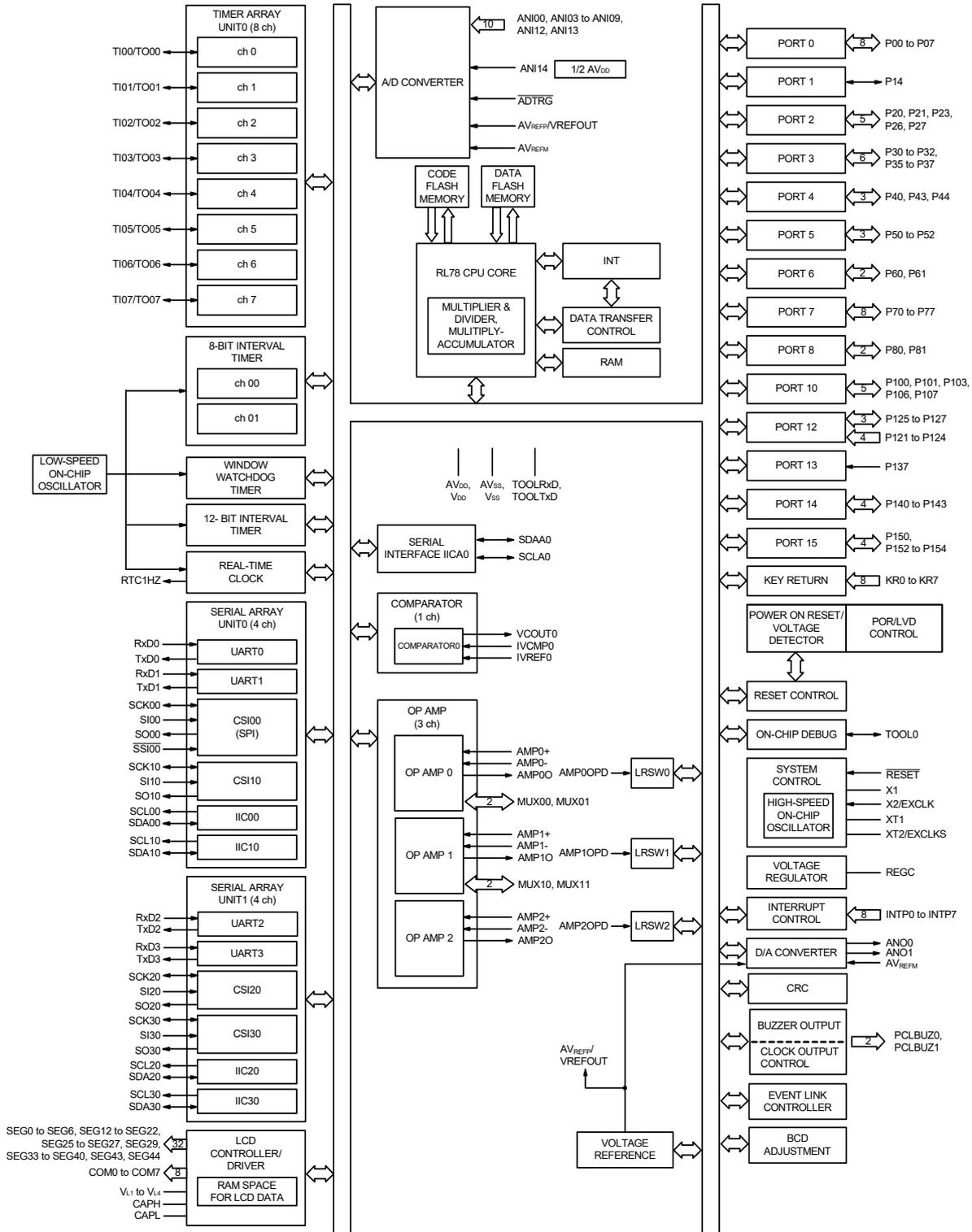
<R>   ## 1.4   Pin Identification

AMP0+ to AMP2+	: OP AMP + Input	PCLBUZ0, PCLBUZ1	: Programmable Clock Output/
AMP0- to AMP2-	: OP AMP - Input		Buzzer Output
AMP0O to AMP2O	: OP AMP Output	REGC	: Regulator Capacitance
AMP0OPD to	: Low Resistance Switch	$\overline{\text{RESET}}$	: Reset
AMP2OPD		RTC1HZ	: Real-time Clock Correction
$\overline{\text{ADTRG}}$	: A/D External Trigger Input	RxD0 to RxD3	: Receive Data
ANI00 to ANI13	: Analog Input	SCK00, SCK10, SCK20,	: Serial Clock Input/Output
ANO0, ANO1	: Analog Output	SCK30	
AVDD	: Analog Power Supply	SCLA0	: Serial Clock Input/Output
AVREFM	: Analog Reference Voltage	SCL00, SCL10, SCL20, SCL30	: Serial Clock Output
	Minus	SDAA0, SDA00, SDA10,	: Serial Data Input/Output
AVREFP	: Analog Reference Voltage	SDA20, SDA30	
	Plus	SEG0 to SEG44	: LCD Segment Output
AVSS	: Analog Ground	SI00, SI10, SI20, SI30	: Serial Data Input
CAPH, CAPL	: Capacitor for LCD	SO00, SO10, SO20, SO30	: Serial Data Output
COM0 to COM7	: LCD Common Output	$\overline{\text{SSI00}}$	: Slave Select Input
EXCLK	: External Clock Input	TI00 to TI07	: Timer Input
	(Main System Clock)	TO00 to TO07	: Timer Output
EXCLKS	: External Clock Input	TOOL0	: Data Input/Output for Tool
	(Sub System Clock)	TOOLRxD, TOOLTxD	: Data Input/Output for
INTP0 to INTP7	: External Interrupt Input		External Device
IVCMP0	: Comparator Input	TxD0 to TxD3	: Transmit Data
IVREF0	: Comparator Reference Input	VCOUT0	: Comparator Output
KR0 to KR7	: Key Return	VDD	: Power Supply
MUX00 to MUX03,	: OP AMP output analog MUX	VL1 to VL4	: LCD Power Supply
MUX10 to MUX13	switch	VREFOUT	: Analog Reference Voltage
P00 to P07	: Port 0		Output
P11 to P17	: Port 1	VSS	: Ground
P20, P21 P23 to P27	: Port 2	X1, X2	: Crystal Oscillator
P30 to P37	: Port 3		(Main System Clock)
P40 to P44	: Port 4	XT1, XT2	: Crystal Oscillator
P50 to P57	: Port 5		(Subsystem Clock)
P60, P61	: Port 6		
P70 to P77	: Port 7		
P80, P81	: Port 8		
P100, P101	: Port 10		
P103 to P107			
P121 to P127	: Port 12		
P130, P137	: Port 13		
P140 to P143	: Port 14		
P150, P152 to P154	: Port 15		

1.5 Block Diagram

<R>   ### 1.5.1 80-pin products

<R> ## 1.5.2 100-pin products

TIMER ARRAY UNIT0 (8 ch)

TI00/TO00 — ch 0
TI01/TO01 — ch 1
TI02/TO02 — ch 2
TI03/TO03 — ch 3
TI04/TO04 — ch 4
TI05/TO05 — ch 5
TI06/TO06 — ch 6
TI07/TO07 — ch 7

8-BIT INTERVAL TIMER
ch 00
ch 01

LOW-SPEED ON-CHIP OSCILLATOR

WINDOW WATCHDOG TIMER

12- BIT INTERVAL TIMER

RTC1HZ — REAL-TIME CLOCK

SERIAL ARRAY UNIT0 (4 ch)
RxD0 / TxD0 — UART0
RxD1 / TxD1 — UART1
SCK00 / SI00 / SO00 / SSI00 — CSI00 (SPI)
SCK10 / SI10 / SO10 — CSI10
SCL00 / SDA00 — IIC00
SCL10 / SDA10 — IIC10

SERIAL ARRAY UNIT1 (4 ch)
RxD2 / TxD2 — UART2
RxD3 / TxD3 — UART3
SCK20 / SI20 / SO20 — CSI20
SCK30 / SI30 / SO30 — CSI30
SCL20 / SDA20 — IIC20
SCL30 / SDA30 — IIC30

SEG0 to SEG44 — 45 — LCD CONTROLLER/ DRIVER
COM0 to COM7 — 8
V_{L1} to V_{L4} / CAPH / CAPL — RAM SPACE FOR LCD DATA

A/D CONVERTER
14 — ANI00 to ANI13
ANI14 — 1/2 AV_{DD}
ADTRG
AV_{REFP}/VREFOUT
AV_{REFM}

CODE FLASH MEMORY
DATA FLASH MEMORY

RL78 CPU CORE
MULTIPLIER & DIVIDER, MULITIPLY-ACCUMULATOR

INT
DATA TRANSFER CONTROL
RAM

AV_{DD}, V_{DD} / AV_{SS}, V_{SS} / TOOLRxD, TOOLTxD

SERIAL INTERFACE IICA0 — SDAA0 / SCLA0

COMPARATOR (1 ch)
COMPARATOR0 — VCOUT0 / IVCMP0 / IVREF0

OP AMP (3 ch)
OP AMP 0 — AMP0+ / AMP0- / AMP0O
4 — MUX00 to MUX03
OP AMP 1 — AMP1+ / AMP1- / AMP1O
4 — MUX10 to MUX13
OP AMP 2 — AMP2+ / AMP2- / AMP2O

AMP0OPD — LRSW0
AMP1OPD — LRSW1
AMP2OPD — LRSW2

AV_{REFP}/ VREFOUT

VOLTAGE REFERENCE

PORT 0 — 8 — P00 to P07
PORT 1 — 7 — P11 to P17
PORT 2 — P20, P21 P23 to P27
PORT 3 — 8 — P30 to P37
PORT 4 — 5 — P40 to P44
PORT 5 — 8 — P50 to P57
PORT 6 — 2 — P60, P61
PORT 7 — 8 — P70 to P77
PORT 8 — 2 — P80, P81
PORT 10 — 7 — P100, P101, P103 to P107
PORT 12 — 3 — P125 to P127 / 4 — P121 to P124
PORT 13 — P130 / P137
PORT 14 — 4 — P140 to P143
PORT 15 — 4 — P150, P152 to P154
KEY RETURN — 8 — KR0 to KR7

POWER ON RESET/ VOLTAGE DETECTOR — POR/LVD CONTROL

RESET CONTROL

ON-CHIP DEBUG — TOOL0

SYSTEM CONTROL
HIGH-SPEED ON-CHIP OSCILLATOR
RESET / X1 / X2/EXCLK / XT1 / XT2/EXCLKS

VOLTAGE REGULATOR — REGC

INTERRUPT CONTROL — 8 — INTP0 to INTP7

D/A CONVERTER — ANO0 / ANO1 / AV_{REFM}

CRC

BUZZER OUTPUT CLOCK OUTPUT CONTROL — 2 — PCLBUZ0, PCLBUZ1

EVENT LINK CONTROLLER

BCD ADJUSTMENT

1.6   Outline of Functions

[80-pin, 100-pin products]   **(1/2)**

Item		80-pin	100-pin
		R5F11MMx (x = D to F)	R5F11MPx (x = E to G)
Code flash memory (KB)		48 to 96	64 to 128
Data flash memory (KB)		8	8
RAM (KB)		5.5	5.5
Memory space		1 MB	
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) 1 to 20 MHz: VDD = 2.7 to 3.6 V, 1 to 8 MHz: VDD = 1.8 to 2.7 V	
	High-speed on-chip oscillator clock	HS (high-speed main) operation mode: 1 to 24 MHz (VDD = 2.7 to 3.6 V), HS (high-speed main) operation mode: 1 to 16 MHz (VDD = 2.4 to 3.6 V), LS (low-speed main) operation mode: 1 to 8 MHz (VDD = 1.8 to 3.6 V)	
Subsystem clock		XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz (TYP.): VDD = 1.8 to 3.6 V	
Low-speed on-chip oscillator clock		15 kHz (TYP.): VDD = 1.8 to 3.6 V	
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)	
Minimum instruction execution time		0.04167 μs (High-speed on-chip oscillator clock: fHOCO = fIH = 24 MHz operation)	
		0.05 μs (High-speed system clock: fMX = 20 MHz operation)	
		30.5 μs (Subsystem clock: fSUB = 32.768 kHz operation)	
Instruction set		• Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits, 16 bits × 16 bits), Division (16 bits ÷ 16 bits, 32 bits ÷ 32 bits) • Multiplication and Accumulation (16 bits × 16 bits + 32 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.	
I/O port	Total	59	79
	CMOS I/O	52	71
	CMOS input	5	5
	CMOS output	0	1
	N-ch open-drain I/O (6 V tolerance)	2	2
Timer	16-bit timer TAU	8 channels (Timer outputs: 8, PWM outputs: 7 Note)	
	8-bit or 16-bit interval timer	2 channels (8 bits) / 1 channel (16 bits)	
	Watchdog timer	1 channel	
	12-bit interval timer	1 channel	
	Real-time clock 2	1 channel	
	RTC output	1 1 Hz (subsystem clock: fSUB = 32.768 kHz)	

Note   The number of outputs varies, depending on the setting of channels in use and the number of the master.

(2/2)

Item	80-pin	100-pin
	R5F11MMx (x = D to F)	R5F11MPx (x = E to G)
Clock output/buzzer output	2	2
	• 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: fMAIN = 20 MHz operation) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: fSUB = 32.768 kHz operation)	
12-bit resolution A/D converter	10 channels	14 channels
12-bit resolution D/A converter	2 channels	2 channels
VREFOUT (voltage reference)	2.5 V/2.048 V/1.8 V/1.5 V	
Operational amplifier	3 channels	3 channels
AMPnO with analog MUX switch	2 channels (2 in-out/channel)	2 channels (4 in-out/channel)
Comparator	1 channel	1 channel
Serial interface	• CSI (SPI supported): 1 channel/UART (LIN-bus supported): 1 channel/simplified I^{2}C: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I^{2}C: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I^{2}C: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I^{2}C: 1 channel	
I^{2}C bus	1 channel	1 channel
LCD controller/driver	Internal voltage boosting method, capacitor split method, and external resistance division method are switchable.	
Segment signal output	32 (28) [Note 1]	45 (41) [Note 1]
Common signal output	4 (8) [Note 1]	
Data transfer controller (DTC)	30 sources	30 sources
Event link controller (ELC)	Event input: 22, Event trigger output: 8	Event input: 22, Event trigger output: 8
Vectored interrupt sources Internal	31	31
External	9	9
Key interrupt	8	8
Reset	• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution [Note 2] • Internal reset by RAM parity error • Internal reset by illegal-memory access	
Power-on-reset circuit	• Power-on-reset: 1.51 ±0.04 V • Power-down-reset: 1.50 ±0.04 V	
Voltage detector	• Rising edge: 1.88 V to 3.13 V (10 stages) • Falling edge: 1.84 V to 3.06 V (10 stages)	
On-chip debug function	Provided	
Power supply voltage	VDD = 1.8 to 3.6 V	
Operating ambient temperature	TA = -40 to +85°C (A: Consumer applications)	

Note 1. The number in parentheses indicates the number of signal outputs when 8 coms are used.

Note 2. The illegal instruction is generated when instruction code FFH is executed.

Reset by the illegal instruction execution not is issued by emulation with the in-circuit emulator or on-chip debug emulator.

2. ELECTRICAL SPECIFICATIONS (A: T_A = -40 to +85°C)

This chapter describes the following electrical specifications.

Target products A: Consumer applications (T_A = -40 to +85°C)

        R5F11MxxAFB

Caution 1. The RL78 microcontroller has an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

Caution 2. The pins mounted depend on the product. Refer to 2.1 Port Function to 2.2.1 With functions for each product in the RL78/L1A User's Manual.

2.1 Absolute Maximum Ratings

Absolute Maximum Ratings (T_A = 25°C)   **(1/3)**

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V_{DD}		-0.5 to +6.5	V
	AV_{DD}	$AV_{DD} \le V_{DD}$	-0.5 to +4.6	V
REGC pin input voltage	V_{IREGC}	REGC	-0.3 to +2.8 and -0.3 to V_{DD} + 0.3 [Note 1]	V
Input voltage	V_{I1}	P00 to P07, P11 to P17, P30 to P37, P40 to P44, P50 to P57, P70 to P77, P80, P81, P121 to P127, P137, EXCLK, EXCLKS, RESET	-0.3 to V_{DD} + 0.3 [Note 2]	V
	V_{I2}	P60, P61 (N-ch open-drain)	-0.3 to +6.5	V
	V_{I4}	IVCMP0	-0.7 to V_{DD} + 0.7	V
	V_{I5}	P20, P21, P23 to P27, P100, P101, P103 to P107, P140 to P143, P150, P152 to P154	-0.3 to AV_{DD} + 0.3 [Note 3]	V
Output voltage	V_{O1}	P00 to P07, P11 to P17, P30 to P37, P40 to P44, P50 to P57, P60, P61, P70 to P77, P80, P81, P125 to P127, P130	-0.3 to V_{DD} + 0.3 [Note 2]	V
	V_{O2}	P20, P21, P23 to P27, P100, P101, P103 to P107, P140 to P143, P150, P152 to P154	-0.3 to AV_{DD} + 0.3 [Note 3]	V
Analog input voltage	V_{AI2}	ANI00 to ANI13	-0.3 to AV_{DD} + 0.3 and $AV_{REF(+)}$ + 0.3 [Notes 2, 4]	V

Note 1. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

Note 2. Must be 6.5 V or lower.

Note 3. Must be 4.6 V or lower.

Note 4. Do not exceed $AV_{REF(+)}$ + 0.3 V in case of A/D conversion target pin.

Caution **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

Remark 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Remark 2. $AV_{REF(+)}$: Positive reference voltage of the A/D converter.

Remark 3. V_{SS}: Reference voltage

Absolute Maximum Ratings (T$_A$ = 25°C)   **(2/3)**

Parameter	Symbols	Conditions		Ratings	Unit
LCD voltage	V$_{LI1}$	V$_{L1}$ input voltage [Note 1]		-0.3 to +2.8	V
	V$_{LI2}$	V$_{L2}$ input voltage [Note 1]		-0.3 to +6.5	V
	V$_{LI3}$	V$_{L3}$ input voltage [Note 1]		-0.3 to +6.5	V
	V$_{LI4}$	V$_{L4}$ input voltage [Note 1]		-0.3 to +6.5	V
	V$_{LI5}$	CAPL, CAPH input voltage [Note 1]		-0.3 to +6.5	V
	V$_{LO1}$	V$_{L1}$ output voltage		-0.3 to +2.8	V
	V$_{LO2}$	V$_{L2}$ output voltage		-0.3 to +6.5	V
	V$_{LO3}$	V$_{L3}$ output voltage		-0.3 to +6.5	V
	V$_{LO4}$	V$_{L4}$ output voltage		-0.3 to +6.5	V
	V$_{LO5}$	CAPL, CAPH output voltage		-0.3 to +6.5	V
	V$_{LO6}$	COM0 to COM7 SEG0 to SEG44 output voltage	External resistance division method	-0.3 to V$_{DD}$ + 0.3 [Note 2]	V
			Capacitor split method	-0.3 to V$_{DD}$ + 0.3 [Note 2]	V
			Internal voltage boosting method	-0.3 to V$_{LI4}$ + 0.3 [Note 2]	V

Note 1. This value only indicates the absolute maximum ratings when applying voltage to the V$_{L1}$, V$_{L2}$, V$_{L3}$, and V$_{L4}$ pins; it does not mean that applying voltage to these pins is recommended. When using the internal voltage boosting method or capacitance split method, connect these pins to V$_{SS}$ via a capacitor (0.47 ± 30%) and connect a capacitor (0.47 ± 30%) between the CAPL and CAPH pins.

Note 2. Must be 6.5 V or lower.

Caution **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

Absolute Maximum Ratings (T_A = 25°C) (3/3)

Parameter	Symbols	Conditions			Ratings	Unit
Output current, high	I_{OH1}	Per pin			-40	mA
		Total of all pins -170 mA	P40 to P44, P130		-70	mA
			P00 to P07, P11 to P17, P30 to P37, P50 to P57, P70 to P77, P80, P81, P125 to P127		-100	mA
	I_{OH2}	Per pin	P20, P21, P23 to P27, P100, P101, P103 to P107, P140 to P143, P150, P152 to P154		-0.1	mA
		Total of all pins			-1.6 Note	mA
Output current, low	I_{OL1}	Per pin			40	mA
		Total of all pins 170 mA	P40 to P44, P130		70	mA
			P00 to P07, P11 to P17, P30 to P37, P50 to P57, P60, P61, P70 to P77, P80, P81, P125 to P127		100	mA
	I_{OL2}	Per pin	P20, P21, P23 to P27, P100, P101, P103 to P107, P140 to P143, P150, P152 to P154		0.4	mA
		Total of all pins			6.4 Note	mA
Operating ambient temperature	T_A	In normal operation mode			-40 to +85	°C
		In flash memory programming mode				
Storage temperature	T_{stg}				-65 to +150	°C

Note Do not exceed the rated value of current even in simultaneous output from the maximum of 16 AV_{DD}-group pins.

Caution **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.2   Oscillator Characteristics

2.2.1   X1 and XT1 oscillator characteristics

(T$_A$ = -40 to +85°C, 1.8 V $\leq$ V$_{DD}$ $\leq$ 3.6 V, V$_{SS}$ = 0 V)

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (fx) Note	Ceramic resonator/crystal resonator	2.7 V $\leq$ V$_{DD}$ $\leq$ 3.6 V	1.0		20.0	MHz
		2.4 V $\leq$ V$_{DD}$ < 2.7 V	1.0		16.0	
		1.8 V $\leq$ V$_{DD}$ < 2.4 V	1.0		8.0	
XT1 clock oscillation frequency (fXT) Note	Crystal resonator		32	32.768	35	kHz

Note   Indicates only permissible oscillator frequency ranges. Refer to **AC Characteristics** for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution   **Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.**

Remark   When using the X1 and XT1 oscillator, refer to **5.4 System Clock Oscillator in the RL78/L1A User's Manual**.

2.2.2 On-chip oscillator characteristics

(TA = -40 to +85°C, 1.8 V $\leq$ VDD $\leq$ 3.6 V, Vss = 0 V)

Oscillators	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency Notes 1, 2	fHOCO	2.7 V $\leq$ VDD $\leq$ 3.6 V		1		24	MHz
		2.4 V $\leq$ VDD $\leq$ 3.6 V		1		16	MHz
		1.8 V $\leq$ VDD $\leq$ 3.6 V		1		8	MHz
High-speed on-chip oscillator clock frequency accuracy		-20 to +85°C	1.8 V $\leq$ VDD $\leq$ 3.6 V	-1.0		+1.0	%
		-40 to -20°C	1.8 V $\leq$ VDD $\leq$ 3.6 V	-1.5		+1.5	%
Low-speed on-chip oscillator clock frequency	fIL				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				-15		+15	%

Note 1. High-speed on-chip oscillator frequency is selected with bits 0 to 4 of the option byte (000C2H/010C2H) and bits 0 to 2 of the HOCODIV register.

Note 2. This only indicates the oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2.3   DC Characteristics

<R>   ### 2.3.1   Pin characteristics

(T$_A$ = -40 to +85°C, 1.8 V $\leq$ AV$_{DD}$ $\leq$ V$_{DD}$ $\leq$ 3.6 V, AV$_{SS}$ = V$_{SS}$ = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high Note 1	I$_{OH1}$	Per pin for P00 to P07, P11 to P17, P30 to P37, P40 to P44, P50 to P57, P70 to P77, P80, P81, P125 to P127, P130				-10.0 Note 2	mA
		Total of P00 to P07, P11 to P17, P30 to P37, P40 to P44, P50 to P57, P70 to P77, P80, P81, P125 to P127, P130 (When duty = 70% Note 3)	2.7 V $\leq$ V$_{DD}$ $\leq$ 3.6 V			-15.0	mA
			1.8 V $\leq$ V$_{DD}$ < 2.7 V			-7.0	mA
	I$_{OH2}$	Per pin for P20, P21, P23 to P27, P100, P101, P103 to P107, P140 to P143, P150, P152 to P154	1.8 V $\leq$ V$_{DD}$ $\leq$ 3.6 V			-0.1 Note 2	mA
		Total of P20, P21, P23 to P27, P100, P101, P103 to P107, P140 to P143, P150, P152 to P154 (When duty = 70% Note 3)	1.8 V $\leq$ V$_{DD}$ $\leq$ 3.6 V			-1.6	mA

Note 1.   Value of current at which the device operation is guaranteed even if the current flows from the V$_{DD}$ pin (I$_{OH1}$) and AV$_{DD}$ pin (I$_{OH2}$) to an output pin.

Note 2.   However, do not exceed the total current value.

Note 3.   Specification under conditions where the duty factor is 70%.
The output current value that has changed the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).
• Total output current of pins = (I$_{OH}$ $\times$ 0.7)/(n $\times$ 0.01)
    <Example>   Where n = 50% and I$_{OH}$ = -10.0 mA
                    Total output current of pins = (-10.0 $\times$ 0.7)/(50 $\times$ 0.01) = -14.0 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Caution   **P00 to P02, P11, P12, P14, P35 to P37, P40, P41, P43, P44, P80, and P81 do not output high level in N-ch open-drain mode.**

Remark   Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T$_A$ = -40 to +85°C, 1.8 V $\leq$ AV$_{DD}$ $\leq$ V$_{DD}$ $\leq$ 3.6 V, AV$_{SS}$ = V$_{SS}$ = 0 V)

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Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low [Note 1]	I$_{OL1}$	Per pin for P00 to P07, P11 to P17, P30 to P37, P40 to P44, P50 to P57, P70 to P77, P80, P81, P125 to P127, P130				20.0 Note 2	mA
		Per pin for P60 and P61				15.0 Note 2	mA
		Total of P40 to P44, P130 (When duty = 70% [Note 3])	2.7 V $\leq$ V$_{DD}$ $\leq$ 3.6 V			15.0	mA
			1.8 V $\leq$ V$_{DD}$ < 2.7 V			9.0	mA
		Total of P00 to P07, P11 to P17, P30 to P37, P50 to P57, P60, P61, P70 to P77, P80, P81, P125 to P127 (When duty = 70% [Note 3])	2.7 V $\leq$ V$_{DD}$ $\leq$ 3.6 V			35.0	mA
			1.8 V $\leq$ V$_{DD}$ < 2.7 V			20.0	mA
		Total of all pins (When duty = 70% [Note 3])				50.0	mA
	I$_{OL2}$	Per pin for P20, P21, P23 to P27, P100, P101, P103 to P107, P140 to P143, P150, P152 to P154	1.8 V $\leq$ V$_{DD}$ $\leq$ 3.6 V			0.4 Note 2	mA
		Total of P20, P21, P23 to P27, P100, P101, P103 to P107, P140 to P143, P150, P152 to P154 (When duty = 70% [Note 3])	1.8 V $\leq$ V$_{DD}$ $\leq$ 3.6 V			6.4	mA

Note 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the V$_{SS}$ pin (I$_{OL1}$) and AV$_{SS}$ pin (I$_{OL2}$).

Note 2. However, do not exceed the total current value.

Note 3. Specification under conditions where the duty factor is 70%.
The output current value that has changed the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).
• Total output current of pins = (I$_{OL}$ $\times$ 0.7)/(n $\times$ 0.01)
  <Example>   Where n = 50% and I$_{OL}$ = 10.0 mA
                 Total output current of pins = (10.0 $\times$ 0.7)/(50 $\times$ 0.01) = 14.0 mA

      However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Remark   Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(TA = -40 to +85°C, 1.8 V ≤ AVDD ≤ VDD ≤ 3.6 V, AVSS = VSS = 0 V)

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Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	Port P00 to P07, P11 to P17, P30 to P37, P40 to P44, P50 to P57, P70 to P77, P80 to P81, P125 to P127	Normal input buffer	0.8 V_{DD}		V_{DD}	V
	V_{IH2}	P00, P01, P11, P14, P35, P36, P40, P41, P44, P80	TTL input buffer 3.3 V ≤ V_{DD} ≤ 3.6 V	2.0		V_{DD}	V
			TTL input buffer 1.8 V ≤ V_{DD} < 3.3 V	1.50		V_{DD}	V
	V_{IH3}	P20, P21, P23 to P27, P100, P101, P103 to P107, P140 to P143, P150, P152 to P154		0.7 AV_{DD}		AV_{DD}	V
	V_{IH4}	P60, P61		0.7 V_{DD}		6.0	V
	V_{IH5}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{RESET}$		0.8 V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	Port P00 to P07, P11 to P17, P30 to P37, P40 to P44, P50 to P57, P70 to P77, P80 to P81, P125 to P127	Normal input buffer	0		0.2 V_{DD}	V
	V_{IL2}	P00, P01, P11, P14 ,P35, P36, P40, P41, P44, P80	TTL input buffer 3.3 V ≤ V_{DD} ≤ 3.6 V	0		0.5	V
			TTL input buffer 1.8 V ≤ V_{DD} < 3.3 V	0		0.32	V
	V_{IL3}	P20, P21, P23 to P27, P100, P101, P103 to P107, P140 to P143, P150, P152 to P154		0		0.3 AV_{DD}	V
	V_{IL4}	P60, P61		0		0.3 V_{DD}	V
	V_{IL5}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{RESET}$		0		0.2 V_{DD}	V

Caution **The maximum value of V_{IH} of pins P00 to P02, P11, P12, P14, P35 to P37, P40, P41. P43, P44, P80, and P81 is V_{DD}, even in the N-ch open-drain mode.**

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = -40 to +85°C, 1.8 V $\leq$ AV_{DD} $\leq$ V_{DD} $\leq$ 3.6 V, AV_{SS} = V_{SS} = 0 V)

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Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH1}	P00 to P07, P11 to P17, P30 to P37, P40 to P44, P50 to P57, P70 to P77, P80, P81, P125 to P127, P130	2.7 V $\leq$ V_{DD} $\leq$ 3.6 V, I_{OH} = -2.0 mA	V_{DD} - 0.6			V
			1.8 V $\leq$ V_{DD} $\leq$ 3.6 V, I_{OH} = -1.5 mA	V_{DD} - 0.5			V
	V_{OH2}	P20, P21, P23 to P27, P100, P101, P103 to P107, P140 to P143, P150, P152 to P154	1.8 V $\leq$ V_{DD} $\leq$ 3.6 V, I_{OH} = -100 μA	AV_{DD} - 0.5			V
Output voltage, low	V_{OL1}	P00 to P07, P11 to P17, P30 to P37, P40 to P44, P50 to P57, P70 to P77, P80, P81, P125 to P127, P130	2.7 V $\leq$ V_{DD} $\leq$ 3.6 V, I_{OL} = 3.0 mA			0.6	V
			2.7 V $\leq$ V_{DD} $\leq$ 3.6 V, I_{OL} = 1.5 mA			0.4	V
			1.8 V $\leq$ V_{DD} $\leq$ 3.6 V, I_{OL} = 0.6 mA			0.4	V
	V_{OL2}	P20, P21, P23 to P27, P100, P101, P103 to P107, P140 to P143, P150, P152 to P154	1.8 V $\leq$ V_{DD} $\leq$ 3.6 V, I_{OL} = 400 μA			0.4	V
	V_{OL3}	P60, P61	2.7 V $\leq$ V_{DD} $\leq$ 3.6 V, I_{OL} = 3.0 mA			0.4	V
			1.8 V $\leq$ V_{DD} $\leq$ 3.6 V, I_{OL} = 2.0 mA			0.4	V

Caution   **P00 to P02, P11, P12, P14, P35 to P37, P40, P41. P43, P44, P80, and P81 do not output high level in N-ch open-drain mode.**

Remark   Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T$_A$ = -40 to +85°C, 1.8 V $\leq$ AV$_{DD}$ $\leq$ V$_{DD}$ $\leq$ 3.6 V, AV$_{SS}$ = V$_{SS}$ = 0 V)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Input leakage current, high	I$_{LIH1}$	P00 to P07, P11 to P17, P30 to P37, P40 to P44, P50 to P57, P60, P61, P70 to P77, P80, P81, P125 to P127, P137, $\overline{RESET}$	V$_I$ = V$_{DD}$				1	μA
	I$_{LIH3}$	P121 to P124 (X1, X2, EXCLK, XT1, XT2, EXCLKS)	V$_I$ = V$_{DD}$	In input port or external clock input			1	μA
				In resonator connection			10	μA
	I$_{LIH4}$	P20, P21, P23 to P27, P100, P101, P103 to P107, P140 to P143, P150, P152 to P154	V$_I$ = AV$_{DD}$				1	μA
Input leakage current, low	I$_{LIL1}$	P00 to P07, P11 to P17, P30 to P37, P40 to P44, P50 to P57, P60, P61, P70 to P77, P80, P81, P125 to P127, P137, $\overline{RESET}$	V$_I$ = V$_{SS}$				-1	μA
	I$_{LIL3}$	P121 to P124 (X1, X2, EXCLK, XT1, XT2, EXCLKS)	V$_I$ = V$_{SS}$	In input port or external clock input			-1	μA
				In resonator connection			-10	μA
	I$_{LIL4}$	P20, P21, P23 to P27, P100, P101, P103 to P107, P140 to P143, P150, P152 to P154	V$_I$ = AV$_{SS}$				-1	μA
On-chip pull-up resistance	R$_{U1}$	P00 to P07, P11 to P17, P30 to P37, P50 to P57, P70 to P77, P80, P81, P125 to P127	V$_I$ = V$_{SS}$	2.4 V $\leq$ V$_{DD}$ $\leq$ 3.6 V	10	20	100	kΩ
				1.8 V $\leq$ V$_{DD}$ < 2.4 V	10	30	100	
	R$_{U2}$	P40 to P44	V$_I$ = V$_{SS}$		10	20	100	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.3.2 Supply current characteristics

(TA = -40 to +85°C, 1.8 V $\leq$ AVDD $\leq$ VDD $\leq$ 3.6 V, VSS = 0 V)   **(1/2)**

Parameter	Symbol						MIN.	TYP.	MAX.	Unit
Supply current [Note 1]	IDD1	Operating mode	HS (high-speed main) mode [Note 5]	f_{IH} = 24 MHz [Note 3]	Basic operation	VDD = 3.6 V		1.7		mA
						VDD = 3.0 V		1.7		
					Normal operation	VDD = 3.6 V		3.6	6.1	
						VDD = 3.0 V		3.6	6.1	
				f_{IH} = 16 MHz [Note 3]	Normal operation	VDD = 3.6 V		2.7	4.7	
						VDD = 3.0 V		2.7	4.7	
			LS (low-speed main) mode [Note 5]	f_{IH} = 8 MHz [Note 3]	Normal operation	VDD = 3.6 V		1.2	2.1	mA
						VDD = 3.0 V		1.2	2.1	
			HS (high-speed main) mode [Note 5]	f_{MX} = 20 MHz [Note 2], VDD = 3.6 V	Normal operation	Square wave input		3.0	5.1	mA
						Resonator connection		3.2	5.2	
				f_{MX} = 20 MHz [Note 2], VDD = 3.0 V	Normal operation	Square wave input		2.9	5.1	
						Resonator connection		3.2	5.2	
				f_{MX} = 16 MHz [Note 2], VDD = 3.6 V	Normal operation	Square wave input		2.5	4.4	
						Resonator connection		2.7	4.5	
				f_{MX} = 16 MHz [Note 2], VDD = 3.0 V	Normal operation	Square wave input		2.5	4.4	
						Resonator connection		2.7	4.5	
				f_{MX} = 10 MHz [Note 2], VDD = 3.6 V	Normal operation	Square wave input		1.9	3.0	
						Resonator connection		1.9	3.0	
				f_{MX} = 10 MHz [Note 2], VDD = 3.0 V	Normal operation	Square wave input		1.9	3.0	
						Resonator connection		1.9	3.0	
			LS (low-speed main) mode [Note 5]	f_{MX} = 8 MHz [Note 2], VDD = 3.6 V	Normal operation	Square wave input		1.1	2.0	mA
						Resonator connection		1.1	2.0	
				f_{MX} = 8 MHz [Note 2], VDD = 3.0 V	Normal operation	Square wave input		1.1	2.0	
						Resonator connection		1.1	2.0	
			Subsystem clock operation	f_{SUB} = 32.768 kHz [Note 4] TA = -40°C	Normal operation	Square wave input		4.0	5.4	μA
						Resonator connection		4.3	5.4	
				f_{SUB} = 32.768 kHz [Note 4] TA = +25°C	Normal operation	Square wave input		4.0	5.4	
						Resonator connection		4.3	5.4	
				f_{SUB} = 32.768 kHz [Note 4] TA = +50°C	Normal operation	Square wave input		4.1	7.1	
						Resonator connection		4.4	7.1	
				f_{SUB} = 32.768 kHz [Note 4] TA = +70°C	Normal operation	Square wave input		4.3	8.7	
						Resonator connection		4.7	8.7	
				f_{SUB} = 32.768 kHz [Note 4] TA = +85°C	Normal operation	Square wave input		4.7	12.0	
						Resonator connection		5.2	12.0	

(**Notes** and **Remarks** are listed on the next page.)

Note 1. Total current flowing into VDD, including the input leakage current flowing when the level of the input pin is fixed to VDD, or VSS. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the LCD controller/driver, A/D converter, D/A converter, rail to rail operational amplifier (with analog multiplexer), general-purpose operational amplifier, voltage reference, low-resistance switch, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

Note 2. When high-speed on-chip oscillator and subsystem clock are stopped.

Note 3. When high-speed system clock and subsystem clock are stopped.

Note 4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (ultra-low power consumption oscillation). However, not including the current flowing into the real-time clock 2, 12-bit interval timer, 8-bit interval timer, and watchdog timer.

Note 5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ VDD ≤ 3.6 V@1 MHz to 24 MHz

                                                          2.4 V ≤ VDD ≤ 3.6 V@1 MHz to 16 MHz

LS (low-speed main) mode: 1.8 V ≤ VDD ≤ 3.6 V@1 MHz to 8 MHz

Remark 1. fMX: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 2. fIH: Frequency when the high-speed on-chip oscillator (24 MHz max.)

Remark 3. fSUB: Subsystem clock frequency (XT1 clock oscillation frequency)

Remark 4. Except subsystem clock operation, temperature condition of the TYP. value is TA = 25°C

(T$_A$ = -40 to +85°C, 1.8 V ≤ AV$_{DD}$ ≤ V$_{DD}$ ≤ 3.6 V, V$_{SS}$ = 0 V) (2/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Note 1	I$_{DD2}$ Note 2	HALT mode	HS (high-speed main) mode Note 7	f$_{IH}$ = 24 MHz Note 4	V$_{DD}$ = 3.6 V		0.42	1.83	mA
					V$_{DD}$ = 3.0 V		0.42	1.83	
				f$_{IH}$ = 16 MHz Note 4	V$_{DD}$ = 5.0 V		0.39	1.38	
					V$_{DD}$ = 3.0 V		0.39	1.38	
			LS (low-speed main) mode Note 7	f$_{IH}$ = 8 MHz Note 4	V$_{DD}$ = 3.0 V		0.25	0.71	mA
					V$_{DD}$ = 2.0 V		0.25	0.71	
			HS (high-speed main) mode Note 7	f$_{MX}$ = 20 MHz Note 3, V$_{DD}$ = 3.6 V	Square wave input		0.26	1.55	mA
					Resonator connection		0.4	1.68	
				f$_{MX}$ = 20 MHz Note 3, V$_{DD}$ = 3.0 V	Square wave input		0.25	1.55	
					Resonator connection		0.4	1.68	
				f$_{MX}$ = 16 MHz Note 3, V$_{DD}$ = 3.6 V	Square wave input		0.23	1.22	
					Resonator connection		0.36	1.39	
				f$_{MX}$ = 16 MHz Note 3, V$_{DD}$ = 3.0 V	Square wave input		0.22	1.22	
					Resonator connection		0.35	1.39	
				f$_{MX}$ = 10 MHz Note 3, V$_{DD}$ = 3.0 V	Square wave input		0.18	0.82	
					Resonator connection		0.28	0.90	
				f$_{MX}$ = 10 MHz Note 3, V$_{DD}$ = 2.0 V	Square wave input		0.18	0.81	
					Resonator connection		0.28	0.89	
			LS (low-speed main) mode Note 7	f$_{MX}$ = 8 MHz Note 3, V$_{DD}$ = 3.0 V	Square wave input		0.09	0.51	mA
					Resonator connection		0.15	0.56	
				f$_{MX}$ = 8 MHz Note 3, V$_{DD}$ = 2.0 V	Square wave input		0.10	0.52	
					Resonator connection		0.15	0.57	
			Subsystem clock operation	f$_{SUB}$ = 32.768 kHz Note 5 T$_A$ = -40°C	Square wave input		0.32	0.75	μA
					Resonator connection		0.51	0.83	
				f$_{SUB}$ = 32.768 kHz Note 5 T$_A$ = +25°C	Square wave input		0.41	0.83	
					Resonator connection		0.62	1.00	
				f$_{SUB}$ = 32.768 kHz Note 5 T$_A$ = +50°C	Square wave input		0.52	1.17	
					Resonator connection		0.75	1.36	
				f$_{SUB}$ = 32.768 kHz Note 5 T$_A$ = +70°C	Square wave input		0.82	1.97	
					Resonator connection		1.08	2.16	
				f$_{SUB}$ = 32.768 kHz Note 5 T$_A$ = +85°C	Square wave input		1.38	3.37	
					Resonator connection		1.62	3.56	
	I$_{DD3}$ Note 6	STOP mode Note 8	T$_A$ = -40°C				0.16	0.51	μA
			T$_A$ = +25°C				0.22	0.51	
			T$_A$ = +50°C				0.27	1.10	
			T$_A$ = +70°C				0.37	1.90	
			T$_A$ = +85°C				0.6	3.30	

(**Notes** and **Remarks** are listed on the next page.)

Note 1. Total current flowing into V$_{DD}$, including the input leakage current flowing when the level of the input pin is fixed to V$_{DD}$ or V$_{SS}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the LCD controller/driver, A/D converter, D/A converter, ail to rail operational amplifier (with analog multiplexer), general-purpose operational amplifier, voltage reference, low-resistance switch, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

Note 2. During HALT instruction execution by flash memory.

Note 3. When high-speed on-chip oscillator and subsystem clock are stopped.

Note 4. When high-speed system clock and subsystem clock are stopped.

Note 5. When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the real-time clock 2 is included. However, not including the current flowing into the 12-bit interval timer, 8-bit interval timer, and watchdog timer.

Note 6. Not including the current flowing into the real-time clock 2, 12-bit interval timer, 8-bit interval timer, and watchdog timer.

Note 7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ V$_{DD}$ ≤ 3.6 V@1 MHz to 24 MHz

                                            2.4 V ≤ V$_{DD}$ ≤ 3.6 V@1 MHz to 16 MHz

LS (low-speed main) mode: 1.8 V ≤ V$_{DD}$ ≤ 3.6 V@1 MHz to 8 MHz

Note 8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

Remark 1. f$_{MX}$:   High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 2. f$_{IH}$:   Frequency when the high-speed on-chip oscillator (24 MHz max.)

Remark 3. f$_{SUB}$:   Subsystem clock frequency (XT1 clock oscillation frequency)

Remark 4. Except subsystem clock operation, temperature condition of the TYP. value is T$_A$ = 25°C

(T$_A$ = -40 to +85°C, 1.8 V ≤ AV$_{DD}$ ≤ V$_{DD}$ ≤ 3.6 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operating current	I$_{FIL}$ Note 1				0.20		μA
RTC2 operating current	I$_{RTC}$ Notes 1, 3	f$_{SUB}$ = 32.768 kHz			0.02		μA
12-bit interval timer operating current	I$_{TMKA}$ Notes 1, 2, 4	f$_{SUB}$ = 32.768 kHz			0.02		μA
8-bit interval timer operating current	I$_{TMRT}$ Notes 1, 19	f$_{SUB}$ = 32.768 kHz	8-bit counter mode × 2-channel operation		0.12		μA
			16-bit counter mode operation		0.10		μA
Watchdog timer operating current	I$_{WDT}$ Notes 1, 5	f$_{IL}$ = 15 kHz			0.22		μA
A/D converter operating current	I$_{ADC}$ Notes 6, 7	AV$_{DD}$ = 3.0 V, when conversion at maximum speed			0.7	1.7	mA
A/D converter AVREF(+) current	I$_{AVREF}$ Note 8	AV$_{DD}$ = 3.0 V, HVSEL[1:0] = 00B Note 7			40	80	μA
		AV$_{DD}$ = 3.0 V, HVSEL[1:0] = 01B Note 10			40	80	
Internal reference voltage (1.45 V) current	I$_{ADREF}$ Notes 1, 9				85		μA
Temperature sensor operating current	I$_{TMPS}$ Note 1				85		μA
D/A converter operating current	I$_{DAC}$ Notes 7, 11	Per D/A converter channel			0.4	0.8	mA
D/A converter AVREF(+) current	I$_{DAREF}$ Note 10	AV$_{REFP}$ = 3.0 V, REF[2:0] = 110B, Per channel			35	80	μA
Comparator operating current	I$_{CMP}$ Notes 1, 12	V$_{DD}$ = 3.6 V, Regulator output voltage = 2.1 V	Window mode		7.0		μA
			Comparator high-speed mode		2.6		μA
			Comparator low-speed mode		1.2		μA
		V$_{DD}$ = 3.6 V, Regulator output voltage = 1.8 V	Window mode		4.1		μA
			Comparator high-speed mode		1.5		μA
			Comparator low-speed mode		0.9		μA
General-purpose operational amplifier operating current (for 1 unit)	I$_{AMP1}$ Notes 7, 18	AV$_{DD}$ = 3.0 V	Low-power consumption mode		2	4	μA
			High-speed mode		140	280	μA
Rail to rail operational amplifier operating current (for 1 unit)	I$_{AMP2}$ Notes 7, 18	AV$_{DD}$ = 3.0 V	Low-power consumption mode		10	16	μA
			High-speed mode		210	350	μA
LVD operating current	I$_{LVI}$ Notes 1, 13				0.06		μA
Self-programming operating current	I$_{FSP}$ Notes 1, 14				2.0	12.2	mA
BGO operating current	I$_{BGO}$ Notes 1, 15				2.0	12.2	mA
SNOOZE operating current	I$_{SNOZ}$ Note 1	CSI/UART operation			0.70	0.84	mA
Voltage reference operating current	I$_{VREF}$	AV$_{DD}$ = V$_{DD}$ = 3.0 V				40	μA

(T$_A$ = -40 to +85°C, 1.8 V $\leq$ AV$_{DD}$ $\leq$ V$_{DD}$ $\leq$ 3.6 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
LCD operating current	I$_{LCD1}$ Notes 16, 17	External resistance division method	f$_{LCD}$ = f$_{SUB}$ LCD clock = 128 Hz	1/3 bias 4-time slice	V$_{DD}$ = 3.6 V, V$_{L4}$ = 3.6 V		0.14		μA
	I$_{LCD2}$ Note 16	Internal voltage boosting method	f$_{LCD}$ = f$_{SUB}$ LCD clock = 128 Hz	1/3 bias 4-time slice	V$_{DD}$ = 3.0 V, V$_{L4}$ = 3.0 V (VLCD = 04H)		0.61		μA
	I$_{LCD3}$ Note 16	Capacitor split method	f$_{LCD}$ = f$_{SUB}$ LCD clock = 128 Hz	1/3 bias 4-time slice	V$_{DD}$ = 3.0 V, V$_{L4}$ = 3.0 V		0.12		μA

(**Notes** and **Remarks** are listed on the next page.)

Note 1. Current flowing to V_{DD}.

Note 2. When high speed on-chip oscillator and high-speed system clock are stopped.

Note 3. Current flowing only to the real-time clock 2 (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2}, and I_{RTC}, when the real-time clock 2 operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added. I_{DD2} subsystem clock operation includes the operational current of the real-time clock 2.

Note 4. Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2}, and I_{TMKA}, when the 12-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added. I_{DD2} subsystem clock operation includes the operational current of the 12-bit interval timer.

Note 5. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The current value of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{WDT} when the watchdog timer operates in STOP mode.

Note 6. Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{ADC}, I_{AVREF}, I_{ADREF} when the A/D converter operates in an operation mode or the HALT mode.

Note 7. Current flowing to the AV_{DD}.

Note 8. Current flowing from the reference voltage source of A/D converter.

Note 9. Operation current flowing to the internal reference voltage.

Note 10. Current flowing to the AV_{REFP}.

Note 11. Current flowing only to the D/A converter. The current value of the RL78 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{DA} when the D/A converter operates in an operation mode or the HALT mode.

Note 12. Current flowing only to the comparator circuit. The current value of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{CMP} when the comparator circuit operates in the Operating, HALT or STOP mode.

Note 13. Current flowing only to the LVD circuit. The current value of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{LVI} when the LVD circuit operates in the Operating, HALT or STOP mode.

Note 14. Current flowing only during self-programming.

Note 15. Current flowing only during data flash rewrite.

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Note 16. Current flowing only to the LCD controller/driver (V_{DD} pin). The current value of the RL78 microcontrollers is the sum of the LCD operating current (I_{LCD1}, I_{LCD2} or I_{LCD3}) to the supply current (I_{DD1}, or I_{DD2}) when the LCD controller/driver operates in an operation mode or HALT mode. Not including the current that flows through the LCD panel.

Note 17. Not including the current that flows through the external divider resistor divider resistor.

Note 18. Current flowing only to the operational amplifier. The current value of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{AMP} when the operational amplifier operates in the operating mode, HALT mode, or STOP mode.

Note 19. Current flowing only to the 8-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2}, and I_{IT}, when the 8-bit interval timer operates in the operating mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added.

Remark 1. f_{IL}: Low-speed on-chip oscillator clock frequency

Remark 2. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

Remark 3. f_{CLK}: CPU/peripheral hardware clock frequency

Remark 4. Temperature condition of the TYP. value is T_A = 25°C

2.4   AC Characteristics

2.4.1   Basic operation

(TA = -40 to +85°C, 1.8 V ≤ AVDD ≤ VDD ≤ 3.6 V, VSS = 0 V)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	TCY	Main system clock (fMAIN) operation	HS (high-speed main) mode	2.7 V ≤ VDD ≤ 3.6 V	0.0417		1	μs
				2.4 V ≤ VDD < 2.7 V	0.0625		1	μs
			LS (low-speed main) mode	1.8 V ≤ VDD ≤ 3.6 V	0.125		1	μs
		Subsystem clock (fSUB) operation		1.8 V ≤ VDD ≤ 3.6 V	28.5	30.5	31.3	μs
		In the self-programming mode	HS (high-speed main) mode	2.7 V ≤ VDD ≤ 3.6 V	0.0417		1	μs
				2.4 V ≤ VDD < 2.7 V	0.0625		1	μs
			LS (low-speed main) mode	1.8 V ≤ VDD ≤ 3.6 V	0.125		1	μs
External main system clock frequency	fEX	EXCLK		2.7 V ≤ VDD ≤ 3.6 V	1.0		20.0	MHz
				2.4 V ≤ VDD < 2.7 V	1.0		16.0	MHz
				1.8 V ≤ VDD < 2.7 V	1.0		8.0	MHz
	fEXT	EXCLKS			32		35	kHz
External main system clock input high-level width, low-level width	tEXH, tEXL	EXCLK		2.7 V ≤ VDD ≤ 3.6 V	24			ns
				2.4 V ≤ VDD < 2.7 V	30			ns
				1.8 V ≤ VDD < 2.7 V	60			ns
	tEXHS, tEXLS	EXCLKS			13.7			μs
Timer input high-level width, low-level width	tTIH, tTIL	TI00 to TI07			1/fMCK + 10			ns
Timer output frequency	fTO	TO00 to TO07	HS (high-speed main) mode	2.7 V ≤ VDD ≤ 3.6 V			8	MHz
				2.4 V ≤ VDD < 2.7 V			8	MHz
			LS (low-speed main) mode	1.8 V ≤ VDD ≤ 3.6 V			4	MHz
Buzzer output frequency	fPCL	PCLBUZ0, PCLBUZ1	HS (high-speed main) mode	2.7 V ≤ VDD ≤ 3.6 V			8	MHz
				2.4 V ≤ VDD < 2.7 V			8	MHz
			LS (low-speed main) mode	1.8 V ≤ VDD ≤ 3.6 V			4	MHz
Interrupt input high-level width, low-level width	tINTH, tINTL	INTP0 to INTP7		1.8 V ≤ VDD ≤ 3.6 V	1			μs
Key interrupt input low-level width	tKR	KR0 to KR7		1.8 V ≤ VDD ≤ 3.6 V	250			ns
RESET low-level width	tRSL	RESET			10			μs

Remark   fMCK: Timer array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of timer mode register mn (TMRmn). m: Unit number (m = 0),
n: Channel number (n = 0 to 7))

Minimum Instruction Execution Time during Main System Clock Operation

TCY vs VDD (HS (high-speed main) mode)
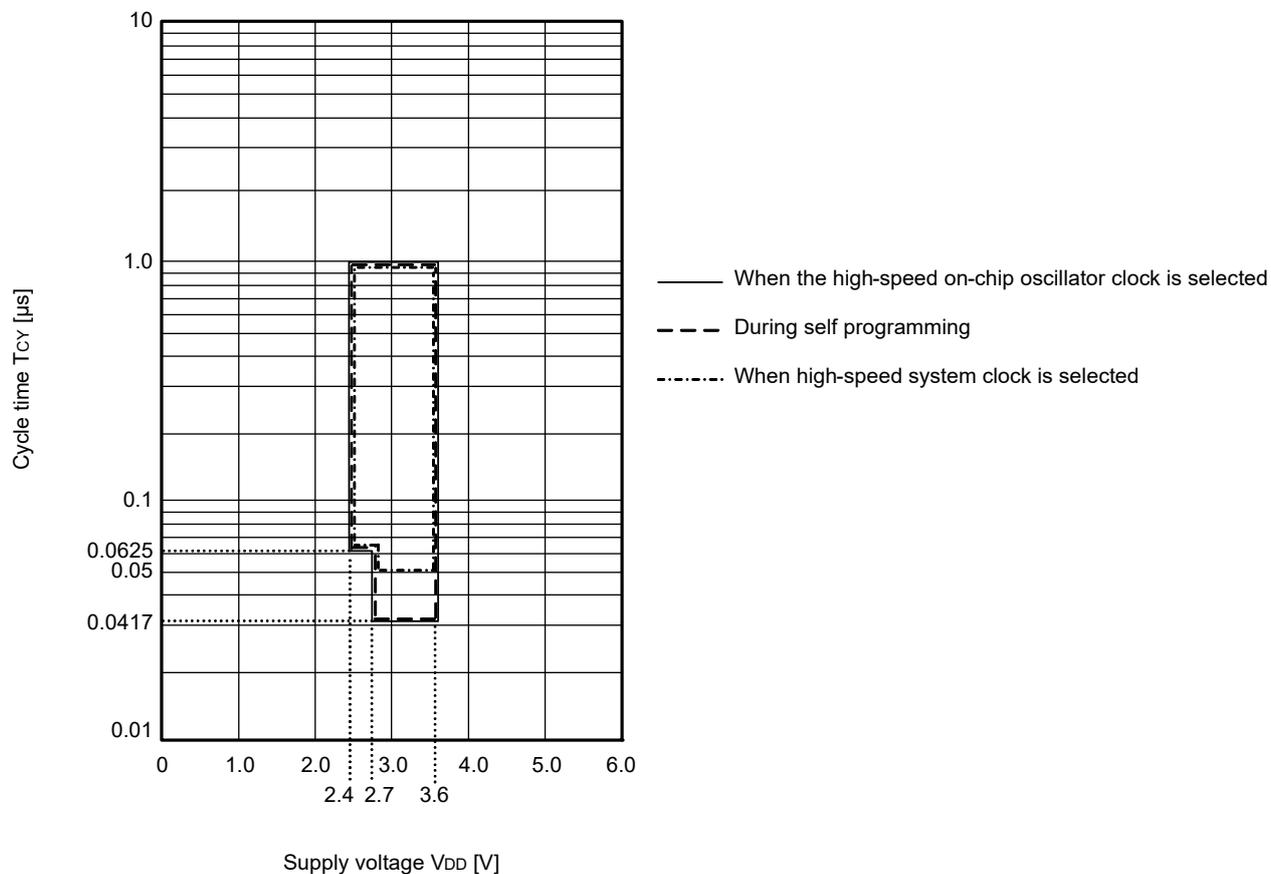
TCY vs VDD (LS (low-speed main) mode)

_____ When the high-speed on-chip oscillator clock is selected

_ _ _ During self programming

-..-..-. When high-speed system clock is selected

AC Timing Test Points

V_{IH}/V_{OH}
V_{IL}/V_{OL}
Test points
V_{IH}/V_{OH}
V_{IL}/V_{OL}
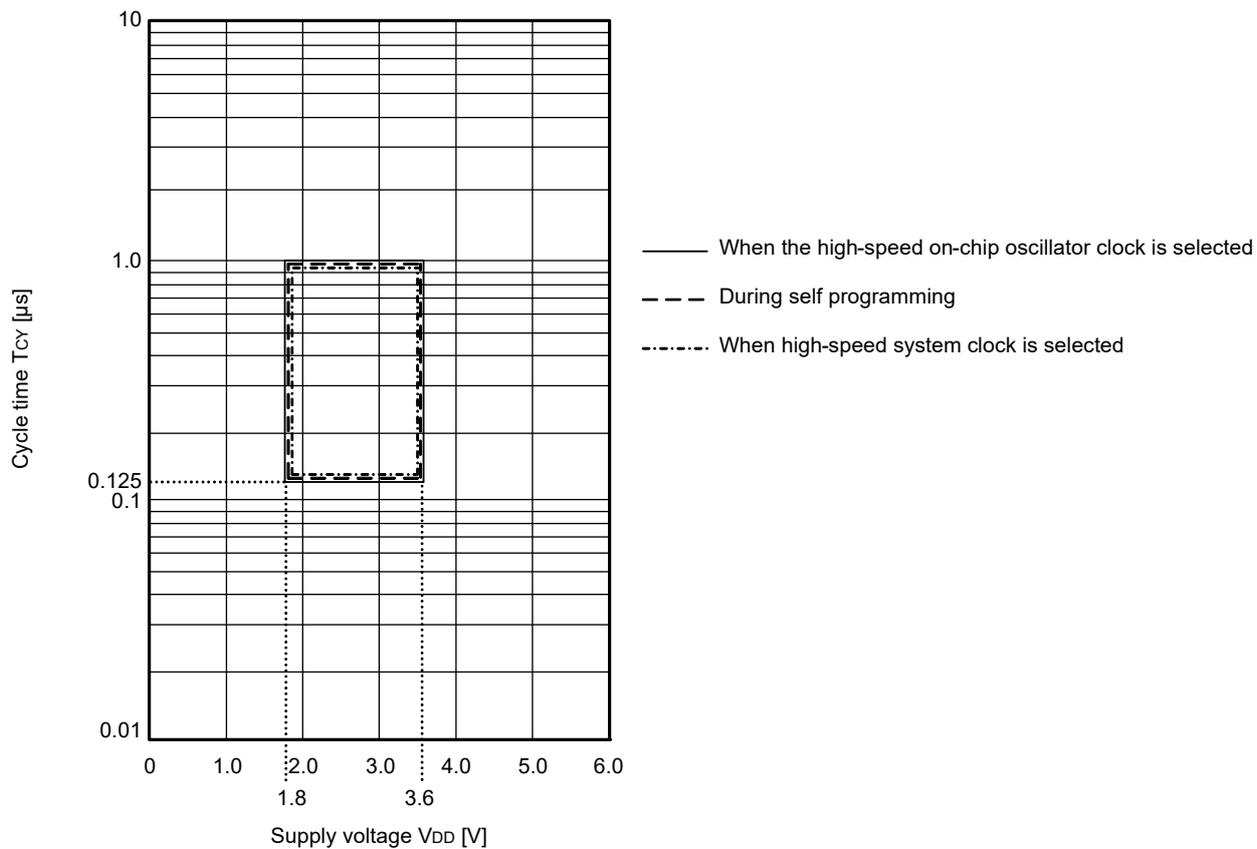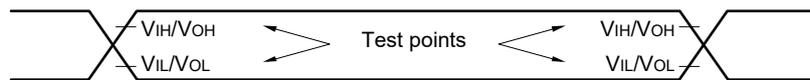
External System Clock Timing

$1/f_{EX}$
$1/f_{EXS}$

t_{EXL}
t_{EXLS}

t_{EXH}
t_{EXHS}

EXCLK/EXCLKS

TI/TO Timing

t_{TIL}
t_{TIH}

TI00 to TI07

$1/f_{TO}$
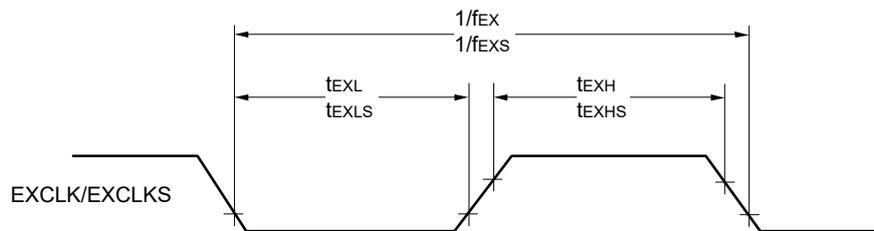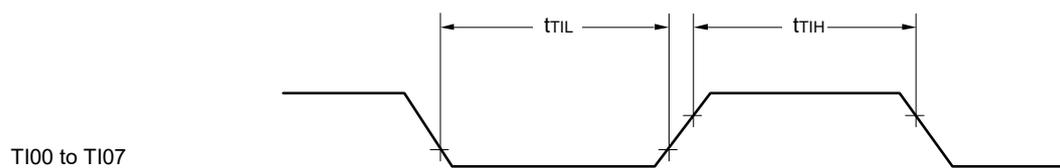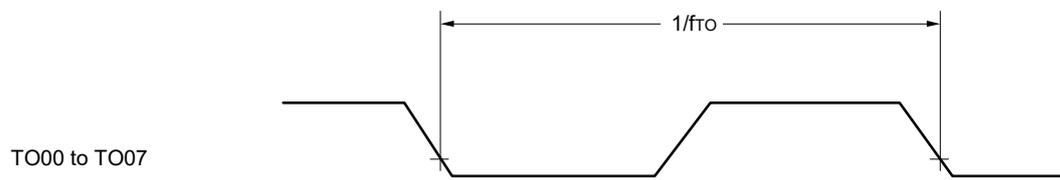
TO00 to TO07

Interrupt Request Input Timing

t_{INTL}
t_{INTH}
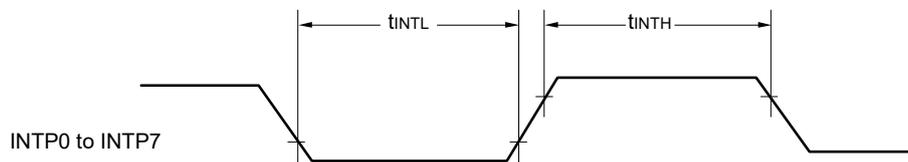
INTP0 to INTP7

Key Interrupt Input Timing

KR0 to KR7
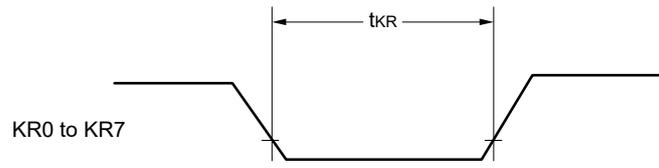
$\overline{\text{RESET}}$ Input Timing

$\overline{\text{RESET}}$
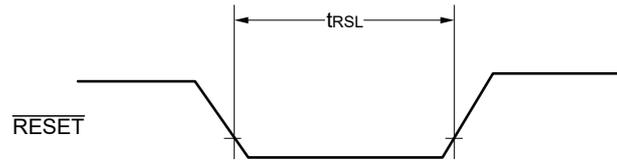
2.5 Peripheral Functions Characteristics

AC Timing Test Points
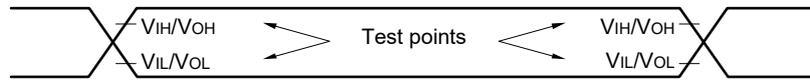
2.5.1 Serial array unit

(1) During communication at same potential (UART mode)

(T_A = -40 to +85°C, 1.8 V $\leq$ V_{DD} $\leq$ 3.6 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
Transfer rate [Note 1]		2.7 V $\leq$ V_{DD} $\leq$ 3.6 V		$f_{MCK}/6$ [Note 2]		$f_{MCK}/6$	bps
		Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ [Note 3]		4.0		1.3	Mbps
		2.4 V $\leq$ V_{DD} $\leq$ 3.6 V		$f_{MCK}/6$ [Note 2]		$f_{MCK}/6$	bps
		Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ [Note 3]		2.6		1.3	Mbps
		1.8 V $\leq$ V_{DD} $\leq$ 3.6 V		—		$f_{MCK}/6$ [Note 2]	bps
		Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ [Note 3]		—		1.3	Mbps

Note 1.   Transfer rate in the SNOOZE mode is 4800 bps only.
Note 2.   The following conditions are required for low voltage interface.
            2.4 V $\leq$ V_{DD} < 2.7 V: MAX. 2.6 Mbps
            1.8 V $\leq$ V_{DD} < 2.4 V: MAX. 1.3 Mbps
Note 3.   The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:
            HS (high-speed main) mode: 24 MHz (2.7 V $\leq$ V_{DD} $\leq$ 3.6 V)
                                            16 MHz (2.4 V $\leq$ V_{DD} $\leq$ 3.6 V)
            LS (low-speed main) mode: 8 MHz (1.8 V $\leq$ V_{DD} $\leq$ 3.6 V)

Caution   **Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

UART mode connection diagram (during communication at same potential)
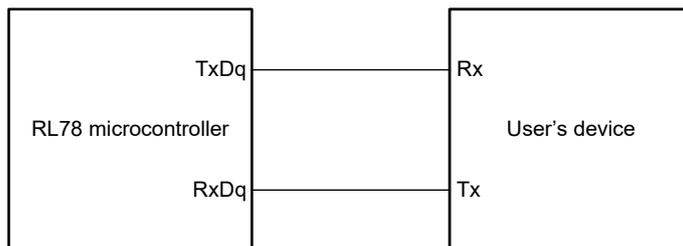
UART mode bit width (during communication at same potential) (reference)
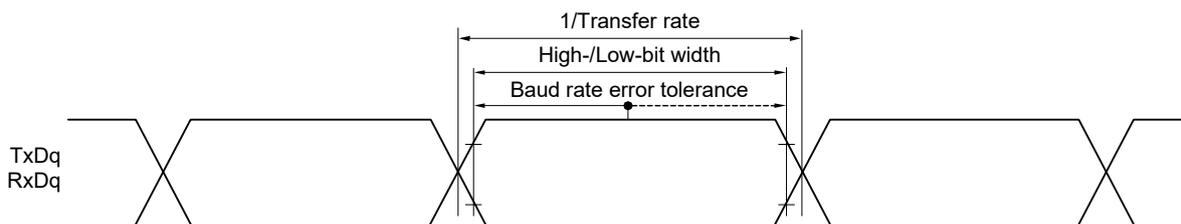
Remark 1. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 3, 4, 8)

Remark 2. f$_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00 to 03, 10 to 13))

(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)

(T$_A$ = -40 to +85°C, 2.7 V $\leq$ V$_{DD}$ $\leq$ 3.6 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t$_{KCY1}$	t$_{KCY1}$ $\geq$ f$_{CLK}$/2	2.7 V $\leq$ V$_{DD}$ $\leq$ 3.6 V	167		250		ns
SCKp high-/low-level width	t$_{KH1}$, t$_{KL1}$	2.7 V $\leq$ V$_{DD}$ $\leq$ 3.6 V		t$_{KCY1}$/2 - 10		t$_{KCY1}$/2 - 50		ns
SIp setup time (to SCKp↑) Note 1	t$_{SIK1}$	2.7 V $\leq$ V$_{DD}$ $\leq$ 3.6 V		33		110		ns
SIp hold time (from SCKp↑) Note 2	t$_{KSI1}$	2.7 V $\leq$ V$_{DD}$ $\leq$ 3.6 V		10		10		ns
Delay time from SCKp↓ to SOp output Note 3	t$_{KSO1}$	C = 20 pF Note 4			10		10	ns

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Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SCKp and SOp output lines.

Caution **Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

Remark 1. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM number (g = 4)

Remark 2. f$_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))

(3)　During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)
(T$_A$ = -40 to +85°C, 1.8 V $\leq$ V$_{DD}$ $\leq$ 3.6 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t$_{KCY1}$	t$_{KCY1}$ $\geq$ f$_{CLK}$/4	2.7 V $\leq$ V$_{DD}$ $\leq$ 3.6 V	167		500		ns
			2.4 V $\leq$ V$_{DD}$ $\leq$ 3.6 V	250		500		ns
			1.8 V $\leq$ V$_{DD}$ $\leq$ 3.6 V	—		500		ns
SCKp high-/low-level width	t$_{KH1}$, t$_{KL1}$	2.7 V $\leq$ V$_{DD}$ $\leq$ 3.6 V		t$_{KCY1}$/2 - 18		t$_{KCY1}$/2 - 50		ns
		2.4 V $\leq$ V$_{DD}$ $\leq$ 3.6 V		t$_{KCY1}$/2 - 38		t$_{KCY1}$/2 - 50		ns
		1.8 V $\leq$ V$_{DD}$ $\leq$ 3.6 V		—		t$_{KCY1}$/2 - 50		ns
SIp setup time (to SCKp↑) Note 1	t$_{SIK1}$	2.7 V $\leq$ V$_{DD}$ $\leq$ 3.6 V		44		110		ns
		2.4 V $\leq$ V$_{DD}$ $\leq$ 3.6 V		75		110		ns
		1.8 V $\leq$ V$_{DD}$ $\leq$ 3.6 V		—		110		ns
SIp hold time (from SCKp↑) Note 2	t$_{KSI1}$	2.4 V $\leq$ V$_{DD}$ $\leq$ 3.6 V		19		19		ns
		1.8 V $\leq$ V$_{DD}$ $\leq$ 3.6 V		—		19		ns
Delay time from SCKp↓ to SOp output Note 3	t$_{KSO1}$	C = 30 pF Note 4	2.7 V $\leq$ V$_{DD}$ $\leq$ 3.6 V		25		50	ns
			2.4 V $\leq$ V$_{DD}$ $\leq$ 3.6 V		25		50	ns
			1.8 V $\leq$ V$_{DD}$ $\leq$ 3.6 V		—		50	ns

Note 1.　When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2.　When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3.　When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4.　C is the load capacitance of the SCKp and SOp output lines.

Caution　**Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

Remark 1.　p: CSI number (p = 00, 10, 20, 30), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),
　　　　　　g: PIM and POM number (g = 0, 1, 3, 4, 8)

Remark 2.　f$_{MCK}$: Serial array unit operation clock frequency
　　　　　　(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
　　　　　　n: Channel number (mn = 00 to 03, 10 to 13))

(4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)
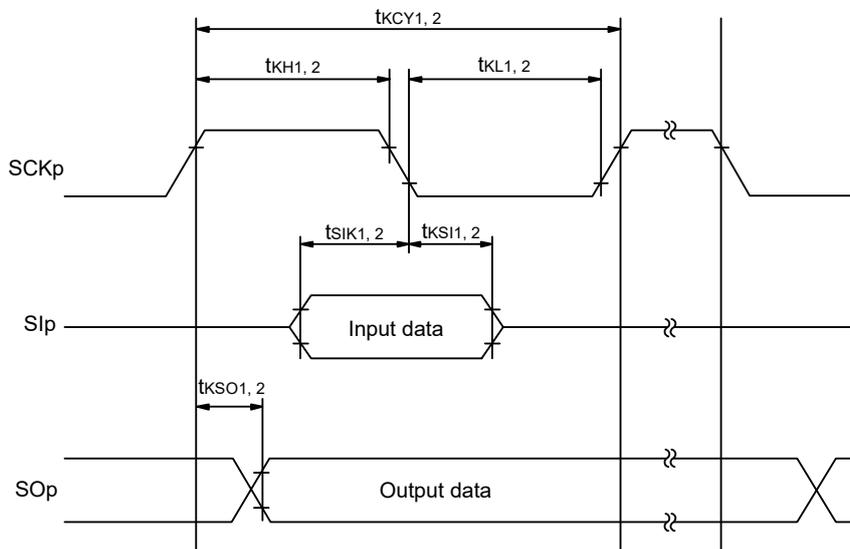**(TA = -40 to +85°C, 1.8 V $\leq$ VDD $\leq$ 3.6 V, VSS = 0 V)**

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCKp cycle time Note 5	tKCY2	2.7 V $\leq$ VDD $\leq$ 3.6 V	fMCK > 16 MHz	8/fMCK		—		ns
			fMCK $\leq$ 16 MHz	6/fMCK		6/fMCK		ns
		2.4 V $\leq$ VDD $\leq$ 3.6 V		6/fMCK and 500		6/fMCK and 500		ns
		1.8 V $\leq$ VDD $\leq$ 3.6 V		—		6/fMCK and 750		ns
SCKp high-/low-level width	tKH2, tKL2	2.7 V $\leq$ VDD $\leq$ 3.6 V		tKCY2/2 - 8		tKCY2/2 - 8		ns
		1.8 V $\leq$ VDD $\leq$ 3.6 V		—		tKCY2/2 - 18		ns
SIp setup time (to SCKp↑) Note 1	tSIK2	2.7 V $\leq$ VDD $\leq$ 3.6 V		1/fMCK + 20		1/fMCK + 30		ns
		2.4 V $\leq$ VDD $\leq$ 3.6 V		1/fMCK + 30		1/fMCK + 30		ns
		1.8 V $\leq$ VDD $\leq$ 3.6 V		—		1/fMCK + 30		ns
SIp hold time (from SCKp↑) Note 2	tKSI2	2.4 V $\leq$ VDD $\leq$ 3.6 V		1/fMCK + 31		1/fMCK + 31		ns
		1.8 V $\leq$ VDD $\leq$ 3.6 V		—		1/fMCK + 31		ns
Delay time from SCKp↓ to SOp output Note 3	tKSO2	C = 30 pF Note 4	2.7 V $\leq$ VDD $\leq$ 3.6 V		2/fMCK + 44		2/fMCK + 110	ns
			2.4 V $\leq$ VDD $\leq$ 3.6 V		2/fMCK + 75		2/fMCK + 110	ns
			1.8 V $\leq$ VDD $\leq$ 3.6 V		—		2/fMCK + 110	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SCKp and SOp output lines.

Note 5. The maximum transfer rate when using the SNOOZE mode is 1 Mbps.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. p: CSI number (p = 00, 10, 20, 30), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),
g: PIM and POM number (g = 0, 1, 3, 4, 8)

Remark 2. fMCK: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00 to 03, 10 to 13))

CSI mode connection diagram (during communication at same potential)
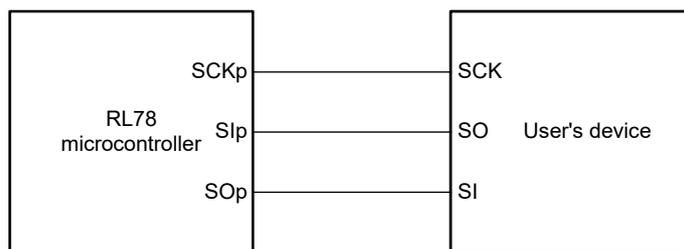
Remark 1. p: CSI number (p = 00, 10, 20, 30)
Remark 2. m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)
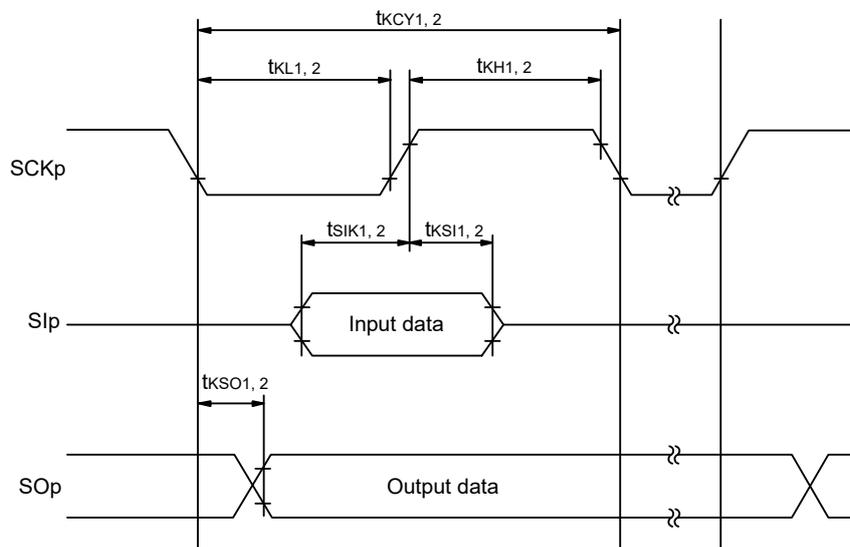
CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)

Remark 1. p: CSI number (p = 00, 10, 20, 30)
Remark 2. m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

(5) During communication at same potential (simplified I²C mode)

(TA = -40 to +85°C, 1.8 V ≤ VDD ≤ 3.6 V, VSS = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SCLr clock frequency	fSCL	2.7 V ≤ VDD ≤ 3.6 V, Cb = 50 pF, Rb = 2.7 kΩ		1000 Note 1		400 Note 1	kHz
		1.8 V ≤ VDD ≤ 3.6 V, Cb = 100 pF, Rb = 3 kΩ		400 Note 1		400 Note 1	kHz
		1.8 V ≤ VDD < 2.7 V, Cb = 100 pF, Rb = 5 kΩ		300 Note 1		300 Note 1	kHz
Hold time when SCLr = "L"	tLOW	2.7 V ≤ VDD ≤ 3.6 V, Cb = 50 pF, Rb = 2.7 kΩ	475		1150		ns
		1.8 V ≤ VDD ≤ 3.6 V, Cb = 100 pF, Rb = 3 kΩ	1150		1150		ns
		1.8 V ≤ VDD < 2.7 V, Cb = 100 pF, Rb = 5 kΩ	1550		1550		ns
Hold time when SCLr = "H"	tHIGH	2.7 V ≤ VDD ≤ 3.6 V, Cb = 50 pF, Rb = 2.7 kΩ	475		1150		ns
		1.8 V ≤ VDD ≤ 3.6 V, Cb = 100 pF, Rb = 3 kΩ	1150		1150		ns
		1.8 V ≤ VDD < 2.7 V, Cb = 100 pF, Rb = 5 kΩ	1550		1550		ns
Data setup time (reception)	tSU: DAT	2.7 V ≤ VDD ≤ 3.6 V, Cb = 50 pF, Rb = 2.7 kΩ	1/fMCK + 85 Note 2		1/fMCK + 145 Note 2		ns
		1.8 V ≤ VDD ≤ 3.6 V, Cb = 100 pF, Rb = 3 kΩ	1/fMCK + 145 Note 2		1/fMCK + 145 Note 2		ns
		1.8 V ≤ VDD < 2.7 V, Cb = 100 pF, Rb = 5 kΩ	1/fMCK + 230 Note 2		1/fMCK + 230 Note 2		ns
Data hold time (transmission)	tHD: DAT	2.7 V ≤ VDD ≤ 3.6 V, Cb = 50 pF, Rb = 2.7 kΩ	0	305	0	305	ns
		1.8 V ≤ VDD ≤ 3.6 V, Cb = 100 pF, Rb = 3 kΩ	0	355	0	355	ns
		1.8 V ≤ VDD < 2.7 V, Cb = 100 pF, Rb = 5 kΩ	0	405	0	405	ns

Note 1.   The value must be equal to or less than fMCK/4.

Note 2.   Set the fMCK value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution   Select the normal input buffer and the N-ch open drain output (VDD tolerance) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).

Simplified I^{2}C mode connection diagram (during communication at same potential)
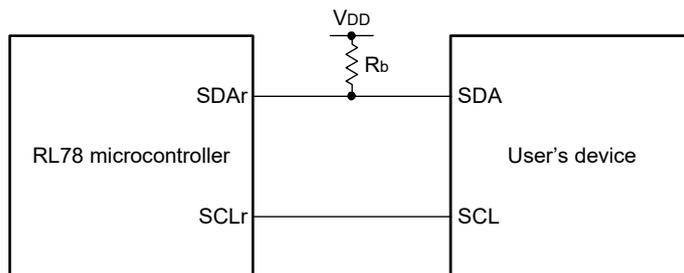
Simplified I^{2}C mode serial transfer timing (during communication at same potential)
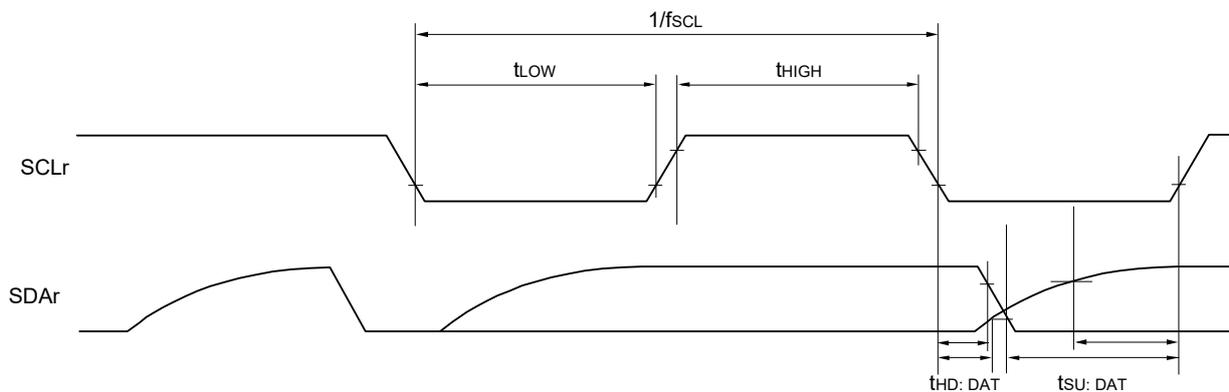
Remark 1. R$_b$[Ω]: Communication line (SDAr) pull-up resistance, C$_b$[F]: Communication line (SCLr, SDAr) load capacitance

Remark 2. r: IIC number (r = 00, 10, 20, 30), g: PIM number (g = 0, 1, 3, 4, 8),

<R>   h: POM number (h = 0, 1, 3, 4, 8)

Remark 3. f$_{MCK}$: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1),

<R>   n: Channel number (n = 0, 2), mn = 0, 02, 10, 12)

(6) Communication at different potential (1.8 V, 2.5 V) (UART mode)

(T_A = -40 to +85°C, 1.8 V ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)(1/2)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
Transfer rate Notes 1, 2		reception	2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V		$f_{MCK}/6$ Note 1		$f_{MCK}/6$ Note 1	bps
			Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ Note 4		4.0		1.3	Mbps
			1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V		$f_{MCK}/6$ Notes 1, 2, 3		$f_{MCK}/6$ Notes 1, 2, 3	bps
			Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ Note 4		4.0		1.3	Mbps

Note 1. Transfer rate in the SNOOZE mode is 4,800 bps only.

Note 2. Use it with V_{DD} ≥ V_b.

Note 3. The following conditions are required for low voltage interface.

       2.4 V ≤ V_{DD} < 2.7 V: MAX. 2.6 Mbps

       1.8 V ≤ V_{DD} < 2.4 V: MAX. 1.3 Mbps

Note 4. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:

       HS (high-speed main) mode: 24 MHz (2.7 V ≤ V_{DD} ≤ 3.6 V)

                                          16 MHz (2.4 V ≤ V_{DD} ≤ 3.6 V)

       LS (low-speed main) mode: 8 MHz (1.8 V ≤ V_{DD} ≤ 3.6 V)

Caution **Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.**

Remark 1. V_b[V]: Communication line voltage

Remark 2. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 3, 4, 8)

Remark 3. f_{MCK}: Serial array unit operation clock frequency

       (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,

       n: Channel number (mn = 00 to 03, 10 to 13))

(6) Communication at different potential (1.8 V, 2.5 V) (UART mode)
(T$_A$ = -40 to +85°C, 1.8 V $\leq$ V$_{DD}$ $\leq$ 3.6 V, V$_{SS}$ = 0 V)(2/2)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
Transfer rate Note 2		transmission	2.7 V $\leq$ V$_{DD}$ $\leq$ 3.6 V, 2.3 V $\leq$ V$_b$ $\leq$ 2.7 V		Note 1		Note 1	bps
			Theoretical value of the maximum transfer rate C$_b$ = 50 pF, R$_b$ = 2.7 kΩ, V$_b$ = 2.3 V		1.2 Note 2		1.2 Note 2	Mbps
			1.8 V $\leq$ V$_{DD}$ < 3.3 V, 1.6 V $\leq$ V$_b$ $\leq$ 2.0 V		Notes 3, 4		Notes 3, 4	bps
			Theoretical value of the maximum transfer rate C$_b$ = 50 pF, R$_b$ = 5.5 kΩ, V$_b$ = 1.6 V		0.43 Note 5		0.43 Note 5	Mbps

Note 1. The smaller maximum transfer rate derived by using f$_{MCK}$/6 or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 2.7 V $\leq$ V$_{DD}$ $\leq$ 3.6 V and 2.3 V $\leq$ V$_b$ $\leq$ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

Note 2. This value as an example is calculated when the conditions described in the "Conditions" column are met.
Refer to Note 1 above to calculate the maximum transfer rate under conditions of the customer.
Note 3. Use it with V$_{DD}$ $\geq$ V$_b$.
Note 4. The smaller maximum transfer rate derived by using f$_{MCK}$/6 or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 1.8 V $\leq$ V$_{DD}$ < 3.3 V and 1.6 V $\leq$ V$_b$ $\leq$ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

Note 5. This value as an example is calculated when the conditions described in the "Conditions" column are met.
Refer to Note 4 above to calculate the maximum transfer rate under conditions of the customer.

Caution **Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V$_{DD}$ tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V$_{IH}$ and V$_{IL}$, see the DC characteristics with TTL input buffer selected.**

UART mode connection diagram (during communication at different potential)
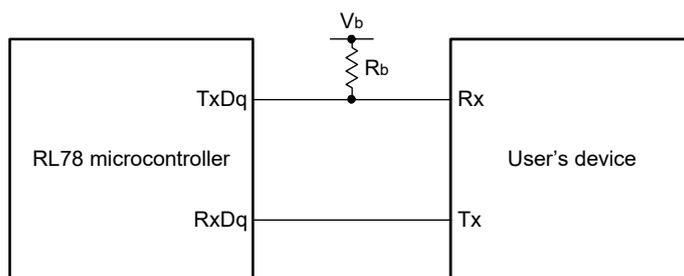
UART mode bit width (during communication at different potential) (reference)
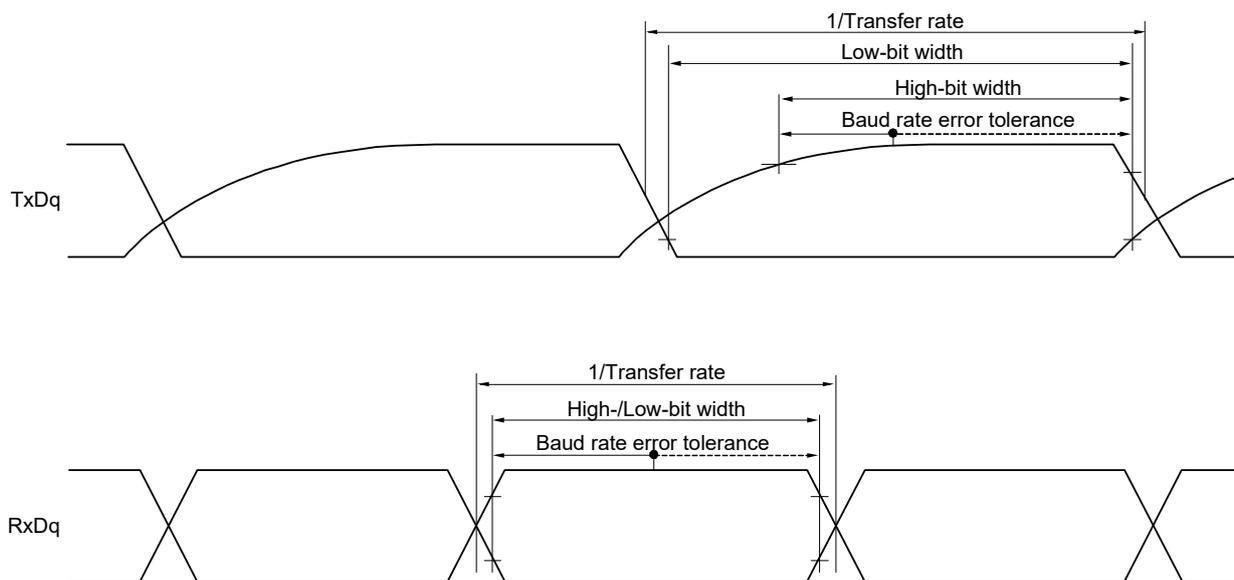
Remark 1. $R_b[\Omega]$: Communication line (TxDq) pull-up resistance, $C_b[F]$: Communication line (TxDq) load capacitance,
$V_b[V]$: Communication line voltage

Remark 2. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 3, 4, 8)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00 to 03, 10 to 13))

(7) Communication at different potential (2.5 V) (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)

(TA = -40 to +85°C, 2.7 V $\leq$ VDD $\leq$ 3.6 V, VSS = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	tKCY1	tKCY1 $\geq$ 2/fCLK	2.7 V $\leq$ VDD < 3.6 V, 2.3 V $\leq$ Vb $\leq$ 2.7 V, Cb = 20 pF, Rb = 1.4 kΩ	300		1150		ns
SCKp high-level width	tKH1	2.7 V $\leq$ VDD < 3.6 V, 2.3 V $\leq$ Vb $\leq$ 2.7 V, Cb = 20 pF, Rb = 2.7 kΩ		tKCY1/2 - 120		tKCY1/2 - 120		ns
SCKp low-level width	tKL1	2.7 V $\leq$ VDD < 3.6 V, 2.3 V $\leq$ Vb $\leq$ 2.7 V, Cb = 20 pF, Rb = 1.4 kΩ		tKCY1/2 - 10		tKCY1/2 - 50		ns
SIp setup time (to SCKp↑) Note 1	tSIK1	2.7 V $\leq$ VDD < 3.6 V, 2.3 V $\leq$ Vb $\leq$ 2.7 V, Cb = 20 pF, Rb = 2.7 kΩ		121		479		ns
SIp hold time (from SCKp↑) Note 1	tKSI1	2.7 V $\leq$ VDD < 3.6 V, 2.3 V $\leq$ Vb $\leq$ 2.7 V, Cb = 20 pF, Rb = 1.4 kΩ		10		10		ns
Delay time from SCKp↓ to SOp output Note 1	tKSO1	2.7 V $\leq$ VDD < 3.6 V, 2.3 V $\leq$ Vb $\leq$ 2.7 V, Cb = 20 pF, Rb = 1.4 kΩ			130		130	ns
SIp setup time (to SCKp↓) Note 2	tSIK1	2.7 V $\leq$ VDD < 3.6 V, 2.3 V $\leq$ Vb $\leq$ 2.7 V, Cb = 20 pF, Rb = 2.7 kΩ		33		110		ns
SIp hold time (from SCKp↓) Note 2	tKSI1	2.7 V $\leq$ VDD < 3.6 V, 2.3 V $\leq$ Vb $\leq$ 2.7 V, Cb = 20 pF, Rb = 2.7 kΩ		10		10		ns
Delay time from SCKp↑ to SOp output Note 2	tKSO1	2.7 V $\leq$ VDD < 3.6 V, 2.3 V $\leq$ Vb $\leq$ 2.7 V, Cb = 20 pF, Rb = 2.7 kΩ			10		10	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
Note 2. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution   Select the TTL input buffer for the SIp pin and the N-ch open drain output (VDD tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

Remark 1. Rb[Ω]: Communication line (SCKp, SOp) pull-up resistance, Cb[F]: Communication line (SCKp, SOp) load capacitance, Vb[V]: Communication line voltage
Remark 2. p: CSI number (p = 00), m: Unit number (m = 0),
n: Channel number (n = 0), g: PIM and POM number (g = 4)
Remark 3. fMCK: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00))

(8) Communication at different potential (1.8 V, 2.5 V) (CSI mode) (master mode, SCKp... internal clock output)

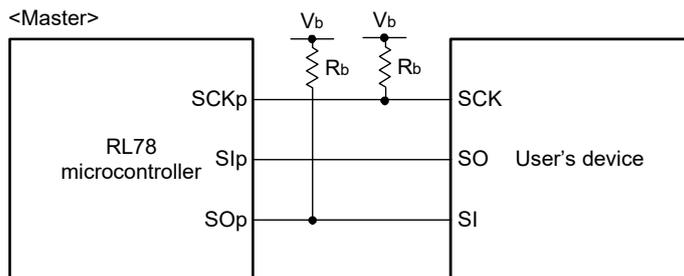**(TA = -40 to +85°C, 1.8 V $\leq$ VDD $\leq$ 3.6 V, VSS = 0 V)(1/2)**

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	tKCY1	tKCY1 $\geq$ 4/fCLK	2.7 V $\leq$ VDD < 3.6 V, 2.3 V $\leq$ Vb $\leq$ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	500 Note		1150		ns
			1.8 V $\leq$ VDD < 3.3 V, 1.6 V $\leq$ Vb $\leq$ 1.8 V, Cb = 30 pF, Rb = 5.5 kΩ	1150 Note		1150		ns
SCKp high-level width	tKH1	2.7 V $\leq$ VDD $\leq$ 3.6 V, 2.3 V $\leq$ Vb $\leq$ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ		tKCY1/2 - 170		tKCY1/2 - 170		ns
		1.8 V $\leq$ VDD < 3.3 V, 1.6 V $\leq$ Vb $\leq$ 2.0 V, Cb = 30 pF, Rb = 5.5 kΩ		tKCY1/2 - 458		tKCY1/2 - 458		ns
SCKp low-level width	tKL1	2.7 V $\leq$ VDD $\leq$ 3.6 V, 2.3 V $\leq$ Vb $\leq$ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ		tKCY1/2 - 18		tKCY1/2 - 50		ns
		1.8 V $\leq$ VDD < 3.3 V, 1.6 V $\leq$ Vb $\leq$ 2.0 V, Cb = 30 pF, Rb = 5.5 kΩ		tKCY1/2 - 50		tKCY1/2 - 50		ns

Note   Use it with VDD $\geq$ Vb.

Caution   **Select the TTL input buffer for the SIp pin and the N-ch open drain output (VDD tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the page after the next page.)
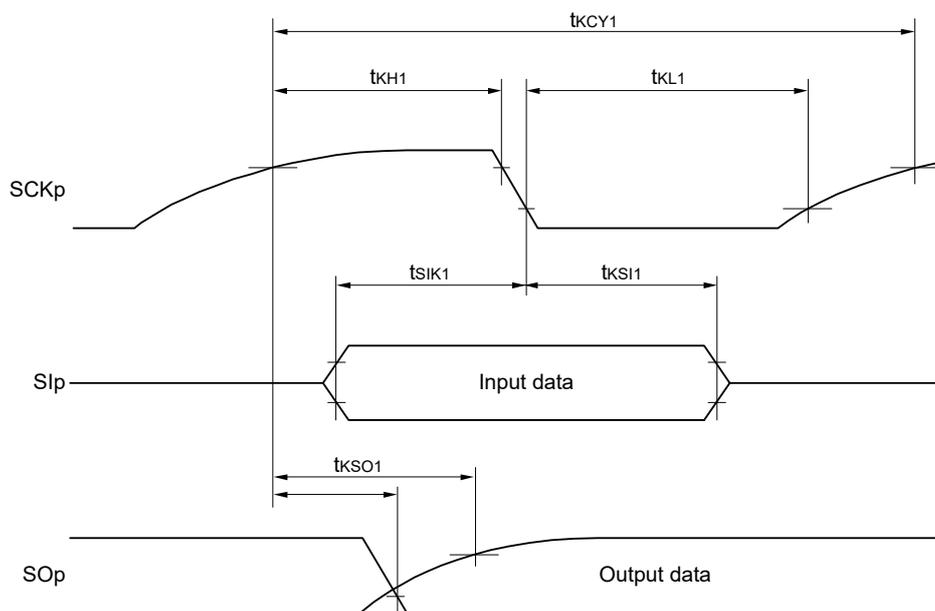
(8) Communication at different potential (1.8 V, 2.5 V) (CSI mode) (master mode, SCKp... internal clock output)

(TA = -40 to +85°C, 1.8 V ≤ VDD ≤ 3.6 V, VSS = 0 V)(2/2)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SIp setup time (to SCKp↑) Note 1	tSIK1	2.7 V ≤ VDD ≤ 3.6 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	177		479		ns
		1.8 V ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 3, Cb = 30 pF, Rb = 5.5 kΩ	479		479		ns
SIp hold time (from SCKp↑) Note 1	tKSI1	2.7 V ≤ VDD ≤ 3.6 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	19		19		ns
		1.8 V ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 3, Cb = 30 pF, Rb = 5.5 kΩ	19		19		ns
Delay time from SCKp↓ to SOp output Note 1	tKSO1	2.7 V ≤ VDD ≤ 3.6 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ		195		195	ns
		1.8 V ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 3, Cb = 30 pF, Rb = 5.5 kΩ		483		483	ns
SIp setup time (to SCKp↓) Note 2	tSIK1	2.7 V ≤ VDD ≤ 3.6 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	44		110		ns
		1.8 V ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 3, Cb = 30 pF, Rb = 5.5 kΩ	110		110		ns
SIp hold time (from SCKp↓) Note 2	tKSI1	2.7 V ≤ VDD ≤ 3.6 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	19		19		ns
		1.8 V ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 3, Cb = 30 pF, Rb = 5.5 kΩ	19		19		ns
Delay time from SCKp↑ to SOp output Note 2	tKSO1	2.7 V ≤ VDD ≤ 3.6 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ		25		25	ns
		1.8 V ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 3, Cb = 30 pF, Rb = 5.5 kΩ		25		25	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
Note 2. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
Note 3. Use it with VDD ≥ Vb.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (VDD tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

(**Remarks** are listed on the next page.)

CSI mode connection diagram (during communication at different potential)

Remark 1. R$_b$[Ω]: Communication line (SCKp, SOp) pull-up resistance, C$_b$[F]: Communication line (SCKp, SOp) load capacitance, V$_b$[V]: Communication line voltage

Remark 2. p: CSI number (p = 00, 10, 20, 30), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0, 1, 3, 4, 8)
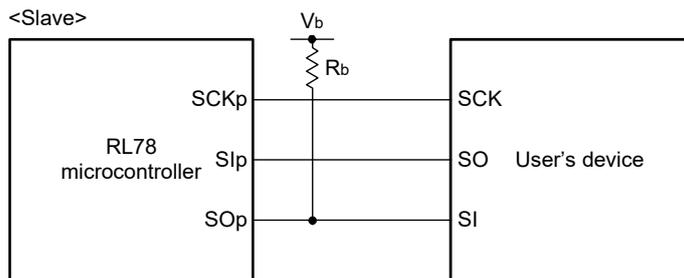
Remark 3. f$_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 02, 10, 12))

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)

Remark   p: CSI number (p = 00, 10, 20, 30), m: Unit number (m = 0, 1), n: Channel number (n = 0, 2),
                     g: PIM and POM number (g = 0, 1, 3, 4, 8)

(9)　Communication at different potential (1.8 V, 2.5 V) (CSI mode) (slave mode, SCKp... external clock input)

(TA = -40 to +85°C, 1.8 V ≤ VDD ≤ 3.6 V, VSS = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCKp cycle time Note 1	tKCY2	2.7 V ≤ VDD ≤ 3.6 V, 2.3 V ≤ Vb ≤ 2.7 V	20 MHz < fMCK ≤ 24 MHz	16/fMCK		—		ns
			16 MHz < fMCK ≤ 20 MHz	14/fMCK		—		ns
			8 MHz < fMCK ≤ 16 MHz	12/fMCK		—		ns
			4 MHz < fMCK ≤ 8 MHz	8/fMCK		16/fMCK		ns
			fMCK ≤ 4 MHz	6/fMCK		10/fMCK		ns
		1.8 V ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 2	20 MHz < fMCK ≤ 24 MHz	36/fMCK		—		ns
			16 MHz < fMCK ≤ 20 MHz	32/fMCK		—		ns
			8 MHz < fMCK ≤ 16 MHz	26/fMCK		—		ns
			4 MHz < fMCK ≤ 8 MHz	16/fMCK		16/fMCK		ns
			fMCK ≤ 4 MHz	10/fMCK		10/fMCK		ns
SCKp high-/low-level width	tKH2, tKL2	2.7 V ≤ VDD ≤ 3.6 V, 2.3 V ≤ Vb ≤ 2.7 V		tKCY2/2 - 18		tKCY2/2 - 50		ns
		1.8 V ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 2		tKCY2/2 - 50		tKCY2/2 - 50		ns
SIp setup time (to SCKp↑) Note 3	tSIK2	2.7 V ≤ VDD ≤ 3.6 V		1/fMCK + 20		1/fMCK + 30		ns
		1.8 V ≤ VDD < 3.3 V		1/fMCK + 30		1/fMCK + 30		ns
SIp hold time (from SCKp↑) Note 4	tKSI2			1/fMCK + 31		1/fMCK + 31		ns
Delay time from SCKp↓ to SOp output Note 5	tKSO2	2.7 V ≤ VDD ≤ 3.6 V, 2.3 V ≤ Vb ≤ 2.7 V Cb = 30 pF, Rb = 2.7 kΩ			2/fMCK + 214		2/fMCK + 573	ns
		1.8 V ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 2 Cb = 30 pF, Rb = 5.5 kΩ			2/fMCK + 573		2/fMCK + 573	ns

Note 1.　Transfer rate in the SNOOZE mode: MAX. 1 Mbps

Note 2.　Use it with VDD ≥ Vb.

Note 3.　When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4.　When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 5.　When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution　**Select the TTL input buffer for the SIp pin and SCKp pin and the N-ch open drain output (VDD tolerance) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the next page.)

CSI mode connection diagram (during communication at different potential)

Remark 1. $R_b[\Omega]$: Communication line (SOp) pull-up resistance, $C_b[F]$: Communication line (SOp) load capacitance, $V_b[V]$: Communication line voltage
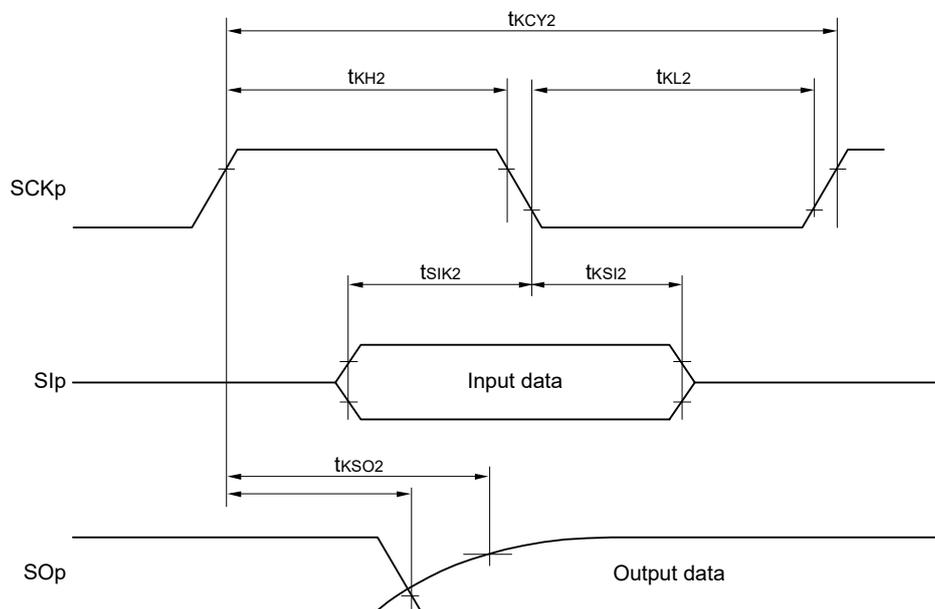
Remark 2. p: CSI number (p = 00, 10, 20, 30), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0, 1, 3, 4, 8)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 02, 10, 12))

CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)

CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)

Remark   p: CSI number (p = 00, 10, 20, 30), m: Unit number (m = 0, 1),
n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0, 1, 3, 4, 8)

(10) Communication at different potential (1.8 V, 2.5 V) (simplified I^{2}C mode)

(TA = -40 to +85°C, 1.8 V $\leq$ VDD $\leq$ 3.6 V, VSS = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SCLr clock frequency	fSCL	2.7 V $\leq$ VDD $\leq$ 3.6 V, 2.3 V $\leq$ Vb < 2.7 V, Cb = 50 pF, Rb = 2.7 kΩ		1000 Note 1		300 Note 1	kHz
		2.7 V $\leq$ VDD $\leq$ 3.6 V, 2.3 V $\leq$ Vb < 2.7 V, Cb = 100 pF, Rb = 2.7 kΩ		400 Note 1		300 Note 1	kHz
		1.8 V $\leq$ VDD < 3.3 V, 1.6 V $\leq$ Vb $\leq$ 2.0 V Note 2, Cb = 100 pF, Rb = 5.5 kΩ		400 Note 1		300 Note 1	kHz
Hold time when SCLr = "L"	tLOW	2.7 V $\leq$ VDD $\leq$ 3.6 V, 2.3 V $\leq$ Vb < 2.7 V, Cb = 50 pF, Rb = 2.7 kΩ	475		1550		ns
		2.7 V $\leq$ VDD < 3.6 V, 2.3 V $\leq$ Vb < 2.7 V, Cb = 100 pF, Rb = 2.7 kΩ	1150		1550		ns
		1.8 V $\leq$ VDD < 3.3 V, 1.6 V $\leq$ Vb $\leq$ 2.0 V Note 2, Cb = 100 pF, Rb = 5.5 kΩ	1550		1550		ns
Hold time when SCLr = "H"	tHIGH	2.7 V $\leq$ VDD $\leq$ 3.6 V, 2.3 V $\leq$ Vb < 2.7 V, Cb = 50 pF, Rb = 2.7 kΩ	200		610		ns
		2.7 V $\leq$ VDD $\leq$ 3.6 V, 2.3 V $\leq$ Vb < 2.7 V, Cb = 100 pF, Rb = 2.7 kΩ	600		610		ns
		1.8 V $\leq$ VDD < 3.3 V, 1.6 V $\leq$ Vb $\leq$ 2.0 V Note 2, Cb = 100 pF, Rb = 5.5 kΩ	610		610		ns
Data setup time (reception)	tSU:DAT	2.7 V $\leq$ VDD $\leq$ 3.6 V, 2.3 V $\leq$ Vb < 2.7 V, Cb = 50 pF, Rb = 2.7 kΩ	1/fMCK + 135 Note 3		1/fMCK + 190 Note 3		ns
		2.7 V $\leq$ VDD $\leq$ 3.6 V, 2.3 V $\leq$ Vb < 2.7 V, Cb = 100 pF, Rb = 2.7 kΩ	1/fMCK + 190 Note 3		1/fMCK + 190 Note 3		ns
		1.8 V $\leq$ VDD < 3.3 V, 1.6 V $\leq$ Vb $\leq$ 2.0 V Note 2, Cb = 100 pF, Rb = 5.5 kΩ	1/fMCK + 190 Note 3		1/fMCK + 190 Note 3		ns
Data hold time (transmission)	tHD:DAT	2.7 V $\leq$ VDD $\leq$ 3.6 V, 2.3 V $\leq$ Vb < 2.7 V, Cb = 50 pF, Rb = 2.7 kΩ	0	305	0	305	ns
		2.7 V $\leq$ VDD $\leq$ 3.6 V, 2.3 V $\leq$ Vb < 2.7 V, Cb = 100 pF, Rb = 2.7 kΩ	0	355	0	355	ns
		1.8 V $\leq$ VDD < 3.3 V, 1.6 V $\leq$ Vb $\leq$ 2.0 V Note 2, Cb = 100 pF, Rb = 5.5 kΩ	0	405	0	405	ns

Note 1. The value must be equal to or less than fMCK/4.

Note 2. Use it with VDD $\geq$ Vb.

Note 3. Set the fMCK value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution **Select the TTL input buffer and the N-ch open drain output (VDD tolerance) mode for the SDAr pin and the N-ch open drain output (VDD tolerance) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the next page.)

Simplified I2C mode connection diagram (during communication at different potential)
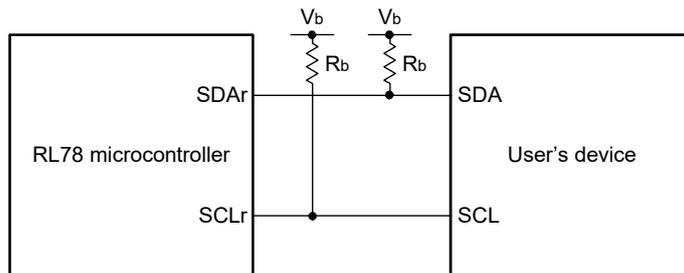
Simplified I2C mode serial transfer timing (during communication at different potential)
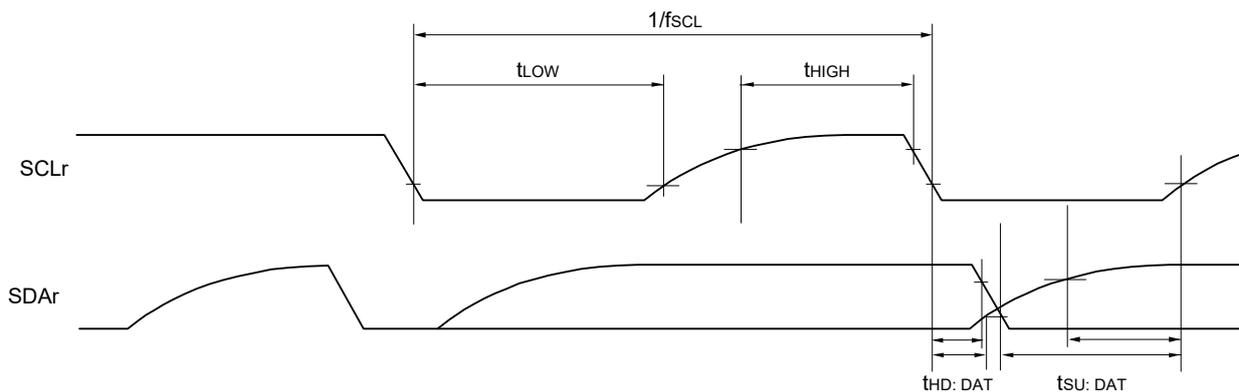
Remark 1. $R_b[\Omega]$: Communication line (SDAr, SCLr) pull-up resistance, $C_b[F]$: Communication line (SDAr, SCLr) load capacitance, $V_b[V]$: Communication line voltage

Remark 2. r: IIC number (r = 00, 10, 20, 30), g: PIM, POM number (g = 0, 1, 3, 4, 8)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1),
n: Channel number (n = 0, 2), mn = 00, 02, 10, 12)

2.5.2   Serial interface IICA

(1)   I²C standard mode

(T$_A$ = -40 to +85°C, 1.8 V $\leq$ V$_{DD}$ $\leq$ 3.6 V, V$_{SS}$ = 0 V)

| Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f$_{SCL}$	Standard mode: f$_{CLK}$ $\geq$ 1 MHz	2.7 V $\leq$ V$_{DD}$ $\leq$ 3.6 V	0	100	0	100	kHz
			1.8 V $\leq$ V$_{DD}$ $\leq$ 3.6 V	—	—	0	100	kHz
Setup time of restart condition	t$_{SU: STA}$	2.7 V $\leq$ V$_{DD}$ $\leq$ 3.6 V		4.7		4.7		μs
		1.8 V $\leq$ V$_{DD}$ $\leq$ 3.6 V		—		4.7		μs
Hold time [Note 1]	t$_{HD: STA}$	2.7 V $\leq$ V$_{DD}$ $\leq$ 3.6 V		4.0		4.0		μs
		1.8 V $\leq$ V$_{DD}$ $\leq$ 3.6 V		—		4.0		μs
Hold time when SCLA0 = "L"	t$_{LOW}$	2.7 V $\leq$ V$_{DD}$ $\leq$ 3.6 V		4.7		4.7		μs
		1.8 V $\leq$ V$_{DD}$ $\leq$ 3.6 V		—		4.7		μs
Hold time when SCLA0 = "H"	t$_{HIGH}$	2.7 V $\leq$ V$_{DD}$ $\leq$ 3.6 V		4.0		4.0		μs
		1.8 V $\leq$ V$_{DD}$ $\leq$ 3.6 V		—		4.0		μs
Data setup time (reception)	t$_{SU: DAT}$	2.7 V $\leq$ V$_{DD}$ $\leq$ 3.6 V		250		250		ns
		1.8 V $\leq$ V$_{DD}$ $\leq$ 3.6 V		—		250		ns
Data hold time (transmission) [Note 2]	t$_{HD: DAT}$	2.7 V $\leq$ V$_{DD}$ $\leq$ 3.6 V		0	3.45	0	3.45	μs
		1.8 V $\leq$ V$_{DD}$ $\leq$ 3.6 V		—		0	3.45	μs
Setup time of stop condition	t$_{SU: STO}$	2.7 V $\leq$ V$_{DD}$ $\leq$ 3.6 V		4.0		4.0		μs
		1.8 V $\leq$ V$_{DD}$ $\leq$ 3.6 V		—		4.0		μs
Bus-free time	t$_{BUF}$	2.7 V $\leq$ V$_{DD}$ $\leq$ 3.6 V		4.7		4.7		μs
		1.8 V $\leq$ V$_{DD}$ $\leq$ 3.6 V		—		4.7		μs

Note 1.   The first clock pulse is generated after this period when the start/restart condition is detected.

Note 2.   The maximum value (MAX.) of t$_{HD:DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Remark   The maximum value of C$_b$ (communication line capacitance) and the value of R$_b$ (communication line pull-up resistor) at that time in each mode are as follows.
Standard mode: C$_b$ = 400 pF, R$_b$ = 2.7 kΩ

(2) I²C fast mode

(T$_A$ = -40 to +85°C, 1.8 V $\leq$ V$_{DD}$ $\leq$ 3.6 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f$_{SCL}$	Fast mode: f$_{CLK}$ $\geq$ 3.5 MHz	2.7 V $\leq$ V$_{DD}$ $\leq$ 3.6 V	0	400	0	400	kHz
			1.8 V $\leq$ V$_{DD}$ $\leq$ 3.6 V	0	400	0	400	kHz
Setup time of restart condition	t$_{SU: STA}$	2.7 V $\leq$ V$_{DD}$ $\leq$ 3.6 V		0.6		0.6		μs
		1.8 V $\leq$ V$_{DD}$ $\leq$ 3.6 V		—		0.6		μs
Hold time Note 1	t$_{HD: STA}$	2.7 V $\leq$ V$_{DD}$ $\leq$ 3.6 V		0.6		0.6		μs
		1.8 V $\leq$ V$_{DD}$ $\leq$ 3.6 V		—		0.6		μs
Hold time when SCLA0 = "L"	t$_{LOW}$	2.7 V $\leq$ V$_{DD}$ $\leq$ 3.6 V		1.3		1.3		μs
		1.8 V $\leq$ V$_{DD}$ $\leq$ 3.6 V		—		1.3		μs
Hold time when SCLA0 = "H"	t$_{HIGH}$	2.7 V $\leq$ V$_{DD}$ $\leq$ 3.6 V		0.6		0.6		μs
		1.8 V $\leq$ V$_{DD}$ $\leq$ 3.6 V		—		0.6		μs
Data setup time (reception)	t$_{SU: DAT}$	2.7 V $\leq$ V$_{DD}$ $\leq$ 3.6 V		100		100		ns
		1.8 V $\leq$ V$_{DD}$ $\leq$ 3.6 V		—		100		ns
Data hold time (transmission) Note 2	t$_{HD: DAT}$	2.7 V $\leq$ V$_{DD}$ $\leq$ 3.6 V		0	0.9	0	0.9	μs
		1.8 V $\leq$ V$_{DD}$ $\leq$ 3.6 V		—		0	0.9	μs
Setup time of stop condition	t$_{SU: STO}$	2.7 V $\leq$ V$_{DD}$ $\leq$ 3.6 V		0.6		0.6		μs
		1.8 V $\leq$ V$_{DD}$ $\leq$ 3.6 V		—		0.6		μs
Bus-free time	t$_{BUF}$	2.7 V $\leq$ V$_{DD}$ $\leq$ 3.6 V		1.3		1.3		μs
		1.8 V $\leq$ V$_{DD}$ $\leq$ 3.6 V		—		1.3		μs

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

Note 2. The maximum value (MAX.) of t$_{HD: DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Remark The maximum value of C$_b$ (communication line capacitance) and the value of R$_b$ (communication line pull-up resistor) at that time in each mode are as follows.
Fast mode: C$_b$ = 320 pF, R$_b$ = 1.1 kΩ

(3) I²C fast mode plus
(T$_A$ = -40 to +85°C, 2.7 V ≤ V$_{DD}$ ≤ 3.6 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f$_{SCL}$	Fast mode plus: f$_{CLK}$ ≥ 10 MHz	2.7 V ≤ V$_{DD}$ ≤ 3.6 V	0	1000	—		kHz
Setup time of restart condition	t$_{SU: STA}$	2.7 V ≤ V$_{DD}$ ≤ 3.6 V		0.26		—		µs
Hold time Note 1	t$_{HD: STA}$	2.7 V ≤ V$_{DD}$ ≤ 3.6 V		0.26		—		µs
Hold time when SCLA0 = "L"	t$_{LOW}$	2.7 V ≤ V$_{DD}$ ≤ 3.6 V		0.5		—		µs
Hold time when SCLA0 = "H"	t$_{HIGH}$	2.7 V ≤ V$_{DD}$ ≤ 3.6 V		0.26		—		µs
Data setup time (reception)	t$_{SU: DAT}$	2.7 V ≤ V$_{DD}$ ≤ 3.6 V		50		—		ns
Data hold time (transmission) Note 2	t$_{HD: DAT}$	2.7 V ≤ V$_{DD}$ ≤ 3.6 V		0	0.45	—		µs
Setup time of stop condition	t$_{SU: STO}$	2.7 V ≤ V$_{DD}$ ≤ 3.6 V		0.26		—		µs
Bus-free time	t$_{BUF}$	2.7 V ≤ V$_{DD}$ ≤ 3.6 V		0.5		—		µs

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.
Note 2. The maximum value (MAX.) of t$_{HD: DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Remark The maximum value of C$_b$ (communication line capacitance) and the value of R$_b$ (communication line pull-up resistor) at that time in each mode are as follows.
Fast mode plus: C$_b$ = 120 pF, R$_b$ = 1.1 kΩ

IICA serial transfer timing
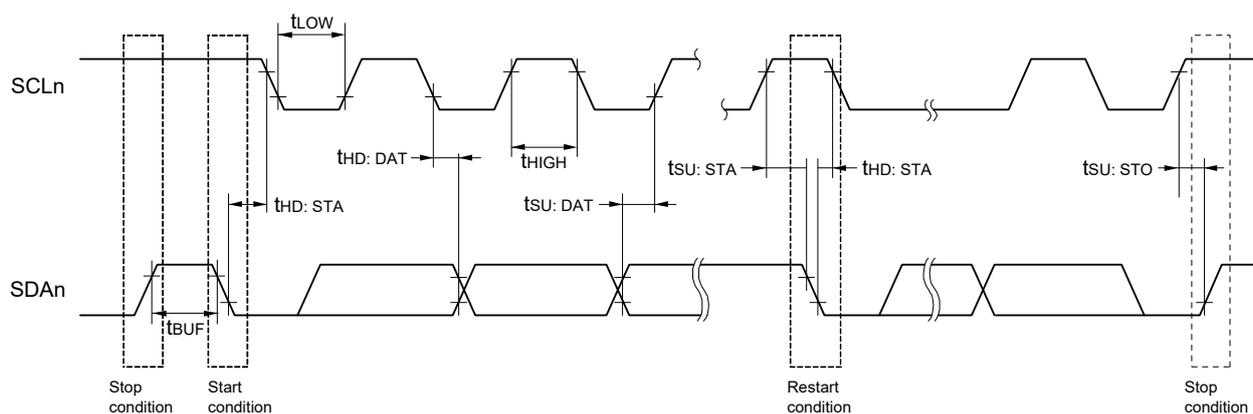
2.6 Analog Characteristics

2.6.1 A/D converter characteristics

(T_A = –40 to +85°C, 1.8 V $\leq$ AV$_{REFP}$ $\leq$ AV$_{DD}$ $\leq$ V$_{DD}$ $\leq$ 3.6 V, V$_{SS}$ = AV$_{SS}$ = 0 V, reference voltage(+) = AV$_{REFP}$, reference voltage(–) = AV$_{REFM}$ = 0 V)

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Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			—	—	12	bit
Analog capacitance	Cs			—	—	15	pF
Analog input resistance	Rs			—	—	2.5	kΩ
Frequency	ADCLK	High-speed mode	2.7 V $\leq$ AV$_{REFP}$ $\leq$ AV$_{DD}$ $\leq$ V$_{DD}$ $\leq$ 3.6 V	1	—	24	MHz
			2.4 V $\leq$ AV$_{REFP}$ $\leq$ AV$_{DD}$ $\leq$ V$_{DD}$ $\leq$ 3.6 V	1	—	16	MHz
		Normal mode	2.7 V $\leq$ AV$_{REFP}$ $\leq$ AV$_{DD}$ $\leq$ V$_{DD}$ $\leq$ 3.6 V	1	—	24	MHz
			2.4 V $\leq$ AV$_{REFP}$ $\leq$ AV$_{DD}$ $\leq$ V$_{DD}$ $\leq$ 3.6 V	1	—	16	MHz
			1.8 V $\leq$ AV$_{REFP}$ $\leq$ AV$_{DD}$ $\leq$ V$_{DD}$ $\leq$ 3.6 V	1	—	8	MHz
Conversion time [Note]	Tconv	High-speed mode ADCSR.ADHSC = 0 ADSSTRn = 28H	2.7 V $\leq$ AV$_{REFP}$ $\leq$ AV$_{DD}$ $\leq$ V$_{DD}$ $\leq$ 3.6 V Permissible signal source impedance max = 0.3 kΩ ADCLK = 24 MHz	3	—	—	µs
			2.4 V $\leq$ AV$_{REFP}$ $\leq$ AV$_{DD}$ $\leq$ V$_{DD}$ $\leq$ 3.6 V Permissible signal source impedance max = 1.3 kΩ ADCLK = 16 MHz	4.5	—	—	µs
		Normal mode ADCSR.ADHSC = 1 ADSSTRn = 28H	2.7 V $\leq$ AV$_{REFP}$ $\leq$ AV$_{DD}$ $\leq$ V$_{DD}$ $\leq$ 3.6 V Permissible signal source impedance max = 1.1 kΩ ADCLK = 24 MHz	3.4	—	—	µs
			2.4 V $\leq$ AV$_{REFP}$ $\leq$ AV$_{DD}$ $\leq$ V$_{DD}$ $\leq$ 3.6 V Permissible signal source impedance max = 2.2 kΩ ADCLK = 16 MHz	5.1	—	—	µs
			1.8 V $\leq$ AV$_{REFP}$ $\leq$ AV$_{DD}$ $\leq$ V$_{DD}$ $\leq$ 3.6 V Permissible signal source impedance max = 5 kΩ ADCLK = 8 MHz	10.1	—	—	µs
Overall error	AINL	High-speed mode ADCSR.ADHSC = 0 ADSSTRn = 28 H	2.7 V $\leq$ AV$_{REFP}$ $\leq$ AV$_{DD}$ $\leq$ V$_{DD}$ $\leq$ 3.6 V	—	±1.25	±5.0	LSB
			2.4 V $\leq$ AV$_{REFP}$ $\leq$ AV$_{DD}$ $\leq$ V$_{DD}$ $\leq$ 3.6 V	—	±1.25	±5.0	LSB
		Normal mode ADCSR.ADHSC = 1 ADSSTRn = 28H	2.7 V $\leq$ AV$_{REFP}$ $\leq$ AV$_{DD}$ $\leq$ V$_{DD}$ $\leq$ 3.6 V	—	±1.25	±5.0	LSB
			2.4 V $\leq$ AV$_{REFP}$ $\leq$ AV$_{DD}$ $\leq$ V$_{DD}$ $\leq$ 3.6 V	—	±1.25	±5.0	LSB
			1.8 V $\leq$ AV$_{REFP}$ $\leq$ AV$_{DD}$ $\leq$ V$_{DD}$ $\leq$ 3.6 V	—	±3.0	±8.0	LSB
Zero-scale error	Ezs	High-speed mode ADCSR.ADHSC = 0 ADSSTRn = 28H	2.7 V $\leq$ AV$_{REFP}$ $\leq$ AV$_{DD}$ $\leq$ V$_{DD}$ $\leq$ 3.6 V	—	±0.5	±4.5	LSB
			2.4 V $\leq$ AV$_{REFP}$ $\leq$ AV$_{DD}$ $\leq$ V$_{DD}$ $\leq$ 3.6 V	—	±0.5	±4.5	LSB
		Normal mode ADCSR.ADHSC = 1 ADSSTRn = 28H	2.7 V $\leq$ AV$_{REFP}$ $\leq$ AV$_{DD}$ $\leq$ V$_{DD}$ $\leq$ 3.6 V	—	±0.5	±4.5	LSB
			2.4 V $\leq$ AV$_{REFP}$ $\leq$ AV$_{DD}$ $\leq$ V$_{DD}$ $\leq$ 3.6 V	—	±0.5	±4.5	LSB
			1.8 V $\leq$ AV$_{REFP}$ $\leq$ AV$_{DD}$ $\leq$ V$_{DD}$ $\leq$ 3.6 V	—	±1	±7.5	LSB

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Full-scale error	EFS	High-speed mode ADCSR.ADHSC = 0 ADSSTRn = 28H	2.7 V ≤ AVREFP ≤ AVDD ≤ VDD ≤ 3.6 V	—	±0.75	±4.5	LSB
			2.4 V ≤ AVREFP ≤ AVDD ≤ VDD ≤ 3.6 V	—	±0.75	±4.5	LSB
		Normal mode ADCSR.ADHSC = 1 ADSSTRn = 28H	2.7 V ≤ AVREFP ≤ AVDD ≤ VDD ≤ 3.6 V	—	±0.75	±4.5	LSB
			2.4 V ≤ AVREFP ≤ AVDD ≤ VDD ≤ 3.6 V	—	±0.75	±4.5	LSB
			1.8 V ≤ AVREFP ≤ AVDD ≤ VDD ≤ 3.6 V	—	±1.5	±7.5	LSB
Differential linearity error	DLE	High-speed mode ADCSR.ADHSC = 0 ADSSTRn = 28H	2.7 V ≤ AVREFP ≤ AVDD ≤ VDD ≤ 3.6 V	—	±1.0	—	LSB
			2.4 V ≤ AVREFP ≤ AVDD ≤ VDD ≤ 3.6 V	—	±1.0	—	LSB
		Normal mode ADCSR.ADHSC = 1 ADSSTRn = 28H	2.7 V ≤ AVREFP ≤ AVDD ≤ VDD ≤ 3.6 V	—	±1.0	—	LSB
			2.4 V ≤ AVREFP ≤ AVDD ≤ VDD ≤ 3.6 V	—	±1.0	—	LSB
			1.8 V ≤ AVREFP ≤ AVDD ≤ VDD ≤ 3.6 V	—	±1.0	—	LSB
Integral linearity error	ILE	High-speed mode ADCSR.ADHSC = 0 ADSSTRn = 28H	2.7 V ≤ AVREFP ≤ AVDD ≤ VDD ≤ 3.6 V	—	±1.0	±3.0	LSB
			2.4 V ≤ AVREFP ≤ AVDD ≤ VDD ≤ 3.6 V	—	±1.0	±4.5	LSB
		Normal mode ADCSR.ADHSC =1 ADSSTRn = 28H	2.7 V ≤ AVREFP ≤ AVDD ≤ VDD ≤ 3.6 V	—	±1.0	±3.0	LSB
			2.4 V ≤ AVREFP ≤ AVDD ≤ VDD ≤ 3.6 V	—	±1.0	±3.0	LSB
			1.8 V ≤ AVREFP ≤ AVDD ≤ VDD ≤ 3.6 V	—	±1.25	±3.0	LSB

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<R> **Note** The conversion time is the sum of sampling time and comparison time. The values indicated in the table are those in the case of 40 clock cycles of ADCLK per sampling state.

Caution **The characteristics above only apply when pins other than those of the A/D converter are not in use. The overall error includes the quantization error. Each of the offset error, full-scale error, DNL differential non-linearity error, and INL integral non-linearity error does not include the quantization error.**

[Reference value for design (not guaranteed)]
We can provide the design reference values for the A/D converter. Note, however, that these values are not guaranteed and can only be used as a reference when using this function. See below for details.

(TA = 0 to +50°C, 2.0 V ≤ AVREFP ≤ AVDD ≤ VDD ≤ 3.6 V, VSS = AVSS = 0 V, reference voltage(+) = AVREFP, reference voltage(–) = AVREFM = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			—	—	—Note 3	bit
Analog capacitance	Cs			—	—	—Note 3	pF
Analog input resistance	Rs			—	—	—Note 3	kΩ
Frequency	fCLK	High-speed mode	2.7 V ≤ AVREFP ≤ AVDD ≤ VDD ≤ 3.6 V	—Note 3	—	—Note 3	MHz
			2.4 V ≤ AVREFP ≤ AVDD ≤ VDD ≤ 3.6 V	—Note 3	—	—Note 3	MHz
		Normal mode	2.7 V ≤ AVREFP ≤ AVDD ≤ VDD ≤ 3.6 V	—Note 3	—	—Note 3	MHz
			2.4 V ≤ AVREFP ≤ AVDD ≤ VDD ≤ 3.6 V	—Note 3	—	—Note 3	MHz
			2.0 V ≤ AVREFP ≤ AVDD ≤ VDD ≤ 3.6 V	—Note 3	—	—Note 3	MHz

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Conversion time	Tconv	High-speed mode ADCSR.ADHSC = 0 ADSSTRn = 28H	2.7 V ≤ AVREFP ≤ AVDD ≤ VDD ≤ 3.6 V Permissible signal source impedance max = 0.3 kΩ ADCLK = 24 MHz	Note 3	—	—	µs
			2.4 V ≤ AVREFP ≤ AVDD ≤ VDD ≤ 3.6 V Permissible signal source impedance max = 1.3 kΩ ADCLK = 16 MHz	Note 3	—	—	µs
		Normal mode ADCSR.ADHSC = 1 ADSSTRn = 28H	2.7 V ≤ AVREFP ≤ AVDD ≤ VDD ≤ 3.6 V Permissible signal source impedance max = 1.1 kΩ ADCLK = 24 MHz	Note 3	—	—	µs
			2.4 V ≤ AVREFP ≤ AVDD ≤ VDD ≤ 3.6 V Permissible signal source impedance max = 2.2 kΩ ADCLK = 16 MHz	Note 3	—	—	µs
			2.0 V ≤ AVREFP ≤ AVDD ≤ VDD ≤ 3.6 V Permissible signal source impedance max = 5 kΩ ADCLK = 8 MHz	Note 3	—	—	µs
Overall error	AINL	High-speed mode ADCSR.ADHSC = 0 ADSSTRn = 28H	2.7 V ≤ AVREFP ≤ AVDD ≤ VDD ≤ 3.6 V	—	Note 3	Note 3	LSB
			2.4 V ≤ AVREFP ≤ AVDD ≤ VDD ≤ 3.6 V	—	Note 3	Note 3	LSB
		Normal mode ADCSR.ADHSC = 1 ADSSTRn = 28H	2.7 V ≤ AVREFP ≤ AVDD ≤ VDD ≤ 3.6 V	—	Note 3	Note 3	LSB
			2.4 V ≤ AVREFP ≤ AVDD ≤ VDD ≤ 3.6 V	—	Note 3	Note 3	LSB
			2.0 V ≤ AVREFP ≤ AVDD ≤ VDD ≤ 3.6 V	—	Note 3	Note 3	LSB
Zero-scale error Notes 1, 2	Ezs	High-speed mode ADCSR.ADHSC = 0 ADSSTRn = 28H	2.7 V ≤ AVREFP ≤ AVDD ≤ VDD ≤ 3.6 V	—	Note 3	Note 3	LSB
			2.4 V ≤ AVREFP ≤ AVDD ≤ VDD ≤ 3.6 V	—	Note 3	Note 3	LSB
		Normal mode ADCSR.ADHSC = 1 ADSSTRn = 28H	2.7 V ≤ AVREFP ≤ AVDD ≤ VDD ≤ 3.6 V	—	Note 3	Note 3	LSB
			2.4 V ≤ AVREFP ≤ AVDD ≤ VDD ≤ 3.6 V	—	Note 3	Note 3	LSB
			2.0 V ≤ AVREFP ≤ AVDD ≤ VDD ≤ 3.6 V	—	Note 3	±4.5	LSB
Full-scale error Notes 1, 2	EFS	High-speed mode ADCSR.ADHSC = 0 ADSSTRn = 28H	2.7 V ≤ AVREFP ≤ AVDD ≤ VDD ≤ 3.6 V	—	Note 3	Note 3	LSB
			2.4 V ≤ AVREFP ≤ AVDD ≤ VDD ≤ 3.6 V	—	Note 3	Note 3	LSB
		Normal mode ADCSR.ADHSC = 1 ADSSTRn = 28H	2.7 V ≤ AVREFP ≤ AVDD ≤ VDD ≤ 3.6 V	—	Note 3	Note 3	LSB
			2.4 V ≤ AVREFP ≤ AVDD ≤ VDD ≤ 3.6 V	—	Note 3	Note 3	LSB
			2.0 V ≤ AVREFP ≤ AVDD ≤ VDD ≤ 3.6 V	—	Note 3	±4.5	LSB
Differential linearity error	DLE	High-speed mode ADCSR.ADHSC = 0 ADSSTRn = 28H	2.7 V ≤ AVREFP ≤ AVDD ≤ VDD ≤ 3.6 V	—	Note 3	—	LSB
			2.4 V ≤ AVREFP ≤ AVDD ≤ VDD ≤ 3.6 V	—	Note 3	—	LSB
		Normal mode ADCSR.ADHSC = 1 ADSSTRn = 28H	2.7 V ≤ AVREFP ≤ AVDD ≤ VDD ≤ 3.6 V	—	Note 3	—	LSB
			2.4 V ≤ AVREFP ≤ AVDD ≤ VDD ≤ 3.6 V	—	Note 3	—	LSB
			2.0 V ≤ AVREFP ≤ AVDD ≤ VDD ≤ 3.6 V	—	Note 3	—	LSB
Integral linearity error	ILE	High-speed mode ADCSR.ADHSC = 0 ADSSTRn = 28H	2.7 V ≤ AVREFP ≤ AVDD ≤ VDD ≤ 3.6 V	—	Note 3	Note 3	LSB
			2.4 V ≤ AVREFP ≤ AVDD ≤ VDD ≤ 3.6 V	—	Note 3	Note 3	LSB
		Normal mode ADCSR.ADHSC = 1 ADSSTRn = 28H	2.7 V ≤ AVREFP ≤ AVDD ≤ VDD ≤ 3.6 V	—	Note 3	Note 3	LSB
			2.4 V ≤ AVREFP ≤ AVDD ≤ VDD ≤ 3.6 V	—	Note 3	Note 3	LSB
			2.0 V ≤ AVREFP ≤ AVDD ≤ VDD ≤ 3.6 V	—	Note 3	Note 3	LSB

Note 1. MAX. value is the average value ±3σ at normalized distribution.

Note 2. These values are the results of characteristic evaluation.

Note 3. The reference value is not available.

Caution **The characteristics above only apply when pins other than those of the A/D converter are not in use. The overall error includes the quantization error. Each of the offset error, full-scale error, DNL differential non-linearity error, and INL integral non-linearity error does not include the quantization error.**

2.6.2 Temperature sensor, internal reference voltage output characteristics

(TA = -40 to +85°C, 2.4 V $\leq$ VDD $\leq$ 3.6 V, VSS = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	VTMPS25	TA = +25°C	—	1.05	—	V
Internal reference voltage	VBGR		1.38	1.45	1.5	V
Temperature coefficient	FVTMPS	Temperature sensor output voltage that depends on the temperature	—	-3.6	—	mV/°C
Operation stabilization wait time	tAMP	2.4 V $\leq$ VDD $\leq$ 3.6 V	5	—	—	µs

2.6.3   D/A converter characteristics

(1) When reference voltage = AV$_{REFP}$, AV$_{REFM}$

(T$_A$ = -40 to +85°C, 1.8 V $\leq$ AV$_{REFP}$ $\leq$ AV$_{DD}$ $\leq$ V$_{DD}$ $\leq$ 3.6 V, V$_{SS}$ = AV$_{SS}$ = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	R$_{ES}$				12	bit
Load resistance	R0		30			kΩ
Load capacitance	C0				50	pF
Output voltage range	T$_{out}$		0.35		AV$_{DD}$ - 0.47	V
Differential linearity error	DNL			±0.5	±1.0	LSB
Integral linearity error	AINL			±0.4	±8.0	LSB
Zero-scale error	E$_{ZS}$				±20	mV
Full-scale error	E$_{FS}$				±20	mV
Output resistance	R$_O$			5		Ω
Conversion time	t$_{con}$				30	μs

(2) When reference voltage = AV$_{DD}$, AV$_{SS}$

(T$_A$ = -40 to +85°C, 1.8 V $\leq$ AV$_{DD}$ $\leq$ V$_{DD}$ $\leq$ 3.6 V, V$_{SS}$ = AV$_{SS}$ = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	R$_{ES}$				12	bit
Load resistance	R0		30			kΩ
Load capacitance	C0				50	pF
Output voltage range	T$_{out}$		0.35		AV$_{DD}$ - 0.47	V
Differential linearity error	DNL			±0.5	±2.0	LSB
Integral linearity error	AINL			±0.4	±8.0	LSB
Zero-scale error	E$_{ZS}$				±30	mV
Full-scale error	E$_{FS}$				±30	mV
Output resistance	R$_O$			5		Ω
Conversion time	t$_{con}$				30	μs

2.6.4   Comparator

(T$_A$ = -40 to +85°C, 1.8 V $\leq$ V$_{DD}$ $\leq$ 3.6 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage range	Ivref			0		V$_{DD}$ - 1.4	V
	Ivcmp			-0.3		V$_{DD}$ + 0.3	V
Output delay	td	V$_{DD}$ = 3.0 V Input slew rate > 50 mV/μs	Comparator high-speed mode, standard mode			1.2	μs
			Comparator high-speed mode, window mode			2.0	μs
			Comparator low-speed mode, standard mode		3	5.0	μs
High-electric-potential judgment voltage	V$_{TW+}$	Comparator high-speed mode, window mode			0.76 V$_{DD}$		V
Low-electric-potential judgment voltage	V$_{TW-}$	Comparator high-speed mode, window mode			0.24 V$_{DD}$		V
Operation stabilization wait time	tCMP			100			μs
Internal reference voltage [Note]	V$_{BGR}$	2.4 V $\leq$ V$_{DD}$ $\leq$ 3.6 V, HS (high-speed main) mode		1.38	1.45	1.50	V

<R>

Note   Not usable in LS (low-speed main) mode, subsystem clock operation, or STOP mode.

2.6.5 Rail to rail operational amplifier characteristics

(TA = -40 to +85°C, 2.2 V ≤ AVDD ≤ VDD ≤ 3.6 V, AVSS = VSS = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Circuit current	Icc1	Low-power consumption mode		—	10	16	μA
	Icc2	High-speed mode		—	210	350	μA
Common mode input range	Vicm1	Low-power consumption mode		0.1	—	AVDD-0.1	V
	Vicm2	High-speed mode		0.1	—	AVDD-0.1	V
Output voltage range	Vo1	Low-power consumption mode		0.1	—	AVDD-0.1	V
	Vo2	High-speed mode		0.1	—	AVDD-0.1	V
Input offset voltage	Fioff	Low-power consumption mode		-10	—	10	mV
		High-speed mode		-5	—	5	mV
Open gain	Av			—	120	—	dB
Gain-bandwidth (GB) product	GBW1	Low-power consumption mode		—	0.06	—	MHz
	GBW2	High-speed mode		—	1	—	MHz
Phase margin	PM	CL = 22 pF		50	—	—	deg
Gain margin	GM	CL = 20 pF		10	—	—	dB
Equivalent input noise	Vnoise1	f = 1 kHz	Low-power consumption mode	—	900	—	nV/√Hz
	Vnoise2	f = 10 kHz		—	450	—	nV/√Hz
	Vnoise3	f = 1 kHz	High-speed mode	—	80	—	nV/√Hz
	Vnoise4	f = 2 kHz		—	50	—	nV/√Hz
Power supply reduction ratio	PSRR			—	90	—	dB
Common mode signal reduction ratio	CMRR			—	90	—	dB
Operation stabilization wait time	Tstd1	CL = 20 pF	Low-power consumption mode	—	110	300	μs
	Tstd2	CL = 20 pF	High-speed mode	—	5	14	μs
Settling time	Tset1	CL = 20 pF	Low-power consumption mode	—	110	300	μs
	Tset2	CL = 20 pF	High-speed mode	—	4	14	μs
Slew rate	Tselw1	CL = 20 pF	Low-power consumption mode	0.01	0.04	—	V/μs
	Tselw2	CL = 20 pF	High-speed mode	0.3	0.7	—	V/μs
Load current	Iload1	Low-power consumption mode		-110	—	110	μA
	Iload2	High-speed mode		-110	—	110	μA
Load capacitance	CL			—	—	22	pF
Analog MUX ON resistance	Ron	One channel		—	—	1	kΩ

<R> (rows: Operation stabilization wait time, Settling time)

[Reference value for design (not guaranteed)]

We can provide the design reference values for the rail-to-rail operational amplifier. Note, however, that these values are not guaranteed and can only be used as a reference when using this function. See below for details.

(TA = 0 to 50°C, 2.0 V $\leq$ AVDD $\leq$ VDD $\leq$ 3.6 V, AVSS = VSS = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Circuit current	Icc1	Low-power consumption mode		—	—Note 3	—Note 3	µA
	Icc2	High-speed mode		—	—Note 3	—Note 3	µA
Common mode input range	Vicm1	Low-power consumption mode		—Note 3	—	—Note 3	V
	Vicm2	High-speed mode		—Note 3	—	—Note 3	V
Output voltage range	Vo1	Low-power consumption mode		—Note 3	—	—Note 3	V
	Vo2	High-speed mode		—Note 3	—	—Note 3	V
Input offset voltage Note 1, Note 2	Fioff	Low-power consumption mode		−7	—	7	mV
		High-speed mode		—Note 3	—	—Note 3	mV
Open gain	Av			—Note 3	—Note 3	—	dB
Gain-bandwidth (GB) product	GBW1	Low-power consumption mode		—	—Note 3	—	MHz
	GBW2	High-speed mode		—	—Note 3	—	MHz
Phase margin	PM	CL = 22 pF		—Note 3	—	—	deg
Gain margin	GM	CL = 20 pF		—Note 3	—	—	dB
Equivalent input noise	Vnoise1	f = 1 kHz	Low-power consumption mode	—	—Note 3	—	nV/√Hz
	Vnoise2	f = 10 kHz		—	—Note 3	—	nV/√Hz
	Vnoise3	f = 1 kHz	High-speed mode	—	—Note 3	—	nV/√Hz
	Vnoise4	f = 2 kHz		—	—Note 3	—	nV/√Hz
Power supply reduction ratio	PSRR			—	—Note 3	—	dB
Common mode signal reduction ratio	CMRR			—	—Note 3	—	dB
Operation stabilization wait time	Tstd1	CL = 20 pF	Low-power consumption mode	—	—Note 3	—Note 3	µs
	Tstd2	CL = 20 pF	High-speed mode	—	—Note 3	—Note 3	µs
Settling time	Tset1	CL = 20 pF	Low-power consumption mode	—	—Note 3	—Note 3	µs
	Tset2	CL = 20 pF	High-speed mode	—	—Note 3	—Note 3	µs
Slew rate	Tselw1	CL = 20 pF	Low-power consumption mode	—Note 3	—Note 3	—	V/µs
	Tselw2	CL = 20 pF	High-speed mode	—Note 3	—Note 3	—	V/µs
Load current	Iload1	Low-power consumption mode		—Note 3	—	—Note 3	µA
	Iload2	High-speed mode		—Note 3	—	—Note 3	µA
Load capacitance	CL			—	—	—Note 3	pF
Analog MUX ON resistance	Ron	One channel		—	—	—Note 3	kΩ

Note 1. MAX. value is the average value ±3σ at normalized distribution.

Note 2. These values are the results of characteristic evaluation.

Note 3. The reference value is not available.

2.6.6   General purpose operational amplifier characteristics

(TA = -40 to +85°C, 1.8 V $\leq$ AVDD $\leq$ VDD $\leq$ 3.6 V, AVSS = VSS = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Circuit current	ICC1	Low-power consumption mode			2	4	μA
	ICC2	High-speed mode			140	280	μA
Common mode input range	Vicm1	Low-power consumption mode		0.2		AVDD-0.5	V
	Vicm2	High-speed mode		0.3		AVDD-0.6	V
Output voltage range	Vo1	Low-power consumption mode		0.1		AVDD-0.1	V
	Vo2	High-speed mode		0.1		AVDD-0.1	V
Input offset voltage	Fioff	3σ		-10		+10	mV
Open gain	Av			60	120		dB
Gain-bandwidth (GB) product	GBW1	Low-power consumption mode			0.04		MHz
	GBW2	High-speed mode			1.7		MHz
Phase margin	PM	CL = 20 pF		50			deg
Gain margin	GM	CL = 20 pF		10			dB
Equivalent input noise	Vnoise1	f = 1 kHz	Low-power consumption mode		230		nV/√‾Hz
	Vnoise2	f = 10 kHz			200		nV/√‾Hz
	Vnoise3	f = 1 kHz	High-speed mode		90		nV/√‾Hz
	Vnoise4	f = 2 kHz			70		nV/√‾Hz
Power supply reduction ratio	PSRR				90		dB
Common mode signal reduction ratio	CMRR				90		dB
Operation stabilization wait time	Tstd1	CL = 20 pF	Low-power consumption mode			650	μs
	Tstd2	CL = 20 pF	High-speed mode			13	μs
Settling time	Tset1	CL = 20 pF	Low-power consumption mode			750	μs
	Tset2	CL = 20 pF	High-speed mode			13	μs
Slew rate	Tselw1	CL = 20 pF	Low-power consumption mode		0.02		V/μs
	Tselw2	CL = 20 pF	High-speed mode		1.1		V/μs
Load current	Iload1	Low-power consumption mode		-100		100	μA
	Iload2	High-speed mode		-100		100	μA
Load capacitance	CL					20	pF

<R>   ## 2.6.7   Voltage reference

(T$_A$ = -40 to +85°C, 1.8 V $\leq$ AV$_{DD}$ $\leq$ V$_{DD}$ $\leq$ 3.6 V, AV$_{SS}$ = V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Reference voltage output Note 2	V$_{REF1}$	VSEL = 00, 2.65 V $\leq$ AV$_{DD}$ $\leq$ 3.6V	2.425	2.5	2.575	V
	V$_{REF2}$	VSEL = 01, 2.2 V $\leq$ AV$_{DD}$ $\leq$ 3.6V	1.987	2.048	2.109	V
	V$_{REF3}$	VSEL = 10, 2.0 V $\leq$ AV$_{DD}$ $\leq$ 3.6V	1.746	1.8	1.854	V
	V$_{REF4}$	VSEL = 11, 1.8 V $\leq$ AV$_{DD}$ $\leq$ 3.6V	1.455	1.5	1.545	V
Settling time		From power-on to AV$_{DD}$ settling (external capacitance: 10 µF)			50	ms
Load current of the AV$_{REFP}$/VREFOUT pin Notes 1, 3	I$_{Load}$				200	µA

Note 1. Connect AV$_{REFP}$/AVREFOUT pins to the ground via a tantalum capacitor (capacity: 10 µF ±30%, ESR: 2Ω (max.), ESL: 10 nH (max.)) and a ceramic capacitor (capacity: 0.1 µF ±30%, ESR: 2Ω (max.), ESL: 10nH (max.)).
Note 2. The values specified in the Reference voltage output column apply when a load is stable. These values cannot be guaranteed when the load is variable.
Note 3. Total load current, including the load current when AV$_{REFP}$/VREFOUT is in use for the on-chip A/D converter and D/A converter reference potential.
When AV$_{REFP}$/VREFOUT is in use for the on-chip A/D converter load reference, the maximum load current is 55 µA.
When AV$_{REFP}$/VREFOUT is in use for the on-chip D/A converter (channel 1), the maximum load current is 55 µA.

<R>   ## 2.6.8   1/2 AV$_{DD}$ voltage output

(T$_A$ = -40 to +85°C, 1.8 V $\leq$ AV$_{DD}$ $\leq$ V$_{DD}$ $\leq$ 3.6 V, AV$_{SS}$ = V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output voltage accuracy			-4.0		+4.0	%
Sampling time for the corresponding channel			20.0			µs

2.6.9   POR circuit characteristics

(TA = -40 to +85°C, VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	VPOR	Power supply rise time	1.47	1.51	1.55	V
	VPDR	Power supply fall timeNote 1	1.46	1.50	1.54	V
Minimum pulse width Note 2	TPW1	Other than STOP/SUB HALT/SUB RUN	300			μs
	TPW2	STOP/SUB HALT/SUB RUN	300			μs

Note 1.   If the power supply voltage falls while the voltage detector is off, be sure to either shift to STOP mode or execute a reset by using the voltage detector or external reset pin before the power supply voltage falls below the minimum operating voltage specified in 2.4 AC Characteristics.

Note 2.   Minimum time required for a POR reset when VDD exceeds below VPDR. This is also the minimum time required for a POR reset from when VDD exceeds below 0.7 V to when VDD exceeds VPOR while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).
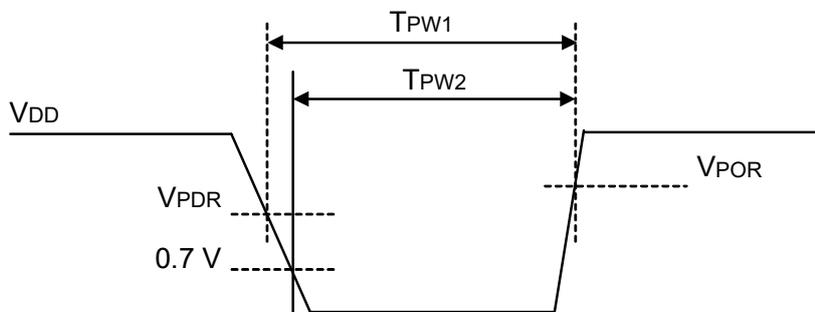
2.6.10   LVD circuit characteristics

LVD Detection Voltage of Reset Mode and Interrupt Mode
(T_A = -40 to +85°C, $V_{PDR} \leq V_{DD} \leq$ 3.6 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{LVD2}	Power supply rise time	3.07	3.13	3.19	V
		Power supply fall time	3.00	3.06	3.12	V
	V_{LVD3}	Power supply rise time	2.96	3.02	3.08	V
		Power supply fall time	2.90	2.96	3.02	V
	V_{LVD4}	Power supply rise time	2.86	2.92	2.97	V
		Power supply fall time	2.80	2.86	2.91	V
	V_{LVD5}	Power supply rise time	2.76	2.81	2.87	V
		Power supply fall time	2.70	2.75	2.81	V
	V_{LVD6}	Power supply rise time	2.66	2.71	2.76	V
		Power supply fall time	2.60	2.65	2.70	V
	V_{LVD7}	Power supply rise time	2.56	2.61	2.66	V
		Power supply fall time	2.50	2.55	2.60	V
	V_{LVD8}	Power supply rise time	2.45	2.50	2.55	V
		Power supply fall time	2.40	2.45	2.50	V
	V_{LVD9}	Power supply rise time	2.05	2.09	2.13	V
		Power supply fall time	2.00	2.04	2.08	V
	V_{LVD10}	Power supply rise time	1.94	1.98	2.02	V
		Power supply fall time	1.90	1.94	1.98	V
	V_{LVD11}	Power supply rise time	1.84	1.88	1.91	V
		Power supply fall time	1.80	1.84	1.87	V
Minimum pulse width	t_{LW}		300			μs
Detection delay time					300	μs

Caution   **Set the detection voltage (V_{LVD}) to be within the operating voltage range. The operating voltage range depends on the setting of the user option byte (000C2H/010C2H). The following shows the operating voltage range.**
HS (high-speed main) mode: V_{DD} = 2.7 to 3.6 V @ 1 MHz to 24 MHz
V_{DD} = 2.4 to 3.6 V @ 1 MHz to 16 MHz
LS (low-speed main) mode: V_{DD} = 1.8 to 3.6 V @ 1 MHz to 8 MHz

LVD Detection Voltage of Interrupt & Reset Mode

(TA = -40 to +85°C, VPDR ≤ VDD ≤ 3.6 V, VSS = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Detection voltage	VLVDB0	VPOC0, VPOC1, VPOC2 = 0, 0, 1, falling reset voltage: 1.8 V			1.80	1.84	1.87	V
	VLVDB1	LVIS0, LVIS1 = 1, 0		Rising release reset voltage	1.94	1.98	2.02	V
				Falling interrupt voltage	1.90	1.94	1.98	V
	VLVDB2	LVIS0, LVIS1 = 0, 1		Rising release reset voltage	2.05	2.09	2.13	V
				Falling interrupt voltage	2.00	2.04	2.08	V
	VLVDB3	LVIS0, LVIS1 = 0, 0		Rising release reset voltage	3.07	3.13	3.19	V
				Falling interrupt voltage	3.00	3.06	3.12	V
	VLVDC0	VPOC0, VPOC1, VPOC2 = 0, 1, 0, falling reset voltage: 2.4 V			2.40	2.45	2.50	V
	VLVDC1	LVIS0, LVIS1 = 1, 0		Rising release reset voltage	2.56	2.61	2.66	V
				Falling interrupt voltage	2.50	2.55	2.60	V
	VLVDC2	LVIS0, LVIS1 = 0, 1		Rising release reset voltage	2.66	2.71	2.76	V
				Falling interrupt voltage	2.60	2.65	2.70	V
	VLVDD0	VPOC0, VPOC1, VPOC2 = 0, 1, 1, falling reset voltage: 2.7 V			2.70	2.75	2.81	V
	VLVDD1	LVIS0, LVIS1 = 1, 0		Rising release reset voltage	2.86	2.92	2.97	V
				Falling interrupt voltage	2.80	2.86	2.91	V
	VLVDD2	LVIS0, LVIS1 = 0, 1		Rising release reset voltage	2.96	3.02	3.08	V
				Falling interrupt voltage	2.90	2.96	3.02	V

2.6.11 Low-resistance switch

(TA = –40 to + 85°C, 1.8 V ≤ AVDD ≤ VDD ≤ 3.6 V, AVSS = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ON resistance 1	Ron1	AMP0OPD, AMP1OPD Load current < 0.1 mA	—	16	50	Ω
ON resistance 2	Ron2	AMP2OPD Load current < 0.1 mA	—	10	30	
Load current	Icas	—	—	—	0.1	mA

[Reference value for design (not guaranteed)]
We can provide the design reference values for the low-resistance switch. Note, however, that these values are not guaranteed and can only be used as a reference when using this function. See below for details.

(TA = 0 to + 50°C, 2.0 V ≤ AVDD ≤ VDD ≤ 3.6 V, AVSS = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ON resistance 1 Note 1, Note 2	Ron1	AMP0OPD, AMP1OPD Load current < 0.1 mA	—	—Note 3	26	Ω
ON resistance 2 Note 1, Note 2	Ron2	AMP2OPD Load current < 0.1 mA	—	—Note 3	15	
Load current	Icas	—	—	—	—Note 3	mA

Note 1.   MAX. value is the average value ±3σ at normalized distribution.
Note 2.   These values are the results of characteristic evaluation.
Note 3.   The reference value is not available.

2.7 Power supply voltage rising slope characteristics

(T_A = -40 to +85°C, V_{SS} = 0 V)

Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	SV_{DD}			54	V/ms

Caution 1. Make sure to keep the internal reset state by the LVD circuit or an external reset until V_{DD} reaches the operating voltage range shown in 2.4 AC Characteristics.

<R>　Caution 2. When the voltages for V_{DD} and AV_{DD} differ and they rise at different rates, if AV_{DD} is lower than 0.8 V at the time of the release from the internal reset state by the power-on reset (POR) circuit, the chip may not start normally. In such cases, apply either of the following countermeasures.
　　　　　　• Hold AV_{DD} ≥ 0.8 V until V_{DD} ≥ 1.47 V.
　　　　　　• Hold the $\overline{RESET}$ pin low until V_{DD} ≥ 1.47 V and AV_{DD} ≥ 0.8 V.

2.8 LCD Characteristics

2.8.1 Resistance division method

(1) Static display mode

(T_A = -40 to +85°C, V_{L4} (MIN.) ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{L4}		2.0		V_{DD}	V

(2) 1/2 bias method, 1/4 bias method

(T_A = -40 to +85°C, V_{L4} (MIN.) ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{L4}		2.7		V_{DD}	V

(3) 1/3 bias method

(T_A = -40 to +85°C, V_{L4} (MIN.) ≤ V_{DD} ≤ 3.6 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{L4}		2.5		V_{DD}	V

2.8.2　Internal voltage boosting method

(1)　1/3 bias method

(T_A = -40 to +85°C, 1.8 V $\leq$ V_{DD} $\leq$ 3.6 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
LCD output voltage variation range	V_{L1}	C1 to C4 Note 1 = 0.47 µF Note 2	VLCD = 04H	0.90	1.00	1.08	V
			VLCD = 05H	0.95	1.05	1.13	V
			VLCD = 06H	1.00	1.10	1.18	V
			VLCD = 07H	1.05	1.15	1.23	V
			VLCD = 08H	1.10	1.20	1.28	V
			VLCD = 09H	1.15	1.25	1.33	V
			VLCD = 0AH	1.20	1.30	1.38	V
			VLCD = 0BH	1.25	1.35	1.43	V
			VLCD = 0CH	1.30	1.40	1.48	V
			VLCD = 0DH	1.35	1.45	1.53	V
			VLCD = 0EH	1.40	1.50	1.58	V
			VLCD = 0FH	1.45	1.55	1.63	V
			VLCD = 10H	1.50	1.60	1.68	V
			VLCD = 11H	1.55	1.65	1.73	V
			VLCD = 12H	1.60	1.70	1.78	V
			VLCD = 13H	1.65	1.75	1.83	V
Doubler output voltage	V_{L2}	C1 to C4 Note 1 = 0.47 µF		2 V_{L1} - 0.1	2 V_{L1}	2 V_{L1}	V
Tripler output voltage	V_{L4}	C1 to C4 Note 1 = 0.47 µF		3 V_{L1} - 0.15	3 V_{L1}	3 V_{L1}	V
Reference voltage setup time Note 2	t_{VWAIT1}			5			ms
Voltage boost wait time Note 3	t_{VWAIT2}	C1 to C4 Note 1 = 0.47µF		500			ms

Note 1.　This is a capacitor that is connected between voltage pins used to drive the LCD.

　　　　　C1: A capacitor connected between CAPH and CAPL

　　　　　C2: A capacitor connected between V_{L1} and GND

　　　　　C3: A capacitor connected between V_{L2} and GND

　　　　　C4: A capacitor connected between V_{L4} and GND

　　　　　C1 = C2 = C3 = C4 = 0.47 µF±30%

Note 2.　This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected (by setting the MDSET1 and MDSET0 bits of the LCDM0 register to 01B) if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).

Note 3.　This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

(2) 1/4 bias method

(TA = -40 to +85°C, 1.8 V ≤ VDD ≤ 3.6 V, VSS = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
LCD output voltage variation range	V_{L1}	C1 to C5 Note 1 = 0.47 μF Note 2	VLCD = 04H	0.90	1.00	1.08	V
			VLCD = 05H	0.95	1.05	1.13	V
			VLCD = 06H	1.00	1.10	1.18	V
			VLCD = 07H	1.05	1.15	1.23	V
			VLCD = 08H	1.10	1.20	1.28	V
			VLCD = 09H	1.15	1.25	1.33	V
			VLCD = 0AH	1.20	1.30	1.38	V
Doubler output voltage	V_{L2}	C1 to C5 Note 1 = 0.47 μF		$2 V_{L1} - 0.08$	$2 V_{L1}$	$2 V_{L1}$	V
Tripler output voltage	V_{L3}	C1 to C5 Note 1 = 0.47 μF		$3 V_{L1} - 0.12$	$3 V_{L1}$	$3 V_{L1}$	V
Quadruply output voltage	V_{L4}	C1 to C5 Note 1 = 0.47 μF		$4 V_{L1} - 0.16$	$4 V_{L1}$	$4 V_{L1}$	V
Reference voltage setup time Note 2	t_{VWAIT1}			5			ms
Voltage boost wait time Note 3	t_{VWAIT2}	C1 to C5 Note 1 = 0.47μF		500			ms

Note 1. This is a capacitor that is connected between voltage pins used to drive the LCD.

C1: A capacitor connected between CAPH and CAPL

C2: A capacitor connected between V_{L1} and GND

C3: A capacitor connected between V_{L2} and GND

C4: A capacitor connected between V_{L3} and GND

C5: A capacitor connected between V_{L4} and GND

C1 = C2 = C3 = C4 = C5 = 0.47 μF±30%

Note 2. This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected (by setting the MDSET1 and MDSET0 bits of the LCDM0 register to 01B) if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).

Note 3. This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

<R>   ## 2.8.3   Capacitor split method

(1)   1/3 bias method

(T_A = -40 to +85°C, 2.2 V $\leq$ V_{DD} $\leq$ 3.6 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
V_{L4} voltage	V_{L4}	C1 to C3 = 0.47 μF [Note 2]		V_{DD}		V
V_{L2} voltage	V_{L2}	C1 to C3 = 0.47 μF [Note 2]	2/3 V_{L4} - 0.1	2/3 V_{L4}	2/3 V_{L4} + 0.1	V
V_{L1} voltage	V_{L1}	C1 to C3 = 0.47 μF [Note 2]	1/3 V_{L4} - 0.1	1/3 V_{L4}	1/3 V_{L4} + 0.1	V
Capacitor split wait time [Note 1]	t_{VWAIT}		100			ms

Note 1.   This is the wait time from when voltage bucking is started (VLCON = 1) until display is enabled (LCDON = 1).

Note 2.   This is a capacitor that is connected between voltage pins used to drive the LCD.

           C1: A capacitor connected between CAPH and CAPL

           C2: A capacitor connected between V_{L1} and GND

           C3: A capacitor connected between V_{L2} and GND

           C1 = C2 = C3 = 0.47 μF$\pm$30%

2.9   RAM data retention characteristics

(T$_A$ = -40 to +85°C, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V$_{DDDR}$		1.46 Note		3.6	V

Note   The value depends on the POR detection voltage. When the voltage drops, the RAM data is retained before a POR reset is effected, but RAM data is not retained when a POR reset is effected.
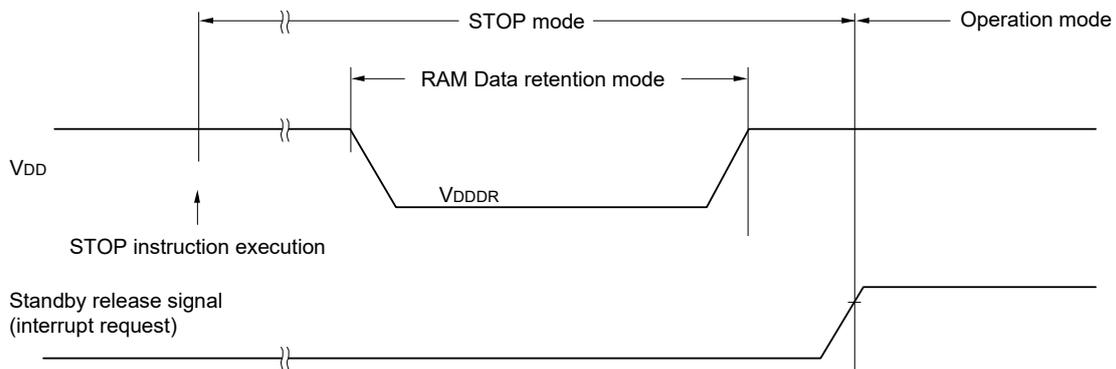
2.10   Flash Memory Programming Characteristics

(T$_A$ = -40 to +85°C, 1.8 V $\leq$ V$_{DD}$ $\leq$ 3.6 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
System clock frequency	f$_{CLK}$	2.4 V $\leq$ V$_{DD}$ $\leq$ 3.6 V	1		24	MHz
Number of code flash rewrites Notes 1, 2, 3	C$_{erwr}$	Retained for 20 years T$_A$ = 85°C	1,000			Times
Number of data flash rewrites Notes 1, 2, 3		Retained for 1 year T$_A$ = 25°C		1,000,000		
		Retained for 5 years T$_A$ = 85°C	100,000			
		Retained for 20 years T$_A$ = 85°C	10,000			

Note 1.   1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

Note 2.   When using flash memory programmer and Renesas Electronics self programming library

Note 3.   These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

2.11   Dedicated Flash Memory Programmer Communication (UART)

(T$_A$ = -40 to +85°C, 1.8 V $\leq$ V$_{DD}$ $\leq$ 3.6 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

2.12   Timing Specs for Switching Modes

(TA = -40 to +85°C, 1.8 V ≤ VDD ≤ 3.6 V, VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
How long from when an external reset ends until the initial communication settings are specified	tSUINIT	POR and LVD reset must end before the external reset ends.			100	ms
How long from when the TOOL0 pin is placed at the low level until an external reset ends	tSU	POR and LVD reset must end before the external reset ends.	10			μs
Time to hold the TOOL0 pin at the low level after an external reset is released (excluding the processing time of the firmware to control the flash memory)	tHD	POR and LVD reset must end before the external reset ends.	1			ms

<R>
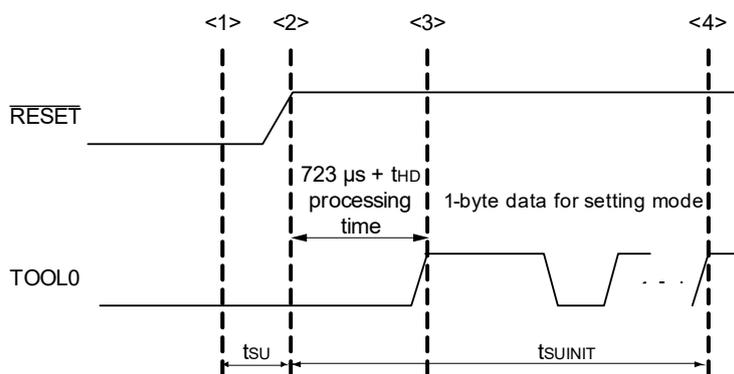
<1> The low level is input to the TOOL0 pin.
<2> The external reset ends (POR and LVD reset must end before the external reset ends.).
<3> The TOOL0 pin is set to the high level.
<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark   tSUINIT: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the resets end.

tSU: How long from when the TOOL0 pin is placed at the low level until an external reset ends

tHD: Time to hold the TOOL0 pin at the low level after an external reset is released (excluding the processing time of the firmware to control the flash memory)

3. PACKAGE DRAWINGS

3.1   80-pin products

R5F11MMDAFB, R5F11MMEAFB, R5F11MMFAFB

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP80-12x12-0.50	PLQP0080KB-A	80P6Q-A	0.5g

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Terminal cross section

Detail F

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	11.9	12.0	12.1
E	11.9	12.0	12.1
A_2	—	1.4	—
H_D	13.8	14.0	14.2
H_E	13.8	14.0	14.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	10°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.3	0.5	0.7
L_1	—	1.0	—

3.2   100-pin products

R5F11MPEAFB, R5F11MPFAFB, R5F11MPGAFB

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP100-14x14-0.50	PLQP0100KB-A	100P6Q-A / FP-100U / FP-100UV	0.6g

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Terminal cross section

Detail F

Index mark

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	——	1.4	——
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	——	——	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	——	0.18	——
c	0.09	0.145	0.20
c_1	——	0.125	——
θ	0°	——	8°
e	——	0.5	——
x	——	——	0.08
y	——	——	0.08
Z_D	——	1.0	——
Z_E	——	1.0	——
L	0.35	0.5	0.65
L_1	——	1.0	——

REVISION HISTORY			RL78/L1A Datasheet	

Rev.	Date	Description		
		Page	Summary	
1.00	Aug 12, 2016	—	First Edition issued	
1.10	Sep 30, 2019	p.2	Modification of 1.1 Features	
		p.6	Modification of description in 1.4 Pin Identification	
		p.7	Modification of block diagram in 1.5.1 80-pin products	
		p.8	Modification of block diagram in 1.5.2 100-pin products	
		p.12, 14	Modification of 2.1 Absolute Maximum Ratings	
		p.17 to 20	Modification of 2.3.1 Pin characteristics	
		p.28	Deletion of note 16 in 2.3.2 Supply current characteristics	
		p.36	Modification of 2.5.1 (2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)	
		p.42	Modification of remarks 2 and 3 in 2.5.1 (5) During communication at same potential (simplified I^2C mode)	
		p.59	Modification of 2.6.1 A/D converter characteristics	
		p.60	Modification of table and addition of note in 2.6.1 A/D converter characteristics	
		p.64	Addition of description in 2.6.4 Comparator	
		p.65	Modification of 2.6.5 Rail to rail operational amplifier characteristics	
		p.68	Modification of 2.6.7 Voltage reference	
		p.68	Modification of 2.6.8 1/2 AV_{DD} voltage output, and the location of this chapter has been moved.	
		p.72	Addition of caution 2 in 2.7 Power supply voltage rising slope characteristics	
		p.75	Modification of note 2 in 2.8.3 Capacitor split method	
		p.77	Modification of 2.12 Timing Specs for Switching Modes	

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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