R5C832

PCI-IEEE1394/SD Card/ Multi Media Card/MemoryStick/ xD Picture Card

Data Sheet

REV. 1.00

RICOH

–REVISION HISTORY–

REVISION	DATE	COMMENTS
0.90	11/22/2004	First draft
0.95	1/07/2005	Changed the pin assignment.
1.00	3/02/2005	First public release

1 OVERVIEW

The R5C832 is a single chip solution offering 5 PCI functions (a PCI bus bridge to an IEEE1394, an SD Card, a Multi Media Card, a Memory Stick and an xD Picture Card).

- Low Power consumption
  - Low operating power consumption due to the improvement of Power Management
  - Software Suspend mode compliant with ACPI
  - Hardware Suspend
  - Supports CLKRUN#
  - Internal regulator allows 3.3V single power operation

- PCI-1394 Bridge/SD Card/Multi Media Card/Memory Stick/xD Picture Card interface
  - 1 port of IEEE1394
  - SD Card, Multi Media Card, Memory Stick and xD Picture Card sharing MDIOxx pins
    - Ricoh's proprietary driver for Multi Media Card, Memory Stick and xD Picture Card

- PCI Bus Interface

  - Compliant with PCI Local Bus Specification3.0
  - Maximum frequency 33MHz
  - Supports PCI Master/Target protocol
  - PCI configuration space for each function
  - 3.3V Interface

- IEEE1394 Interface
  - Compliant with IEEE1394-1995 Standard Specification and IEEE1394a-2000 Standard Specification
  - Compliant with 1394 OHCI Release 1.1/1.0 Standard Specification
  - Provides Asynchronous receive/transmit FIFO and Isochronous receive/transmit FIFO
  - Data transmission rate of 100, 200 and 400Mbps
  - 1 port of 1394 Cable interface
  - 24.576MHz crystal oscillator and Internal 393.216MHz PLL
  - Programmable low power consumption modes for PHY block

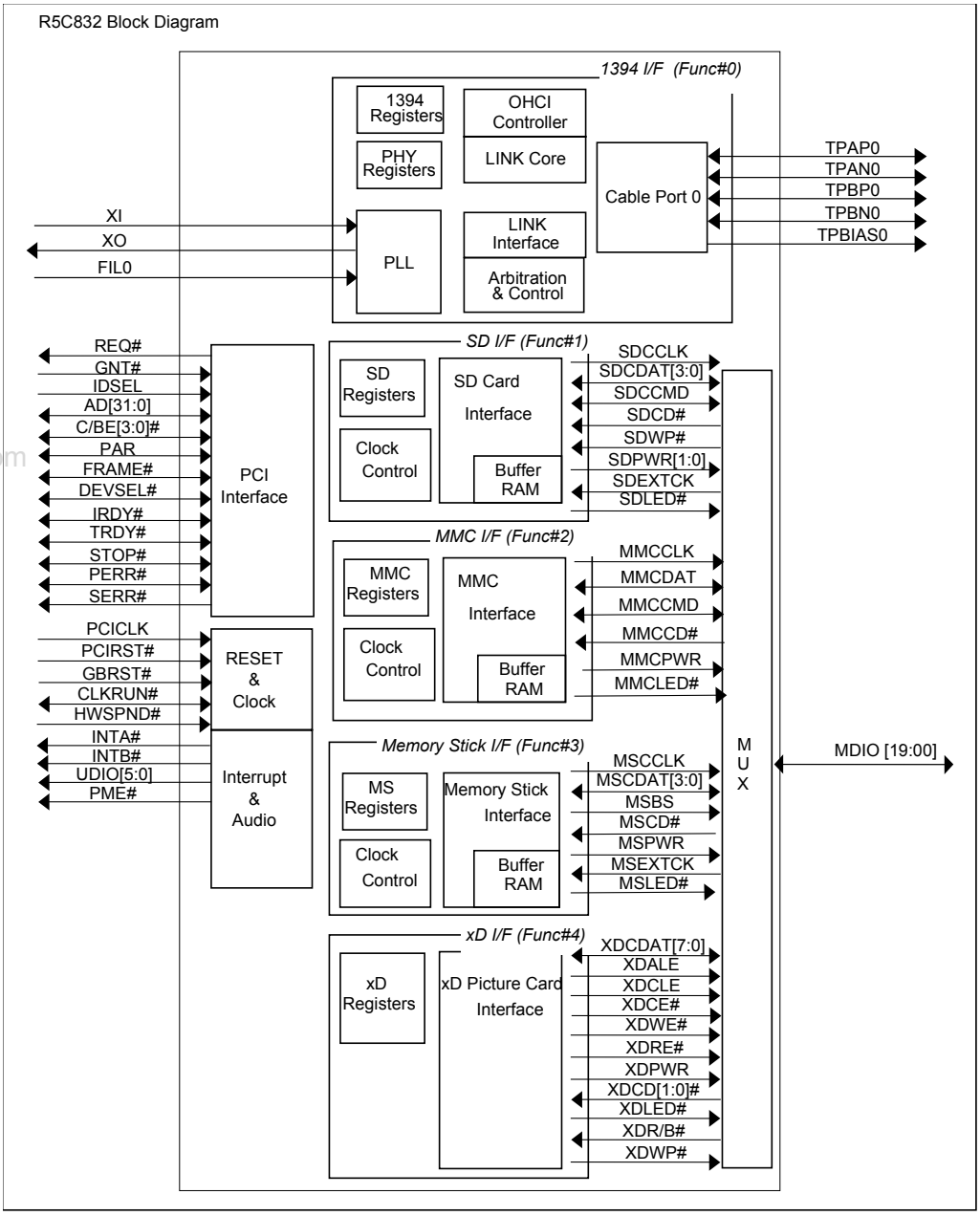
- Media Card Interface
  - SD Card
    - Compliant with SD Memory Card Specification Version 1.1
    - Compliant with SD Input/Output (SDIO) Card Specification Version 1.1
    - Compliant with SD Host Controller Standard Specification Version 1.0
  - Multi Media Card
    - Compatible with Multi Media Card System
  - Memory Stick
    - Compliant with Memory Stick Standard Format Specification Version 1.4
    - Compliant with Memory Stick PRO Format Specification Version 1.00
  - xD Picture Card
    - Compliant with xD Picture Card Specification Version 1.20
    - Compliant with xD Picture Card Host Guideline Version 1.20
    - Supports Type M. Card as well as conventional cards
    - Supports Smart Media technology

- System Interrupt
  - Supports INTA# and INTB# for PC system interrupt (Each unit is programmable.)

- Supports 1394 LED, SD LED, MMC LED, Memory Stick LED and xD Picture Card LED as activity indicators

- Package
  - 116pin CSP (size=11x11mm, pitch= 0.8mm, t=1.4mm)
  - 128pin TQFP (size=14x14mm, pitch= 0.4mm, t=1.2mm)

2 BLOCK DIAGRAM

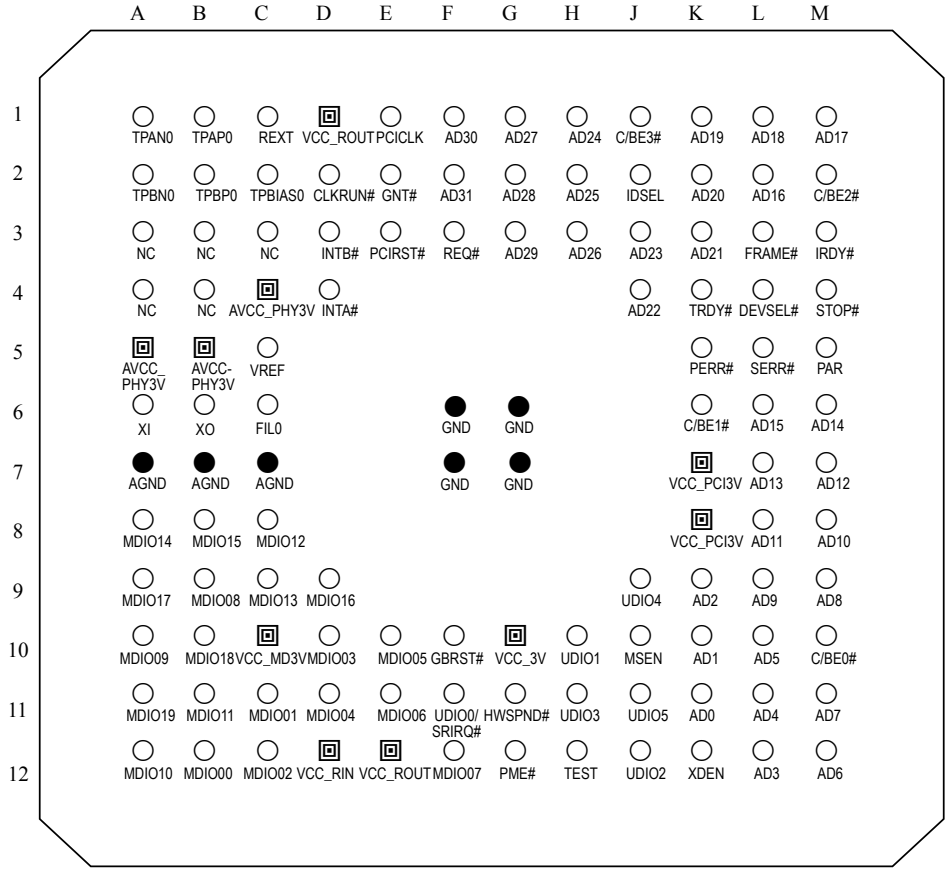


3 PIN DESCRIPTION

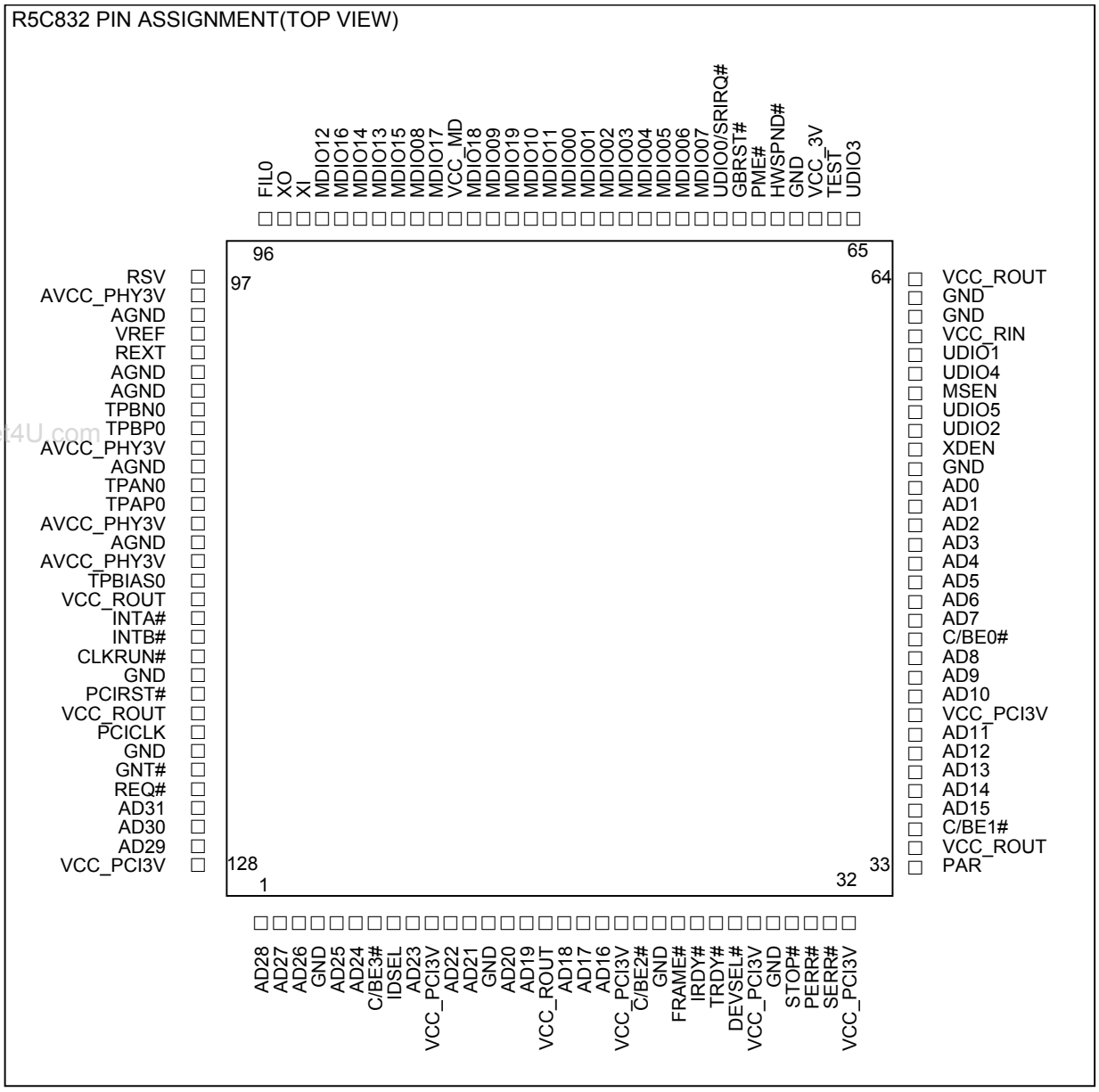
3.1 Pin Assignments

3.1.1 116 pin CSP

Bottom View



3.1.2 128 pin TQFP



3.2 Pin Characteristics

3.2.1 116 pin CSP

Ball No.			Pin Characteristics		Note
	Pin Name	Dir	PwrRail	Drive	
J11	UDIO5	O	3V	4mA	
J9	UDIO4	I/O	3V	4mA	
H11	UDIO3	I/O	3V	4mA	
J12	UDIO2	I/O	3V	4mA	
H10	UDIO1	I/O	3V	4mA	
F11	UDIO0/SRIRQ#	I/O	3V	4mA	
D4	INTA#	O (OD)	P	PCI	
D3	INTB#	O (OD)	P	PCI	
D2	CLKRUN#	I/O	P	PCI	
E3	PCIRST#	I	P	–	
E1	PCICLK	I	P	–	
E2	GNT#	I	P	–	
F3	REQ#	O (TS)	P	PCI	
F2	AD31	I/O	P	PCI	
F1	AD30	I/O	P	PCI	
G3	AD29	I/O	P	PCI	
G2	AD28	I/O	P	PCI	
G1	AD27	I/O	P	PCI	
H3	AD26	I/O	P	PCI	
H2	AD25	I/O	P	PCI	
H1	AD24	I/O	P	PCI	
J1	C/BE3#	I/O	P	PCI	
J2	IDSEL	I	P	–	
J3	AD23	I/O	P	PCI	
J4	AD22	I/O	P	PCI	
K3	AD21	I/O	P	PCI	
K2	AD20	I/O	P	PCI	
K1	AD19	I/O	P	PCI	
L1	AD18	I/O	P	PCI	
M1	AD17	I/O	P	PCI	
L2	AD16	I/O	P	PCI	
M2	C/BE2#	I/O	P	PCI	
L3	FRAME#	I/O	P	PCI	
M3	IRDY#	I/O	P	PCI	
K4	TRDY#	I/O	P	PCI	
L4	DEVSEL#	I/O	P	PCI	
M4	STOP#	I/O	P	PCI	

Ball No.			Pin Characteristics		Note
	Pin Name	Dir	PwrRail	Drive	
K5	PERR#	I/O	P	PCI	
L5	SERR#	O (OD)	P	PCI	
M5	PAR	I/O	P	PCI	
K6	C/BE1#	I/O	P	PCI	
L6	AD15	I/O	P	PCI	
M6	AD14	I/O	P	PCI	
L7	AD13	I/O	P	PCI	
M7	AD12	I/O	P	PCI	
L8	AD11	I/O	P	PCI	
M8	AD10	I/O	P	PCI	
L9	AD9	I/O	P	PCI	
M9	AD8	I/O	P	PCI	
M10	C/BE0#	I/O	P	PCI	
M11	AD7	I/O	P	PCI	
M12	AD6	I/O	P	PCI	
L10	AD5	I/O	P	PCI	
L11	AD4	I/O	P	PCI	
L12	AD3	I/O	P	PCI	
K9	AD2	I/O	P	PCI	
K10	AD1	I/O	P	PCI	
K11	AD0	I/O	P	PCI	
C2	TPBIAS0	I/O	AP	1394	
B1	TPAP0	I/O	AP	1394	
A1	TPAN0	I/O	AP	1394	
B2	TPBP0	I/O	AP	1394	
A2	TPBN0	I/O	AP	1394	
C1	REXT	I/O	AP	–	
C5	VREF	I/O	AP	–	
C6	FIL0	I/O	AP	–	
B6	XO	O	AP	–	
A6	XI	I	AP	–	
A11	MDIO19	I/O(PU)	M	8mA	
B10	MDIO18	I/O(PU)	M	8mA	
A9	MDIO17	I/O(PU)	M	8mA	
D9	MDIO16	I/O(PU)	M	8mA	
B8	MDIO15	I/O(PU)	M	8mA	
A8	MDIO14	I/O(PU)	M	8mA	
C9	MDIO13	I/O(PU)	M	8mA	
C8	MDIO12	I/O(PU)	M	8mA	

Ball No.			Pin Characteristics		Note
	Pin Name	Dir	PwrRail	Drive	
B11	MDIO11	I/O(PU)	M	8mA	
A12	MDIO10	I/O(PU)	M	8mA	
A10	MDIO09	I/O(PU)	M	8mA	
B9	MDIO08	I/O(PU)	M	8mA	
F12	MDIO07	I	3V	–	
E11	MDIO06	O	3V	8mA	
E10	MDIO05	O	3V	8mA	
D11	MDIO04	O	3V	8mA	
D10	MDIO03	I (PU)	3V	–	
C12	MDIO02	O (PU)	3V	8mA	
C11	MDIO01	I (PU)	3V	–	
B12	MDIO00	I (PU)	3V	–	
H12	TEST	I	3V	–	
G11	HWSPND#	I	3V	–	
J10	MSEN	I	3V	–	
K12	XDEN	I	3V	–	
G12	PME#	O (OD)	3V	4mA	
F10	GBRST#	I	3V	–	

Pin Type
I: Inpt Pin, O: Output Pin, I/O: Input Output Pin,
I (PU): Input Pin with Internal Pullup Resister,
I (PD): Input Pin with Internal Pulldown Resister,
I/O (PU): Input Output Pin with Internal Pullup Resister,
I/O (PD): Input Output Pin with Internal Pulldown Resister,
O (TS): Three State Output Pin, O (OD): Open Drain Output Pin

Power Rail
P: VCC_PCI 3V AP: AVCC_PHY3V R: VCC_RIN
3V: VCC_3V M: VCC_MD3V C: VCC_ROUT
G: GND AG: AGND

Drive
PCI: PCI Compliant
1394: IEEE1394a-2000 Compliant

Pin Name	Ball No.	Pin Name	Ball No.
VCC_PCI3V	K7, K8	AVCC_PHY3V	A5, B5, C4
VCC_3V	G10	AGND	A7, B7, C7
VCC_MD3V	C10	GND	F6, F7, G6, G7
VCC_RIN	D12	NC	A3, A4, B3, B4, C3
VCC_ROUT	D1, E12		

3.2.2 128 pin TQFP

Pin No.			Pin Characteristics		Note
	Pin Name	Dir	PwrRail	Drive	
1	AD28	I/O	P	PCI	
2	AD27	I/O	P	PCI	
3	AD26	I/O	P	PCI	
4	GND	DC	G	–	
5	AD25	I/O	P	PCI	
6	AD24	I/O	P	PCI	
7	C/BE3#	I/O	P	PCI	
8	IDSEL	I	P	–	
9	AD23	I/O	P	PCI	
10	VCC_PCI3V	DC	P	–	
11	AD22	I/O	P	PCI	
12	AD21	I/O	P	PCI	
13	GND	DC	G	–	
14	AD20	I/O	P	PCI	
15	AD19	I/O	P	PCI	
16	VCC_ROUT	DC	C	–	
17	AD18	I/O	P	PCI	
18	AD17	I/O	P	PCI	
19	AD16	I/O	P	PCI	
20	VCC_PCI3V	DC	P	–	
21	C/BE2#	I/O	P	PCI	
22	GND	DC	G	–	
23	FRAME#	I/O	P	PCI	
24	IRDY#	I/O	P	PCI	
25	TRDY#	I/O	P	PCI	
26	DEVSEL#	I/O	P	PCI	
27	VCC_PCI3V	DC	P	–	
28	GND	DC	G	–	
29	STOP#	I/O	P	PCI	
30	PERR#	I/O	P	PCI	
31	SERR#	O (OD)	P	PCI	
32	VCC_PCI3V	DC	P	–	
33	PAR	I/O	P	PCI	
34	VCC_ROUT	DC	C	–	
35	C/BE1#	I/O	P	PCI	
36	AD15	I/O	P	PCI	
37	AD14	I/O	P	PCI	
38	AD13	I/O	P	PCI	
39	AD12	I/O	P	PCI	

Pin No.			Pin Characteristics		Note
	Pin Name	Dir	PwrRail	Drive	
40	AD11	I/O	P	PCI	
41	VCC_PCI3V	DC	P	–	
42	AD10	I/O	P	PCI	
43	AD9	I/O	P	PCI	
44	AD8	I/O	P	PCI	
45	C/BE0#	I/O	P	PCI	
46	AD7	I/O	P	PCI	
47	AD6	I/O	P	PCI	
48	AD5	I/O	P	PCI	
49	AD4	I/O	P	PCI	
50	AD3	I/O	P	PCI	
51	AD2	I/O	P	PCI	
52	AD1	I/O	P	PCI	
53	AD0	I/O	P	PCI	
54	GND	DC	G	–	
55	XDEN	I	3V	–	
56	UDIO2	I/O	3V	4mA	
57	UDIO5	O	3V	4mA	
58	MSEN	I	3V	–	
59	UDIO4	I/O	3V	4mA	
60	UDIO1	I/O	3V	4mA	
61	VCC_RIN	DC	R	–	
62	GND	DC	G	–	
63	GND	DC	G	–	
64	VCC_ROUT	DC	C	–	
65	UDIO3	I/O	3V	4mA	
66	TEST	I	3V	–	
67	VCC_3V	DC	3V	–	
68	GND	DC	G	–	
69	HWSPND#	I	3V	–	
70	PME#	O (OD)	3V	4mA	
71	GBRST#	I	3V	–	
72	UDIO0/SRIRQ#	I/O	3V	4mA	
73	MDIO07	I	3V	–	
74	MDIO06	O	3V	8mA	
75	MDIO05	O	3V	8mA	
76	MDIO04	O	3V	8mA	
77	MDIO03	I (PU)	3V	–	

Pin No.			Pin Characteristics		Note
	Pin Name	Dir	PwrRail	Drive	
78	MDIO02	O(PU)	3V	8mA	
79	MDIO01	I (PU)	3V	–	
80	MDIO00	I (PU)	3V	–	
81	MDIO11	I/O(PU)	M	8mA	
82	MDIO10	I/O(PU)	M	8mA	
83	MDIO19	I/O(PU)	M	8mA	
84	MDIO09	I/O(PU)	M	8mA	
85	MDIO18	I/O(PU)	M	8mA	
86	VCC_MD3V	DC	M	–	
87	MDIO17	I/O(PU)	M	8mA	
88	MDIO08	I/O(PU)	M	8mA	
89	MDIO15	I/O(PU)	M	8mA	
90	MDIO13	I/O(PU)	M	8mA	
91	MDIO14	I/O(PU)	M	8mA	
92	MDIO16	I/O(PU)	M	8mA	
93	MDIO12	I/O(PU)	M	8mA	
94	XI	I	AP	–	
95	XO	O	AP	–	
96	FIL0	I/O	AP	–	
97	RSV	I/O	AP	–	
98	AVCC_PHY3V	DC	AP	–	
99	AGND	DC	AG	–	
100	VREF	I/O	AP	–	
101	REXT	I/O	AP	–	
102	AGND	DC	AG	–	
103	AGND	DC	AG	–	
104	TPBN0	I/O	AP	1394	
105	TPBP0	I/O	AP	1394	
106	AVCC_PHY3V	DC	AP	–	
107	AGND	DC	AG	–	
108	TPAN0	I/O	AP	1394	
109	TPAP0	I/O	AP	1394	
110	AVCC_PHY3V	DC	AP	–	
111	AGND	DC	AG	–	
112	AVCC_PHY3V	DC	AP	–	

Pin No.			Pin Characteristics		Note
	Pin Name	Dir	PwrRail	Drive	
113	TPBIAS0	I/O	AP	1394	
114	VCC_ROUT	DC	C	–	
115	INTA#	O(OD)	P	PCI	
116	INTB#	O(OD)	P	PCI	
117	CLKRUN#	I/O	P	PCI	
118	GND	DC	G	–	
119	PCIRST#	I	P	PCI	
120	VCC_ROUT	DC	C	–	
121	PCICLK	I	P	–	
122	GND	DC	G	–	
123	GNT#	I	P	–	
124	REQ#	O (TS)	P	PCI	
125	AD31	I/O	P	PCI	
126	AD30	I/O	P	PCI	
127	AD29	I/O	P	PCI	
128	VCC_PCI3V	DC	P	–	

Pin Type

I: Inpt Pin, O: Output Pin, I/O: Input Output Pin,
I (PU): Input Pin with Internal Pullup Resister,
I (PD): Input Pin with Internal Pulldown Resister,
I/O (PU): Input Output Pin with Internal Pullup Resister,
I/O (PD): Input Output Pin with Internal Pulldown Resister,
O (TS): Three State Output Pin, O (OD): Open Drain Output Pin

Power Rail

P: VCC_PCI 3V AP: AVCC_PHY3V R: VCC_RIN
3V: VCC_3V M: VCC_MD3V C: VCC_ROUT
G: GND AG: AGND

Drive

PCI: PCI Compliant
1394: IEEE1394a-2000 Compliant

3.2.3 Media Card Pin Assignments

Pin	Media I/F	SD Card	Multi Media Card	Memory Stick	xD Picture Card
1	MDIO00	SDCD#	MMCCD#	-	XDCD0#
2	MDIO01	-	-	MSCD#	XDCD1#
3	MDIO02	-	-	-	XDCE#
4	MDIO03	SDWP#	-	-	XDR/B#
5	MDIO04	SDPWR0	MMCPWR	MSPWR	XDPWR
6	MDIO05	SDPWR1	-	-	XDWP#
7	MDIO06	SDLED#	MMCLED#	MSLED#	XDLED#
8	MDIO07	SDEXTCK	-	MSEXTCK	-
9	MDIO08	SDCCMD	MMCCMD	MSBS	XDWE#
10	MDIO09	SDCCLK	MMCCLK	MSCCLK	XDRE#
11	MDIO10	SDCDAT0	MMCDAT	MSCDAT0	XDCDAT0
12	MDIO11	SDCDAT1	-	MSCDAT1	XDCDAT1
13	MDIO12	SDCDAT2	-	MSCDAT2	XDCDAT2
14	MDIO13	SDCDAT3	-	MSCDAT3	XDCDAT3
15	MDIO14	-	-	-	XDCDAT4
16	MDIO15	-	-	-	XDCDAT5
17	MDIO16	-	-	-	XDCDAT6
18	MDIO17	-	-	-	XDCDAT7
19	MDIO18	-	-	-	XDCLE
20	MDIO19	-	-	-	XDALE

3.3 Pin Functions Outline

In this chapter, the detailed signal pins in the R5C832 are explained. Every signal is divided according to their relational interface.
mark means the signal is on either active or asserted when the signal is low−level. Otherwise, no−mark means the signal is asserted when the signal is high−level.
The following the notations are used to describe the signal type.

IN	Input Pin
OUT	Output Pin
OUT (TS)	Three State Output Pin
OUT (OD)	Open Drain Output Pin
I/O	Input Output Pin
I/O (OD)	Input Output Pin (Output is Open Drain)
s/h/z	Sustained Tri−State is an active low tri−state signal owned and driven by one and only one agent at a time. The agent that drives an s/h/z pin low must drive it high for at least one clock before letting it float. A new agent cannot start driving an s/h/z signal any sooner than one clock after the previous owner tri−state is.

3.3.1 PCI Local Bus interface signals

Pin Name	Type	Description
		PCI Bus Interface Pin Descriptions
PCICLK	IN	***PCI CLOCK:*** PCICLK provides timing for all transactions on PCI. All other PCI signals are sampled on the rising edge of PCICLK.
CLKRUN#	I/O (OD)	***PCI CLOCK RUN:*** This signal indicates the status of PCICLK and an open drain output to request the starting or speeding up of PCICLK. This pin complies with Mobile PCI specification. If CLKRUN# is not implemented, then this pin should be tied low. During PCI bus reset is asserted, this pin placed in a high-impedance state.
PCIRST#	IN	***PCI RESET:*** This input is used to initialize all registers, sequences and signals of the R5C832 to their reset states. PCIRST# causes the R5C832 to place all output buffers in a high-impedance state. The negation of PCIRST# requires no-bounds.
AD [31:0]	I/O	***ADDRESS AND DATA:*** Address and Data are multiplexed on the same PCI pins.
C/BE [3:0]#	I/O	***BUS COMMAND AND BYTE ENABLES:*** Bus Command and Byte Enables are multiplexed on the same PCI pins. During the address phase of transaction, C/BE [3:0]# define the bus command. During the data phase C/BE [3:0]# are used as Byte Enables. The Byte Enables are valid for the entire data phase and determine which byte lanes carry meaningful data.
PAR	I/O	***PARITY:*** Parity is even parity across AD [31:0] and C/BE [3:0]#. PAR is stable and valid one clock after the address phase. For data phases, PAR is stable and valid one clock after either IRDY# is asserted on a write transaction or TRDY# is asserted on a read transaction. The master drives PAR for address and write data phases; the target drives PAR for read data phases.
FRAME#	I/O s/h/z	***CYCLE FRAME:*** This signal is driven by the current master to indicate the beginning and duration of an access. FRAME# is asserted to indicate a bus transaction is beginning. While FRAME# is asserted, data transfers continue. When FRAME# is deasserted, the transaction is in the final data phase or has complete.
TRDY#	I/O s/h/z	***TARGET READY:*** This signal indicates the initialing agent's ability to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. A data phase is completed on any clock both TRDY# and IRDY# are sampled asserted. During a read, TRDY# and IRDY# are sampled asserted. During a read, TRDY# indicates that valid data is present on AD [31:0]. During a write, it indicates the target is prepared to accept data. Wait cycles are inserted both IRDY# and TRDY# are asserted together.
IRDY#	I/O s/h/z	***INITIATOR READY:*** This signal indicates the initiating agent's ability to complete the current data phase of the transaction. IRDY# is used in conjunction with TRDY#. A data phase is completed on any clock both TRDY# and IRDY# are sampled asserted. During a write, IRDY# indicates that valid data is present on AD [31:0]. During a read, it indicates the target is prepared to accept data. Wait cycles are inserted both IRDY# and TRDY# are asserted together.
STOP#	I/O s/h/z	***STOP:*** This signal indicates the current target is requesting the master to stop the current transaction.
IDSEL	IN	***INITIALIZATION DEVICE SELECT:*** This signal is used as chips select during configuration read and write transactions.
DEVSEL#	I/O s/h/z	***DEVICE SELECT:*** When actively driven, indicates the driving device has decoded its address as the target of the current access. As an input, DEVSEL# indicates whether any device on the bus has been selected.
PERR#	I/O s/h/z	***PARITY ERROR:*** This signal is only for the reporting of data parity errors during all PCI transactions except a Special Cycle. The R5C832 drives this output active "low" if it detects a data parity error during a write phase.

Pin Name	Type	Description
		PCI Bus Interface Pin Descriptions (Continued)
SERR#	OUT (OD)	***SYSTEM ERROR:*** This signal is pure open drain. The R5C832 actively drives this output for a single PCI clock when it detects an address parity error on either the primary bus or the secondary bus.
REQ#	OUT (TS)	***REQUEST:*** This signal indicates to the arbiter that the R5C832 desires use of the bus. This is a point to point signal.
GNT#	IN	***GRANT:*** This signal indicates the R5C832that access to the bus has been granted. This is a point to point signal.
GBRST#	IN	***GLOBAL RESET:*** This input is used to initialize registers for control of PME_Context register. This should be asserted only once when system power supply is on.

3.3.2 System Interrupt signals

Pin Name	Type	Description
		System Interrupt Pin Descriptions
INTA#	OUT (OD)	***PCI INTERRUPT REQUEST A:*** This signal indicates a programmable interrupt request generated from the IEEE1394 interface. This signal is connected to the interrupt line of the PCI bus.
INTB#	OUT (OD)	***PCI INTERRUPT REQUEST B:*** This signal indicates a programmable interrupt request generated from the SD Card interface, Multi Media Card interface, Memory Stick interface or xD Picture Card interface. This signal is connected to the interrupt line of the PCI bus.
UDIO0/SRIRQ# UDIO1/GPIO0 UDIO2/GPIO1 UDIO3/GPIO2 UDIO4/GPIO3 UDIO5/LED0#	I/O (TS)	***USER DEFINABLE INPUT/OUTPUT:*** These signals can be used as user-definable input/output. Users can define functions such as *GPIO, LED, IRQ and so on for each pin in the Global Misc Control 1 Register. *GPIO : General Purpose I/O
PME#	OUT (OD)	***POWER MANAGEMENT EVENT:*** When PME_En bit in Power Management Control/Status register is set or when Power Status is set to any state mode except D0, this signal is assigned as PME#.

3.3.3 Other signals

Pin Name	Type	Description
		Other Signals Descriptions
HWSPND#	IN	***Hardware Suspend:*** This signal works as HWSPND# input. PCIRST# is not accepted as long as HWSPND# is asserted so that VCC_PCI3V can be powered off. When Serial IRQ mode is set, HWSPND# must be asserted after Serial IRQ mode on the chip-set has been deasserted. When Hardware Suspend mode is off, HWSPND# must be deasserted before Serial IRQ mode is enabled. When a power is on, follow the reset sequence shown in the chapter 4.5 in order to confirm the input of PCIRST# and PCLK.
MSEN	IN	***Memory Stick Function Enable:*** Memory Stick Function Enable signal.
XDEN	IN	***xD Function Enable:*** xD Picture Card Function Enable signal.
TEST	IN	***TEST:*** This signal is a test mode pin. Usually, this pin must be tied low.
RSV	I/O	***Reserved:*** This signal is reserved. Usually, this pin must be open.

3.3.4 IEEE1394 PHY Interface signals

Pin Name	Type	Description
		IEEE1394 Cable Interface Pin Descriptions
TPAP0	I/O	***TPA Positive :*** Twisted-pair cable A (positive) differential signal terminals.
TPBP0	I/O	***TPB Positive :*** Twisted-pair cable B (positive) differential signal terminals.
TPAN0	I/O	***TPA Negative :*** Twisted-pair cable A (negative) differential signal terminals.
TPBN0	I/O	***TPB Negative :*** Twisted-pair cable B (negative) differential signal terminals.
TPBIAS0	I/O	***TP Bias :*** Twisted-pair bias output. This pin is compliant with the IEEE1394a-2000, and also monitors Insertion/desertion of other cables

3.3.5 IEEE1394 Control signals

Pin Name	Type	Description
		IEEE1394 Control Pin Descriptions
VREF	I/O	***Voltage reference Resistance :*** It is necessary to connect a capacitance of 0.01uF between this pin and AGND.
REXT	I/O	***Resistance External:*** It is necessary to connect a resistor of 10kΩ±1% between this pin and AGND.
XI	IN	***X'tal In :*** 24.576MHz
XO	OUT	***X'tal Out :*** 24.576MHz
FIL0	I/O	***Filter :*** This pin connects to the PLL Filter. It is necessary to connect a capacitance of 0.01uF between this pin and AGND.

3.3.6 Media Card Interface signals

- **SD Card**

Pin Name	MDIO Pin Name	Type	Description
			SD Card Control Pin Descriptions
SDCDAT0	MDIO10	I/O	***SD Data [3:0] :*** SD Card 4bit data bus signals.
SDCDAT1	MDIO11	I/O	
SDCDAT2	MDIO12	I/O	
SDCDAT3	MDIO13	I/O	
SDCCMD	MDIO08	I/O	***SD Command :*** SD Card Command signal.
SDCCLK	MDIO09	OUT	***SD Clock :*** SD Card Clock signal.
SDWP#	MDIO03	IN	***SD Write Protect :*** This signal indicates the state of SD card's write protect switch. This pin is connected to a reserved pin of the SD card socket.
SDCD#	MDIO00	IN	***SD Card Detect :*** This signal indicates whether the SD card is inserted to a socket. This pin is connected to a reserved pin of the SD card socket.
SDEXTCK	MDIO07	IN	***SD External Clock :*** This signal must be connected to GND because the R5C832 does not support SDEXTCK for the SD Card.
SDPWR0	MDIO04	OUT	***SD Card Power0 Control :*** This signal is provided to control the power supply (3.3V) for an SD card.
SDPWR1	MDIO05	OUT	***SD Card Power1 Control :*** This signal is provided to control the power supply (1.8V) for an SD card. R5C832 does not support this signal.
SDLED#	MDIO06	OUT	***SD Card LED Control :*** This signal indicates an access state to the SD card.

- **Multi Media Card**

Pin Name	MDIO Pin Name	Type	Description
Multi Media Card Control Pin Descriptions			
MMCDAT	MDIO10	I/O	***MMC Data :*** Multi Media Card 1bit data bus signal.
MMCCMD	MDIO08	I/O	***MMC Command :*** Multi Media Card Command signal.
MMCCLK	MDIO09	OUT	***MMC Clock :*** Multi Media Card Clock signal.
MMCCD#	MDIO00	IN	***MMC Detect :*** This signal indicates whether the Multi Media Card is inserted to a socket. This pin is connected to a reserved pin of the Multi Media Card socket.
MMCPWR	MDIO04	OUT	***MMC Power Control :*** This signal is provided to control the power supply (3.3V) for an Multi Media card.
MMCLED#	MDIO06	OUT	***MMC LED Control :*** This signal indicates an access state to the Multi Media card.

- **Memory Stick**

Pin Name	MDIO Pin Name	Type	Description
Memory Stick Control Pin Descriptions			
MSCDAT0	MDIO10	I/O	***Memory Stick Data [3:0] :*** Memory Stick Data signals. Normally, MSCDAT0 only is used.
MSCDAT1	MDIO11	I/O	
MSCDAT2	MDIO12	I/O	
MSCDAT3	MDIO13	I/O	
MSBS	MDIO08	OUT	***Memory Stick Bus State :*** Memory Stick Bus State signal.
MSCCLK	MDIO09	OUT	***Memory Stick Clock :*** Memory Stick Clock signal.
MSCD#	MDIO01	IN	***Memory Stick Card Detect :*** This signal indicates whether the Memory Stick is inserted to a socket. This pin is connected to the INS signal of Memory Stick.
MSEXTCK	MDIO07	IN	***Memory Stick External Clock :*** This signal is input to the Memory Stick block. This clock supports 0 - 40MHz. If the internal PCICLK is used, this signal can be connected to GND.
MSPWR	MDIO04	OUT	***Memory Stick Power Control :*** This signal is provided to control the power supply for the Memory Stick.
MSLED#	MDIO06	OUT	***Memory Stick LED Control :*** This signal indicates an access state to the Memory Stick.

- **xD Picture Card**

Pin Name	MDIO Pin Name	Type	Description
			xD Picture Card Control Pin Descriptions
XDCDAT0	MDIO10	I/O	***xD Picture CardData [7:0] :*** xD Picture Card Data bus signals.
XDCDAT1	MDIO11	I/O	
XDCDAT2	MDIO12	I/O	
XDCDAT3	MDIO13	I/O	
XDCDAT4	MDIO14	I/O	
XDCDAT5	MDIO15	I/O	
XDCDAT6	MDIO16	I/O	
XDCDAT7	MDIO17	I/O	
XDCLE	MDIO18	OUT	***xD Picture Card CLE :*** xD Picture Card Command Latch Enable signal.
XDALE	MDIO19	OUT	***xD Picture Card ALE :*** xD Picture Card Address Latch Enable signal.
XDCD0#	MDIO00	IN	***xD Picture Card Detect :*** These signals indicate a detection of the xD Picture Card when two signals are set to 'Low' by insertion of xD Picture Card.
XDCD1#	MDIO01		
XDWP#	MDIO05	OUT	***xD Picture Card Write Protect :*** This signal indicates the state of xD Picture Card's write protect. This pin is connected to the -WP signal of the xD Picture Card.
XDPWR	MDIO04	OUT	***xD Picture Card Power Control :*** This signal is provided to control the power supply for the xD Picture Card.
XDR/B#	MDIO03	IN	***xD Picture Card R/B :*** xD Picture Card Ready/Busy signal. When this signal is low, xD Picture Card is busy.
XDLED#	MDIO06	OUT	***xD Picture Card LED Control:*** This signal indicates an access state to the xD Picture Card.
XDWE#	MDIO08	OUT	***xD Picture Card Write Enable:*** xD Picture Card Write Enable signal.
XDCE#	MDIO02	OUT	***xD Picture Card Enable:*** xD Picture Card Enable signal.
XDRE#	MDIO09	OUT	***xD Picture Card Read Enable:*** xD Picture Card Read Enable signal.

3.3.7 Power and GND signals

Pin Name	Type	Description
		Power Pin Descriptions
VCC_PCI3V	PWR	***PCI VCC:*** Power Supply pins for the PCI interface signals. This pin can be powered at 3.3V.
VCC_3V	PWR	***3V VCC :*** This supply pin is connected to 3.3V. This pin must not be off on the suspend mode because of the power supply for PME# and GBRST#.
VCC_MD3V	PWR	***Media VCC:*** Power Supply pins for the Media interface signals. This pin can be powered at 3.3V.
VCC_RIN	PWR	***Regulator Input:*** Power supply input pins for an internal regulator. This pin is connected to 3.3V.
VCC_ROUT	PWR	***Regulator Output:*** Power supply output pins for an internal regulator. This pin is powered as an output from an internal regulator and as an input to the core logic. Add bypass condensers between this pin and GND.
AVCC_PHY3V	PWR	***1394 PHY VCC:*** Power supply for PHY analog block. This pin can be powered at 3.3V. This pin must not be off on the suspend mode because of the power supply for Cable interface block.
GND	PWR	***Digital GND:***
AGND	PWR	***Analog GND:***

4 FUNCTIONAL DESCRIPTION

4.1 Device Configuration

The R5C832 supports the PCI-IEEE1394 bridge function, the SD Card interface, the Multi Media Card interface, the Memory Stick interface and the xD Picture Card interface. Logically the R5C832 looks to the primary PCI as a separate secondary bus residing in a single device. The IEEE 1394, the SD Card, the Multi Media Card, the Memory Stick and the xD Picture Card have their own register spaces.

4.1.1 PCI Configuration Register Space

The PCI Configuration registers are used to control the basic operations, as settings and status control of the PCI device. Each function has 256 byte of configuration space.

4.1.2 1394 OHCI-LINK Register Space

The 1394 OHCI-LINK registers are 2Kbyte of register compliant with the 1394 OHCI specifications. The 1394 OHCI Register Base Address register points to the 2Kbyte memory mapped I/O space. These registers are used to control OHCI-LINK and to set DMA context.

4.1.3 1394 PHY Register Space

The 1394 PHY registers are compliant with the IEEE1394a-2000 standard specifications. These registers are used to set the PHY block (ex. the value of Gap count.) and are accessed through the PHY Control register in the 1394 OHCI-LINK register space.

4.1.4 SD Card Control Register Space

The SD Card Control registers, compliant with the SD Host Controller Standard specification, are 256byte of register assigned to control the SD card. These registers are used to set for access to the SD card, to give commands and to read/write data. These are placed in the memory mapped I/O space by the SD Card Register Base Address register.

4.1.5 Multi Media Card Control Register Space

The Multi Media Card Control registers are 256byte of register assigned to control the Multi Media Card. These registers are used to set for access to the Multi Media Card, to give commands and to read/write data. These are placed in the memory mapped I/O space by the Multi Media Card Register Base Address register.

4.1.6 Memory Stick Control Register Space

The Memory Stick Control registers are 256byte of register assigned to control the Memory Stick. These registers are used to set for access to the Memory Stick, to give commands and to read/write data. These are placed in the memory mapped I/O space by the Memory Stick Register Base Address register.

4.1.7 xD Picture Card Control Register Space

The xD Picture Card Control registers are 256byte of register assigned to control the xD Picture Card. These registers are used to set for access to the xD Picture Card, to give commands and to read/write data. These are placed in the memory mapped I/O space by the xD Picture Card Register Base Address register.

4.2 Error Support

4.2.1 Parity Error

The R5C832 provides the parity generation and the parity error detection on the primary PCI bus. Having detected an address parity error, the R5C832 asserts SERR# and sets the Detected Parity Error bit in the PCI Status register. Having detected a data parity error, the R5C832 asserts PERR# and sets the Detected Parity Error bit in the PCI Status register.

4.2.2 PCI Bus Error concerned with 1394 OHCI

On the 1394 OHCI function, the R5C832 provides occurred PCI Bus errors and some information to recover the errors to system software, via the Context register or the descriptor.

4.3 Interrupts

The R5C832 supports PCI interrupt signals INTA# and INTB#. They transmit to the system the Card Status Change Interrupt as a card insert/remove event, the DMA Interrupt and the Device Interrupt defined on 1394 OHCI, and interrupts defined on the SD Card/ Multi Media Card/ Memory Stick/ xD Picture Card interface. INTA# is assigned to the 1394 OHCI and INTB# is assingned to the SD Card/ Multi Media Card/ Memory Stick/xD Picture Card interfaces. Interrupts of the 1394 can be reassigned by the INT Select bit (bit1) of the 1394 Misc Control 2 register, and Interrupts of SD Card/ Multi Media Card/ Memory Stick/ xD Picture Card interfaces can be reassigned by the INT Select bit (bit25) of the SD Misc Control register/ the MMC Misc Control register/ the MS Misc Control register/the xD Misc Control register.

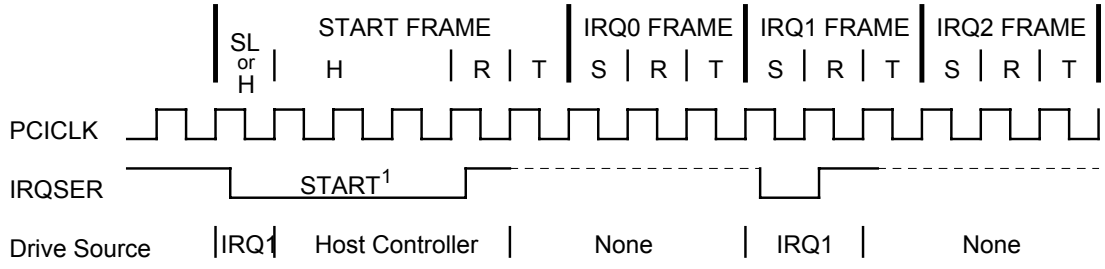
INT Select Bit1	1394
1	INTB#
0	INTA#

INT Select Bit25	SD/MMC/MS/xD
1	INTA#
0	INTB#

On the 1394 OHCI, the R5C832 transmits interrupt signals to the host on the end of the DMA transaction, and also transmits interrupts of the LINK layer and the PHY layer. The IntEvent register and the IntMask register in the OHCI registers control these interrupts. The IntEvent register is used to indicate generations of an interrupt event and the IntMask register is used to enable the selected interrupt. Writing into the IntEventClear by software enables to clear the interrupt.
On the SD Card interface, the Multi Media Card interface, the Memory Stick interface and the xD Picture Card interface, the R5C832 can inform a card insert/remove event or an error as an interrupt to the system. PCI interrupt signals are open drain outputs.

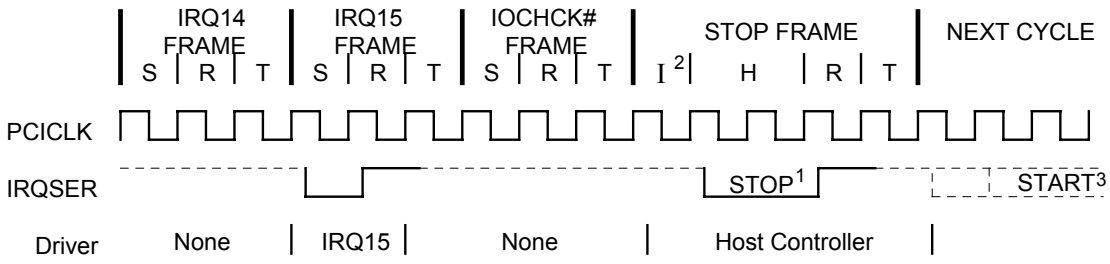
In addition to primary interrupt functions, the R5C832 supports Serialized IRQ. When SRIRQ Enable bit (bit 29) of the Global Misc Control register is set to '1b', UDIO0 works as SRIRQ#. And GPIO and LED0# are also enabled. SRIRQ# output enables a Wired-OR structure that simply transfer a state of one or more device's IRQ to the host controller. Both of a device and a host controller enables a transferring start.
A transferring, called an IRQSER Cycle, consists of three frame types: one Start Frame, several IRQ/Data Frames, and one Stop Frame. Frames of INTA#, INTB#, INTC# and INTD# (PCI Interrupt signals) are output after IOCHK# frame is output.
All cycle uses PCICLK as its clock source. The IRQSER Start Frame has two operation modes: Quiet (Active) mode and Continuous (Idle) mode. On the Quiet (Active) mode, any device can initiate a Start Frame. By occurring of interruptive requests, the R5C832 outputs 1-pulse of PCICLK (Low) and Serialized IRQ is kept on Hi-Z during the rest of a Start Frame. After that, IRQ/DATA Frame follows.
In Continuous (Idle) mode, only Host Controller can initiate a Start Frame. The R5C832 becomes waiting state to detect 4-8 PCICLK of Start Pulse. These modes change automatically by monitoring the Stop pulse width in a Stop Frame. Quiet (Active) mode is repeated when width of Stop Pulse is 2PCICLK, and Continuous (Idle) mode is repeated when it is 3PCICLK. After assertion of the GBRST#, the default is Continuous (Idle) mode.
Timing of the Start Frame and the Stop Frame is as follows:

Start Frame timing with source sampled a low pulse on IRQ1



1. Start Frame pulse can be 4-8 clocks wide.

Stop Frame Timing with Host using 17 IRQSER sampling period



H=Host, SL=Slave Control, R=Recovery, T=Turn-around, S=Sample

1. Stop Pulse is 2 clocks wide for Quiet mode, and 3 clocks wide for Continuous mode.
2. There may be none, one or more Idle states during the Stop Frame.
3. The next IRQSER cycle's Start Frame pulse may or may not start immediately after the turn-around clock of the Stop Frame.

IRQSER Sampling Periods		
IRQ/Data Frame	**Signal Sampled**	**# of clocks past Start**
1	IRQ0	2
2	IRQ1	5
3	SMI#	8
4	IRQ3	11
5	IRQ4	14
6	IRQ5	17
7	IRQ6	20
8	IRQ7	23
9	IRQ8	26
10	IRQ9	29
11	IRQ10	32
12	IRQ11	35
13	IRQ12	38
14	IRQ13	41
15	IRQ14	44
16	IRQ15	47
17	IOCHCK#	50
18	INTA#	53
19	INTB#	56
20	INTC#	59
21	INTD#	62
32:22	Unassigned	95

4.4 Mixed Voltage Operation

The R5C832 has 4 independent power rails. The power for PCI (VCC_PCI3V) is powered at 3.3V, and VCC_RIN is powered at 3.3V. The 1394 OHCI interface (AVCC_PHY3V) is powered at 3.3V. The SD Card interface, the Multi Media Card interface, the Memory Stick interface and the xD Picture Card interface (VCC_3V and VCC_MD3V) are powered at 3.3V.

4.5 Reset Event

Anytime GBRST# is asserted, all R5C832 internal state machines are reset and all registers are set to their default values (provided that each signals has followed the reset sequence below). PCIRST# is asserted, all registers are set to their default value except the following. The default values of each register are described in each register description.

1. These registers are initialized only by GBRST#, not by PCIRST#. (PCI RESET Resistant register).

1394 OHCI-LINK Config. Space:

- 2Ch Subsystem Vendor ID [15:0]
- 2Eh Subsystem ID [15:0]
- 3Eh MIN Grant & MAX Latency [15:0]
- ACh Writable Subsystem Vendor ID [15:0]
- AEh Writable Subsystem ID [15:0]
- 80h 1394 Misc Control [15:0]
- 9Ch 1394 Misc Control 2 [7:0]
- 9Eh 1394 Misc Control 3 [7:0]
- BEh Writable MIN_GNT & MAX_LAT [15:0]
- 98h PHY Power Management [7:0]
- 99h PHY Shadow [7:0]

SD Card Interface Config Space:

· 2Ch	Subsystem Vendor ID	[15:0]
· 2Eh	Subsystem ID	[15:0]
· ACh	Writable Subsystem Vendor ID	[15:0]
· AEh	Writable Subsystem ID	[15:0]
· B0h	SD Clock Control	[23:0]
· BAh	PME Trigger Disable	[7:0]
· BCh	SD Card Detect Control	[23:0]
· E0h	SD Capabilities 0	[15:0]
· E2h	SD Capabilities 1	[15:0]
· E4h	SD Capabilities_RSV	[31:0]
· E8h	SD Maximum Current Capabilities	[31:0]
· ECh	SD Maximum Current Capabilities_RSV	[31:0]
· F8h	SD Misc Control	[31:0]
· FCh	Key	[7:0]

Multi Media Card Interface Config Space:

· 2Ch	Subsystem Vendor ID	[15:0]
· 2Eh	Subsystem ID	[15:0]
· ACh	Writable Subsystem Vendor ID	[15:0]
· AEh	Writable Subsystem ID	[15:0]
· B0h	MMC Clock Control	[23:0]
· BAh	PME Trigger Disable	[7:0]
· BCh	MMC Card Detect Control	[23:0]
· E0h	MMC Misc Control 0	[15:0]
· F8h	MMC Misc Control 1	[31:0]
· FCh	Key	[7:0]

Memory Stick Interface Config Space:

· 2Ch	Subsystem Vendor ID	[15:0]
· 2Eh	Subsystem ID	[15:0]
· 40h	Memory Stick Clock Control	[23:0]
· 4Ah	PME Trigger Enable	[7:0]
· ACh	Writable Subsystem Vendor ID	[15:0]
· AEh	Writable Subsystem ID	[15:0]
· F8h	MS Misc Control	[31:0]
· FCh	Key	[7:0]

xD Picture Card Interface Config Space:

· 2Ch	Subsystem Vendor ID	[15:0]
· 2Eh	Subsystem ID	[15:0]
· 40h	xD Picture Card Clock Control	[23:0]
· 4Ah	PME Trigger Enable	[7:0]
· ACh	Writable Subsystem Vendor ID	[15:0]
· AEh	Writable Subsystem ID	[15:0]
· F8h	xD Misc Control	[31:0]
· FCh	Key	[7:0]

1394 OHCI Register:

· 24h	Global Unique ID High	[31:0]
· 28h	Global Unique ID Low	[31:0]

1394 PHY Register:

·All Registers

SD Card Register:

·All Registers

Multi Media Card Register:

·All Registers

Memory Stick Register:

·All Registers

xD Picture Card Register:

·All Registers

2. These registers are not initialized by PCIRST# when the power state is D3 and PME Enable bit is set to "1". (PME_Context register)

1394 OHCI-LINK Config. Space:
- · DEh Power Management Capabilities [15]
- · E0h Power Management Control/ Status [15,8]

SD Card Config. Space:
- · 82h Power Management Capabilities [15]
- · 84h Power Management Control/ Status [15,8]

Multi Media Card Config. Space:
- · 82h Power Management Capabilities [15]
- · 84h Power Management Control/ Status [15,8]

Memory Stick Config. Space:
- · 82h Power Management Capabilities [15]
- · 84h Power Management Control/ Status [15,8]

xD Picture Card Config. Space:
- · 82h Power Management Capabilities [15]
- · 84h Power Management Control/ Status [15,8]

3. Excepting the above registers (PCI RESET Resistant register, PME_Context register) and the global register, all the registers are initialized by the power state transition from D3 to D0 as long as the power state is D3.

≡Reset Sequence≡

Follow the sequence for initialization when a power is on.
1. Supply power to VCC_3V, AVCC_PHY3V, VCC_MD3V and VCC_RIN.
2. Supply power to VCC_PCI3V.
3. Deassert GBRST#.
4. Deassert HWSPND#.
5. Deassert PCIRST#. (PCLK has to be supplied for 100µsec@33MHz before deasserting PCIRST#.)

Following Step3 by Step2 has no problem.

See the timing a detail of the timing shown in Chapter 5.3.3.

4.6 Power Management

The R5C832 implements two kinds of power management, software suspend mode and hardware suspend mode, in order to reduce the power consumption on suspend, in addition to the adoption of circuit to reduce the power consumption when power on. The software suspend mode conforms to the ACPI (Advanced Configuration and Power Interface) specification and the PCI Bus Power Management Standard. The R5C832, as a PCI device, implements four power states of D0, D1, D2, and D3.
The power management events for the R5C832 and their sources are listed below. The PME# source supports the Card Detect Change event only.
When the power state is except D0, the interrupt is disabled and only PME# can be asserted.

Event	Source
1394 LINKON	R5C832
SD Card Detect Change	R5C832
Multi Media Card Detect Change	R5C832
Memory Stick Detect Change	R5C832
xD Picture Card Detect Change	R5C832

4.6.1 Function on 1394 OHCI-LINK

D0	Fully function of OHCI device state. Unmasked interrupts generate INTx#. And also, PME# can be generated by PME_EN after setting PME_STS.
D1	Ack_tardy is returned on accesses from the 1394. The PCI configuration space, the 1394 OHCI register and the GUID register are preserved. Functional interrupts are masked. Unmasked interrupts can be generated by PME_EN after setting PME_STS. All transmit contexts must be inactive before it attempts to place the R5C832 into the D1 power state. IEEE1394 bus manager shall not be placed into D1. Placing the R5C832 into D1 enables the ack_tardy generation. Software must ensure that IntEve.ack_tardy is 0b and should unmask wake-up interrupt events such as IntEvent.phy and IntEvent.ack_tardy before placing the R5C832 into D1.
D2	LPS is deasserted and stopping supply of SCLK is requested to the PHY. The PCI configuration space is retained and capable of access. The GUID register is retained, but the1394 OHCI register is lost. Functional interrupts are masked. But when the LinkOn signal that is occurred by accepting LinkOn packet or PHY.INTERRUPT is accepted from the PHY, PME# is generated by PME_EN after setting PME_STS.
D3hot	LPS is deasserted and stopping SCLK supply is requested to the PHY. The PCI configuration Space is capable of access, but all register except the PME context is lost. The GUID register is retained, but the1394 OHCI register is lost. On transitioning back to D0, the internal reset is automatically done even if PCIRST# is not asserted. Functional interrupts are masked. But when the LinkOn signal is accepted from the PHY, PME# is generated by PME_EN after setting PME_STS.
D3cold	In addition to the conditions of the D3hot state, VCC_RIN, VCC_3V, VCC_MD3V and AVCC_PHY3V are shifted to the auxiliary power source. D3cold supports functions like D3hot's.

PHY function

On D2 and D3 states, the PHY block can be set to one of the following low power consumption modes by register setting.

	Doze Mode	**Sleep Mode**
Select Condition	Status of both ports is Disconnected, Disabled or Suspended.	
Resume Time	200ns or less	10ms or less

Doze Mode: Power consumption is lowered by:

a) stopping the clock of the PHY digital block, and
b) getting down the power of the PHY analog block.

Sleep Mode: Power consumption is further lowered than Doze Mode by a), b), and

c) getting down the power of PLL and the oscillator.

Setting D2PhyPM bit or D3PhyPM bit on the PHY Power Management register (the 1394 OHCI-LINK Configuration register addr.98h) enables a selection of Doze mode or Sleep mode. On Doze mode or Sleep mode, LinkOn event enables to resume from the power saving mode automatically and PME# is asserted. Each power saving modes cannot be set without the above selected conditions, even if the R5C832 is set to D2 state or D3 state. If the above Ports conditions are not satisfied, the R5C832 transacts as the Repeater PHY. In this time, setting D2ForcePM bit or D3ForcePM bit to 1b enables to ignore above conditions and to set Doze mode or Sleep mode automatically. But, it is disabled LinkOn event to resume from the power consumption mode automatically and to assert PME#. Writing into Power State bits enables to return to D0 state.
In addition, don't cut power supply of VCC_RIN, VCC_3V, VCC_MD3V and AVCC_PHY3V on the suspend mode in spite of the Software and the Hardware.

4.6.2 Function on SD Card/ Multi Media Card/ Memory Stick/ xD Picture Card

D0	The maximum powered state. All PCI/ SD Card/ Multi Media Card/ Memory Stick/ xD Picture Card transactions are acceptable.
D1	Only the PCI Configuration Space access is allowed while the power and clock are provided. SDCCLK, MMCCLK and MSCCLK are output.
D2	Only the PCI Configuration Space access is allowed while the power and clock are provided. SDCCLK, MMCCLK and MSCCLK are output.
D3hot	Only the PCI Configuration Space access is allowed while the power and clock are provided. SDCCLK, MMCCLK and MSCCLK are stopped compulsorily. When the function is brought back to the D0 state, the reset is automatically performed regardless of the assertion of PCIRST#.
D3cold	In addition to the conditions of the D3hot state, VCC_RIN, VCC_3V and VCC_MD3V are shifted to the auxiliary power source. The R5C832 supports power management events from D3cold with the auxiliary power source. The R5C832 can generate PME# even in D3cold state without PCI clock if the event source is SD Card Detect Change or Multi Media Card Detect Change or Memory Stick Detect Change or xD Picture Card Detect Change.

4.7 GPIO

UDIO1, 2, 3 and 4 pins work as GPIO (General Purpose I/O) pins when GPIO Enable bit of the Global Misc Control 1 register (C4h bit31) is set to “1” on Serialized IRQ mode (default) or on UDIO_Select mode of the Global Misc Control 1 register. When GPIO Enable bit is set to “0”, GPIO outputs are Hi-Z and GPIO inputs are disabled. Users can change the characteristics of the GPIO pins to either Input or Output by setting the General Purpose I/O 1 register of the Config register space (C8h). When GPIO Enable bit is set to “1”, setting of GPIO is input mode (default). And it is possible to read the states of their pins through each bit of the GPIO register. On Output mode, the written states of each bit are output. If GPIO functions are not used on Serialized IRQ mode, no pull-up is required.

4.8 Subsystem ID, Subsystem Vendor ID

The R5C832 supports Subsystem ID and Subsystem Vendor ID to meet PC98/99/2001 Design Requirements. There are three ways to write into the Subsystem ID and the Subsystem Vendor ID registers from the system through BIOS.

1. Write Enable bit (1394: bit4 in the 1394 Misc Control 2, SD: bit0 in the Key, MMC: bit0 in the Key, Memory Stick: bit0 in the Key, xD Picture Card: bit0 in the Key) control method.
   The BIOS can turn this bit on, change the Subsystem IDs, and turn it off.
2. Copy of the Subsystem ID and the Subsystem Vendor ID in PCI user defined space method.
   1394/SD/MMC/MS/xD: ACh, AEh
3. Load the Subsystem IDs from the Serial ROM method.
   Connecting UDIO5 to pull-down enables to use the Serial ROM. The R5C832 has the Serial ROM interface, and load the Subsystem ID and the Subsystem Vendor ID after PCI reset disabled.

These registers are initialized only by GBRST#.

4.9 Power Up/Down Sequence

Follow the sequence when the power sequence is ON/OFF.

* When the power sequence is ON:

    1. Supply power to VCC_ RIN.
    2. Supply power to VCC_3V, VCC_MD3V and AVCC_PHY3V.
    3. Supply power to VCC_PCI3V.

* When the power sequence is OFF:

    1. Stop supplying power to VCC_PCI3V.
    2. Stop supplying power to VCC_3V, VCC_MD3V and AVCC_PHY3V.
    3. Stop supplying power to VCC_RIN.

When the power sequence is on, sustain to timing of Global Reset (Chapter 5.3.3) in regards to the control of HWSPND# and GBRST#. GBRST# must be specially asserted on the power supply to AVCC_PHY3V, because the only GBRST# enables to initialize the Cable interface block. The rising of VCC_PCI3V should be within HWSPND# asserted time. When the power sequence is off, the special limit for Delay Time is none.

The R5C832 can operate the PHY as Repeater. Follow the power sequence when the R5C832 operates PHY as Repeater without providing VCC_PCI3V.

* When the power sequence is ON:

    1. Supply power to VCC_ RIN.
    2. Supply power to VCC_3V, VCC_MD3V, and AVCC_PHY3V.

* When the power sequence is OFF:

    1. Stop supplying power to VCC_3V, VCC_MD3V, and AVCC_PHY3V.
    2. Stop supplying power to VCC_ RIN.

In this case also, the special limit for delay time is none when the power sequence is off. Note the following.

a. Asserting GBRST# enables to supply power to AVCC_PHY3V, because the only GBRST# enables to initialize Cable interface. Also, sustain the delay time shown in the chapter 5.3.3 on use of GBRST#.

b. HWSPND# is always set to 'Low'.

4.10 1394 OHCI

The 1394 OHCI block in the R5C832 employs DMA engines for high-performance data transfer, host bus interface and FIFO. The R5C832 supports two types of data transfer: asynchronous and isochronous. Prefer to the 1394 OHCI release 1.1/1.0 specifications for settings and procedures of the controller.

4.10.1 Asynchronous Functions

The R5C832 supports all of transmission and reception defined in 1394 packet formats. Transmitted packets are read out of host memory and received packets are written into host memory, both using DMA. And the R5C832 can be programmed as a bus bridge between the host bus and the 1394 interface by the direct execution of the 1394 read/write requests to the host bus memory space.

4.10.2 Isochronous Functions

The R5C832 includes the cycle master function as defined in the 1394 specification. The cycle start packet is transferred at intervals of 8KHz cycle clock. This cycle master uses the internal cycle clock. When the R5C832 is not the cycle master, the R5C832 can sustain its internal cycle timer sychronized with the cycle master node by correcting its own cycle timer with the reload value from the cycle start packet. The R5C832 supports each DMA controller for each isochronous transmit and isochronous receive. Each DMA controller supports 4 different DMA contexts.

4.10.3 DMA

The R5C832 supports seven types of DMA. Each type of DMA has register space and data stream referred to as a DMA context.

DMA Type	Number of Contexts
Asynchronous Transmit	Request x 1, Response x 1
Asynchronous Receive	Request x 1, Response x 1
Isochronous Transmit	X 4
Isochronous Receive	X 4
Self-ID Receive	X 1
Physical Request & Physical Response	No Context

Each asynchronous and isochronous context is composed of buffer descriptor lists called a DMA context program, which is stored in main memory. The DMA controller finds the necessary data buffers through the DMA context programs.
The Self-ID receive controller is controlled not by the DMA context program but by the two other registers. The R5C832 supports the Physical Request DMA and the Physical Response DMA controllers in order to transmit the receive request, which is to read and write directly to the bus memory space. These controllers are also controlled not by the DMA context program but by the other reserved register.

4.10.4 LINK

The Link module sends packets which appear at the transmit FIFO interfaces to the PHY, and places correctly addressed packets into the receive FIFO. The features are as follows.

- Transmits and receives correctly formatted 1394 serial bus packets.
- Generates the appropriate acknowledge for all received asynchronous packets.
- Performs the cycle master function.
- Generates and checks 32-bit CRC.
- Detects missing cycle start packets.
- Interfaces to PHY.
- Receives isochronous packets at all times (Supports of asynchronous streams and cycle start packets including a CRC error).
- Ignores asynchronous packets received during the isochronous phase.

4.11 SD Card Interface

The R5C832 has one port of SD Card interface, consists of four serial data lines, one serial command line, card detection, write protection and SD clock.

4.11.1 Protocol

After the SD Card interface block in the R5C832 is initialized, the R5C832 outputs the data through the serial SDCMD signal by the host's command (Writing into the SD_CMD register), and the SD Card's response to the command is inputted to the SDCMD signal. The contents of this card's response are stored into the SD_RSP register. The SD Card is initialized after the SD Card interface block checked CRC, etc. After that, the data is transmitted between the R5C832 and the SD Card through the data lines. When the data is written into the SD memory card, the host writes the divided data (default 512byte) into the SD buffer of SD interface block, and the R5C832 transmits the serialized data from the SDDAT [3:0] of SD Interface block.
Conversely, when the data is read from the SD memory card, the SD Card writes the divided data (default 512byte) into the SDDAT [3:0] of SD interface block after initialization of the SD Card by the command response signal.

4.12 Multi Media Card Interface

The R5C832 has one port of Multi Media Card interface, consists of one serial data line, one serial command line, card detection and MMC clock.

4.12.1 Protocol

After the Multi Media Card interface block in the R5C832 is initialized, the R5C832 outputs the data through the serial MMCCMD signal by the host's command (Writing into the MMC_CMD register), and the Multi Media Card's response to the command is input to the MMCCMD signal. The contents of this card's response are stored into the MMC_RSP register. The Multi Media Card is initialized after the Multi Media Card interface block checked CRC, etc. After that, the data is transmitted between the R5C832 and the Multi Media Card through the data lines. When the data is written into the Multi Media Card, the host writes the divided data (default 512byte) into the MMC buffer of Multi Media Card interface block, and the R5C832 transmits the serialized data from the MMCDAT of Multi Media Card Interface block. Conversely, when the data is read from the Multi Media Card, the Multi Media Card writes the divided data (default 512byte) into the MMCDAT of Multi Media Card interface block after initialization of the Multi Media Card by the command response signal.

4.13 Memory Stick Interface

The R5C832 has one port of Memory Stick interface, consists of four serial data lines, one bus state line, card detection and MS clock.

4.13.1 Protocol

The Memory Stick interface block accesses to the Memory Stick registers and the Page Buffer by the Transfer Protocol Command (TPC) in compliance with the host. The R5C832 checks transmission of data between the Page Buffer in the Memory Stick and the Flash Memory and a status after accepting INT signal of the Memory Stick. After that, the R5C832 starts to read / write / erase the data.

4.14 xD Picture Card Interface

The R5C832 has one port of xD Picture Card interface, consists of eight serial data lines, seven control signals and card detection.

4.14.1 Protocol

The R5C832 accesses to the xD Picture Card through the 32-bit Data port register. Writing to the Data port register can transfer address, command and data to the xD Picture Card. The data transfer to the xD Picture Card enables in units of 8-bit, 16-bit or 32-bit. On the 16-bit or 32-bit access, the R5C832 can access to the xD Picture Card by increments of 8-bit unit automatically. Note that only lower 1byte works when write of address and command data.

4.15 Serial ROM Interface

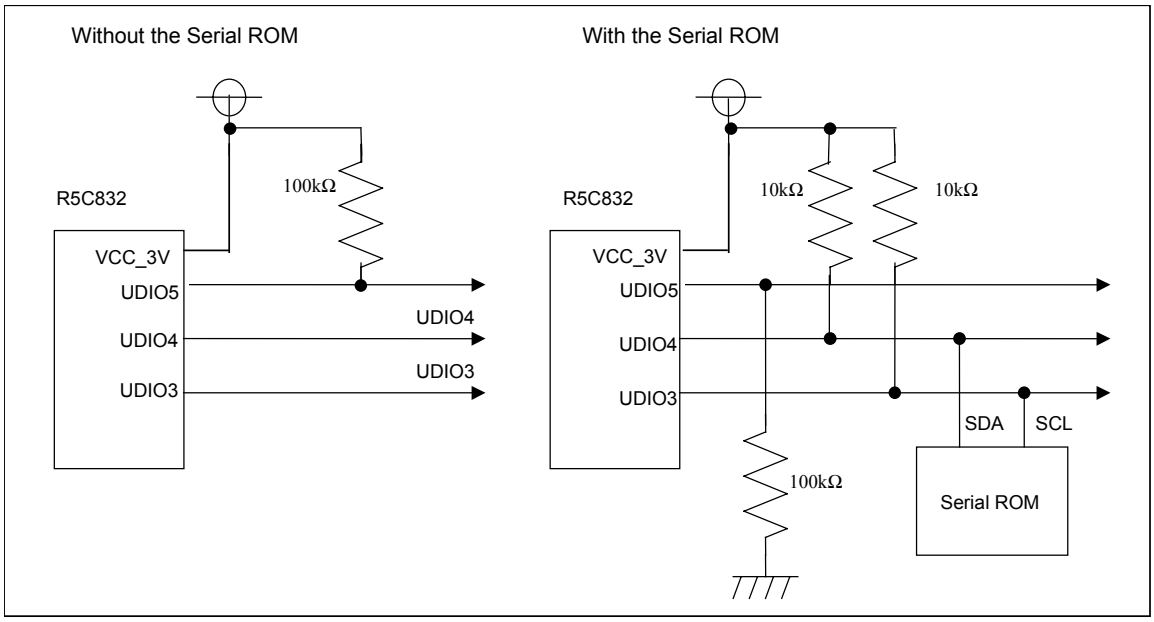
The R5C832 can load data for Subsystem ID, Subsystem Vendor ID (the PCI Interface) and some PCI configuration registers default value from the Serial ROM (I^2C BUS). After that, the R5C832 can set them to each register automatically.

4.15.1 Outline

The R5C832 supports 100k mode and 7-bit address, and automatically stores the data (See Chapter 4.15.3) from the Serial ROM when the first PCI Reset is deasserted after deassertion of the GBRST#.

4.15.2 User's Setting

Connecting the UDIO5 pin to a pull-down resistor of 100kΩ enables the use of the Serial ROM. When the first PCI Reset is deasserted, the R5C832 starts to sample UDIO5 pin. When UDIO5 pin is connected to a pull-down resistor of 100kΩ, the R5C832 attempts to load data through the Serial ROM. In this case, UDIO3 is reassigned to SCL (the clock signal) and UDIO4 is reassigned to SDA (the data signal). The SDA and the SCL must be connected to VCC_3V through pull-up resistors of 10kΩ. When the UDIO5 pin is connected to VCC_3V through a pull-up resistor of 100kΩ, the R5C832 does not load data through the Serial ROM. See the Global Misc Control 1 register for setting of UDIO3 and UDIO4.



4.15.3 Format

The R5C832 starts accesses to the Serial ROM by detecting a pull-down of the UDIO5 when the first PCI Reset is deasserted after deassertion of the GBRST#. The accessed data is stored to each register as follows. The retry states don't allow PCI's slave access during accesses to the Serial ROM. Each parts register of 1394 OHCI-LINK Configuration Space, 1394 OHCI Registers Space, SD Card Configuration Space, Multi Media Card Configuration Space, Memory Stick Configuration Space and xD Picture Card Configuration Space.

4.15.3.1 1394OHCI-LINK Configuration Space

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00h	Subsystem Vendor ID[7:0]							
01h	Subsystem Vendor ID[15:8]							
02h	Subsystem ID[7:0]							
03h	Subsystem ID[15:8]							
04h	LEDTX[1]	LEDTX[0]	LEDRX[1]	LEDRX[0]	-	-	-	-
05h	OHCI10	-	-	-	-	-	-	-
06h	-							
07h	-							
08h	-							
09h	-							
0Ah	-							
0Bh	-							
0Ch	-							
0Dh	-							
0Eh	-							
0Fh	-							
10h	-							
11h	-							
12h	-							
13h	-							
14h	-							
15h	-							
16h	-							
17h	-							
18h	-							
19h	-							
1Ah	-							
1Bh	-							
1Ch	D2PhyPM[1:0]		D2ForcePM	D3PhyPM[1:0]		D3ForcePM	CPSDis	CPSFixVal
1Dh	CMC Shadow	PrwCShadow[2:0]			P0Dis Shadow	-	-	-
1Eh	-							
1Fh	-							
20h	-			SIDWREN	PMbit15 WrEn	-	-	INTXSel
21h	-							
22h	-			-	1394LED toLED0#	LEDDurationSel[1:0]		-
23h	-							
24h	Max Latency[3:0]				Min Grant[3:0]			
25h	-	-	-	-	-	-	-	-

4.15.3.2 1394 OHCI Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
26h	ProgPhyEn	aPhy EnhanceEn	-	-	-	-	-	-
27h	MiniROM Address[7:0]							
28h	Config ROM Header[7:0]							
29h	Config ROM Header[15:8]							
2Ah	Config ROM Header[23:16]							
2Bh	Config ROM Header[31:24]							
2Ch	Bus Option[7:0]							
2Dh	Bus Option[15:8]							
2Eh	Bus Option[23:16]							
2Fh	Bus Option[31:24]							
30h	Global Unique ID High[7:0]							
31h	Global Unique ID High[15:8]							
32h	Global Unique ID High[23:16]							
33h	Global Unique ID High[31:24]							
34h	Global Unique ID Low[7:0]							
35h	Global Unique ID Low[15:8]							
36h	Global Unique ID Low[23:16]							
37h	Global Unique ID Low[31:24]							

4.15.3.3 SD Card Configuration Space

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
38h	-	-	-	-	-	LED Control[2:0]		
39h	Class Code[7:0](specific register-level programming interface)							
3Ah	Class Code[15:8](sub-class code)							
3Bh	Class Code[23:16](base class code)							
3Ch	Subsystem Vendor ID[7:0]							
3Dh	Subsystem Vendor ID[15:8]							
3Eh	Subsystem ID[7:0]							
3Fh	Subsystem ID[15:8]							
40h	-	-	Timeout Clock Select{1:0}		-	-	CLKSelection[1:0]	
41h	-	-	-	-	-	PMETrgDis (Card Removed by SDCD#)	PMETrgDis (Card Inserted by SDCD#)	PMETrgDis (Card Interrupt by SDCDAT1)
42h	Card Detect Counter[3:0]				-	-	Card Detect Mode[1:0]	
43h	-	-	-	-	-	-	-	Counter cut
44h	-	SDLED toLED0#	-	-	-	-	-	-
45h	Write Enable 0xFC							
46h	-	-	SDWPPol	-	-	-	CLKRUNDis,	SDPWRPol
47h	-	-	LEDDurationSel[1:0]		-	-	INTSEL	-
48h	Capability0[7:0]							
49h	Capability0[15:8]							
4Ah	Capability1[7:0]							
4Bh	Capability1[15:8]							
4Ch	Maximum Current for 3.3V							
4Dh	Maximum Current for 3.0V							
4Eh	Maximum Current for 1.8V							
4Fh	-							

4.15.3.4 Multi Media Card Configuration Space

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
50h	-	-	-	-	-	LED Control[2:0]		
51h	Class Code[7:0](specific register-level programming interface)							
52h	Class Code[15:8](sub-class code)							
53h	Class Code[23:16](base class code)							
54h	Subsystem Vendor ID[7:0]							
55h	Subsystem Vendor ID[15:8]							
56h	Subsystem ID[7:0]							
57h	Subsystem ID[15:8]							
58h	-	-	Timeout Clock Select{1:0}		-	-	CLKSelection[1:0]	
59h	-	-	-	-	-	PMETrgDis (Card Removed by MMCCD#)	PMETrgDis (Card Inserted by MMCCD#)	-
5Ah	Card Detect Counter[3:0]				-	-	Card Detect Mode[1:0]	
5Bh	-	-	-	-	-	-	-	Counter cut
5Ch	-	MMCLED toLED0#	-	-	-	-		
5Dh	Write Enable 0xFC							
5Eh	-	-	-	-	-	-	CLKRUNDis,	MMCPWRPol
5Fh	-	-	LEDDurationSel[1:0]		-	-	INTSEL	-
60h	-							
61h	-							
62h	-							
63h	XD_Disable	-	-	MS_Disable	SD_Disable	1394_Disable	MMC_Disable	SDMMC_ Enable
64h	UDIO1				UDIO0			
65h	UDIO3				UDIO2			
66h	UDIO5				UDIO4			
67h	GPIOEN	-	SIRQEN	-	-			

4.15.3.5 Memory Stick Configuration Space

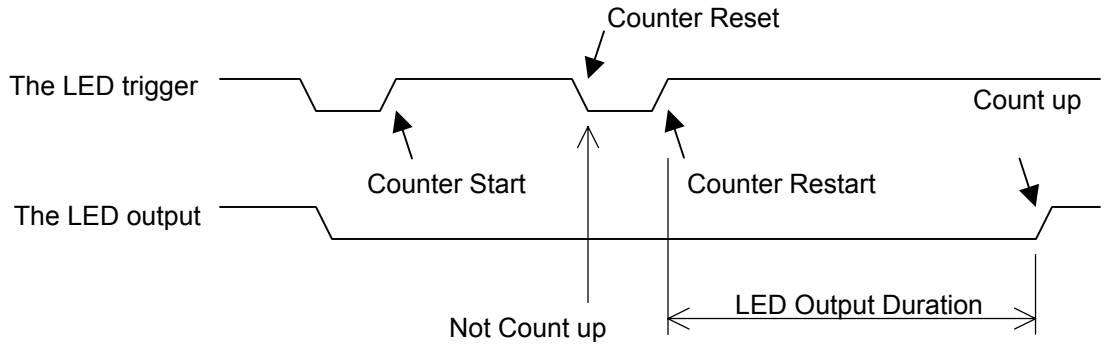
Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
68h	Counter cut	-	-	-	-	-	Card Detect Mode[1:0]	
69h	-	-	-	-	-	-	CLK selection[1:0]	
6Ah	-	-	-	-	-	-	PMETrgIn (Card Inserted by MSCD#)	PMETrgRM (Card Removed by MSCD#)
6Bh	-							
6Ch	Subsystem Vendor ID[7:0]							
6Dh	Subsystem Vendor ID[15:8]							
6Eh	Subsystem ID[7:0]							
6Fh	Subsystem ID[15:8]							
70h	-	MSLED toLED0#	-	-	-	-	-	-
71h	Write Enable 0xFD							
72h	-	-	-	-	-	-	CLKRUNDis,	MSPWRPol
73h	-	-	LEDDurationSel[1:0]		-	INTSEL[1:0]		-

4.15.3.6 xD Picture Card Configuration Space

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
74h	Subsystem Vendor ID[7:0]							
75h	Subsystem Vendor ID[15:8]							
76h	Subsystem ID[7:0]							
77h	Subsystem ID[15:8]							
78h	-	XDLED toLED0#	-	-	-	-	-	-
79h	Write Enable 0xFD							
7Ah	-	-	-	-	-	-	CLKRUNDis,	XDPWRPol
7Bh	-	-	LEDDurationSel[1:0]		-	INTSEL[1:0]		-
7Ch	Counter cut	-	-	-	-	-	Card Detect Mode[1:0]	
7Dh	-	-	-	-	-	-	CLK selection	-
7Eh	-	-	-	-	-	-	PMETrgIn (Card Inserted by XDCD#)	PMETrgRM (Card Removed by XDCD#)

4.16 LED# Output

The R5C832 can output the activity signals of the 1394OHCI, the SD Card, the Multi Media Card, the Memory Stick and the xD PictureCard, as LED0#. The R5C832 uses UDIO0 pin as LED0#. See the Global Misc Control 1 register for the use of this pin. The default of the LED signal is 'Low' active. But, setting the LED Polarity bit of the Global Misc Control 1 register (C4h bit30) to "1b" enables to set the LED signal to 'high' active. This bit is common to the 1394 OHCI, the SD Card, the Multi Media Card, the Memory Stick and the xD Picture Card.
The LED signal is asserted at the same time the trigger of its signal is asserted. And the internal counter works after the trigger is deasserted. In default, the LED signal is kept for 64msec after the deassertion of the trigger, and is deasserted. When the trigger is reasserted in operation of the counter, the counter is cleared and restarted to count up at the same time the deassertion of the LED signal. See the below chart.



The LED Output Duration is selected from among 64msec(default), 1msec and No Duration time (through the trigger). The card and the 1394 have the different registers for selecting each other (See the following). The trigger signals for them also are different.
The R5C832 uses a counter operating PCLK for the LED Output Duration and therefore a stop request of PCLK by the CLKRUN protocol is refused in operation of the counter. When PCLK must be stopped for 64msec on system, modify the LED Output Duration.

LED0#: 1394 LED# + SD LED# + Multi Media Card LED# + Memory Stick LED# + xD LED#

4.16.1 1394 LED

The 1394 LED signal indicates the condition of the IEEE1394 interface block in the R5C832. This signal is asserted when the R5C832 is on transmission/reception.

Bit 2 and bit 1 of the Config (Func.0) 9Eh register can set the counter's duration.

bit 2 1	the LED Output Duration
0 0	64 msec (default)
1 1	1 msec
1 0	No Duration Time (through)
0 1	Test Mode(3.8µsec)

4.16.2 SD LED/MMC LED

The SD LED and the MMC LED signals indicate conditions of the SD Card interface and the Multi Media Card interface in the R5C832. This signal is asserted when the R5C832 is on the transmission, the reception and the debounce duration of the card detection. Bit 29 and bit 28 of the Config (SD: Func.1, MMC: Func.2) F8h register can set the counter's duration.

bit 29 28	the LED Output Duration
0 0	64 msec (default)
1 1	1 msec
1 0	No Duration Time (through)
0 1	Test Mode (3.8µsec)

4.16.3 MS LED/xD LED

The MS LED and the xD LED signals indicate conditions of the Memory Stick interface and the xD Picture Card interface in the R5C832. This signal is asserted when the R5C832 is on the transmission and the reception. Bit 29 and bit 28 of the Config (MS: Func.3, xD: Func.4) F8h register can set the counter's duration.

bit 29 28	the LED Output Duration
0 0	64 msec (default)
1 1	1 msec
1 0	No Duration Time (through)
0 1	Test Mode (3.8µsec)

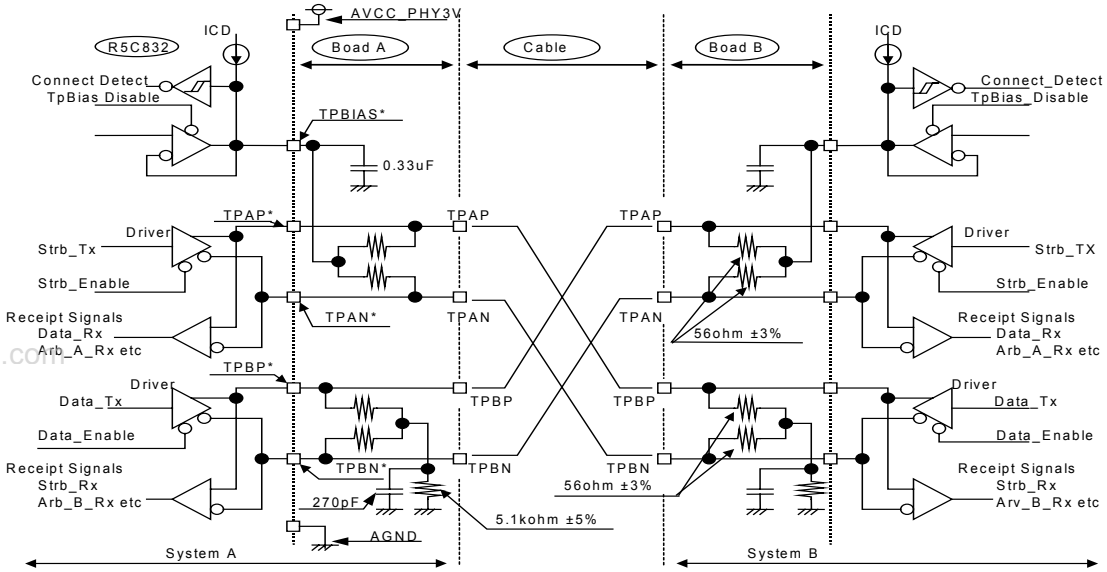
4.16.4 LED Output Selection

Outputs to LED0# can be controlled by setting configuration registers. The LED for the 1394 is output by setting Config (Func.0) 9Eh bit3, the LED for the SD Card is output by setting Config (Func.1) F8h bit 6, the LED for the Multi Media Card is output by setting Config (Func.2) F8h bit6, the LED for the Memory Stick is output by setting Config (Func.3) F8h bit6, and the LED for the xD Picture Card is output by setting Config (Func.4) F8h bit6.

4.17 1394 Cable Interface

The R5C832 builds in 1 port of 1394 Cable interface that supports the transmission speed of 400/200/100Mbps compliant with the IEEE1394a-2000 standard.

4.17.1 Cable Interface Circuit



* means a port number in this figure.
(Example: TPBIAS*→TPBIAS0 or TPBIAS1)

The port consists of two twist-pairs; TPA and TPB. The TPA and the TPB are used in order to monitor transmission/reception of a control signal (Arbitration signal) and data, and the state of a cable line (the insert of a cable).
It is necessary for the TPA and the TPB to be connected to a termination of 55Ω resistances according to the cable impedance. This termination resistance should be arranged near the R5C832. On TPA side, TPBIAS should be placed to the center node of the termination resistance in order to set up a cable's common-mode DC potential. A capacitor of 0.33μF for decoupling should be connected to the TPBIAS. On TPB side, a termination of 5.1kΩ and a capacitor of 270pF should be connected to between the center node of the termination resistance and AGND. See the application manual for the substrate layout.

4.17.2 Transaction of Unused Ports

On no use of ports, TPBP* and TPBN* are directly connected to AGND, and TPAP*, TPAN* and TPBIAS* are OPEN. After that, set Port Disable bit of the 1394 PHY Register. The PHY Shadow register in the 1394 Configuration registers space also can set the Port disable bit. See the Read/Write of the 1394PHY register (Ch. 4.17.4).

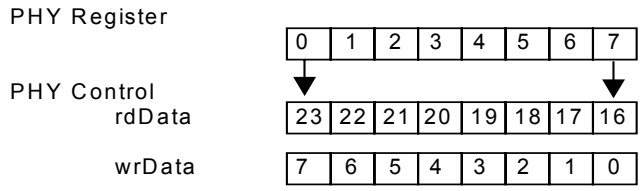
4.17.3 CPS (Cable Power State)

The R5C832 does not support the CPS detect circuit.

4.17.4 Read/Write of 1394 PHY Registers

The R5C832 builds in the 1394 PHY registers compliant with IEEE 1394-1995 and IEEE1394a-2000 standard. Refer to the 1394PHY Registers for details. Access to these registers is enabled by the PHY Control register of the 1394 OHCI Registers, and offsetting [31-11] bits of the 1394 OHCI Register Base Address (10h) in the 1394 Configuration register space enables access to the PHY Control register (0ECh).

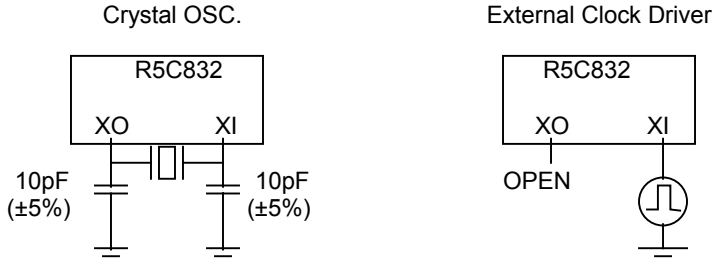
The data of 1394 PHY register is the little endian description. On access of the PHY Control register, the R5C832 converts the data from a little endian to a big endian. So the data is dealt only in a row without the bit number of data.



For example, when 53h is written in wrData of the PHY Control register (bit 6, 4, 1, and 0 are set to "1"), 53h is written in the PHY Register as they are (bit 1, 3, 6, and 7 are set to "1"). Access to Contender bit, Power_class field, and Disable bit for Port0/Port1 in the 1394 PHY register is enabled through the PHY Shadow register (99h) in the 1394 configuration register space. Refer to the PHY Shadow register in the Registers Description for details.

4.17.5 Clock Circuit

The PHY block of the R5C832 requires 24.576MHz of clock frequency.



Recommended Conditions

Crystal Oscillator

Normal Frequency	: 24.576MHz
Frequency Tolerance	: ±50ppm(at 25°C)
Temperature stability	: ±50ppm(reference to 25°C)
Operating Temperature Range	: -20~70°C
Load Capacitance	: 10pF
Driver Level	: 0.1mW
Equivalent Series Resistance	: 50ohm Max
Insulation resistance	: 500M ohm Min (at DC100V±15V)
Shunt Capacitance	: 7.0pF Max

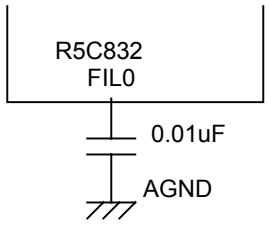
External Clock Driver

Normal Frequency	: 24.576MHz
Frequency Tolerance	: ±50ppm(at 25°C)

4.17.6 PLL

The PHY block of the R5C832 produces 393.216MHz of the internal clock that is 16 times as long as the 24.576MHz produced by the internal PLL circuit. Setting the Sleep Mode of the PHY block can stop the PLL circuit. Refer to the Power Management (Ch. 4.6) for settings of the Sleep Mode.

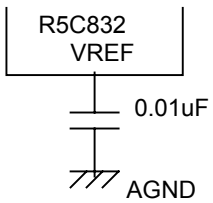
PLL External Circuit



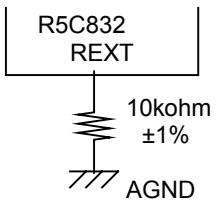
4.17.7 Reference Voltage Circuit and Reference Current Circuit

The PHY block of R5C832 supports terminals of the external parts for the Reference voltage circuit and the Reference current circuit. Each terminal should be connected to indicated capacitors and resistors.

Reference Voltage Circuit



Reference Current Circuit



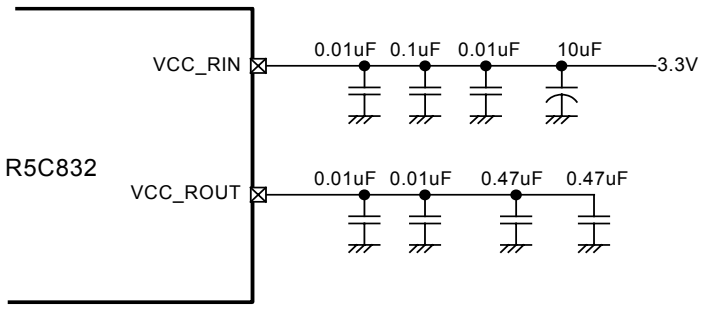
4.18 Function's Selection

The R5C832 can make each function disable by UDIO3 and UDIO4, MSEN and XDEN. Setting UDIO3 to pull-down disables the SD Card interface, setting UDIO4 to pull-down disables the Multi Media Card interface, setting MSEN to pull-down disables the Memory Stick interface, and setting XDEN to pull-down disables the xD Picture Card interface. Disabled function cannot detect the corresponding configuration register (Master Aborts). The function's selection is shown below.
When using the Serial ROM, set the Global Function Disable register with the Serial ROM, because UDIO3 and UIDO4 are set to pull-up.

Function Set Pin				Function Enable/Disable				Function No.				
UDIO3	**UDIO4**	**MSEN**	**XDEN**	**SD**	**MMC**	**MS**	**xD**	**0**	**1**	**2**	**3**	**4**
Pull-up	Pull-up	Pull-up	Pull-up	Enable	Enable	Enable	Enable	1394	SD	MMC	MS	xD
Pull-down	Pull-up	Pull-up	Pull-up	Disable	Enable	Enable	Enable	1394	MMC	MS	xD	-
Pull-up	Pull-down	Pull-up	Pull-up	Enable	Disable	Enable	Enable	1394	SD	MS	xD	-
Pull-down	Pull-down	Pull-up	Pull-up	Disable	Disable	Enable	Enable	1394	MS	xD	-	-
Pull-up	Pull-up	Pull-down	Pull-up	Enable	Enable	Disable	Enable	1394	SD	MMC	xD	-
Pull-down	Pull-up	Pull-down	Pull-up	Disable	Enable	Disable	Enable	1394	MMC	xD	-	-
Pull-up	Pull-down	Pull-down	Pull-up	Enable	Disable	Disable	Enable	1394	SD	xD	-	-
Pull-down	Pull-down	Pull-down	Pull-up	Disable	Disable	Disable	Enable	1394	xD	-	-	-
Pull-up	Pull-up	Pull-up	Pull-down	Enable	Enable	Enable	Disable	1394	SD	MMC	MS	-
Pull-down	Pull-up	Pull-up	Pull-down	Disable	Enable	Enable	Disable	1394	MMC	MS	-	-
Pull-up	Pull-down	Pull-up	Pull-down	Enable	Disable	Enable	Disable	1394	SD	MS	-	-
Pull-down	Pull-down	Pull-up	Pull-down	Disable	Disable	Enable	Disable	1394	MS	-	-	-
Pull-up	Pull-up	Pull-down	Pull-down	Enable	Enable	Disable	Disable	1394	SD	MMC	-	-
Pull-down	Pull-up	Pull-down	Pull-down	Disable	Enable	Disable	Disable	1394	MMC	-	-	-
Pull-up	Pull-down	Pull-down	Pull-down	Enable	Disable	Disable	Disable	1394	SD	-	-	-
Pull-down	Pull-down	Pull-down	Pull-down	Disable	Disable	Disable	Disable	1394	-	-	-	-

4.19 Internal Regulator

The R5C832 has an internal regulator, which converts the single 3.3V power into the power for the internal core logic. The following is the recommended circuit diagram.



5 ELECTRICAL CHARACTERISTICS

5.1 Absolute Maximum Rating

Symbol	Parameter	Range	Unit	Condition	Note
Vcc	Supply Voltage Range	-0.3 ~ 4.6	V	GND=0V	1
Vte	Voltage on Any Pin	-0.3 ~ VCC+0.3	V	GND=0V	
Topr	Ambient Temperature under bias	-40 ~ 85	ºC		
Tstg	Storage Temperature Range	-55 ~ 125	ºC		
ESD1	Human Body Model	±2.0	kV	C=100pF R=1.5kΩ	
ESD2	Charged Device Model	±1.0	kV		
LATUP	Latch-up	±100	mA	5ms	2

Note 1: Applied for VCC_RIN, VCC_3V, VCC_PCI3V and VCC_MD3V and AVCC_PHY3V.
Note 2: The clamping voltage of the trigger pulse power source should be below a value of Vte.

Note: Stresses above those listed may cause permanent damage to system components. These are stress ratings only. Functional operation at these or any conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

5.2 DC Characteristics

5.2.1 Recommended Operating Conditions for Power Supply

Power Pin	Parameter	Min	Typ	Max	Unit	Note
VCC_PCI3V	Supply Voltage for PCI interface (3.3V Operation)	3.0	3.3	3.6	V	
VCC_RIN	Supply Voltage for Regulator	3.0	3.3	3.6	V	
VCC_3V	Supply Voltage for System and Card Interface Signals	3.0	3.3	3.6	V	
VCC_MD3V	Supply Voltage for Media interface block	3.0	3.3	3.6	V	
AVCC_PHY3V	Supply Voltage for Cable interface block	3.0	3.3	3.6	V	

5.2.2 PCI Interface

For 3.3V signaling
(VCC_PCI3V=3.0~3.6V, Ta=0~70ºC)

Symbol	Parameter	Min	Max	Unit	Test Condition	Note
VIH	Input High Voltage	0.5xVCC_PCI3V	VCC_PCI3V+0.3	V		1
VIL	Input Low Voltage	-0.3	0.3xVCC_PCI3V	V		1
VOH	Output High Voltage	0.9xVCC_PCI3V		V	Iout=-500μA	1
VOL	Output Low Voltage		0.1xVCC_PCI3V	V	Iout=1500μA	1
IILk	Input Leakage Current		±10	μA	Vin=0~ VCC_PCI3V	1
Cin	Input Pin Capacitance		10	pF		1
Cclk	PCICLK Pin Capacitance		12	pF		1

Note 1: Applied for PCICLK, CLKRUN#, PCIRST#, AD[31:0], C/BE#[3:0], PAR, FRAME#, IRDY#, TRDY#,STOP#, DEVSEL#, IDSEL, PERR#, SERR#, REQ#, GNT#, INTA#, INTB# pins

5.2.3 System Interface Pins

System Interface Pins
(VCC_3V=3.0~3.6V, Ta=0~70ºC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition	Note
VIH1	Input High Voltage	0.8xVCC_3V		VCC_3V+0.3	V		2
VIL1	Input Low Voltage	-0.3		0.3xVCC_3V	V		2
VIH3	Input High Voltage	2.4		VCC_3V+0.3	V		4
VIL3	Input Low Voltage	-0.3		0.8	V		4
VOH1	Output High Voltage	2.4			V	Iout=-4mA	3
VOL1	Output Low Voltage			0.4	V	Iout=4mA	3
IILk	Input Leakage Current			±10	μA	Vin=0~VCC_3V	4
IIL1	Input Leakage Current (Pull-up)		-80		μA	Vin=0	2
IOZ	Hi-Z Output Leakage Current			±10	μA	Vout=0~VCC_3V	3

Note 2: Applied for MDIO00, MDIO01, MDIO03 pins
Note 3: Applied for MDIO04, MDIO05, MDIO06 pins
Note 4: Applied for GBRST#, HWSPND#, MDIO07 pins

5.2.4 Cable Interface

(AVCC_PHY3V=3.0~3.6V, Ta=0~70ºC)

Symbol	Parameter	Min	Max	Unit	Test Condition	Note
VID	Differential Input Voltage	118	260	mV	Cable input, during data reception	5,6
		168	265	mV	Cable input, during arbitration	
VICM	TpB Common Mode Input Voltage	1.165	2.515	V	100Mbps speed signaling off	6
		0.935	2.515	V	200Mbps speed signaling	
		0.523	2.515	V	400Mbps speed signaling	
VOD	Differential Output Voltage	172	265	mV	Cable output, load 56Ω	5,6
ICM	TpA, TpB Common Mode Output Current	-0.81	0.44	mA	Driver enable, speed signal off	5,6
ISPD2	TpB200Mbps Speed Signal	-4.81	-2.53	mA		6
ISPD4	TpB400Mbps Speed Signal	-12.40	-8.10	mA		6
VTPBIAS	TpBias Output Voltage	1.665	2.015	V		7

Note 5: Applied for TPAP0, TPAN0 pins
Note 6: Applied for TPBP0, TPBN0 pins
Note 7: Applied for TPBIAS0 pin

5.2.5 UDIO0-5 pins

For PCI 3.3V signaling
(VCC_3V=3.0~3.6V, Ta=0~70ºC)

Symbol	Parameter	Min	Max	Unit	Test Condition	Note
VIH	Input High Voltage	0.5xVCC_3V	VCC_3V +0.3	V		9
VIL	Input Low Voltage	-0.3	0.3xVCC_3V	V		9
IILK	Input Leakage Current		±10	μA	Vin=0~VCC_3V	9
VOH	Output High Voltage	2.4		V	Iout=-4mA	8
VOL	Output Low Voltage		0.4	V	Iout=4mA	8
IOZ	Hi-Z Output Leakage Current		±10	μA	Vout=0~VCC_3V	8

Note 8: Applied for UDIO1-5 pins
Note 9: Applied for UDIO1-4 pins

5.2.6 SD Card Interface

(VCC_MD3V=3.0~3.6V, Ta=0~70ºC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition	Note
VIH	Input High Voltage	0.625x VCC_MD3V		VCC_MD3V +0.3	V		10
VIL	Input Low Voltage	-0.3		0.25x VCC_MD3V	V		10
VOH	Output High Voltage	0.75x VCC_MD3V			V	Iout=-100μA@3V	10,11
VOL	Output Low Voltage			0.125xVCC_MD3V	V	Iout=100μA@3V	10,11
IIL	Input Leakage Current (Pull-up)		-80		μA	Vin=0	10
IOZ	HI-Z Output Leakage Current			±10	μA	Vout=0~ VCC_MD3V	11

Note 10: Applied for SDCDAT [3:0], SDCCMD pins
Note 11: Applied for SDCCLK pin

5.2.7 Multi Media Card Interface

(VCC_MD3V=3.0~3.6V, Ta=0~70ºC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition	Note
VIH	Input High Voltage	0.625x VCC_MD3V		VCC_MD3V +0.3	V		12
VIL	Input Low Voltage	-0.3		0.25x VCC_MD3V	V		12
VOH	Output High Voltage	0.75x VCC_MD3V			V	Iout=-100μA@3V	12,13
VOL	Output Low Voltage			0.125xVCC_MD3V	V	Iout=100μA@3V	12,13
IIL	Input Leakage Current (Pull-up)		-80		μA	Vin=0	12
IOZ	HI-Z Output Leakage Current			±10	μA	Vout=0~ VCC_MD3V	13

Note 12: Applied for MMCDAT, MMCCMD pins
Note 13: Applied for MMCCLK pin

5.2.8 Memory Stick Interface

(VCC_MD3V=3.0~3.6V, Ta=0~70ºC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition	Note
VIH	Input High Voltage	0.8x VCC_MD3V		VCC_MD3V	V		14
VIL	Input Low Voltage	0		0.2xVCC_MD3V	V		14
VOH	Output High Voltage	VCC_MD3V -0.3			V	Iout=-8mA	14
VOL	Output Low Voltage			0.4	V	Iout=8mA	14
IOZ	HI-Z Output Leakage Current			±10	µA		14

Note 14: Applied for MSCDAT [3:0], MSCCLK, MSBS pins

5.2.9 xD Picture Card Interface

(VCC_MD3V=3.0~3.6V, Ta=0~70ºC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition	Note
VIH	Input High Voltage	2.1		VCC_MD3V+0.3	V		15
VIL	Input Low Voltage	-0.3		0.7	V		15
VOH	Output High Voltage	2.6			V	Iout=-8mA	15,16
VOL	Output Low Voltage			0.4	V	Iout=8mA	15,16
IOZ	HI-Z Output Leakage Current			±10	µA		15,16

Note 15: Applied for XDDAT [7:0] pins
Note 16: Applied for XDRE#, XDWE#, XDCE#, XDALE, XDCLE, XDWP# pins

5.2.10 Serial ROM Interface

For 3.3V signaling
(VCC_3V=3.0~3.6V, Ta=0~70ºC)

Symbol	Parameter	Min	Max	Unit	Test Condition	Note
VIH	Input High Voltage	0.7xVCC_3V	VCC_3V+0.3	V		17
VIL	Input Low Voltage	-0.3	0.3xVCC_3V	V		17
VOL1	Output Low Voltage		0.4	V	Iout=3mA	17
Tof	Output fall time from V_{IHmin} to V_{ILmax} with a bus capacitance from 10 pF to 400 pF:	-	250	ns	with up to 3 mA sink current at V_{OL1}	17
I_I	Input current each I/O pin		±10	µA	Vin=0.4~0.9xVCC_3V	17
Cin	Input Pin Capacitance		10	pF		17

Note 17: Applied for UDIO3-4 (On use of Serial ROM) pins

5.2.11 Power Consumption

Power Supply Current

Power Pin	Parameter	Min	Typ	Max	Unit	Condition	Note
Icc	Power Supply Current, Operating			75	mA	PCICLK=33MHz VCC_3V=3.6V VCC_MD3V=3.6V VCC_PCI3V=3.6V AVCC_PHY3V=3.6V VCC_RIN=3.6V Vin=0V or VCC	

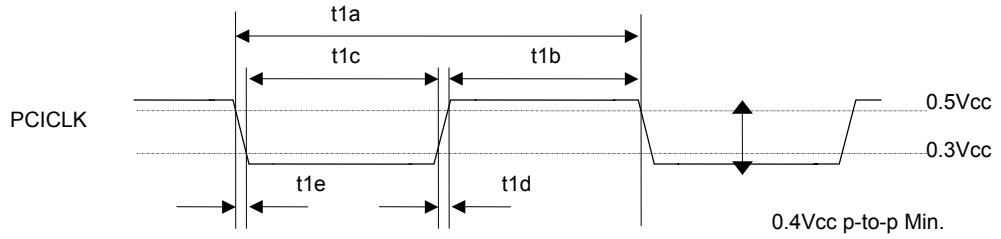
5.3 AC Characteristics

5.3.1 PCI Interface signals

PCI Clock
(VCC_PCI3V=3.0~3.6V, Ta=0~70ºC)

Symbol	Parameter	Min	Max	Unit	Note
	PCICLK				
t1a	Cycle Time, PCICLK	30		ns	
t1b	Pulse Width Duration, PCICLK High	11		ns	
t1c	Pulse Width Duration, PCICLK Low	11		ns	
t1d	Slew Rate, PCICLK Rising Edge	1	4	V/ns	
t1e	Slew Rate, PCICLK Falling Edge	1	4	V/ns	

PCICLK Timing

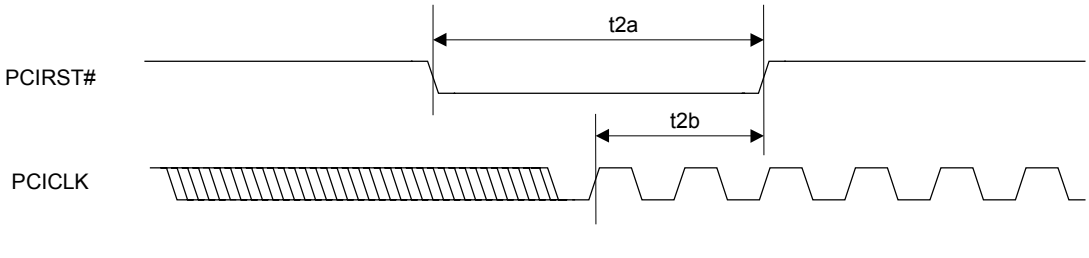


PCICLK Timing

PCI Reset
(VCC_PCI3V=3.0~3.6V, Ta=0~70ºC)

Symbol	Parameter	Min	Max	Unit	Note
	PCIRST#				
t2a	Pulse Duration, PCIRST#	1		ms	
t2b	Setup Time, PCICLK active at PCIRST# Negation	100		µs	

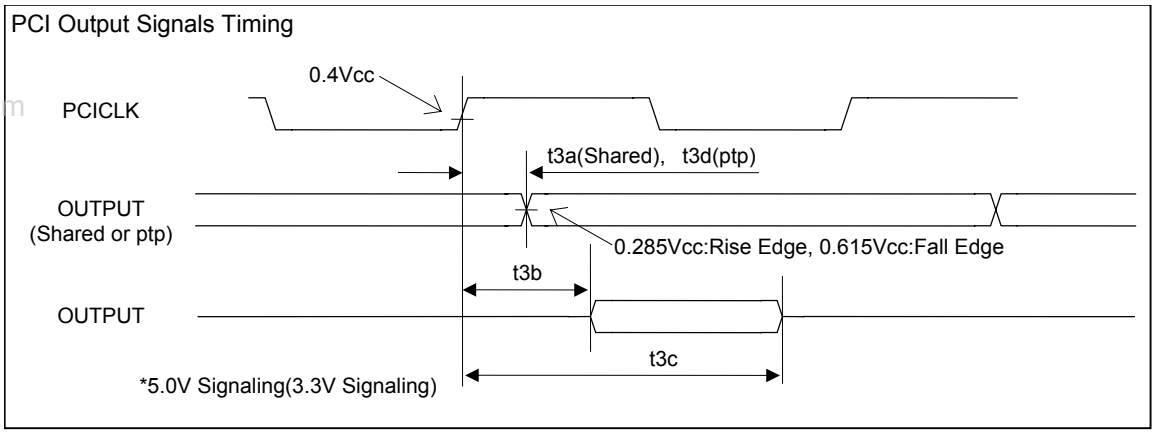
PCI Reset Timing



PCI Reset Timing

PCI Interface Output Signals
(VCC_PCI3V=3.0~3.6V, Ta=0~70ºC)

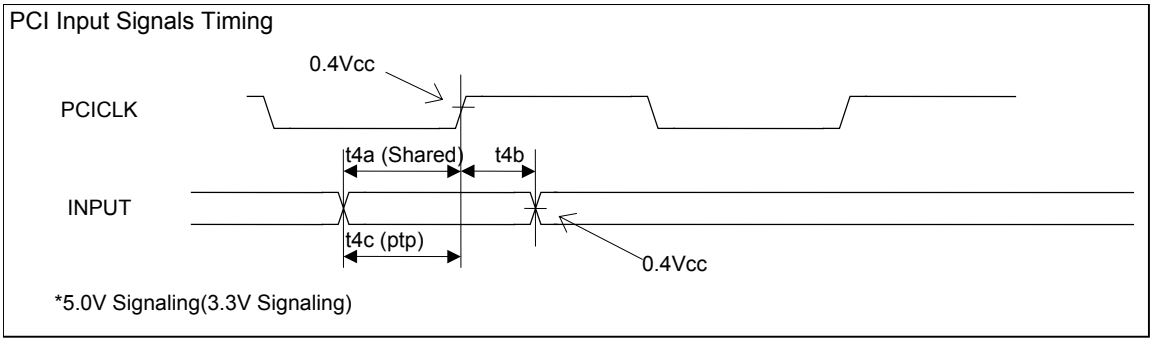
Symbol	Parameter	Min	Max	Unit	Note
	AD [31:0], C/BE#[3:0], PAR, FRAME#, DEVSEL#, IRDY#, TRDY#, STOP#, PERR#, SERR#, CLKRUN#				
t3a	Shared Signal Valid delay time from PCICLK	2	11	ns	Min: CL=0 pF Max: CL=50 pF (10 pF 3.3v)
t3b	Enable Time, Hi-Z to active delay from PCICLK	2		ns	
t3c	Disable Time, Active to Hi-Z delay from PCICLK		28	ns	
	REQ#				
t3d	Point to Point Signal Valid delay time from PCICLK	2	12	ns	Min: CL=0 pF Max: CL=50 pF (10 pF 3.3v)



PCI Output Signals Timing

PCI Interface Input Signals
(VCC_PCI3V=3.0~3.6V, Ta=0~70ºC)

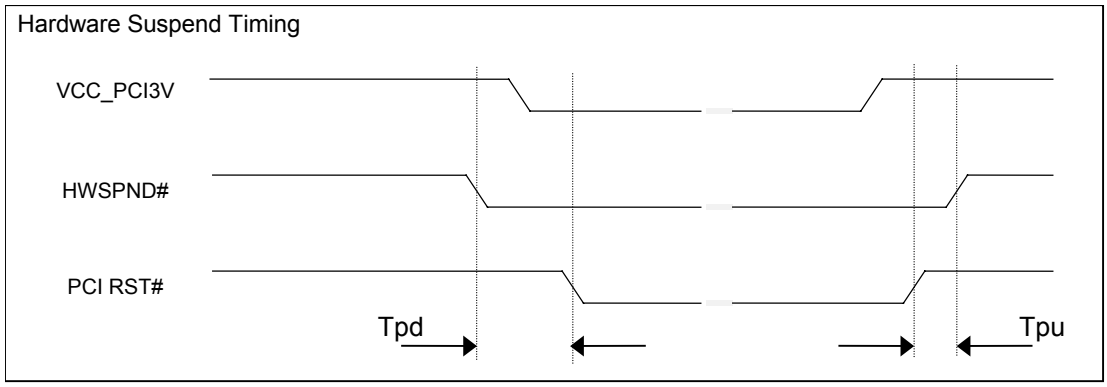
Symbol	Parameter	Min	Max	Unit	Note
	AD [31:0], C/BE#[3:0], PAR, FRAME#, DEVSEL#, IRDY#, TRDY#, STOP#, IDSEL, PERR#, SERR#, CLKRUN#				
t4a	Setup Time, Shared Signal Valid before PCICLK	7		ns	
t4b	Hold Time, Shared Signal Hold Time after PCICLK High	0		ns	
	GNT#				
t4c	Setup Time, Point to Point Signal Valid before PCICLK	10		ns	



PCI Input Signals Timing

5.3.2 Hardware Suspend mode

Timing chart for keeping the value of the internal register on the Suspend mode.

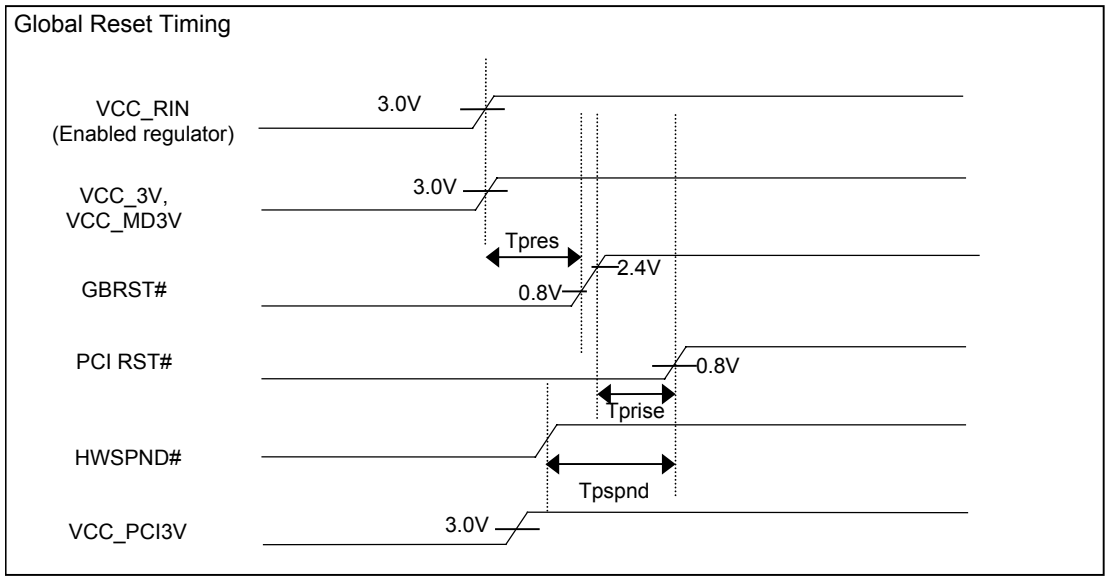


Symbol	Parameter	Min	Typ	Max	Unit
Tpd	HWSPND# to PCIRST# delay	100*1			ns
Tpu	PCIRST# Setup time to HWSPND#	100*1			ns

*1 : PCICLK=33MHz

5.3.3 Global Reset signals

Timing chart for initializing the internal register on the Power's on.



Symbol	Parameter	Min	Typ	Max	Unit
Tpres	Power_On to GBRST# delay	1		100	ms
Tprise	GBRST# to PCIRST# delay	60*2			ns
Tpspnd	HWSPND# to PCIRST# delay	100*2			ns

*2 : PCICLK=33MHz

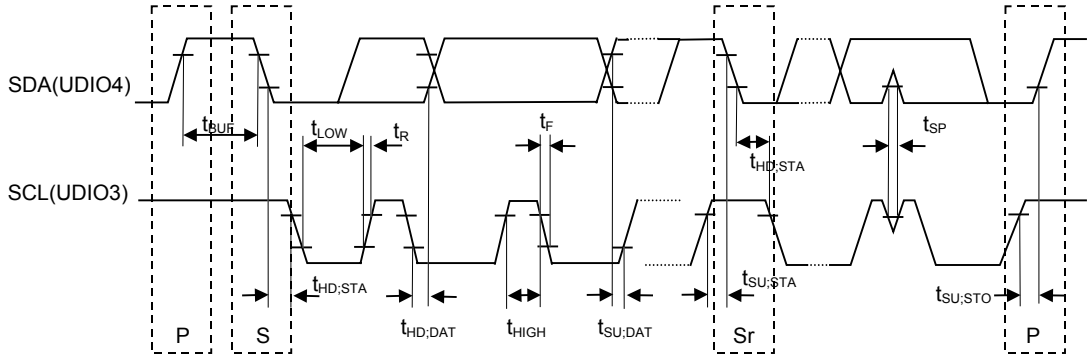
5.3.4 Serial ROM Interface signals

SDA (UDIO4), SCL (UDIO3)
(VCC_3V=3.0~3.6V, Ta=0~70ºC)

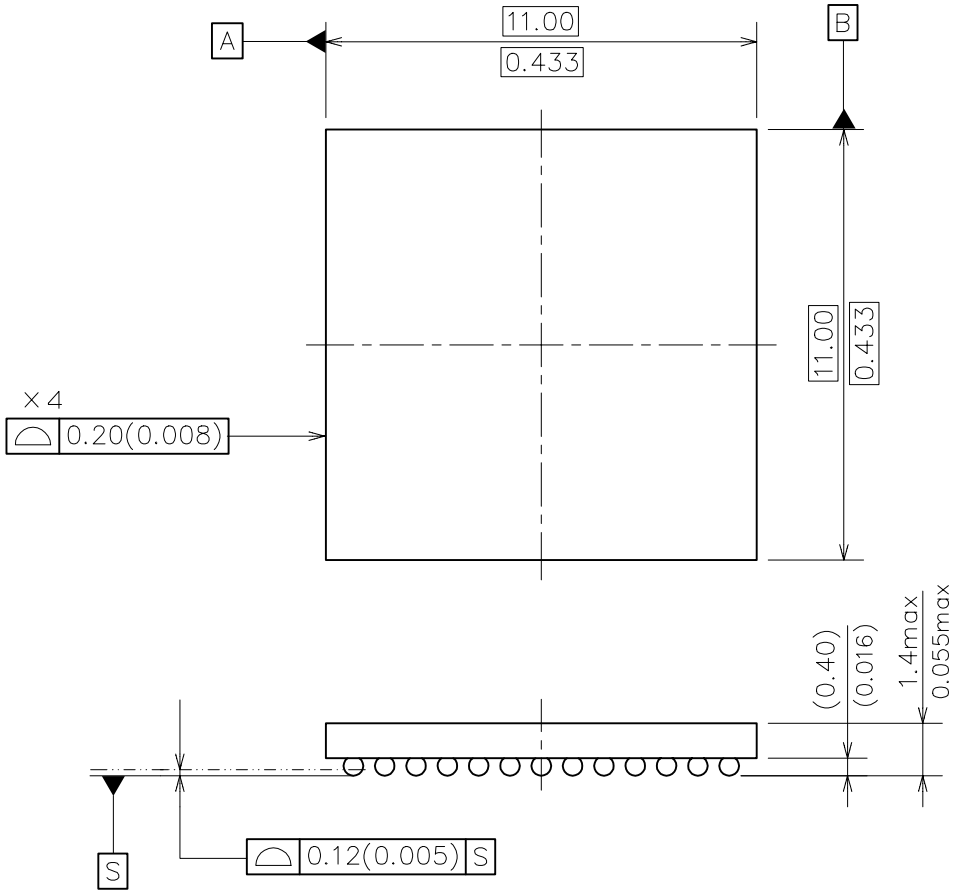
Symbol	Parameter	Min	Max	Unit	Note
	SDA (UDIO4), SCL (UDIO3)				
f SCL	SCL clock frequency	0	100	kHz	
t BUF	Bus free time between a STOP and START condition	4.7	-	us	
t HD;STA	Hold time (repeated) START condition. After this period, the first clock pulse is generated	4.0	-	us	
t LOW	LOW period of the SCL clock	4.7	-	us	
t HIGH	HIGH period of the SCL clock	4.0	-	us	
t SU;STA	Set–up time for a repeated START condition	4.7	-	us	
t HD;DAT	Data hold time for I 2 C–bus devices	0		us	
t SU;DAT	Data set–up time	250	-	ns	
t R	Rise time of both SDA and SCL signals	-	1000	ns	
t F	Fall time of both SDA and SCL signals	-	300	ns	
t SU;STO	Set–up time for STOP condition	4.0	-	us	
t sp	Pulse width of spikes which must be suppressed by the input filter	n/a	n/a	ns	
C b	Capacitive load for each bus line	-	400	pF	

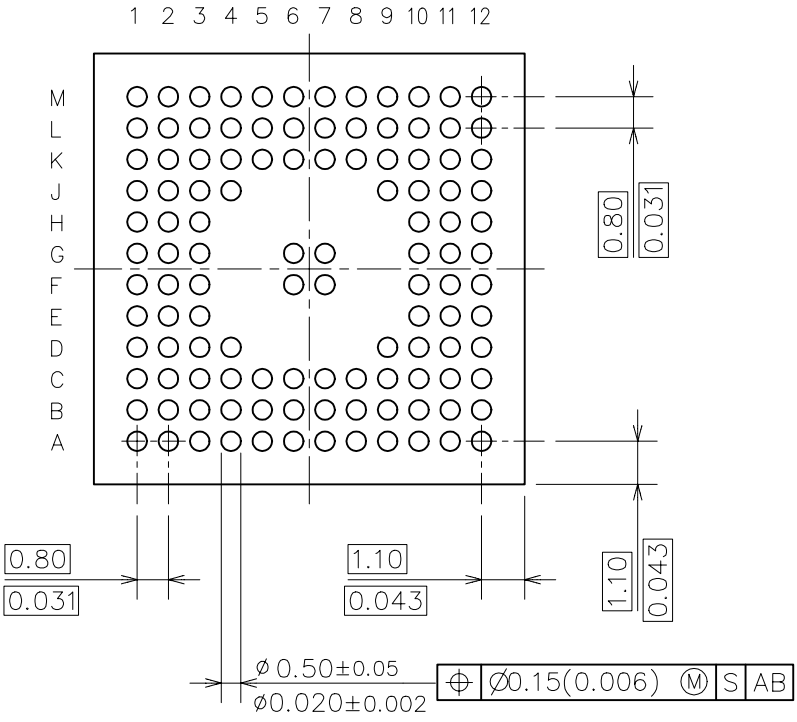
All values referred to V IHmin and V ILmax levels (see 5.2.10).

Serial ROM if SDA,SCL timing



PACKAGE CODE	CSP−116−P1(1111)





UNIT: mm / inch

DIMENSIONAL TOLERANCE (±)			
DIMENSION X \ CLASS	1	2	3
X ≦ 16	0.1	0.1	0.2
16< X ≦ 63	0.1	0.2	0.3
63< X ≦ 250	0.2	0.3	0.5
250< X ≦ 1000	0.3	0.5	0.8
1000< X ≦ 4000			0.8

SPECIFIED GRADE	VISUAL GRADE
ANGLE TOL	SCALE NTS

DATE	CHANGE NOTICE / DRAW UP DATE	SIGN
	2004.11.26	

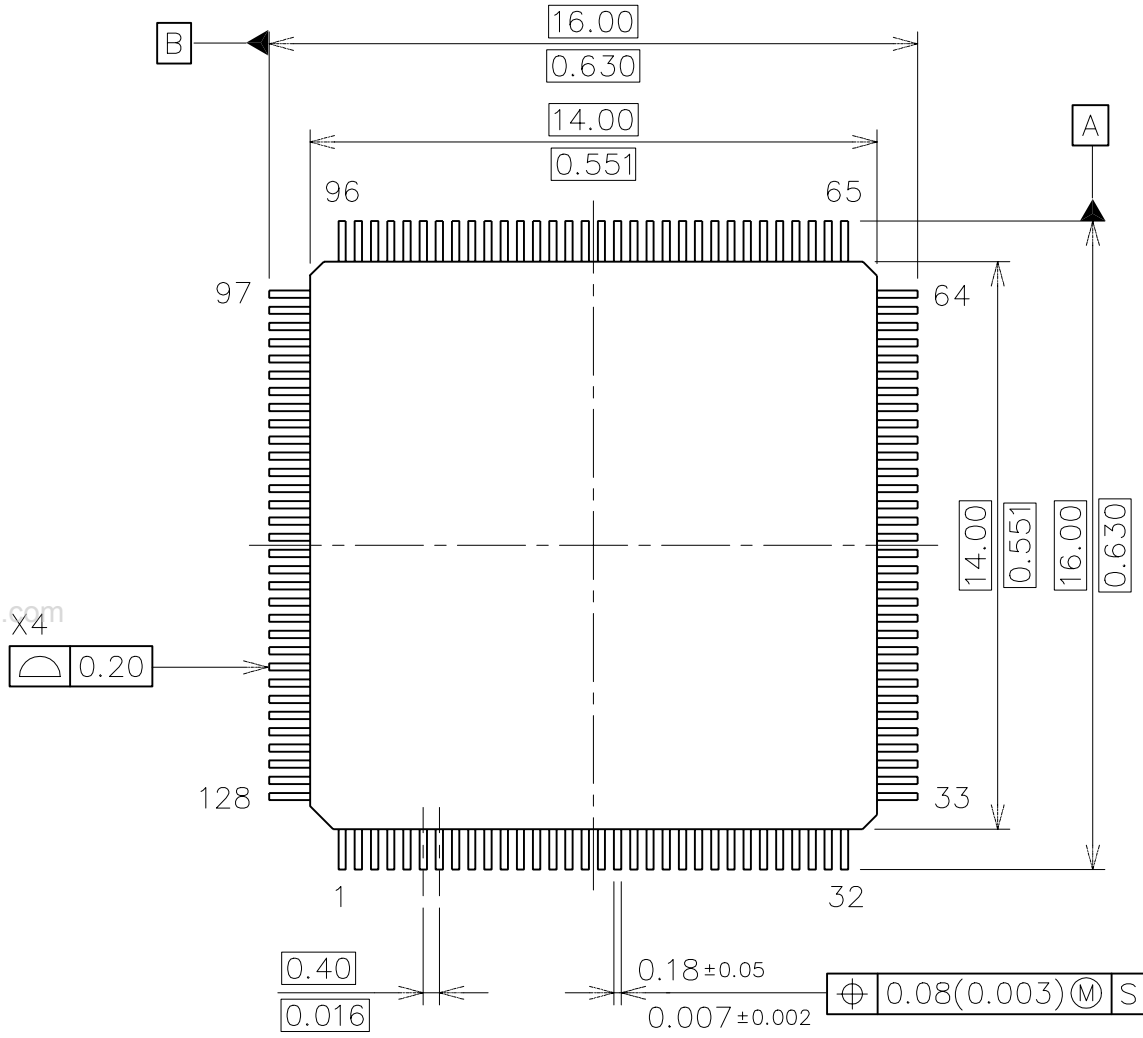
PART NAME: CSP116PIN(P1) PACKAGE OUTLINE

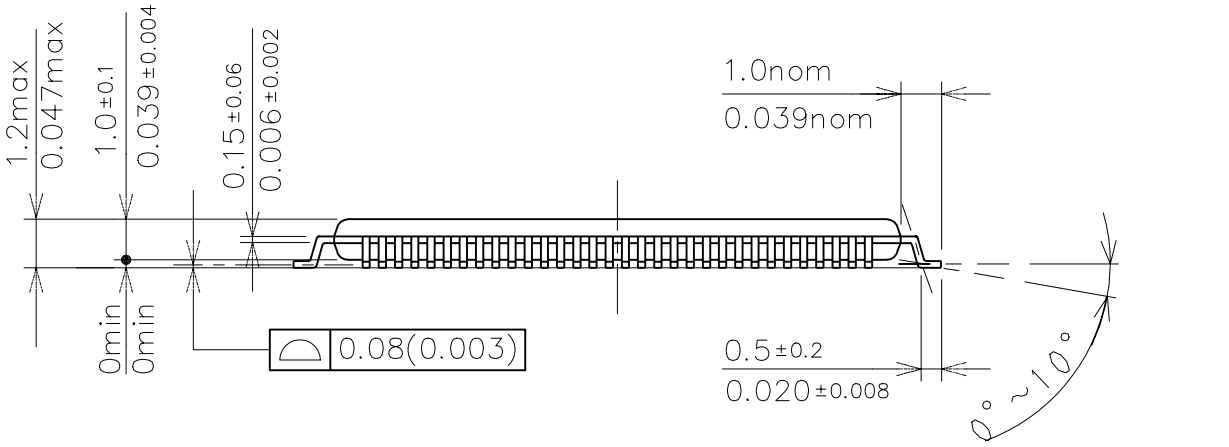
APPROVED BY	CHECKED BY	DESIGNED BY	DRAWN BY
T.YOSHIMURA	H.GOTOH	H.EGUCHI	K.SHIMOKAWA

PART NO. DF−116CSP−001 A

RICOH

PACKAGE CODE	TQFP−128−P1 (1414)





UNIT: mm / inch

DIMENSIONAL TOLERANCE (±)				SPECIFIED GRADE	VISUAL GRADE
DIMENSION X / CLASS	1	2	3		
X ≦ 16	0.1	0.1	0.2		
16< X ≦ 63	0.1	0.2	0.3		
63< X ≦ 250	0.2	0.3	0.5	ANGLE TOL	SCALE
250< X ≦ 1000	0.3	0.5	0.8		NTS
1000< X ≦ 4000			0.8		

DATE	CHANGE NOTICE / DRAW UP DATE	SIGN
	2004.12.6	

PART NAME: TQFP128PIN(P1) PACKAGE OUTLINE

APPROVED BY	CHECKED BY	DESIGNED BY	DRAWN BY	PART NO.		
T.YOSHIMURA	H.GOTOH	H.EGUCHI	K.SHIMOKAWA	DF−128TQFP−001	A	/

RICOH

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5. The products listed in this Data Sheet are intended and designed for use as general electronic components in standard applications (office equipment, computer equipment, measuring instruments, consumer electronic products, amusement equipment etc.). Those customers intending to use a product in an application requiring extreme quality and reliability, for example, in a highly specific application where the failure or miss-operation of the product could result in human injury or death (aircraft, spacevehicle, nuclear reactor control system, traffic control system, automotive and transportation equipment, combustion equipment, safety devices, life support system etc.) should first contact us.
6. We are making our continuous effort to improve the quality and reliability of our products, but semiconductor products are likely to fail with certain probability. In order prevent any injury to persons or damages to property resulting from such failure, customers should be careful enough to incorporate safety measures in their design, such as redundancy feature, fire-containment feature, and fail-safe feature. We do not assume any liability or responsibility for any loss or damage arising from misuse or inappropriate use of the products.
7. Anti-radiation design is not implemented in the products described in this Data Sheet.
8. Please contact Ricoh sales representatives should you have any questions or comments concerning the products or the technical information.

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