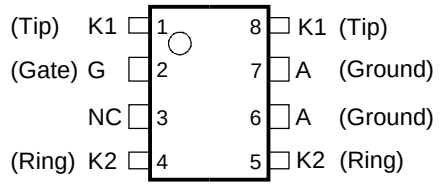
DECEMBER 1995 - REVISED SEPTEMBER 1997

OVERVOLTAGE PROTECTION FOR ERICSSON COMPONENTS LINE INTERFACE CIRCUITS

- **PBA 3357/3 DCLIC Overvoltage Protector**
- **Dual Voltage-Programmable Protector**
  - **Wide 0 to -70 V Programming Range**
  - **Low Voltage Overshoot Crowbar and Diode**
  - **Low 5 mA max. Triggering Current**
  - **Does not Charge Gate Supply**
  - **Specified for 0°C to 70°C Operation**
  - **Plastic Dual-in-line Package**
- **Rated for International Surge Wave Shapes**

WAVE SHAPE	STANDARD	I_{TSP} A
2/10 µs	TR-NWT-001089	80
0.5/700 µs	RLM88	38
10/700 µs	K17, K20, K21	38
10/1000 µs	TR-NWT-001089	30

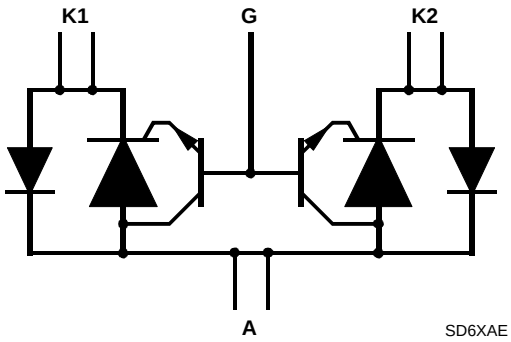
P PACKAGE
(TOP VIEW)



MD6XAV

NC - No internal connection
Terminal typical application names shown in parenthesis

device symbol



SD6XAE

Terminals K1, K2 and A correspond to the alternative line designators of T, R and G or A, B and C. The negative protection voltage is controlled by the voltage, $V_{GG,}$ applied to the G terminal.

description

The R3612 is a dual forward-conducting buffered p-gate over voltage protector in a plastic DIP package. It is designed to protect the Ericsson Components PBA 3357/3 DCLIC (Dual Channel Complete Line Interface Circuit) against over voltages on the telephone line caused by lightning, a.c. power contact and induction. The R3612 limits voltages that exceed the DCLIC supply rail voltage.

The DCLIC line driver section is powered from 0 V (ground) and a negative voltage in the region of -44 V to -56 V. The protector gate is connected to this negative supply. This references the protection (clipping) voltage to the negative supply voltage. As the protection voltage will track the negative supply voltage the over voltage stress on the DCLIC is minimised.

Positive over voltages are clipped to ground by a low voltage overshoot diode. Negative over voltages are initially clipped close to the DCLIC negative supply rail value. If sufficient current is available from the over voltage, then the protector will crowbar into a low voltage on-state condition. As the over voltage subsides the high holding current of the crowbar prevents d.c. latchup.

The buffered gate design reduces the loading on the DCLIC supply during over voltages caused by power cross and induction. The gate characteristic is designed to produce a net current drain on the interface circuit voltage supply during low level power cross or induction. This removes the need for a separate clamping diode across the voltage supply.

These monolithic protection devices are fabricated in ion-implanted planar vertical power structures for high reliability and in normal system operation they are virtually transparent.

Characteristic values for the R3612 are measured either at the extremes of the DCLIC recommended operating voltage range (-44 V to -56 V) or at the DCLIC maximum rated supply voltage (-70 V).

absolute maximum ratings

RATING	SYMBOL	VALUE	UNIT
Non-repetitive peak off-state voltage, I_G = 0, 0°C ≤ T_J ≤ 70°C	V_{DSM}	-90	V
Repetitive peak off-state voltage, I_G = 0, 0°C ≤ T_J ≤ 70°C	V_{DRM}	-80	V
Repetitive peak gate-cathode voltage, V_{KA} = 0, 0°C ≤ T_J ≤ 70°C	V_{GKRM}	-80	V
Non-repetitive peak on-state pulse current (see Notes 1 and 2)			
10/1000 µs (Bellcore TR-NWT-001089, Section 4 and Appendix A)	I_{TSP}	30	A
0.2/310 µs (RLM88, open-circuit voltage wave shape 1.5 kV 0.5/700 µs)		38	
5/310 µs (CCITT K17, K20 & K21, open-circuit voltage wave shape 1.5 kV 10/700 µs))		38	
2/10 µs (Bellcore TR-NWT-001089, Section 4 and Appendix A)		80	
Non-repetitive peak on-state current, 50 Hz (see Notes 1 and 2)			
200 ms	I_{TSM}	5.6	A
1 s		3.5	
25 s		0.7	
900 s		0.42	
Non-repetitive peak gate current, 1/2 µs,(see Notes 1 and 2)	I_{GSM}	25	A
Junction temperature	T_J	-55 to +150	°C
Storage temperature range	T_{stg}	-55 to +150	°C

NOTES: 1. Initially the protector must be in thermal equilibrium with 0°C ≤ T_J ≤ 70°C. The surge may be repeated after the device returns to its initial conditions.
2. Above 70°C, derate linearly to zero at 150°C lead temperature.

recommended operating conditions

		MIN	TYP	MAX	UNIT
C_G	Gate decoupling capacitor		220		nF

electrical characteristics, T_{amb} = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_D	Off-state current	$V_D = V_{DRM}$, V_{GK} = 0	T_J = 0°C			5	µA
			T_J = 70°C			50	µA
$V_{(BO)}$	Breakover voltage	I_T = 20 A, I3124 generator, open-circuit voltage wave shape 1 5 kV 0.5/700 µs, board resistance R_S = 35 Ω, C_G = 220 nF, V_{GG} = -56 V (See Note 3 and Figure 1.)				-80	V
$t_{(BR)}$	Breakdown time	I_T = 20 A, I3124 generator, open-circuit voltage wave shape 1 5 kV 0.5/700 µs, board resistance R_S = 35 Ω, C_G = 220 nF, V_{GG} = -56 V (See Note 3 and Figure 1.)	$V_{(BR)}$ < -70 V $V_{(BR)}$ < -58.5 V			1 10000	µs
V_F	Forward voltage	I_F = 5 A, t_w = 500 µs				3	V
V_{FRM}	Peak forward recovery voltage	I_F = 20 A,I3124 generator, open-circuit voltage wave shape 1 5 kV 0.5/700 µs, board resistance R_S = 35 Ω, C_G = 220 nF, V_{GG} = -56 V (See Note 4 and Figure 1.)				15	V
t_{FRM}	Forward recovery time	I_T = 20 A, I3124 generator, open-circuit voltage wave shape 1 5 kV 0.5/700 µs, board resistance R_S = 35 Ω, C_G = 220 nF, V_{GG} = -56 V (See Note 4 and Figure 1.)	V_F > 10 V V_F > 5 V V_F > 1 V			0.25 1 10000	µs
I_H	Holding current	I_T = 1 A, di/dt = -1A/ms, V_{GG} = -70 V, 0°C ≤ T_J ≤ 70°C		105			mA
I_{GAS}	Gate reverse current	V_{GG} = -70 V, V_{AK} = 0	T_J = 0°C			-5	µA
			T_J = 70°C			-50	
I_{GAT}	Gate reverse current, on state	I_T = 0.5 A, t_w = 500 µs, V_{GG} = -70 V				-1	mA

electrical characteristics, T_{amb} = 25°C (unless otherwise noted) (Continued)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{GAF}	Gate reverse current, forward conducting state	I_F = 1 A, t_w = 500 µs, V_{GG} = -70 V			-10		mA
I_{GT}	Gate trigger current	I_T = 5 A, $t_{p(g)} \geq$ 20 µs, V_{GG} = -44 V				5	mA
V_{GT}	Gate trigger voltage	I_T = 5 A, $t_{p(g)} \geq$ 20 µs, V_{GG} = -44 V				2.5	V
C_{AK}	Anode-cathode off-state capacitance	f = 1 MHz, V_d = 1 V, I_G = 0, (see Note 5)	V_D = -3 V			110	pF
			V_D = -56 V			60	

NOTES: 3.PBA 3357/3 maximum negative voltage pulse rating is -120 V for 0.25 µs, -90 V for 1 µs, -70 V for 10 ms and -70 V for d.c. Compliance to these conditions is guaranteed by the maximum breakover voltage and the breakdown times of the R3612.
4.PBA 3357/3 maximum positive voltage pulse rating is 15 V for 0.25 µs, 10 V for 1 µs, 5 V for 10 ms and 1 V for d.c.. Compliance to these conditions is guaranteed by the peak forward recovery voltage and the forward recovery times of the R3612
5. These capacitance measurements employ a three terminal capacitance bridge incorporating a guard circuit. The unmeasured device terminals are a.c. connected to the guard terminal of the bridge.

thermal characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction to free air thermal resistance	P_{tot} = 0.8 W, T_A = 25°C, 5 cm^2, FR4 PCB			100	°C/W

PARAMETER MEASUREMENT INFORMATION

PBA 3357/3 DCLIC RING AND TIP VOLTAGE WITHSTAND
vs
TIME

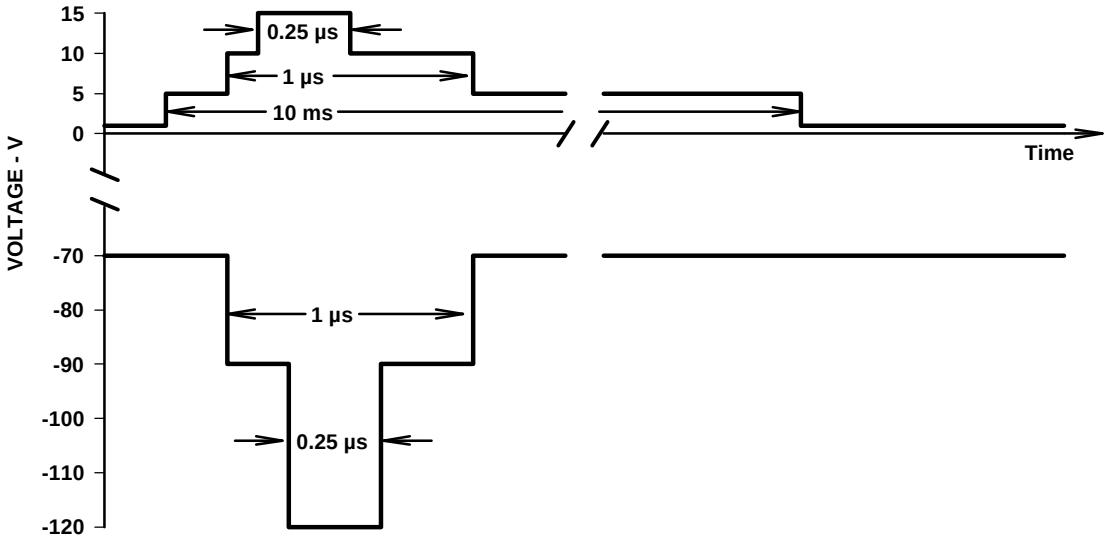


Figure 1. TRANSIENT LIMITS FOR R3612 LIMITING VOLTAGE

PARAMETER MEASUREMENT INFORMATION

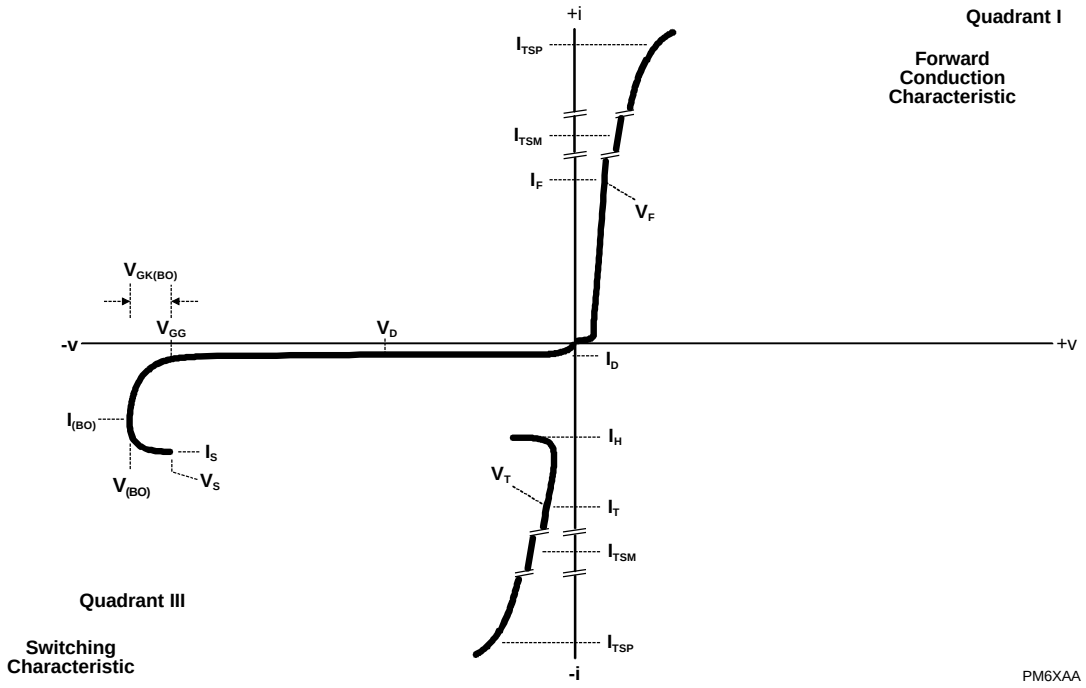


Figure 2. VOLTAGE-CURRENT CHARACTERISTIC

THERMAL INFORMATION

MAXIMUM NON-RECURRING 50 Hz CURRENT
vs
CURRENT DURATION

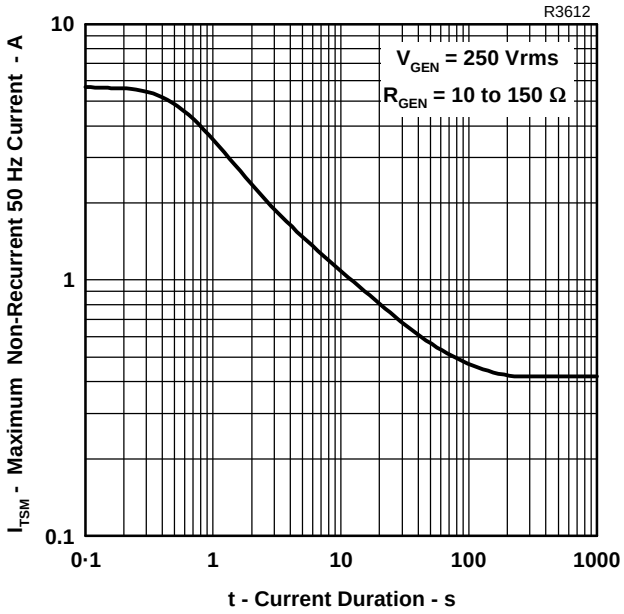


Figure 3.

DEVICE PARAMETERS

general

Thyristor based over voltage protectors, for telecommunications equipment, became popular in the late 1970s. These were fixed voltage breakover triggered devices, likened to solid state gas discharge tubes. As these were new forms of thyristor, the existing thyristor terminology did not cover their special characteristics. This resulted in the invention of new terms based on the application usage and device characteristic. Initially, there was a wide diversity of terms to describe the same thing, but today the number of terms have reduced and stabilised. Information on fixed voltage over voltage protector terms, symbols and their definitions is given in the publication SLPDE05, “Over-voltage Protection For Telecommunication Systems - Data Manual and Application Information”, pp 1-4 to 1-6, Texas Instruments Limited, Bedford, 1994.

Programmable, (gated), over voltage protectors are relatively new and require additional parameters to specify their operation. Similarly to the fixed voltage protectors, the introduction of these devices has resulted in a wide diversity of terms to describe the same thing. This section has a list of alternative terms and the parameter definitions used for this data sheet. In general, the Texas Instruments approach is to use terms related to the device internal structure, rather than its application usage as a single device may have many applications each using a different terminology for circuit connection.

terms, definitions and symbols

Thyristor over voltage protectors have substantially different characteristics and usage to the type of thyristor covered by IEC 747-6. These differences necessitate the modification of some characteristic descriptions and the introduction of new terms. Where possible terms are used from the following standards.

IEC 747-1:1983, *Semiconductor devices - Discrete devices and integrated circuits - Part 1: General*

IEC 747-2:1983, *Semiconductor devices - Discrete devices and integrated circuits - Part 2: Rectifier Diodes*

IEC 747-6:1983, *Semiconductor devices - Discrete devices and integrated circuits - Part 6: Thyristors*

main terminal ratings

Repetitive Peak Off-State Voltage, V_{DRM}
Rated maximum (peak) instantaneous voltage that may be applied in the off-state conditions including all d.c. and repetitive voltage components.

Repetitive Peak On-State Current, I_{TRM}
Rated maximum (peak) value of a.c. power frequency on-state current of specified waveshape and frequency which may be applied continuously.

Non-Repetitive Peak On-State Current, I_{TSM}
Rated maximum (peak) value of a.c. power frequency on-state surge current of specified waveshape and frequency which may be applied for a specified time or number of a.c. cycles.

Non-Repetitive Peak Pulse Current, I_{TSP}
Rated maximum value of peak impulse pulse current of specified amplitude and waveshape that may be applied.

Non-Repetitive Peak Forward Current, I_{FSM}
Rated maximum (peak) value of a.c. power frequency forward surge current of specified waveshape and frequency which may be applied for a specified time or number of a.c. cycles.

Repetitive Peak Forward Current, I_{FRM}
Rated maximum (peak) value of a.c. power frequency forward current of specified waveshape and frequency which may be applied continuously.

Critical rate of rise of on-state current, di/dt, $(di_T/dt)cr$
Rated value of the rate of rise of current which the device can withstand without damage.

main terminal characteristics

Off-State Voltage, V_D
The d.c. voltage when the device is in the off-state.

Off-State Current, I_D
The d.c. value of current that results from the application of the off-state voltage, V_D.

Repetitive Peak Off-State Current, I_{DRM}
The maximum (peak) value of off-state current that results from the application of the repetitive peak off-state voltage, V_{DRM}.

Breakover Voltage, $V_{(BO)}$
The maximum voltage across the device in or at the breakdown region measured under specified voltage rate of rise and current rate of rise.

NOTE - Where a breakdown characteristic has several $V_{(BO)}$ values that need to be referenced, a numeric suffix can be added and the relevant part of the breakdown current range specified (e.g. $V_{(BO)1}$, $0 < I_{(BR)} < 10$ mA).

Holding Current, I_H
The minimum current required to maintain the device in the on-state.

Off-State Capacitance, C_O, C_J
The capacitance in the off-state measured at specified frequency, f, amplitude, V_d, and d.c. bias, V_D.

Peak Forward Recovery Voltage, V_{FRM}
The maximum value of forward conduction voltage across the device upon the application of a specified voltage rate of rise and current rate of rise following a zero or specified reverse-voltage condition.

Critical rate of rise of off-state voltage, dv/dt, $(dv_D/dt)cr$
The maximum rate of rise of voltage (below V_{DRM}) that will not cause switching from the off-state to the on-state.

Breakover Current, $I_{(BO)}$
The instantaneous current flowing at the breakover voltage, $V_{(BO)}$.

Switching Voltage, V_S
The instantaneous voltage across the device at the final point in the breakdown region prior to switching into the on-state.

Switching Current, I_S
The instantaneous current flowing through the device at the switching voltage, V_S.

On-State Voltage, V_T
The voltage across the device in the on-state condition at a specified current I_T.

On-State Current, I_T
The current through the device in the on-state condition.

Forward Voltage, V_F
The voltage across the device in the forward conducting state at a specified current I_F.

Forward Current, I_F
The current through the device in the forward conducting state.

thermal characteristics

Temperature Derating
Derating with temperature above a specified base temperature, expressed as a percentage, such as may be applied to peak pulse current.

Thermal Resistance, $R_{\theta JL}$, $R_{\theta JC}$, $R_{\theta JA}$
The effective temperature rise per unit power dissipation of a designated junction, above the temperature of a stated external reference point (lead, case, or ambient) under conditions of thermal equilibrium.

Transient thermal impedance, $Z_{\theta JL(t)}$, $Z_{\theta JC(t)}$, $Z_{\theta JA(t)}$
The change in the difference between the virtual junction temperature and the temperature of a specified reference point or region (lead, case, or ambient) at the end of a time interval divided by the step function change in power dissipation at the beginning of the same time interval which causes the change of temperature-difference.

NOTE - It is the thermal impedance of the junction under conditions of change and is generally given in the form of a curve as a function of the duration of an applied pulse.

(Virtual-)Junction Temperature, T_J
A theoretical temperature representing the temperature of the junction(s) calculated on the basis of a simplified model of the thermal and electrical behaviour of the device.

Maximum Junction Temperature, T_{JM}
The maximum value of permissible junction temperature, due to self heating, which a TSS can withstand without degradation.

gate terminal parameters

Gate Trigger Current, I_{GT}
The lowest gate current required to switch a device from the off state to the on state.

Gate Trigger Voltage, V_{GT}
The gate voltage required to produce the gate trigger current, I_{GT}.

Gate-to-Adjacent Terminal Peak Off-State Voltage, V_{GDM}
The maximum gate to cathode voltage for a p-gate device or gate to anode voltage for an n-gate device that may be applied such that a specified off-state current, I_D, at a rated off-state voltage, V_D, is not exceeded.

Peak Off-State Gate Current, I_{GDM}
The maximum gate current that results from the application of the peak off-state gate voltage, V_{GDM}.

Gate Reverse Current, Adjacent Terminal Open, I_{GAO} , I_{GKO}
The current through the gate terminal when a specified gate bias voltage, V_G, is applied and the cathode terminal for a p-gate device or anode terminal for an n-gate device is open circuited.

Gate Reverse Current, Main Terminals Short Circuited, I_{GAS}, I_{GKS}
The current through the gate terminal when a specified gate bias voltage, V_G, is applied and the cathode terminal for a p-gate device or anode terminal for an n-gate device is short-circuited to the third terminal.

NOTE-This definition only applies to devices with integrated series gate blocking diodes.

Gate Reverse Current, On-State, I_{GAT}, I_{GKT}
The current through the gate terminal when a specified gate bias voltage, V_G, is applied and a specified on-state current, I_T, is flowing.

NOTE-This definition only applies to devices with integrated series gate blocking diodes.

Gate Reverse Current, Forward Conducting State, I_{GAF}, I_{GKF}
The current through the gate terminal when a specified gate bias voltage, V_G, is applied and a specified forward conduction current, I_F, is flowing.

NOTE-This definition only applies to devices with integrated series gate blocking diodes.

Gate Switching Charge, Q_{GS}
The charge through the gate terminal, under impulse conditions, during the transition from the off-state to the switching point, when a specified gate bias voltage, V_G, is applied.

Peak Gate Switching Current, I_{GSM}
The maximum value of current through the gate terminal during the transition from the off-state to the switching point, when a specified gate bias voltage, V_G, is applied.

Gate-to-Adjacent Terminal Breakover Voltage, $V_{GK(BO)}$, $V_{GA(BO)}$
The gate to cathode voltage for a p-type device or gate to anode voltage for an n-gate device at the breakover point. This is equivalent to the voltage difference between the breakover voltage, $V_{(BO)}$, and the specified gate voltage, V_G.

APPLICATIONS INFORMATION

electrical characteristics

The electrical characteristics of a thyristor over voltage protector are strongly dependent on junction temperature, T_J. Hence a characteristic value will depend on the junction temperature at the instant of measurement. The values given in this data sheet were measured on commercial testers, which generally minimise the temperature rise caused by testing.

gated protector evolution and characteristics

discrete gated protection

The first gated thyristor protection arrangement used discrete components, Figure 4. Positive line over voltages were clipped to ground by diodes D1 and D2. Negative line over voltages, via diodes D3 and D4, pulled the cathode of thyristor TH negative. Voltage limiting occurred when the negative over voltage caused the series gate diode, D5, and the thyristor gate-cathode to conduct. As the series gate diode was connected to the SLIC negative supply, the limiting voltage approximated to:

$$V_{FD3/4} + V_{GK} + V_{FD5} + V_{GG}$$

where

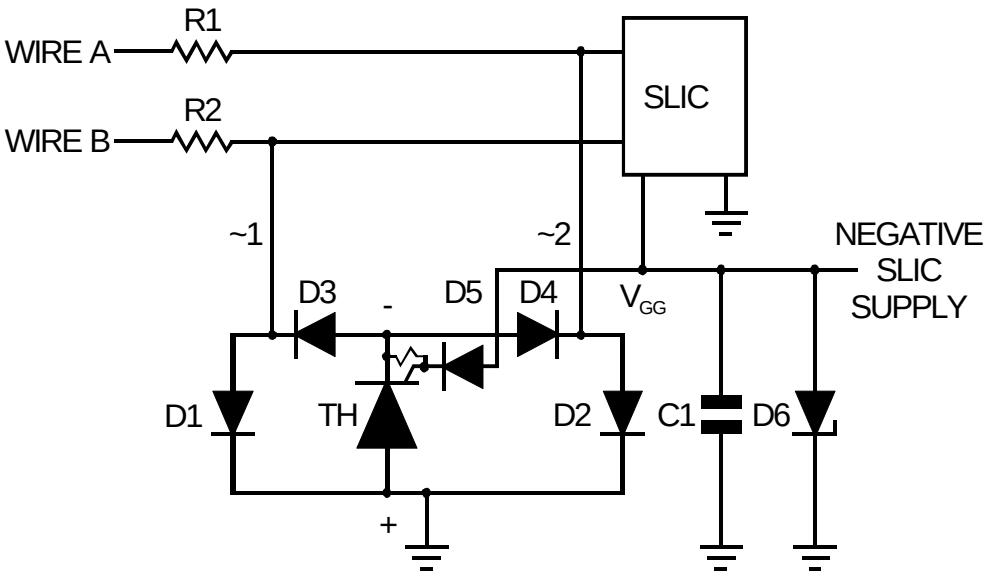


Figure 4. DISCRETE GATED THYRISTOR PROTECTION CIRCUIT

$V_{FD3/4}$ is the forward voltage of diode D3 or D4

V_{FD5} is the forward voltage of diode D5

V_{GG} is the gate reference voltage provided from the negative SLIC supply voltage V_{BAT}.

V_{GK} is the gate-cathode voltage of the thyristor.

The basic protection voltage is equal to the SLIC supply voltage plus a few volts. If the over voltage produced sufficient cathode current, the thyristor would regenerate and crowbar into a low voltage on-state condition. This action removes the voltage stress from the SLIC. The series gate diode, D5, is needed to prevent shorting the SLIC supply rail when the thyristor crowbars. When the thyristor comes to delatch it will be conducting the combined current of both SLIC outputs, via diodes D3 and D4, and so its holding current needs to be above this current level.

This protection arrangement minimises the voltage stress on the SLIC, no matter what value of supply voltage. In some SLIC designs, to minimise power consumption, the supply voltage is automatically adjusted to a value that is just sufficient to drive the required line current. For short lines the supply voltage would be low, but for long lines a higher supply voltage would be generated to drive sufficient line current. Thus a protection scheme which tracks the battery voltage is ideal for this type of application. The normal protection implementation used a small diode bridge (D1 to D4), an RCA SGT10S10 high holding current thyristor (TH) and a fast diode (D5).

One or possibly two extra components are needed to ensure the correct functioning of the protection. Figure 5 shows how the finite thyristor regeneration time allows a small fraction of the fast impulse (12 A/µs) to appear as gate current. The following negative gate current is the series gate diode recovery as the thyristor switches. A gate decoupling capacitor, C1, is needed to maintain a reasonably constant gate supply voltage during the clamping period.

In Figure 5, the positive gate charge (Q_{GS}) is about 0.1 µC which, with the 1 µF gate decoupling capacitor used, increased the gate supply by about 0.1 V (= Q_{GS}/C5). This change is not visible on the -72 V gate

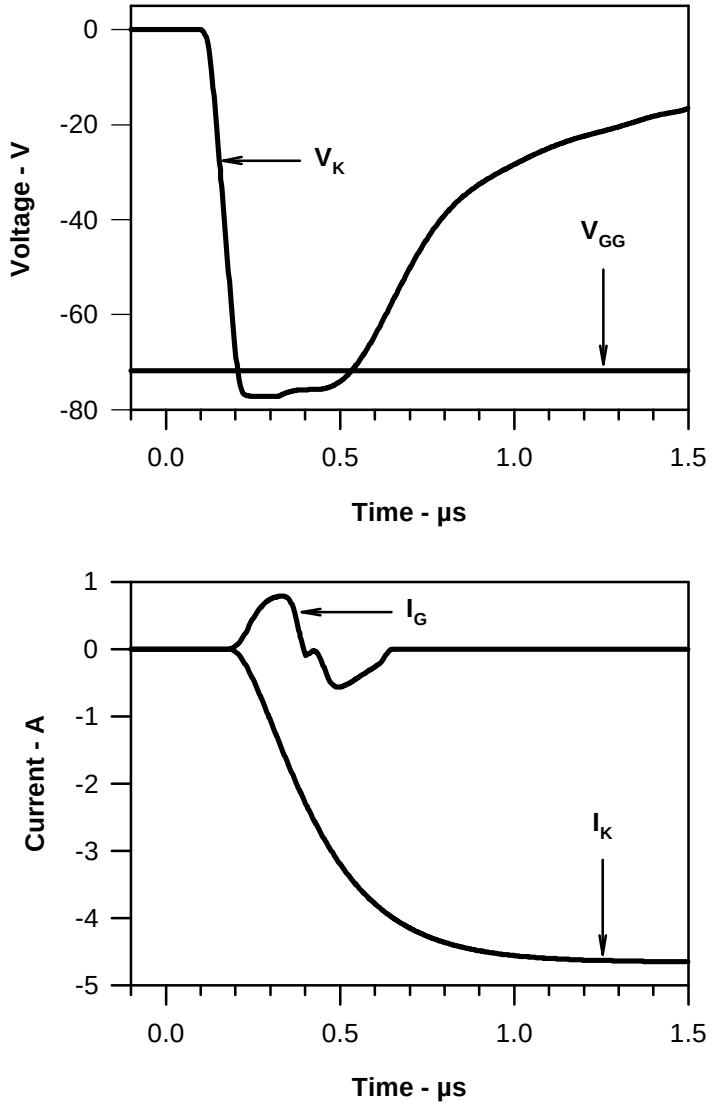


Figure 5. PROTECTOR FAST IMPULSE CLAMPING AND SWITCHING WAVEFORMS

voltage, V_{GG}. This increase does not directly add to the protection voltage as the supply voltage change reaches a maximum as the gate current reverses polarity; whereas the protection voltage peaks earlier than this. In Figure 5, the peak clamping voltage ($V_{(BO)}$) is -77.5 V, an increase of 5.5 V on the nominal gate supply voltage. This 5.5 V increase is the sum of the supply rail increase, (0.04 V), and the protection circuits cathode diode to supply rail breakover voltage (5.46 V). In practice, the gate decoupling capacitor would be about 80% smaller (e.g. 200 nF), giving a five times increase in supply voltage (5*0.04 = 0.2 V) and a $V_{(BO)}$ value of about -77.7 V.

Figure 5 shows the thyristor waveforms under a high impedance power cross condition. Positive half cycles are clamped to ground by the diodes D1 and D2, producing a peak current of 350 mA. Negative half cycles are clamped to the -70 V gate supply voltage. The peak cathode current of 120 mA is not enough to cause thyristor switching. As the thyristor first starts to conduct, the cathode and gate currents are the same. (I_K = I_G). At about 70 mA the thyristor starts to become active and anode current starts to flow. The increasing anode current progressively reduces the gate current, until the gate current is nearly zero at 15 ms. After that,

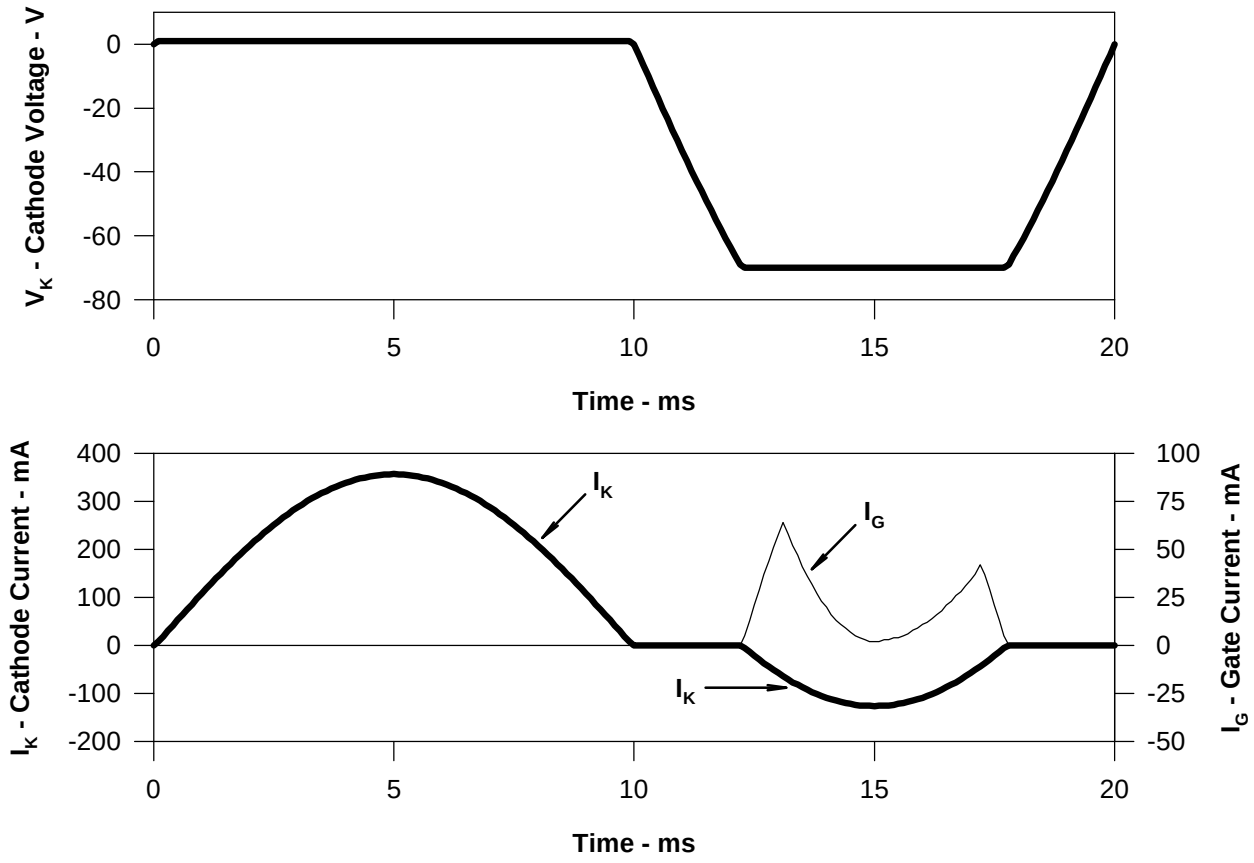


Figure 6. PROTECTOR HIGH IMPEDANCE POWER CROSS CLAMPING WAVEFORMS

the cathode and anode current decrease, increasing the gate current which peaks for a second time at about 40 mA. The second gate current peak is lower due to the heating caused by the clipping action.

The gate current behaviour is unusual. In the normal common cathode mode operation, once the gate current reaches its triggering value, I_{GT}, the thyristor switches on. In this case the thyristor is being operated in common gate mode which results in negative feedback. The negative feedback counteracts the thyristors internal positive feedback (regeneration) preventing switching until the thyristor does not need a gate current supplement from the gate supply voltage. In common gate mode, thyristor switches at zero gate current and the gate current peaks earlier as the thyristor starts to become active.

In Figure 5, although the full cycle average gate current is only 6 mA, peaks of 70 mA and 40 mA occur during the clamping period. This current is a charging current which tries to make the SLIC supply rail even more negative. If the current drawn by the SLIC is less than the gate current, the SLIC supply rail may increase to a point where the SLIC suffers an over voltage on its supply rail. In such cases the shunt avalanche diode, D6, provides the necessary protection by limiting the maximum supply voltage.

IC protectors

In 1986 an IC version was proposed (A 90 V Switching Regulator and Lightning Protection Chip Set, Robert K. Chen, Thomas H. Lerch, Johnathan S. Radovsky, D. Alan Spires, IEEE Solid-State Circuits Conference, February 20, 1986, pp 178/9 and pp 340/1). Commercially, this resulted in the AT&T Microelectronics LB1201AB device and the higher current Texas Instruments Inc. TCM1060 device, Figure 5.

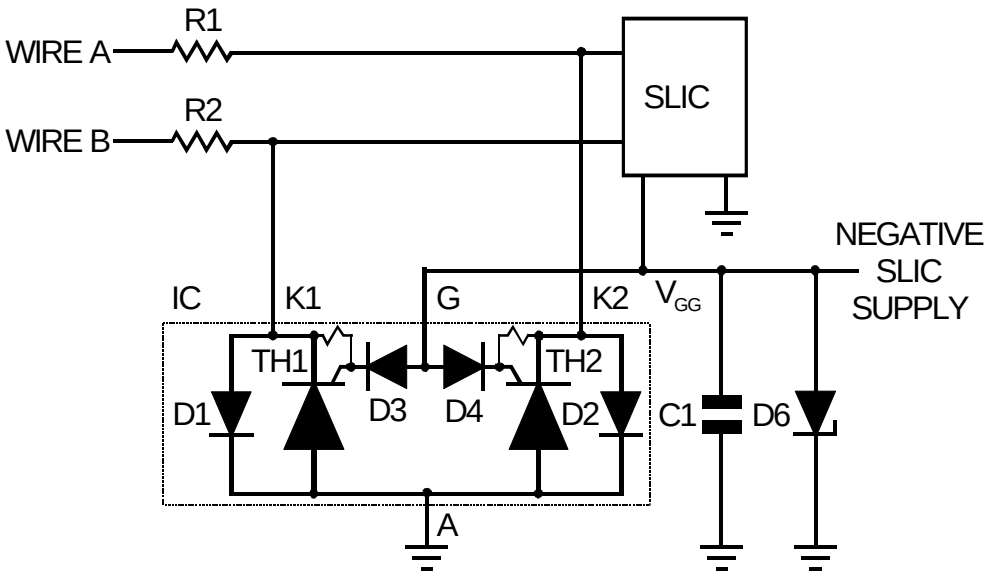


Figure 7. IC VERSION OF Figure 4

To avoid the problems of diode bridge implementation, the thyristor and series gate diode were duplicated which allowed the bridge series thyristor diodes to be removed. This had the benefit that the protection voltage was lowered by one diode forward voltage drop. The circuit performance of the IC was similar to the discrete solution. Due to the integration, when the thyristor was in the on-state or the shunt diode in conduction, about 10 mA of current was drawn from the gate supply, Figure 5. The direction of this current is the same as that drawn by the SLIC, so it represented a small additional load on the SLIC supply and resulted in some additional dissipation in the protector.

buffered gate protectors

The original IC design has been improved in two ways, Figure 5. Firstly, the lateral IC structure has been changed to a vertical power device structure for increased surge current capability. Second, the series gate diodes have been changed to transistors. The maximum current injected into the gate supply is then reduced by the transistors gain factor (H_{FE}). In most cases, just the lower peak gate current allows any previously used SLIC supply rail shunt protection diode to be removed. By designing the protector such that $I_{GT} < I_{GAF}$, the net gate current can be made to be a current drain, rather than a current injection, on the gate supply.

Fast rising surges will initially be clipped to the gate supply via the series combination of thyristor gate-cathode diode and the transistor base-emitter diode. The overall wave forms will be similar to Figure 5 and the supply decoupling capacitor, C1, should be dimensioned according to the text that accompanies Figure 5.

Although the SLIC supply is taken to a terminal that is internally connected to transistor bases, the terminal is designated as the gate terminal, G.

R3612 parameters

The PBA 3357/3 DCLIC is characterised over a 0°C to 70°C temperature range. To ensure correct operation, the R3612 protector is characterised on key paraters over the same temperature range. To ensure service restoration after an over voltage, the R3612 holding current is 105 mA minimum, which matches the 105 mA maximum line current of the PBA 3357/3. Typically the PBA3357/3 supply voltage will be -50 V ±6 V, but this could rise to a maximum rated value of -70 V. To cover these conditions the R3612 is rated at -100 V with electrical characteristics given at -48 V. The series overcurrent protector characteristic should be coordinated with the a.c. ratings of the R3612. Overshoot voltages are measured under 0.5/700 µs conditions. This

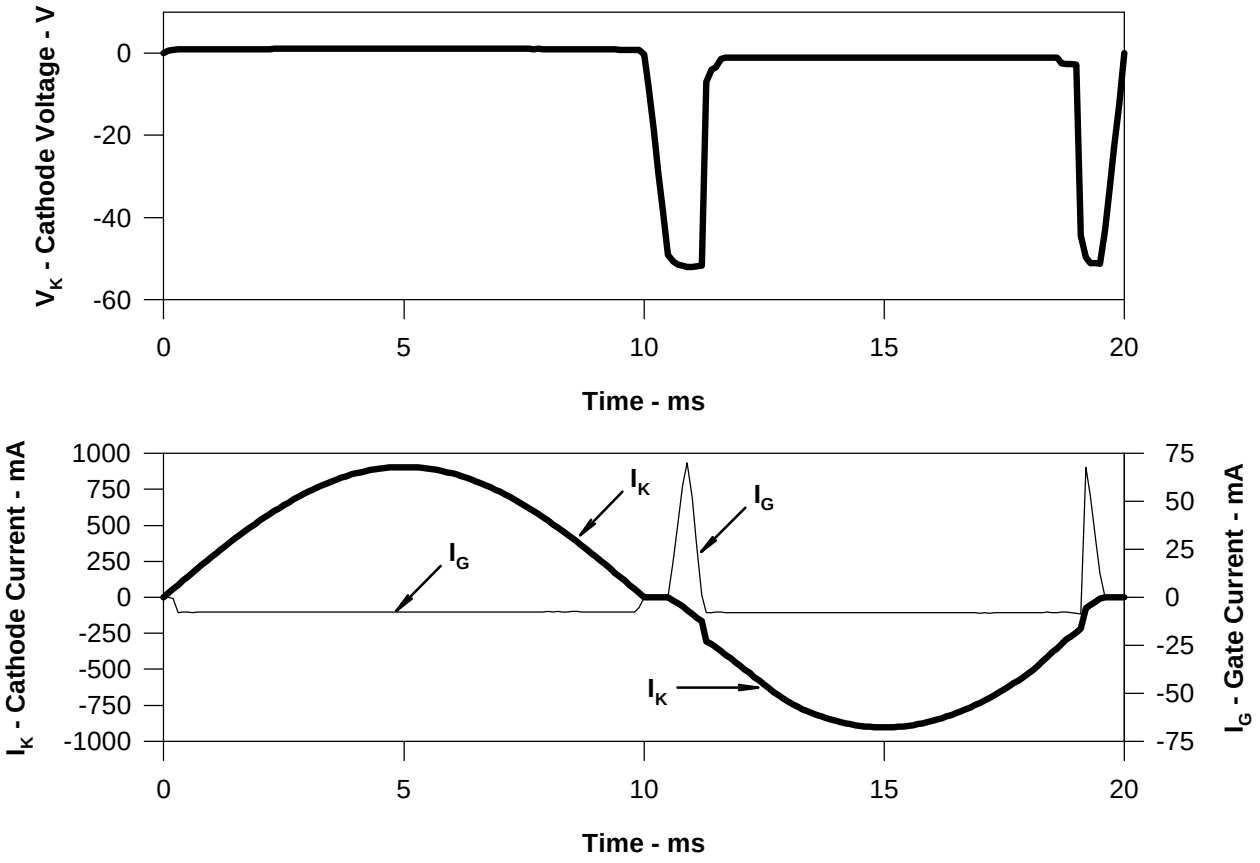


Figure 8. TCM1060 POWER CROSS WAVEFORMS

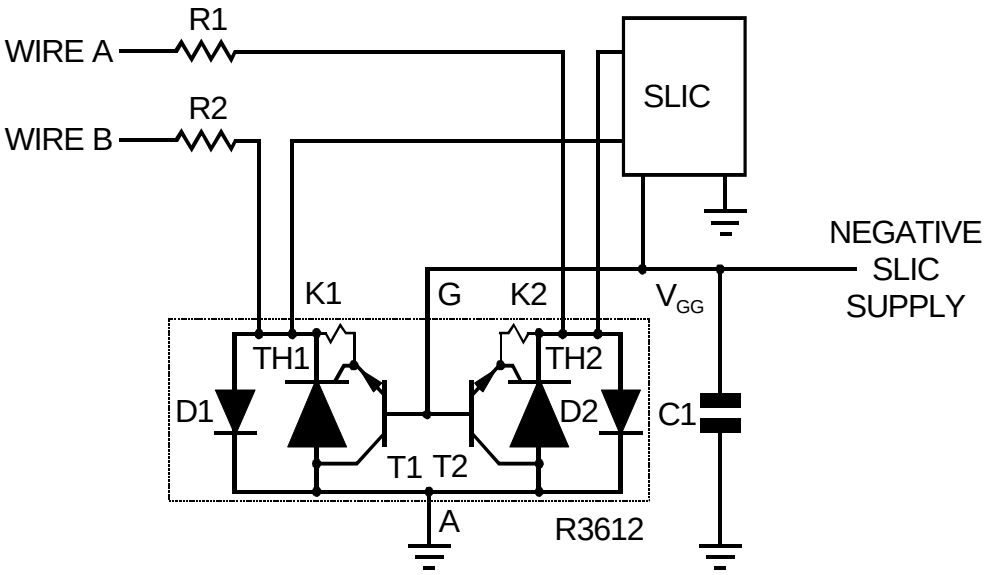


Figure 9. BUFFERED GATE PROTECTOR

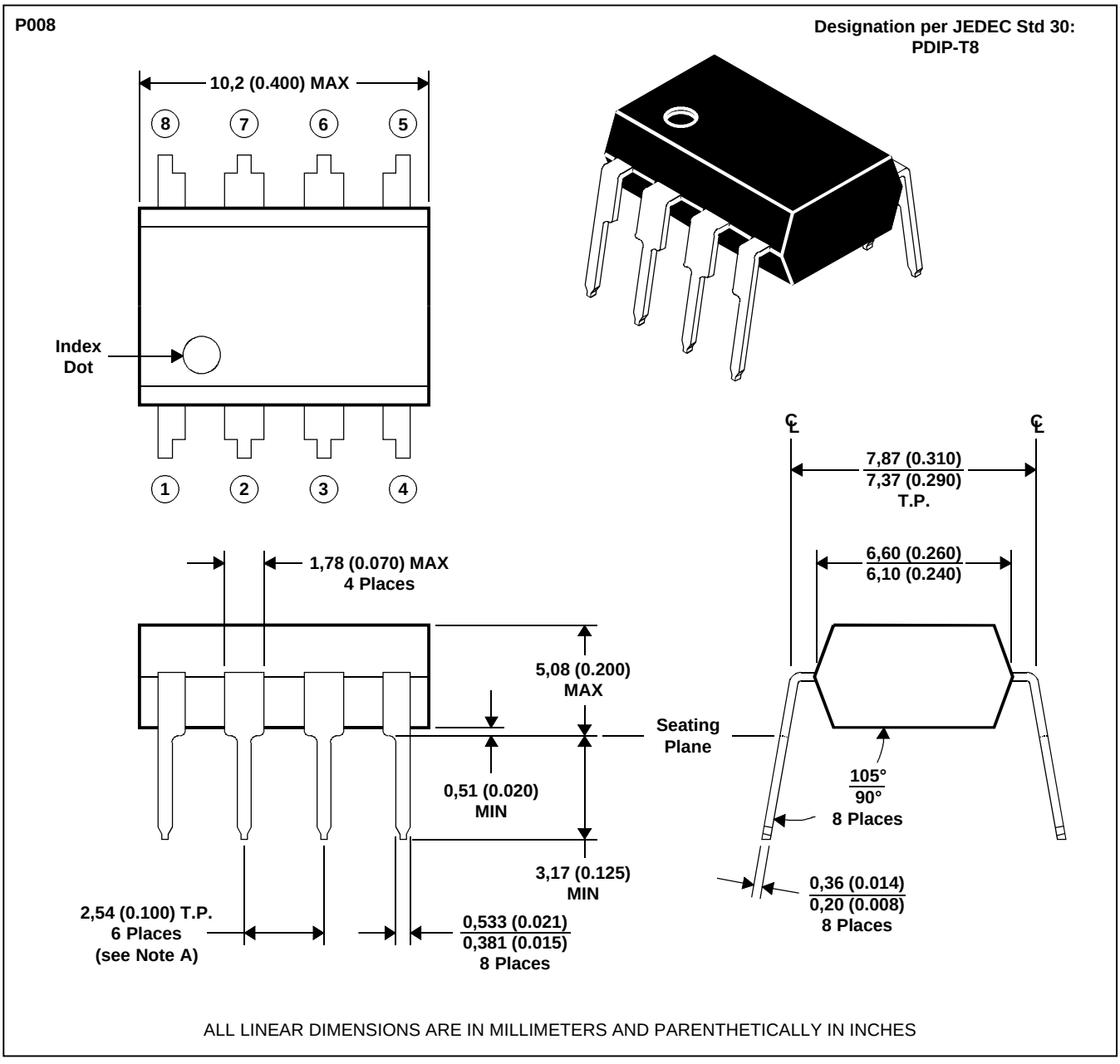
particular lightning surge wave shape has the fastest rise time and gives the largest voltage overshoot values. It is at least 20 times faster than the 10/1000 µs and 10/700 µs surges and so the 0.5/700 µs surge represents a worse case condition.

MECHANICAL DATA

P00

plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high humidity conditions The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position

MDXXABA

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