国芯科技
GUOXIN

Secret Distinction:

DVB-S Receiver IC

——— GX1101 family

Products Specification

HANGZHOU GUOXIN SCIENCE AND TECHNOLOGY CO.,LTD

2005.2 V1.6

CAUTION

This document is preliminary and is subject to change. Contact a **Guoxin Science**, representative to determine if this is the current information on this device.

The information contained in this document has been carefully checked and is believed to be reliable. However, **Guoxin Science** makes no guarantee or warranty concerning the accuracy of said information and shall not be responsible for any loss or damage of whatever nature resulting from the use of, or reliance upon, it **Guoxin Science** does not guarantee that the use of any information contained herein will not infringe upon the patent, trademark, copyright, mask work right or other rights of third parties, and no patent or other license is implied hereby.

This document does not in any way extend **Guoxin Science** warranty on any product beyond that set forth in its standard terms and conditions of sale. **Guoxin Science** reserves the right to make changes in the products or specifications, or both, presented in this publication at any time and without notice.

LIFE SUPPORT APPLICATIONS: **Guoxin Science** products are not intended for use ad critical components in life support appliances, devices, or systems in which the failure of a **Guoxin Science** product to perform could be expected to result in personal injury.

Guoxin Science reserves the right to do any kind of modifications in this datasheet regarding hardware or software implementations without notice.

Addr: 5F East Software Park Innovation Building, No.99 Huaxing Road, Hangzhou P.R.China, 310012
Tel: +86-571-88156088 Fax: +86-571-88156081 http://www.nationalchip.com

QPSK LINK IC WITH A/D CONVERTER GX1101P

Description

The GX1101P is a complete single-chip channel receiver for satellite television reception, which conforms to DVB-S standard (ETS 300 421). It consists of two A/D converters for I-input and Q-input, QPSK demodulator, and a forward error correction (FEC).

It supports high speed scanning mode for blind symbol rate and code rate acquisition, which allows all signals from a given satellite to be captured for channel frequency, symbol rate and code rate without any known information.

Minimal software is required to control the chip because of the built-in automatic search functions.

The carrier recovery loop and timing recovery loop are fully digital, which means that no external feedback loop is required. On-chip acquisition range is up to ±45MHz.

The FEC unit is compliant with the DVB-S specification. Processing is fully digital.

The high sampling rate (up to 90M) facilitates the implementation of low-cost, direct conversion tuners.

The GX1101P also provides outputs, such as noise-free serial bus dedicated to tuner control, which will ease the design of good quality application boards.

To sum up, the GX1101P is an excellent choice for satellite receivers, set-top boxes and satellite tuners.

Addr: 5F East Software Park Innovation Building, No.99 Huaxing Road, Hangzhou P.R.China, 310012
Tel: +86-571-88156088 Fax: +86-571-88156081 http://www.nationalchip.com

Key Features

- QPSK demodulator and FEC conform to EBU specification for DVB-S.
- High performance integrated 6-bit 90MHz dual-ADC.
- High speed scanning mode for blind symbol rate/code rate acquisition.
- Integrated PLL clock generation using external low cost passive crystal.
- AGC output with PDM mode.
- Digital Cancellation of A/D offset.
- Interpolating and anti-alias filters support 1 to 45Mbaud symbol rates.
- Full digital timing recovery loop with lock detector.
- Full digital carrier recovery loop with lock detector. Acquisition range up to ±45MHz.
- Digital Nyquist root filter with roll-off of 0.35.
- Viterbi soft decoder with constraint length K=7, rate=1/2.
  Automatic code rate search or programmable within 1/2, 2/3, 3/4, 5/6 and 7/8.
- Automatic spectrum inversion ambiguity resolution.
- Automatic frame synchronization.
- Convolutional deinterleaver, Reed Solomon decoder and de-scrambler according to DVB-S specifications.
- Channel quality estimation.
- Programmable parallel and serial output interface.
- DiSEqC™ v2.2 modulation output for full control of LNB and dish.
- Advanced software interface for convenient software control.
- Serial 2-wire bus interface and repeater.
- BIST.
- 64-pin LQFP package.
- Applications
  - Satellite digital television receivers and set-top boxes.
  - Satellite digital television tuner.

Addr: 5F East Software Park Innovation Building, No.99 Huaxing Road, Hangzhou P.R.China, 310012
Tel: +86-571-88156088 Fax: +86-571-88156081 http://www.nationalchip.com

CONTENTS

Addr: 5F East Software Park Innovation Building, No.99 Huaxing Road, Hangzhou P.R.China, 310012
Tel: +86-571-88156088 Fax: +86-571-88156081 http://www.nationalchip.com

Addr: 5F East Software Park Innovation Building, No.99 Huaxing Road, Hangzhou P.R.China, 310012
Tel: +86-571-88156088 Fax: +86-571-88156081 http://www.nationalchip.com

Addr: 5F East Software Park Innovation Building, No.99 Huaxing Road, Hangzhou P.R.China, 310012
Tel: +86-571-88156088 Fax: +86-571-88156081 http://www.nationalchip.com

1 Function Overview

1.1 ADC

The GX1101P contains dual 6-bit 100MHz A/D converters, which have optional single-ended/differential input and programmed full-scale input range of 0.25V, 0.5V and 0.75V. The fixed sampling clock 90MHz is provided on-chip using a programmable PLL needing only a low cost crystal.

1.2 QPSK Demodulator

The QPSK demodulator in the GX1101P consists of automatic gain control (AGC), carrier recovery, anti-alias filters, matched filter, timing recovery, etc.

1.2.1 Automatic Gain Control

The power of the input signal is compared to the programmable standard threshold, and the difference is integrated. The integrated difference is then converted into a modulation signal to drive the AGC output. It needs only a simple RC filter outside the chip. The dynamic characters and jitter performance of the AGC will be the best.

1.2.2 Carrier Recovery

The tracking range of the carrier recovery can exceed one time symbol rate, up to ±45MHz. Therefore the search of the initial channel frequency can go alone without reconfiguring the tuner even when there are relatively large carrier offsets introduced by the low noise block (LNB).

1.2.3 Anti-alias Filter and Matched Filter

Anti-alias filter is designed for all symbol rates from 1 to 45Mbaud. The GX1101P selects the most efficient anti-alias filters automatically according to the given symbol rate.

The matched filter is a root-raised-cosine filter with roll-off factor 0.35.

1.2.4 Timing Recovery

Addr: 5F East Software Park Innovation Building, No.99 Huaxing Road, Hangzhou P.R.China, 310012
Tel: +86-571-88156088 Fax: +86-571-88156081 http://www.nationalchip.com

In the normal mode, the only thing needs to do is to configure the symbol rate, and the on-chip advanced software interface (ADSI) will automatically change it to the data style used in timing recovery. Consequently, the recovery loop will work out quickly.

1.2.5 Signal Quality Indicator

The signal quality indicator shows the quality estimation of the signals into GX1101P. It can be used during the installation of the front-end, including the antenna, LNB, cable and tuner.

1.3 Forward Error Correction

1.3.1 Viterbi Decoder

The convolutional code is generated by the polynomial $G_x = 171, G_y = 133$, with rates 1/2, 2/3, 3/4, 5/6 and 7/8. The Viterbi decoder block can search the code rate automatically.

1.3.2 Synchronization

In DVB standard，204 bytes constitute a packet, and the first byte of each packet is a sync word (i.e. 0xB8 or 0x47). The sync word of 0xB8 occurs once every 8 packets, and the other 7 sync words are 0x47. The synchronizer can establish synchronization in a short time with an effective algorithm.

1.3.3 Convolutional deinterleaver

To mitigate any burst or impulse noise and increase the error correction ability of the Reed-Solomon FEC code, the bytes are interleaved after RS encoding at the transmitter, so it must be deinterleaved before RS decoding at the receiver. The convolutional deinterleaver is 17×12 (B=12,M=17), and there are 204 bytes in every packet.

1.3.4 Reed-Solomon Decoder

The input blocks are 204-byte long with 16 parity bytes in DVB, and up to 8 byte errors may be corrected. RS decoder also supplies statistic performance, e.g. bit error rate after viterbi decoder.

Addr: 5F East Software Park Innovation Building, No.99 Huaxing Road, Hangzhou P.R.China, 310012
Tel: +86-571-88156088 Fax: +86-571-88156081 http://www.nationalchip.com

1.3.5 Sync Byte Matching and Descrambling

In DVB, the frame header is synchronized at the start of every 8 packets before de-scrambling.

Before RS encoding in transmitter data will be scrambled, so it must be de-scrambled after RS decoding in receiver.

1.4 Blind Search Mode

The GX1101P can work in blind search mode when the channel frequency, symbol rate and code rate are unknown. For a given channel frequency range, the chip will search the signals quickly with the simple control of the software. The search time is less than five minutes.

1.5 Transport Stream Output Interface

The GX1101P offers several kinds of MPEG/TS output formats (DVB-specified 'Common Interface' format), and a specific parallel/serial format. There are D7, D6, D5, D4, D3, D2, D1, D0, DatVld, Error, Sync, BytClk output pins.

D7~D0: parallel data output, D7 in serial mode.

BytClk: Byte clock in parallel mode while bit clock in serial mode whose polarity can be configured.

DatVld: High if valid. Strobe signal that indicates whether the byte (bit in serial mode) supplied on D7~D0 (D7 in serial mode), to be clocked in by the active edge of BytClk, is one of the 188 valid bytes of the MPEG packet.

Error: High if valid. This signal goes high during transmission of an MPEG/TS packet if this packet contains errors that could not be corrected by RS decoder.

Sync: High if valid. This signal flags the first byte (bit in serial mode) of an MPEG/TS packet.

1.6 Control

1.6.1 Advanced Software Interface

Addr: 5F East Software Park Innovation Building, No.99 Huaxing Road, Hangzhou P.R.China, 310012
Tel: +86-571-88156088 Fax: +86-571-88156081 http://www.nationalchip.com

The GX1101P has an advanced software interface (ADSI) to simplify the software design. The ADSI maps high level inputs such as symbol rate in MBaud to low level on-chip register settings, and as well as maps low level register settings to high level symbol rate outputs for software.

1.6.2 Serial 2-Wire Control Bus

The GX1101P is controlled via a serial 2-wire bus and is a pure slave. Its 7-bit chip address is "110100A", where A is determined by applying VDD or VSS to the DevAddr pin. So its 8-bit write address is "110100A0" and its 8-bit read address is "110100A1".

The serial 2-wire bus supports the speed up to 400kHz. Write and read operations are described in Figure 1 and 2.

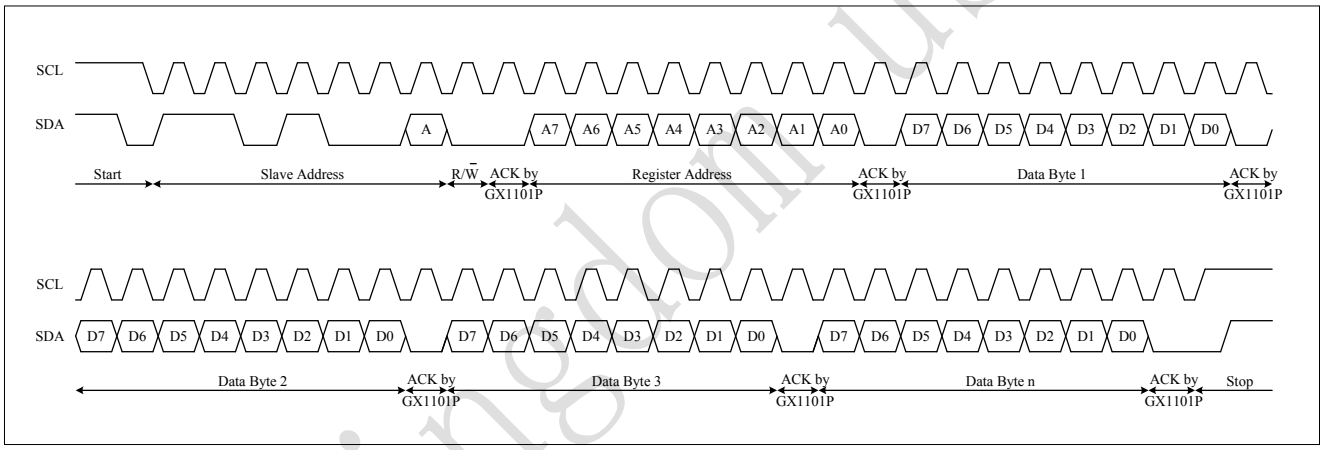


Figure 1 The 2-Wire Bus Write Operation

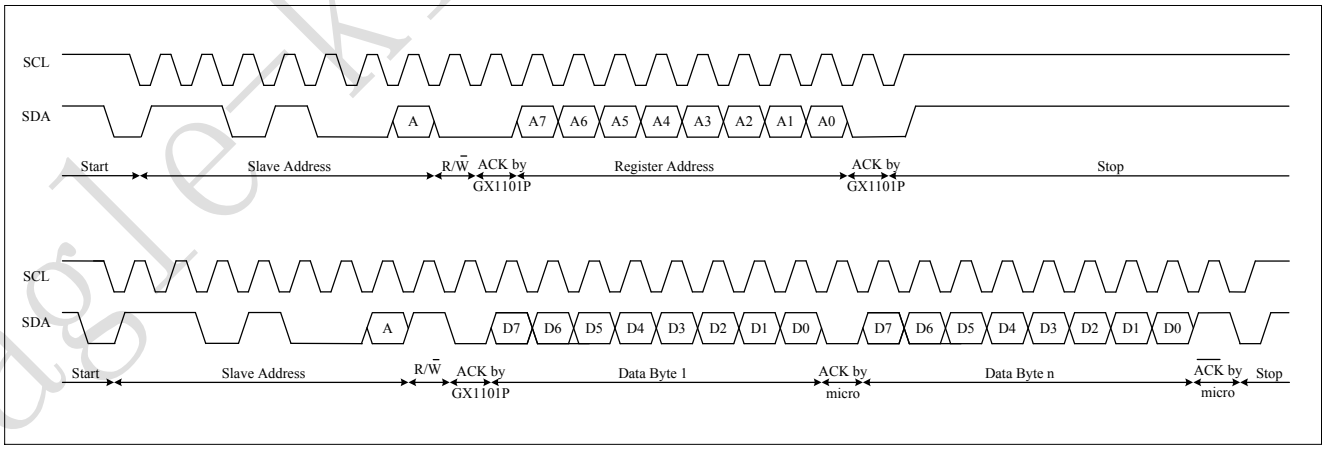


Figure 2 The 2-Wire Bus Read Operation

1.6.3 2-Wire Bus Repeater

Addr: 5F East Software Park Innovation Building, No.99 Huaxing Road, Hangzhou P.R.China, 310012
Tel: +86-571-88156088 Fax: +86-571-88156081 http://www.nationalchip.com

The goal of this block is to remove all disturbances to the tuner and thus improves tuner performance. The tuner can connect to pins SCLT and SDAT, as illustrated in Figure 3. When enabled, the repeater behaves as a fully bidirectional link between the main 2-wire bus (SCL, SDA) and the private bus (SCLT, SDAT). When disabled, pins SCLT and SDAT are completely isolated from the main 2-wire bus and are inactive (high level).

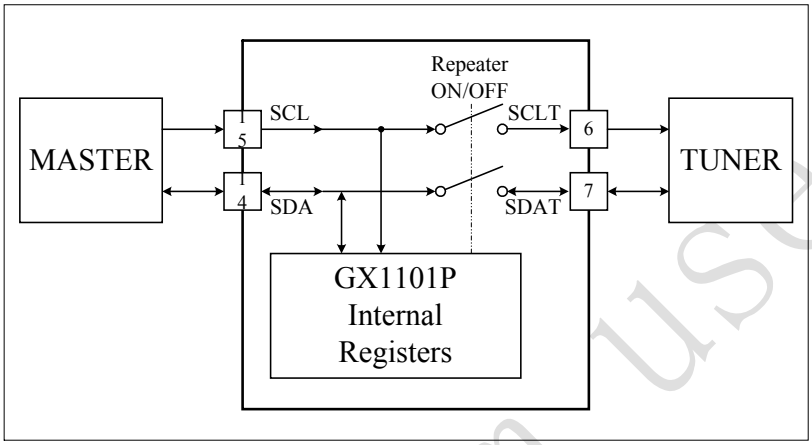


Figure 3 2-Wire Bus Repeater

1.6.4 DiSEqC™ Control

The GX1101P has the capability to send and receive DiSEqC™ messages, which can simplify the communication between microcontrollers and LNBs. Eight registers are provided to store a message for transmission and a further eight registers are provided to store a received message. And a programmable output pin HVselect can control the horizontal/vertical polarization.

The sequence of events to send and receive a message is as follows:

1. Load the required message bytes into the DISEQC_INS register.
2. Load the number of bytes in DiSEqC™ message minus 1 in the register DISEQC_MODE[5:3].
3. Set DISEQC_MODE[2:0] = 4 to command the GX1101P to encode the data and transmit the message.
4. If no reply required, an interrupt TX_INT is generated 16ms after the last message byte has been sent and DISEQC_MODE[2:0] reset to 0 automatically. If reply required, GX1101P will listen for DiSEqC™ message 5ms after a message has been transmit and TX_INT isn't

Addr: 5F East Software Park Innovation Building, No.99 Huaxing Road, Hangzhou P.R.China, 310012
Tel: +86-571-88156088 Fax: +86-571-88156081 http://www.nationalchip.com

generated. If SILENT_INT = 1 and END_MSG_INT = 0, there has been no message received. If a message has been received, END_MESSAGE_INT will be set and DISEQC_INT[7:4] indicate how many bytes have been received. The microcontroller can read the received message from DISEQC_RESP. Besides, ERR_INT indicates an error in the received message, while PAR_ERR_INT refers to a parity error.

The data loaded into DISEQC_INS register is retained, so that if the same message is to be repeated, the data loading stage 1 above can be omitted. But the received data in DISEQC_RESP will be cleared when transmitting another message.

Addr: 5F East Software Park Innovation Building, No.99 Huaxing Road, Hangzhou P.R.China, 310012
Tel: +86-571-88156088 Fax: +86-571-88156081 http://www.nationalchip.com

2 GX1101P Initialization

2.1 Clock Generation

An integrated PLL generates ADC sampling clock (90.0MHz) and chip internal system clock. PLL output frequency is calculated from the following equation:

$$clk = xin * \frac{PLL\_M + 2}{(PLL\_N + 2) * 2^{(PLL\_K[1]+PLL\_K[0])}}$$

Where xin is the PLL input crystal frequency, clk is ADC sampling clock and chip internal system clock 90MHz, other parameters are according to the following registers:

Name	Addr	B7	B6	B5	B4	B3	B2	B1	B0	Flag	Default
PLL KN	02H	PLL_K [1:0]		PLL_N [4:0]					PLL_M [8]	R/W	C0H
PLL M	03H	PLL_M [7:0]								R/W	B2H

Note: All registers and their default values are hexadecimal values. Read/write registers are flagged as R/W, while the read only registers are flagged as R.

In order to obtain good duty cycle, pll_k is suggested to be 2'b11, while $xin \in [2MHz, 50MHz]$, $pll\_n \in [0,31]$, $pll\_m \in [0,511]$. As an example, for a 4MHz crystal, the system clock frequency is 90MHz with pll_k=3 and (pll_m+2)/(pll_n+2)=90.

2.2 ADC Configuration

The full-scale input range of ADC can be programmed with the following register:

Name	Addr	B7	B6	B5	B4	B3	B2	B1	B0	Flag	Default
ADC GAIN	04H	6'b0						ADC_GAIN		R/W	01H

B1-0: ADC_GAIN Select the full scale input range of ADC

00: 0.25Vpp

01: 0.50Vpp

10: 0.75Vpp

Addr: 5F East Software Park Innovation Building, No.99 Huaxing Road, Hangzhou P.R.China, 310012
Tel: +86-571-88156088 Fax: +86-571-88156081 http://www.nationalchip.com

2.3 Standby Mode

A low power consumption mode (standby mode) can be controlled via the following register:

Name	Addr	B7	B6	B5	B4	B3	B2	B1	B0	Flag	Default
STBY	01H	STANDBY	TS_OEN	6'b0						R/W	00H

B7: STANDBY The chip is in normal or Standby mode

1: Standby mode

0: Normal mode

Chip internal blocks are shut down in standby mode, and they would resume quickly when standby mode is cancelled.

B6: TS_OEN TS output normal or tri-state

1: Tri-state

0: Normal

2.4 Chip ID

Name	Addr	B7	B6	B5	B4	B3	B2	B1	B0	Flag	Default
ID	00H	ID[7:0] Chip Identification								R	01H

This register provides an identification number related to the GX1101P version.

Addr: 5F East Software Park Innovation Building, No.99 Huaxing Road, Hangzhou P.R.China, 310012
Tel: +86-571-88156088 Fax: +86-571-88156081 http://www.nationalchip.com

3 Tuner Control

3.1 Simple Channel Change Sequence

If the GX1101P is running, to

i. change the channel frequency,

ii. keep the symbol rate,

iii. change the Viterbi code rate,

It is only necessary to change the tuner data and possibly the DiSEqC™ data. No other configurations including Viterbi code rate and reset are necessary.

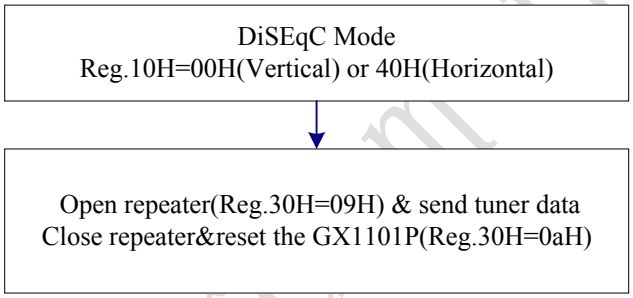


Figure 4 Simple Channel Change Sequence

3.2 Channel Change Sequence with a new Symbol Rate

If the GX1101P is running, to

i. change the channel frequency,

ii. change the symbol rate,

iii. change the Viterbi code rate,

It is only necessary to change the tuner data and possibly the DiSEqC™ data and symbol rate. No other configurations including Viterbi code rate and reset are necessary.

Addr: 5F East Software Park Innovation Building, No.99 Huaxing Road, Hangzhou P.R.China, 310012
Tel: +86-571-88156088 Fax: +86-571-88156081 http://www.nationalchip.com

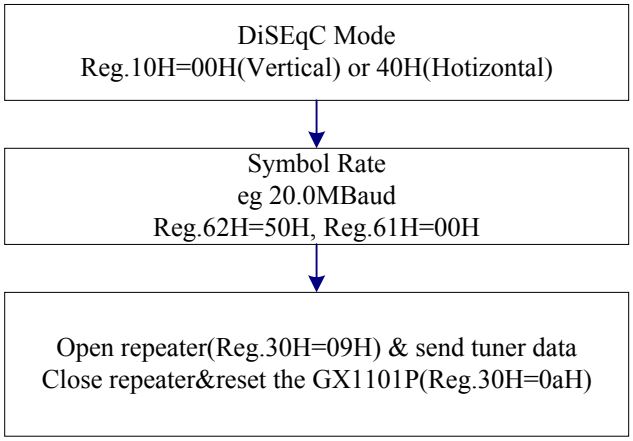


Figure 5 Channel Change Sequence with a new Symbol Rate

3.3 Blind Search Mode

If the signal parameters are unknown, it is easy to instruct the GX1101P to search for digital signals in the range required and report parameters, including channel and symbol rate and code rate, by software programs.

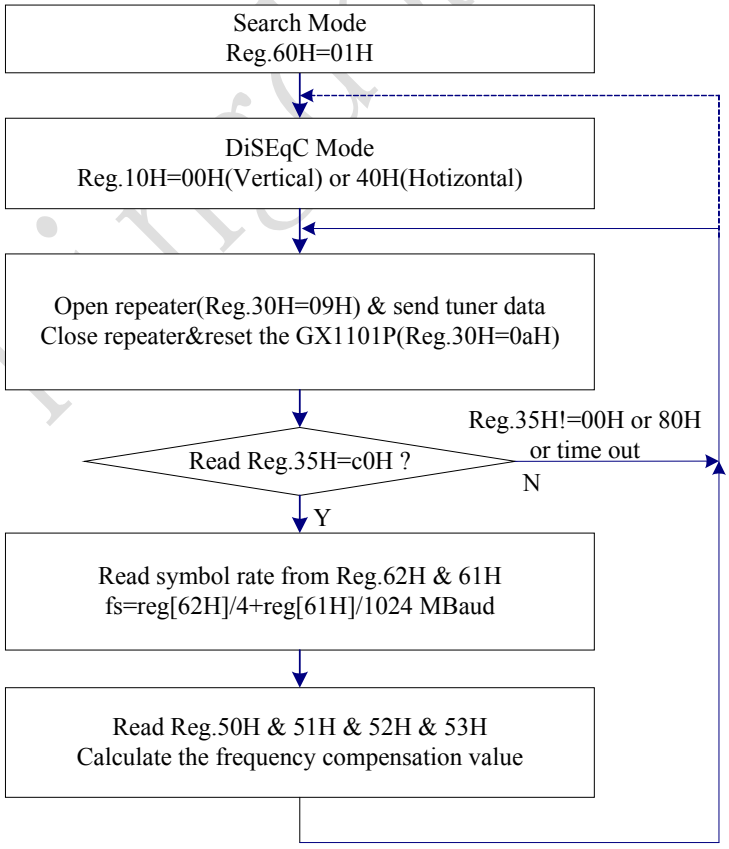


Figure 6 Blind Search Mode

Addr: 5F East Software Park Innovation Building, No.99 Huaxing Road, Hangzhou P.R.China, 310012
Tel: +86-571-88156088 Fax: +86-571-88156081 http://www.nationalchip.com

3.4 Tuner Control Registers

3.4.1 Repeater and Reset Control Register 30H

Name	Addr	B7	B6	B5	B4	B3	B2	B1	B0	Flag	Default
GLB CTRL	30H	RESERVED			RPT_TIME_SEL		COOL_RST	HOT_RST	RPTER_EN	R/W	08H

B4-3: RPT_ TIME_SEL — Select the Repeater's response time, i.e. the rise times on SDAT and SCLT.

00: 150ns

01: 250ns

10: 350ns

11: 450ns

B2: COOL_RST — Full reset of the chip

1: Reset all registers

0: Release the full reset

B1: HOT_RST — Partial reset of the chip, automatically set low again after use.

1: Reset all registers except configuration registers

0: Release the partial reset

B0: RPTER_EN — Switch of serial 2-wire control bus repeater for tuner

1: On

0: Off

3.4.2 GPOP0 Control Register 31H

Name	Addr	B7	B6	B5	B4	B3	B2	B1	B0	Flag	Default
GPOP0	31H	RESERVED			1'b1	PO0/AUD_OUT				R/W	16H

B3-0: PO0/AUD_OUT — Select GPOP0 outputs

0110: Audio output

Addr: 5F East Software Park Innovation Building, No.99 Huaxing Road, Hangzhou P.R.China, 310012
Tel: +86-571-88156088 Fax: +86-571-88156081 http://www.nationalchip.com

0111: High level

1000: Low level

The audio signal output on the GPOP0 pin indicates the signal quality during dish alignment, also see QPSK demodulator for detail.

3.4.3 GPOP1 Control Register 32H

Name	Addr	B7	B6	B5	B4	B3	B2	B1	B0	Flag	Default
GPOP1	32H	RESERVED			4'b1100				PO1	R/W	18H

B0: PO1 Select GPOP1 outputs

0: High level

1: Low level

3.4.4 State Indicator Register 34H

Name	Addr	B7	B6	B5	B4	B3	B2	B1	B0	Flag	Default
STATE	34H	STATE_INDICATOR								R	00H

B7: AGC_LOCK QPSK AGC LOCK indicator, active high

B6: CARRIER_LOCK QPSK carrier LOCK indicator, active high

B5: TIMING_LOCK QPSK timing LOCK indicator, active high

B4: VIT_LOCK Viterbi LOCK indicator, active high

B3: VIT_FAIL Viterbi FAIL indicator, active high

B2: DEI_LOCK Deinterleaver LOCK indicator, active high

B1: RS_FAIL RS decoder FAIL indicator, active high

B0: DSC_LOCK De-scrambler LOCK indicator, active high

3.4.5 State Indicator with Search Mode Register 35H

Name	Addr	B7	B6	B5	B4	B3	B2	B1	B0	Flag	Default
BLIND STATE	35H	BLIND_STATE_INDICATOR								R	00H

B7: QPSK_FIND QPSK search signal successes, active high

Addr: 5F East Software Park Innovation Building, No.99 Huaxing Road, Hangzhou P.R.China, 310012
Tel: +86-571-88156088 Fax: +86-571-88156081 http://www.nationalchip.com

B6:	FEC_FIND	FEC search signal successes, active high
B5:	FEC_FAIL	FEC search signal fails, active high
B4:	CARRIER_FAIL	Carrier recovery search signal fails, active high
B3:	TIMING_FAIL1	Timing recovery search signal fails1, active high
B2:	TIMING_FAIL2	Timing search signal fails2, active high
B1:	QPSK_FAIL	QPSK search signal fails, active high
B0:	AGC_FAIL	AGC search signal fails, active high

In the blind search mode, a signal is found only if the value 8'b11000000 is read from this register. That any bit among B5-B0 is high means no signal is found, and it is time to change the tuner data.

Addr: 5F East Software Park Innovation Building, No.99 Huaxing Road, Hangzhou P.R.China, 310012
Tel: +86-571-88156088 Fax: +86-571-88156081 http://www.nationalchip.com

4 DiSEqC™ Control

4.1 DiSEqC™ Control Read/Write Registers

4.1.1 DiSEqC™ Mode Control Register10H

Name	Addr	B7	B6	B5	B4	B3	B2	B1	B0	Flag	Default
DISEQC MODE	10H	RESERVED	HVSELECT	TX_BYTES			DISEQC_MODE			R/W	00H

B6: HVSELECT H/V polarization control, to output on HVSelect pin

1: Horizontal

0: Vertical

B5-3: TX_BYTES Number of bytes in DiSEqC™ instruction minus 1

B2-0: DISEQC_MODE DiSEqC™ mode

000: 22kHz off

001: 22kHz on continuous

010: Burst mode – on for 12.5ms = '0'

011: Burst mode – modulated 1:2 for 12.5ms = '1'

100: Modulated with bytes from DISEQC INS

101-111: Reserved

For mode 2 and 3, an interrupt is generated 16ms after the '0' or '1' burst. For mode 4, there is a 16ms delay before the message bytes, and an interrupt is generated 16ms after the last message byte has been sent. The requisite number of bytes must be pre-loaded into DISEQC INS (register 12H) before this bit is set.

4.1.2 DiSEqC™ Ratio Register 11H

Name	Addr	B7	B6	B5	B4	B3	B2	B1	B0	Flag	Default
DISEQC RATIO	11H	DISEQC_RATIO								R/W	2DH

Addr: 5F East Software Park Innovation Building, No.99 Huaxing Road, Hangzhou P.R.China, 310012
Tel: +86-571-88156088 Fax: +86-571-88156081 http://www.nationalchip.com

B7-0: DISEQC_RATIO It must be programmed to set the DiSEqC™ output tone frequency.

$F_{out}=F_{xtal}$ / (4*DISEQC_RATIO[7:0])

4.1.3 DiSEqC™ Instruction Register 12H

Name	Addr	B7	B6	B5	B4	B3	B2	B1	B0	Flag	Default
DISEQC INS	12H	DISEQC_INS								R/W	00H

B7-0: DISEQC_INS Instruction data

Up to eight instruction data bytes can be loaded into registers 12H~19H through this register, because the 2-wire bus register address would increase automatically.

4.1.4 DiSEqC™ Control Register 1BH

Name	Addr	B7	B6	B5	B4	B3	B2	B1	B0	Flag	Default
DISEQC CTRL	1BH	RESERVED				MIN_PULSE		MAX_TONE	MIN_TONE	R/W	0CH

B3-2: MIN_PULSE Minimum pulse period

00: 24*diseqc_ratio

01: 26*diseqc_ratio

10: 28*diseqc_ratio

11: 30*diseqc_ratio

B1: MAX_TONE Maximum tone period

0: 5.5*diseqc_ratio (16kHz)

1: 6.0*diseqc_ratio (14.67kHz)

B0: MIN_TONE Minimum tone period

0: 3.0*diseqc_ratio (29.3kHz)

1: 2.75*diseqc_ratio (32kHz)

Addr: 5F East Software Park Innovation Building, No.99 Huaxing Road, Hangzhou P.R.China, 310012
Tel: +86-571-88156088 Fax: +86-571-88156081 http://www.nationalchip.com

4.2 DiSEqC™ Control Read Registers

4.2.1 DiSEqC™ Interrupt Indicators Register 1CH

Name	Addr	B7	B6	B5	B4	B3	B2	B1	B0	Flag	Default
DISEQC INT	1CH	RX_BYTES			TX_INT	SILENT_INT	END_MSG_INT	ERR_INT	PAR_ERR_INT	R	00H

B7-5: RX_BYTES Number of bytes received minus 1

B4: TX_INT End of sending message interrupt

B3: SILENT_INT Silent period exceeds 176ms interrupt

B2: END_MSG_INT End of receiving message interrupt. The end of a message is identified by a silent period of about 6ms following a byte.

B1: ERR_INT Receive error interrupt.

B0: PAR_ERR_INT Parity error interrupt.

4.2.2 DiSEqC™ Response Register 1EH

Name	Addr	B7	B6	B5	B4	B3	B2	B1	B0	Flag	Default
DISEQC RESP	1EH	DISEQC_RESP								R	00H

B7-0: DISEQC_RESP Received data

Up to eight received data bytes can be read from registers 1EH~25H through this register, because the 2-wire bus register address would increase automatically.

Addr: 5F East Software Park Innovation Building, No.99 Huaxing Road, Hangzhou P.R.China, 310012
Tel: +86-571-88156088 Fax: +86-571-88156081 http://www.nationalchip.com

5 QPSK Demodulator

5.1 AGC Registers

5.1.1 AGC Control Register 40H

Name	Addr	B7	B6	B5	B4	B3	B2	B1	B0	Flag	Default
AGC CTRL	40H	FREEZE	CLK		SPEED			PLR	1'b0	R/W	52H

B7: FREEZE AGC is freezed or normal

1: Freezed

0: Normal

B6-5: CLK Select AGC working frequency, default is 2

00: System clock

01: System clock divided by 2

10: System clock divided by 4

11: System clock divided by 8

The smaller RC can be selected by increasing the working frequency of AGC, however the disturbances will increase at the same time.

B4-2: SPEED Speed control of the AGC loop, default is 4

AGC loop gain = K*2^SPEED, K is a constant. The AGC loop's convergence rate will increase in exponential rate as the SPEED comes from 0 to 7. At the same time, it will introduce severe jitter after the loop is locked, which maybe results in larger BER. So, in application, we'd better make a balance between the loop's converge speed and bit error rate.

B1: PLR Select the polarity, default is 1

0: Positive slope i.e. RF gain proportional to AGC voltage.

1: Negative slope i.e. RF gain inversely proportional to AGC voltage.

Addr: 5F East Software Park Innovation Building, No.99 Huaxing Road, Hangzhou P.R.China, 310012
Tel: +86-571-88156088 Fax: +86-571-88156081 http://www.nationalchip.com

5.1.2 AGC Standard Power Register 41H

Name	Addr	B7	B6	B5	B4	B3	B2	B1	B0	Flag	Default
AGC STD	41H	AGC_STD								R/W	1C H

B7-0: AGC_STD AGC power reference value, unsigned

After the AGC loop locked, Intermediate-Frequency signals can be enlarged by configure the AGC_STD a larger value, and more sufficient use of the ADC's sample precision can be made. But the signal level can't exceed the ADC's Full-Scale, otherwise, it will deteriorate the system performance. Default value is suggested.

5.1.3 Signal Intensity Indicator Register 42H

Name	Addr	B7	B6	B5	B4	B3	B2	B1	B0	Flag	Default
INTENSITY	42H	SIGNAL_INTENSITY								R	00H

B7-0: SIGNAL_INTENSITY Signal intensity indicator, unsigned

The signal intensity indicator has a value between 0 and 255 after the AGC loop locked, which is almost inversely proportional to the real RF signal level. Read the register to get the RF signal level (signal intensity).

5.2 Carrier Recovery Registers

5.2.1 Carrier Frequency Error1 Register 50H & 51 H

Name	Addr	B7	B6	B5	B4	B3	B2	B1	B0	Flag	Default
FREQ ERR1 L	50H	FREQ_ERR1[7:0]								R/W	00H

B7-0: FREQ ERR1[7:0] Low byte of the carrier frequency coarse adjustment error

Name	Addr	B7	B6	B5	B4	B3	B2	B1	B0	Flag	Default
FREQ ERR1 H	51H	FREQ_ERR1[15:8]								R/W	00H

B7-0: FREQ_ERR1[15:8] High byte of the carrier frequency coarse adjustment error

It's a signed value. By configuring the registers above without the tuner operation, we can

Addr: 5F East Software Park Innovation Building, No.99 Huaxing Road, Hangzhou P.R.China, 310012
Tel: +86-571-88156088 Fax: +86-571-88156081 http://www.nationalchip.com

compensate the carrier frequency error; by reading the registers, the values show a coarse estimation of the carrier frequency error. The relation between the registers and the frequency error is:

$$Ferr1 = \frac{FREQ\_ERR1 \times SYS\_CLK}{65536}$$

The $Ferr1$ is the coarse estimation of the carrier frequency error, SYS_CLK is the system clock (90MHz).

5.2.2 Carrier Frequency Error2 Register 52H & 53H

Name	Addr	B7	B6	B5	B4	B3	B2	B1	B0	Flag	Default
FREQ ERR2 L	52H	FREQ_ERR2[7:0]								R	00H

B7-0: FREQ ERR2[7:0] Low byte of the carrier frequency fine adjustment error

Name	Addr	B7	B6	B5	B4	B3	B2	B1	B0	Flag	Default
FREQ ERR2 H	53H	FREQ_ERR2[15:8]								R	00H

B7-0: FREQ_ERR2[15:8] High byte of the carrier frequency fine adjustment error

FREQ ERR2 expresses the fine estimation of the residual carrier frequency error. The relation between the registers and the frequency error $Ferr2$ is:

$Ferr2 = \frac{FREQ\_ERR2 \times SYM\_RATE}{65536}$, SYM_RATE is the symbol rate.

The four registers 50H~53H can be read continuously, and all carrier frequency errors can be rectified by combine the two parts.

$Ferr = Ferr1 + Ferr2$.

5.2.3 Signal Quality Indicator Register 54H

Name	Addr	B7	B6	B5	B4	B3	B2	B1	B0	Flag	Default
SNR	54H	SNR[7:0]								R	00H

B7-0: SNR[7:0] SNR indicator, unsigned

This register indicates the received signal quality, which can be used to facilitate the antenna setup.

Addr: 5F East Software Park Innovation Building, No.99 Huaxing Road, Hangzhou P.R.China, 310012
Tel: +86-571-88156088 Fax: +86-571-88156081 http://www.nationalchip.com

5.2.4 QPSK Function Switch Register 55H

Name	Addr	B7	B6	B5	B4	B3	B2	B1	B0	Flag	Default
AUDIO DEROT	55H	AUDIO_ON	DRT_ON	6'b101110						R/W	6EH

B7: AUDIO_ON Switch of the AUDIO function, default is 0

1: Open the AUDIO function, signal is outputted from the pin GPOP0

0: Close the AUDIO function, the pin GPOP0 putouts low.

AUDIO signal frequency is proportional to the signal quality $SNR_{dB,}$ which can help to adjust the antenna with a beeper outside.

B6: DRT_ON Switch of the carrier frequency coarse adjustment function, default is 1.

1: On

0: Off

5.2.5 QPSK Spectral Inversion Register 58H

Name	Addr	B7	B6	B5	B4	B3	B2	B1	B0	Flag	Default
IQ SWAP	58H	IQ_SP	7'b0110100							R/W	34H

B7： IQ_SP Swap I and Q inputs before QPSK demodulation, default is 0.

1： Swap

0： No swap

Swap I and Q inputs before QPSK demodulation to overcome spectral inversion caused by the receiver front-end, for example through the swapping I and Q wires on the board.

5.2.6 Carrier Recovery Loop Parameter Register 59H

Name	Addr	B7	B6	B5	B4	B3	B2	B1	B0	Flag	Default
CRL PARA	59H	CRL_PARA								R/W	58H

Addr: 5F East Software Park Innovation Building, No.99 Huaxing Road, Hangzhou P.R.China, 310012
Tel: +86-571-88156088 Fax: +86-571-88156081 http://www.nationalchip.com

B7-0: CRL_PARA [7:0] Carrier Recovery Loop Parameter, default is 58H. The recommended value is:

58H： When Viterbi Code Rate is 1/2

3CH： When Viterbi Code Rate is 2/3, 3/4,5/6 or 7/8

5.3 Timing Recovery Registers

5.3.1 Blind Search Mode Control Register 60H

Name	Addr	B7	B6	B5	B4	B3	B2	B1	B0	Flag	Default
BLIND SEL	60H	7'b0000000							BLD_MOD	R/W	00H

B0: BLD_MOD Select the blind search mode

1: Blind search mode.

0: Normal mode.

5.3.2 Symbol Rate Register 61H 62H

Name	Addr	B7	B6	B5	B4	B3	B2	B1	B0	Flag	Default
SYM RATE L	61H	SYM_RATE [7:0]								R/W	AEH

B7-0: SYM_RATE [7:0] Low byte of the symbol rate

Name	Addr	B7	B6	B5	B4	B3	B2	B1	B0	Flag	Default
SYM RATE H	62H	SYM_RATE [15:8]								R/W	11H

B7-0: SYM_RATE [15:8] High byte of the symbol rate

Suppose that SR is symbol rate in MBaud, these two registers should be configured as follows: $SYM\_RATE[15:0] = SR \times 1024$, e.g. using the default value, SR = 4.42MBaud, then SYM_RATE[15:0]=4.42*1024=4526=11ae(hex)；So write AEH to register SYM RATE L and 11H to register SYM RATE H.

Reading these two registers, then calculating by the formula above, we can get the accurate symbol rate.

5.3.3 Timing Recovery Loop Parameter Register 69H

Addr: 5F East Software Park Innovation Building, No.99 Huaxing Road, Hangzhou P.R.China, 310012
Tel: +86-571-88156088 Fax: +86-571-88156081 http://www.nationalchip.com

Name	Addr	B7	B6	B5	B4	B3	B2	B1	B0	Flag	Default
TRL PARA	69H	TRL_PARA								R/W	24H

B7-0: TRL_PARA [7:0] Timing Recovery Loop Parameter, default is 24H. The recommended value is 1EH.

5.3.4 Blind Search Step Size Register 6BH

Name	Addr	B7	B6	B5	B4	B3	B2	B1	B0	Flag	Default
SCAN LEN	6BH	4'b0110				SCAN_LEN				R/W	67H

B3-0： SCAN_LEN The limit of blind search step size, default is 7.

In the blind search mode, the blind search step size in software can't be larger than three times of SCAN_LEN generally. The recommended value is 2.

Addr: 5F East Software Park Innovation Building, No.99 Huaxing Road, Hangzhou P.R.China, 310012
Tel: +86-571-88156088 Fax: +86-571-88156081 http://www.nationalchip.com

6 FEC

6.1 Viterbi Decoder Registers

6.1.1 Viterbi Code Rate Register 84H

Name	Addr	B7	B6	B5	B4	B3	B2	B1	B0	Flag	Default
VIT RAT CUR	84H	VIT_RAT_CUR			RESERVED					R	00H

B7-5： VIT_RAT_CUR The code rate found by Viterbi Decoder

0： 1/2

1： 2/3

2： 3/4

3： 5/6

4： 7/8

6.1.2 Viterbi Mode Register 85H

Name	Addr	B7	B6	B5	B4	B3	B2	B1	B0	Flag	Default
VIT MODE	85H	3'b0			AUT_IQ	VIT_RAT			AUT_RAT	R/W	10H

B4： AUT_IQ Automatic spectrum inversion ambiguity resolution

0： Disable Automatic spectrum inversion ambiguity resolution

1： Enable Automatic spectrum inversion ambiguity resolution

B3-1： VIT_RAT Specify code rate when manual set

0： 1/2

1： 2/3

2： 3/4

3： 5/6

4： 7/8

B0： AUT_RAT Automatic code rate search

0： Enable automatic code rate search

Addr: 5F East Software Park Innovation Building, No.99 Huaxing Road, Hangzhou P.R.China, 310012
Tel: +86-571-88156088 Fax: +86-571-88156081 http://www.nationalchip.com

1： Use the code rate specified in VIT RAT.

User can either use automatic code rate search (AUT RAT = 0) or specify a code rate (AUT RAT = 1) in VIT RAT. Automatic code rate search (AUT RAT = 0) is recommended

It is recommended to enable automatic spectrum inversion ambiguity resolution (AUT IQ = 1).

6.1.3 Viterbi Error Mode Register 80H

Name	Addr	B7	B6	B5	B4	B3	B2	B1	B0	Flag	Default
VIT ERR MODE	80H	RESERVED			VIT_ERR_CNT_MOD					R/W	11H

B4-0： VIT_ERR_CNT_MOD Mode of error rate counter for data at the input of Viterbi Decoder

0xxxx： Disable the counter

100xx： Count for bit error rate

101xx： Count for symbol error rate

1xx00： Count for 2^12 bytes

1xx01： Count for 2^14 bytes

1xx10： Count for 2^16 bytes

1xx11： Count for 2^18 bytes

6.1.4 Viterbi Error Count Register 81H & 82H & 83H

Name	Addr	B7	B6	B5	B4	B3	B2	B1	B0	Flag	Default
VIT ERR CNT L	81H	VIT_ERR_CNT[7:0]								R	00H
VIT ERR CNT M	82H	VIT_ERR_CNT[15:8]								R	00H
VIT ERR CNT H	83H	VIT_ERR_CNT[23:16]								R	00H

VIT_ERR_CNT [23:0] indicates the number of errors at the input of Viterbi decoder. The count mode is decided by the register 80H. Only when VIT_ERR_CNT_L is read, will the VIT_ERR_CNT_M and VIT_ ERR_CNT_H be updated to keep consistency. Therefore, the sequence of reading these three registers should be VIT_ERR_CNT_L, VIT_ERR_CNT_M and VIT_ERR_CNT_H, or VIT_ERR_CNT_L, VIT_ERR_CNT_H and VIT_ERR_CNT_M. These

Addr: 5F East Software Park Innovation Building, No.99 Huaxing Road, Hangzhou P.R.China, 310012
Tel: +86-571-88156088 Fax: +86-571-88156081 http://www.nationalchip.com

three registers represent the quality of QPSK demodulator.

$$QPSK\_ERR = \frac{K \times VIT\_RAT \times VIT\_ERR\_CNT[23:0]}{8 \times BYTE\_CNT},$$

In the above equation, $BYTE\_CNT$ is the count period in byte. When counting for bit error rate (i.e. VIT_ERR_CNT_MOD = 100xx), $K = 1$, and when counting for symbol error rate (i.e. VIT_ERR_CNT_MOD = 101xx), $K = 2$. For example, if VIT_ERR_CNT_MOD = 0x11, and VIT_RAT = 3/4, which can be obtained in VIT_RAT_CUR，then the bit error rate is

$$QPSK\_BER = \frac{1 \times 3/4 \times VIT\_ERR\_CNT[23:0]}{8 \times 2\text{^}14}$$

6.2 RS Decoder Registers

6.2.1 RS Decode Error Mode Register A0H

Name	Addr	B7	B6	B5	B4	B3	B2	B1	B0	Flag	Default
RS ERR MODE	A0H	RESERVED				CNT_KND		ERR_KND		R/W	07H

B3-2: CNT_KND Number of packet

0: 2^12

1: 2^10

2: 2^8

3: 2^6

B1-0: ERR _KND Type of error accumulated

0: Uncorrectable packet error sum

1: Packet error sum

2: Byte error sum

3: Bit error sum

Default: 2^10 packets, Bit error sum.

6.2.2 RS Decode Error Count Register A1H & A2H

Name	Addr	B7	B6	B5	B4	B3	B2	B1	B0	Flag	Default

Addr: 5F East Software Park Innovation Building, No.99 Huaxing Road, Hangzhou P.R.China, 310012
Tel: +86-571-88156088 Fax: +86-571-88156081 http://www.nationalchip.com

RS ERR CNT L	A1H	RS_ERR_CNT [7:0]	R	00H
RS ERR CNT H	A2H	RS_ERR_CNT [15:8]	R	00H

RS_ERR_CNT [15:0] shows the number of error before RS decoder. You can configure the statistic length (Reg.A0H). While system is stabile, two registers can be read and the error rate can be known.

Bit Error Rate: $VIT\_BER = \frac{RS\_ERR\_CNT[15:0]}{204 \times 8 \times PACKET\_CNT}$

$PACKET\_CNT$ is the statistic number. For example: Reg. A0H default, the bit error rate is:

$VIT\_BER = \frac{RS\_ERR\_CNT[15:0]}{204 \times 8 \times 2\text{^}10}$

Addr: 5F East Software Park Innovation Building, No.99 Huaxing Road, Hangzhou P.R.China, 310012
Tel: +86-571-88156088 Fax: +86-571-88156081 http://www.nationalchip.com

7 MPEG Packet Data Output

7.1 Data Output Control Registers

7.1.1 Data Control Register B0H

Name	Addr	B7	B6	B5	B4	B3	B2	B1	B0	Flag	Default
TS DATA CTRL	B0H	TEI_EN	PKT_LEN	HEAD	5'b11101					R/W	BDH

B7: TEI_EN Show the uncorrectable packet error

1: Set the MSB of first byte of an uncorrectable packet, and clear it when the packet is corrected (default).

0: Not set

B6: PKT_LEN Output data length is 188 bytes or 204 bytes

1: 188 bytes

0: 204 bytes (default)

B5: HEAD Sync

1: Sync B8H is replaced by 47H (default)

0: Not replaced

7.1.2 Data Format Control Register B1H

Name	Addr	B7	B6	B5	B4	B3	B2	B1	B0	Flag	Default
TS FMT CTRL	B1H	PO_EN	POS_EN	4'b1011				RS0	1'b0	R/W	ACH

B7: PO_EN Output in parallel or serial mode

1: Parallel (default)

0: Serial

B6: POS_EN Define the output date aligning with output byte clock's positive edge or negative edge.

Parallel:

Addr: 5F East Software Park Innovation Building, No.99 Huaxing Road, Hangzhou P.R.China, 310012
Tel: +86-571-88156088 Fax: +86-571-88156081 http://www.nationalchip.com

	1:	Align with positive edge
	0:	Align with negative edge (default)
	Serial:	
	1:	Bit clock valid in low (suggested)
	0:	Bit clock valid in high
B1:	RS0	Output clock signal configuration during parity bytes
	1:	D7 is low during the parity bytes. If the packet contains more than 8 errors, Error only remains high during the data transmission. In parallel mode, clock remains low during the parity bytes. In serial mode, the output bit clock always running.
	0:	Clock is continuous and the parity bytes are transmitted. if the packet contains more than 8 errors, Error remains high during the entire packet.

It is suggested that set this register to ACH in parallel mode and 7CH in serial mode.

7.2 Output In Parallel Mode

Every packet has 188 or 204 bytes. Data and other signals are clocked by the positive or negative edge of clock, referring to figure 7 and figure 8.

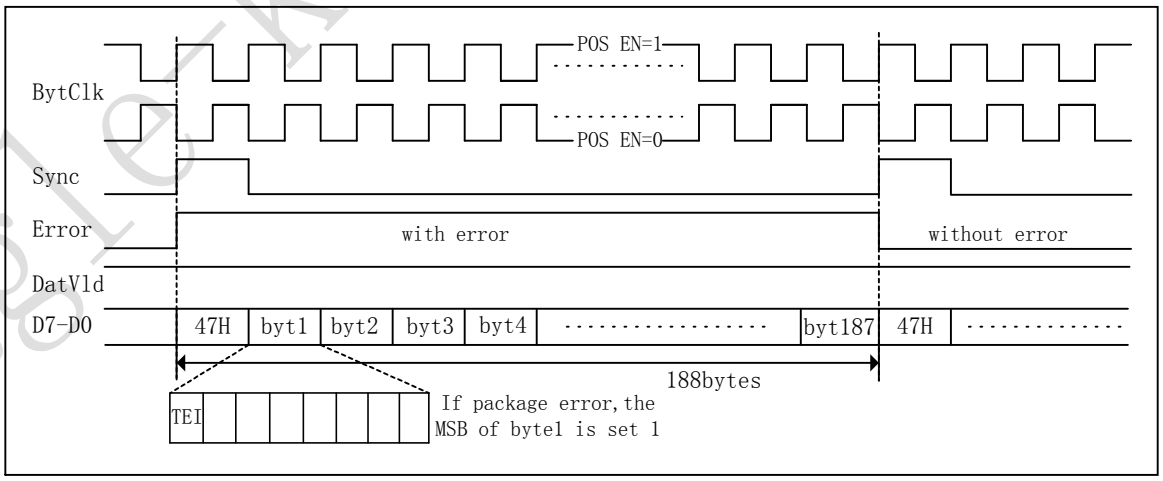


Figure 7 Parallel Output (188 bytes/packet and 188 bytes valid)

Addr: 5F East Software Park Innovation Building, No.99 Huaxing Road, Hangzhou P.R.China, 310012
Tel: +86-571-88156088 Fax: +86-571-88156081 http://www.nationalchip.com

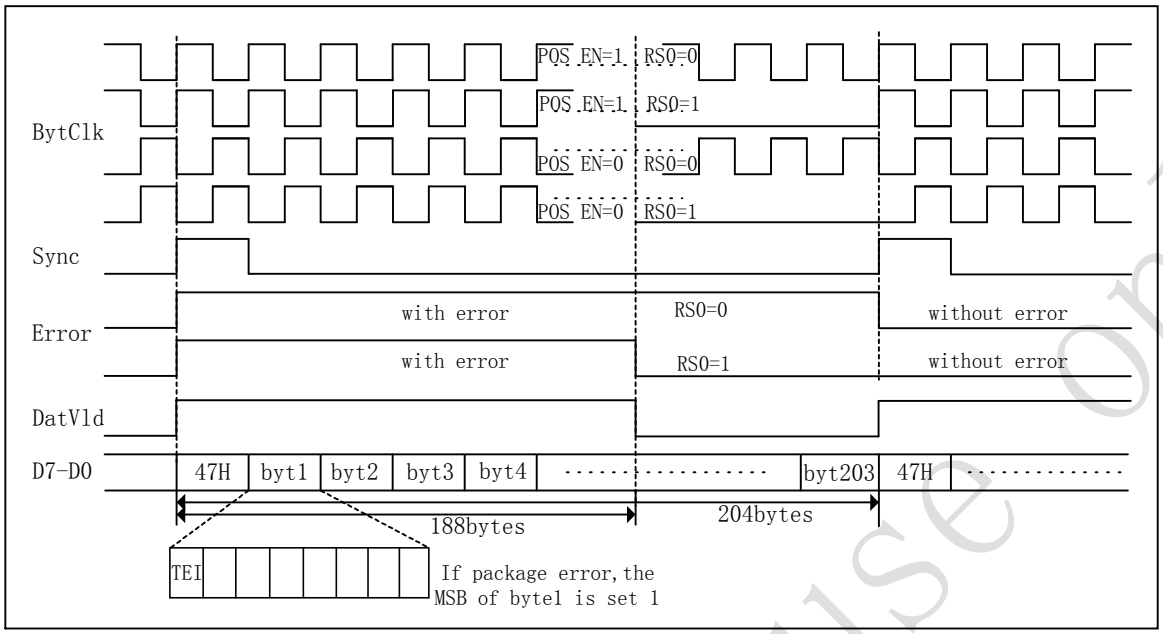


Figure 8 Parallel Output (204 bytes/packet and 188 bytes valid)

7.3 Output In Serial Mode

The serial bit stream is available on D7, and BytClk is the bit clock. Data and other signals are clocked by the positive or negative edge of clock, referring to figure 9 and figure 10.

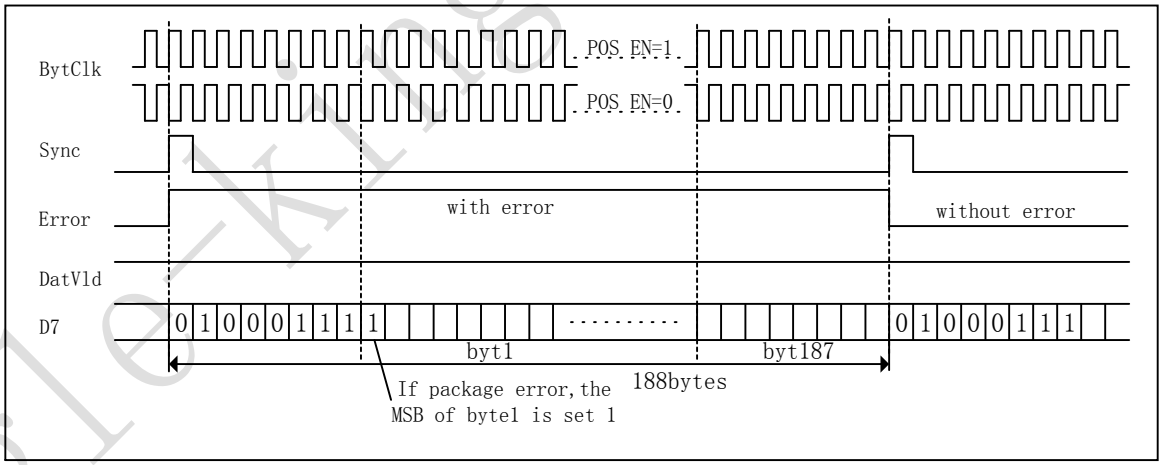


Figure 9 Serial Output (188 bytes/packet and 188 bytes valid)

Addr: 5F East Software Park Innovation Building, No.99 Huaxing Road, Hangzhou P.R.China, 310012
Tel: +86-571-88156088 Fax: +86-571-88156081 http://www.nationalchip.com

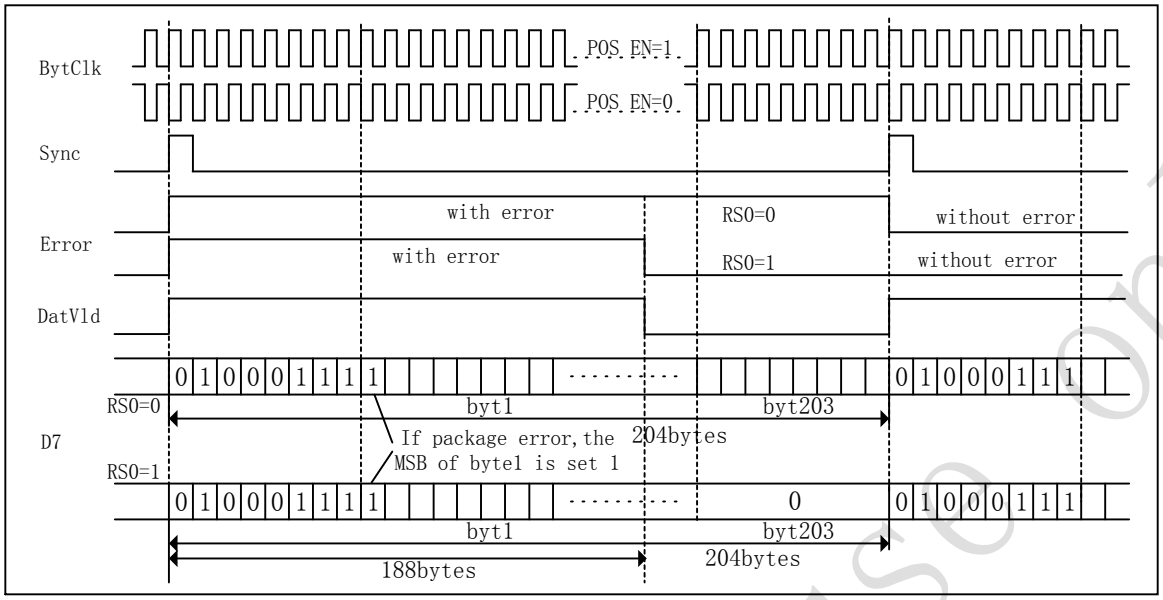


Figure 10 Serial Output (204 bytes/packet and 188 bytes valid)

Addr: 5F East Software Park Innovation Building, No.99 Huaxing Road, Hangzhou P.R.China, 310012
Tel: +86-571-88156088 Fax: +86-571-88156081 http://www.nationalchip.com

8 Application Notes

8.1 Recommended Operating Conditions

Parameters	Pins	Min	Typ	Max	Units
1.8V Power Supply Voltage	5,14,28,36,42,56,58,64	1.62	1.80	1.98	V
1.8V Power Supply Current	5,14,28,36,42,56,58,64	6[1]	120	160[2]	mA
3.3V Power Supply Voltage	18,30,47,54,60	3.0	3.3	3.6	V
3.3V Power Supply Current	18,30,47,54,60	6[1]	45	50[2]	mA
Input clock frequency	61		4.000		MHz
Ambient Operation Temperature		0	20	70	℃

[1]Conditions: Stand-By mode；
[2]Conditions: Symbol Rate 44.9MSPS, Code Rate 7/8, and TS serial output.

8.2 Absolute Maximum Ratings

Parameters	Pins	Min	Max	Units
1.8V Power Supply Voltage	5,14,28,36,42,56,58,64	-0.3	2.0	V
3.3V Power Supply Voltage	18,30,47,54,60	-0.3	3.6	V
Voltage on I/O Pins		-0.3	5.5	V
Storage Temperature		-65	150	℃
Operating Ambient Temperature		0	70	℃
Junction Temperature		0	125	℃

8.3 DC Electronic Characteristics

Parameters	Pins	Min	Typ	Max	Units
1.8V Power Supply Voltage	5,14,28,36,42,56,58,64	1.62	1.80	1.98	V
1.8V Power Supply Current	5,14,28,36,42,56,58,64	6[1]	120	160[2]	mA
3.3V Power Supply Voltage	18,30,47,54,60	3.0	3.3	3.6	V
3.3V Power Supply Current	18,30,47,54,60	6[1]	45	50[2]	mA
Output High Level (VOH)		2.4			V
Output Low Level (VOL)				0.4	V
Output Drive Strength				24	mA
Input High Level (VIH)		2.0		5.5	V
Input Low Level (VIL)		-0.3		0.8	V
Input Leakage Current				10	uA

Addr: 5F East Software Park Innovation Building, No.99 Huaxing Road, Hangzhou P.R.China, 310012
Tel: +86-571-88156088 Fax: +86-571-88156081 http://www.nationalchip.com

[1]Conditions: Stand-By mode；
[2]Conditions: Symbol Rate 44.9MSPS, Code Rate 7/8, and TS serial output.

8.4 GX1101P Register Map

8.4.1 Read/Write Register Map

Name	Addr	B7	B6	B5	B4	B3	B2	B1	B0	Flag	Default
STBY	01H	STANDBY	TS_OEN	6'B0						R/W	00H
PLL KN	02H	PLL_K		PLL_N					PLL_M[8]	R/W	C0H
PLL M	03H	PLL_M[7:0]								R/W	B2H
ADC GAIN	04H	6'B0						ADC_GAIN		R/W	01H
DISEQC MODE	10H	RESERVED	HV SELECT	TX_BYTES			DISEQC_MODE			R/W	00H
DISEQC RATIO	11H	DISEQC_RATIO								R/W	2DH
DISEQC INS	12H	DISEQC_INS								R/W	00H
DISEQC CTRL	1BH	RESERVED				MIN_PULSE		MAX_ TONE	MIN_ TONE	R/W	0CH
GLB CTRL	30H	RESERVED			RPT_TIME_ SEL		COOL_ RST	HOT_ RST	RPTER_ EN	R/W	0AH
GPOP0	31H	RESERVED			1' B 1	PO0/AUD_OUT				R/W	16H
GPOP1	32H	RESERVED			4'B1100				PO1	R/W	18H
AGC CTRL	40H	FREEZE	CLK		SPEED			PLR	1'B0	R/W	52H
AGC STD	41H	AGC_STD								R/W	1CH
FREQ ERR1 L	50H	FREQ_ERR1 [7:0]								R/W	00H
FREQ ERR1 H	51H	FREQ_ERR1 [15:8]								R/W	00H
AUDIO DEROT	55H	AUDIO_ON	DRT_ON	6'B101110						R/W	6EH
IQ SWAP	58H	IQ_SP	7'b0110100							R/W	34H
CRL PARA	59H	CRL_PARA								R/W	58H
BLIND SEL	60H	RESERVED，SET TO 7'B0							BLD MOD	R/W	00H
SYM RATE L	61H	SYM_RATE [7:0]								R/W	AEH
SYM RATE H	62H	SYM_RATE [15:8]								R/W	11H
TRL PARA	69H	TRL_PARA								R/W	24H
SCAN LEN	6BH	4'b0110			SCAN_LEN					R/W	67H
VIT ERR MODE	80H	RESERVED			VIT_ERR_CNT_MOD					R/W	11H

Addr: 5F East Software Park Innovation Building, No.99 Huaxing Road, Hangzhou P.R.China, 310012
Tel: +86-571-88156088 Fax: +86-571-88156081 http://www.nationalchip.com

VIT MODE	85H	3'B0			AUT_ IQ	VIT_RAT		AUT_ RAT	R/W	10H
RS ERR MODE	A0H	RESERVED				CNT_KND	ERR_KND		R/W	07H
TS DATA CTRL	B0H	TEI_EN	PKT_ LEN	HEAD	5'B11101				R/W	BDH
TS FMT CTRL	B1H	PO_EN	POS_EN	4'B1011			RS0	1'B0	R/W	ACH

8.4.2 Read Only Register Map

Name	Addr	B7	B6	B5	B4	B3	B2	B1	B0	Flag	Default
ID	00H	ID [7:0] CHIP IDENTIFICATION								R	01H
DISEQC INT	1CH	RX_BYTES			TX_INT	SILENT _INT	END_ MSG_INT	ERR_ INT	PAR_ERR _INT	R	00H
DISEQC RESP	1EH	DISEQC_RESP								R	00H
STATE	34H	STATE_INDICATOR								R	00H
BLIND STATE	35H	BLIND_STATE_INDICATOR								R	00H
INTENSITY	42H	SIGNAL_INTENSITY								R	00H
FREQ ERR2 L	52H	FREQ_ERR2 [7:0]								R	00H
FREQ ERR2 H	53H	FREQ_ERR2 [15:8]								R	00H
SNR	54H	SNR [7:0]								R	00H
VIT ERR CNT L	81H	VIT_ERR_CNT [7:0]								R	00H
VIT ERR CNT M	82H	VIT_ERR_CNT [15:8]								R	00H
VIT ERR CNT H	83H	VIT_ERR_CNT [23:16]								R	00H
VIT RAT	84H	VIT_ RAT			RESERVED					R	00H
RS ERR CNT L	A1H	RS_ ERR_CNT [7:0]								R	00H
RS ERR CNT H	A2H	RS_ERR_CNT [15:8]								R	00H

Addr: 5F East Software Park Innovation Building, No.99 Huaxing Road, Hangzhou P.R.China, 310012
Tel: +86-571-88156088 Fax: +86-571-88156081 http://www.nationalchip.com

8.5 Application Schematic

8.5.1 ADC External Circuit

The GX1101P supports both differential and single-ended mode input, and the common mode voltage (VCM) is 0.6*AVDD. So, resister dividers between AVDD and AGND are necessary for this DC bias, as shown in Figure11 and Figure12.

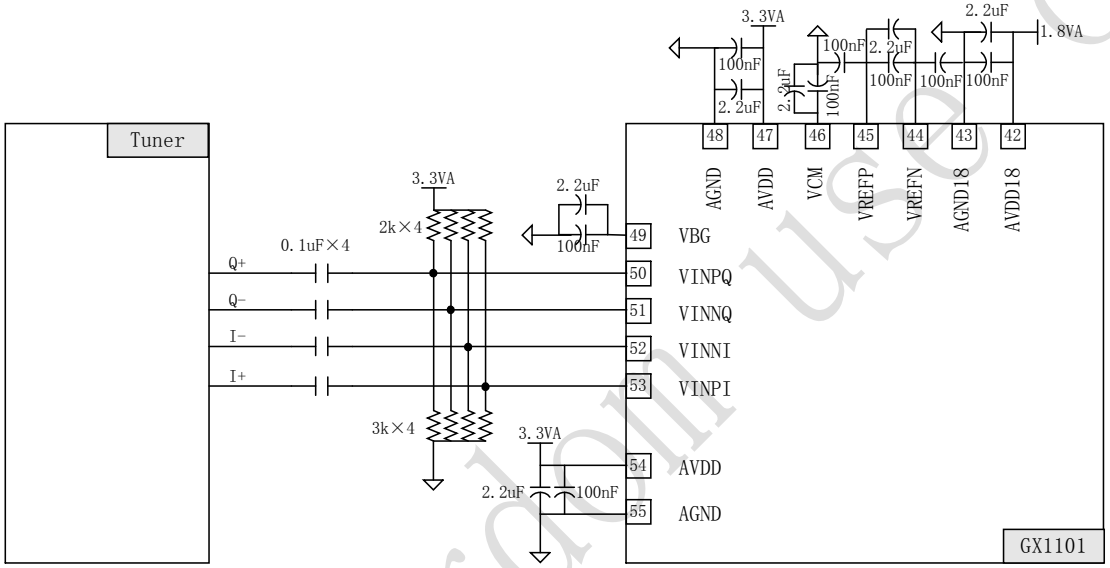


Figure 11 Differential Mode

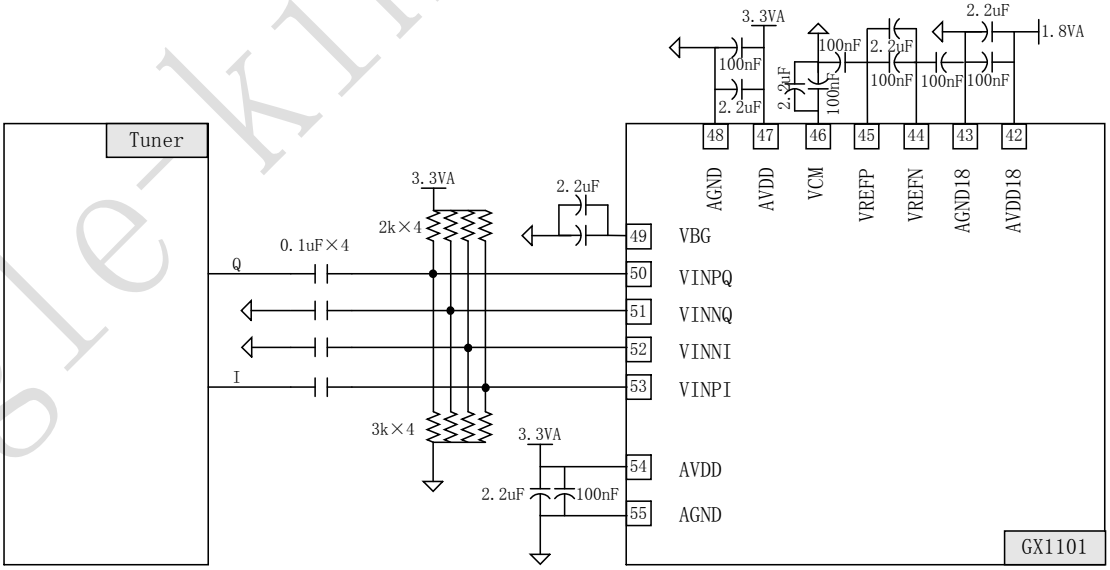


Figure 12 Single-ended Mode

Addr: 5F East Software Park Innovation Building, No.99 Huaxing Road, Hangzhou P.R.China, 310012
Tel: +86-571-88156088 Fax: +86-571-88156081 http://www.nationalchip.com

8.5.2 Crystal and PLL

Parallel resonant fundamental frequency (typ.)	4MHz
Tolerance overall	±50ppm
Tolerance over operating temperature range	±25ppm
Equivalent series resistance	<50Ohm
Nominal load capacitance	30pF

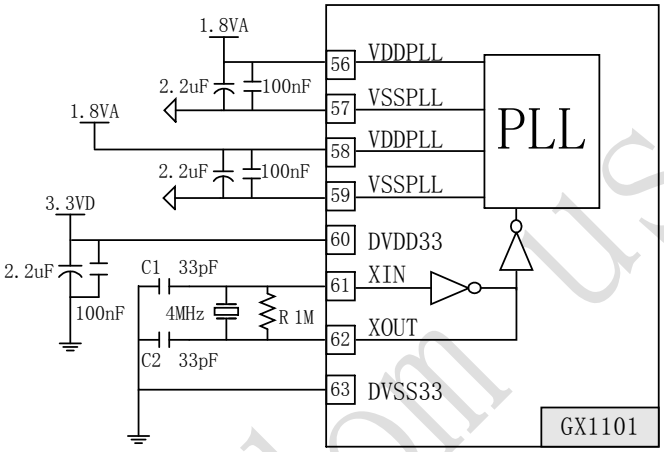


Figure 13 Crystal and PLL

Note:

1, The crystal frequency is flexible, but users should confirm the system clock frequency is no less than two times of the highest symbol rate,

2, In Figure13, C1 and C2 are determined by the crystal's load capacitance. We suggest users to adjust their values slightly to get a precise enough oscillation frequency.

3, GX1101's clock may be driven by another IC. To do this, please remove the crystal and the two capacitors, connect another IC's CLKOUT pin to GX1101's XIN pin through a 0.1uF capacitor, and remain the feed-back resister (1Mohm). This circuit is shown in Figure 14.

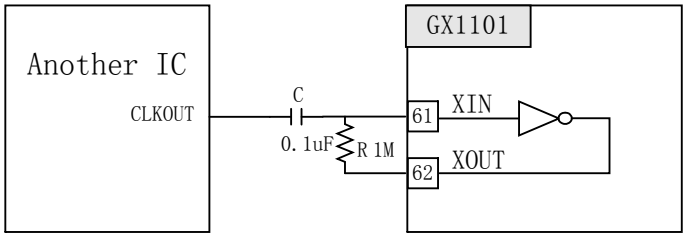


Figure 14 GX1101's Clock Driven by Another IC

8.5.3 AGC Circuit

Addr: 5F East Software Park Innovation Building, No.99 Huaxing Road, Hangzhou P.R.China, 310012
Tel: +86-571-88156088 Fax: +86-571-88156081 http://www.nationalchip.com

Most of the tuners have maximum (V_{max}) and minimum (V_{min}) control voltage limits. If the control voltage (V_{agc}) is higher than V_{max}, the tuner may be destroyed. On the other hand, if V_{agc} is lower than V_{min}, it is out of AGC effective range. Users can get V_{max} and V_{min} from tuner's AGC curve. To make best use of AGC effective range, we provide a general circuit, as shown in Figure15.

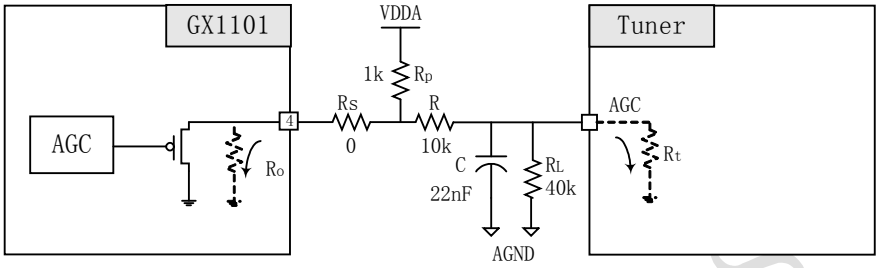


Figure 15 AGC

The components can be derived by:

(1) $\tau \approx R*C=0.2ms$

(2) $VDDA*(R_L//R_t)/((R_L//R_t)+R+R_P)= V_{max}$

(3) $VDDA*(R_S+R_O) /(R_P+R_S+R_O)= V_{min}$ $(R_S, R_O, R_P << R, R_L, R_t)$

where Ro is about 50Ohm, VDDA is 5V or 3.3V. If V_{min}=0, Rs is equal to 0.

8.5.4 LNB Controller

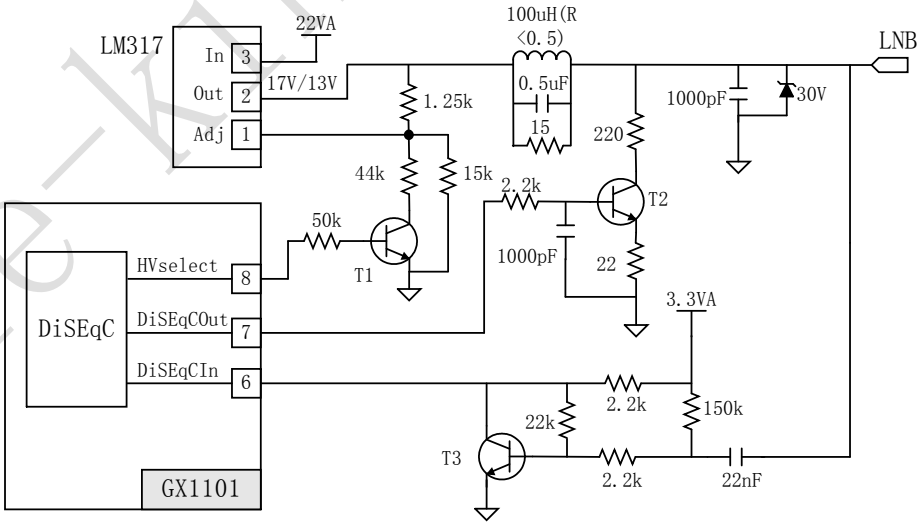


Figure 16 LNB power supply and control

The receive part is only necessary for DiSEqC™ 2.x versions. For DiSEqC™ 1.x versions,

Addr: 5F East Software Park Innovation Building, No.99 Huaxing Road, Hangzhou P.R.China, 310012
Tel: +86-571-88156088 Fax: +86-571-88156081 http://www.nationalchip.com

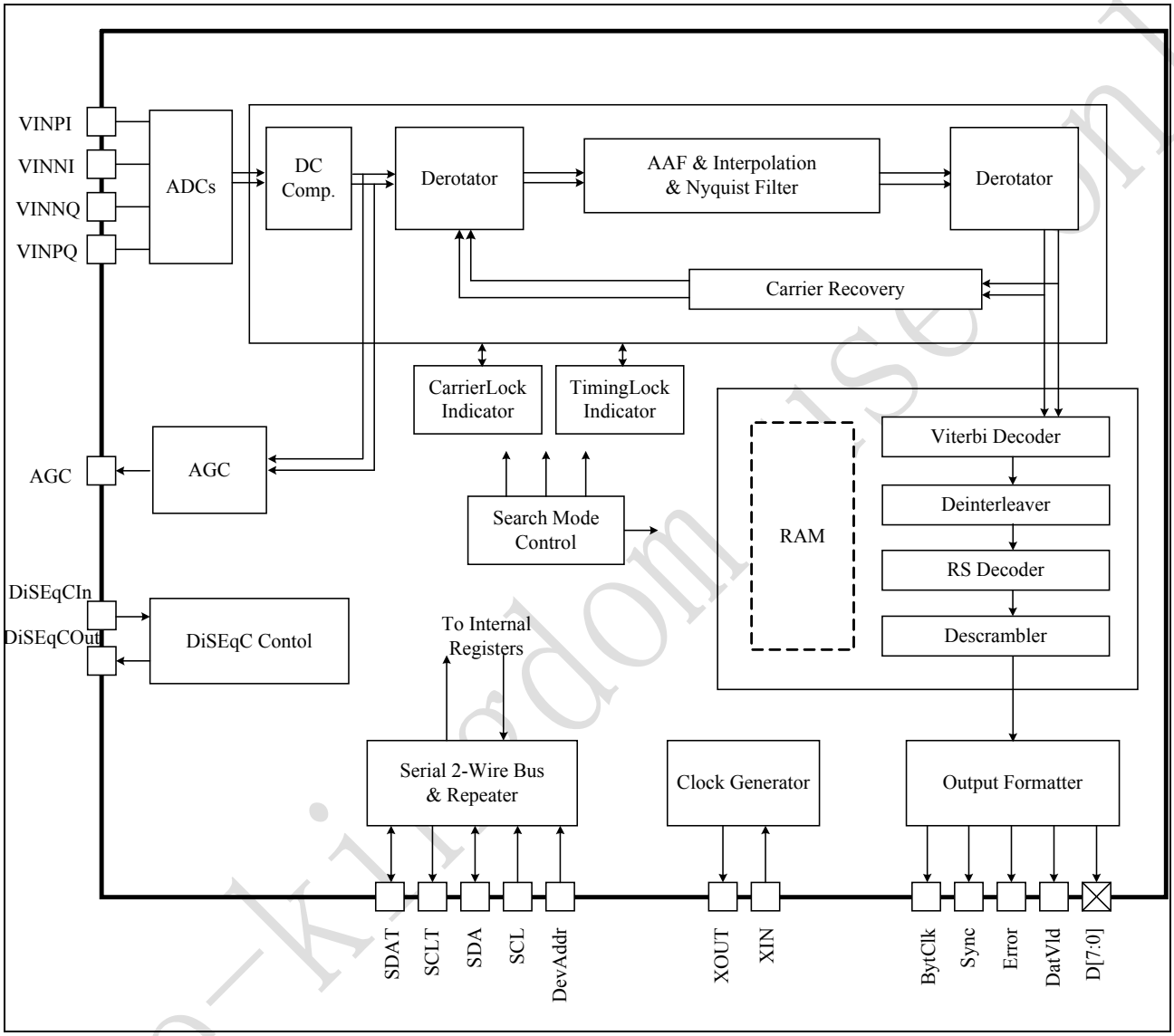
pin6 should be connected to the ground.

8.5.5 Power Sequence

In order to avoid latch, please confirm the core powers (1.8V) are built behind the I/O powers (3.3V).

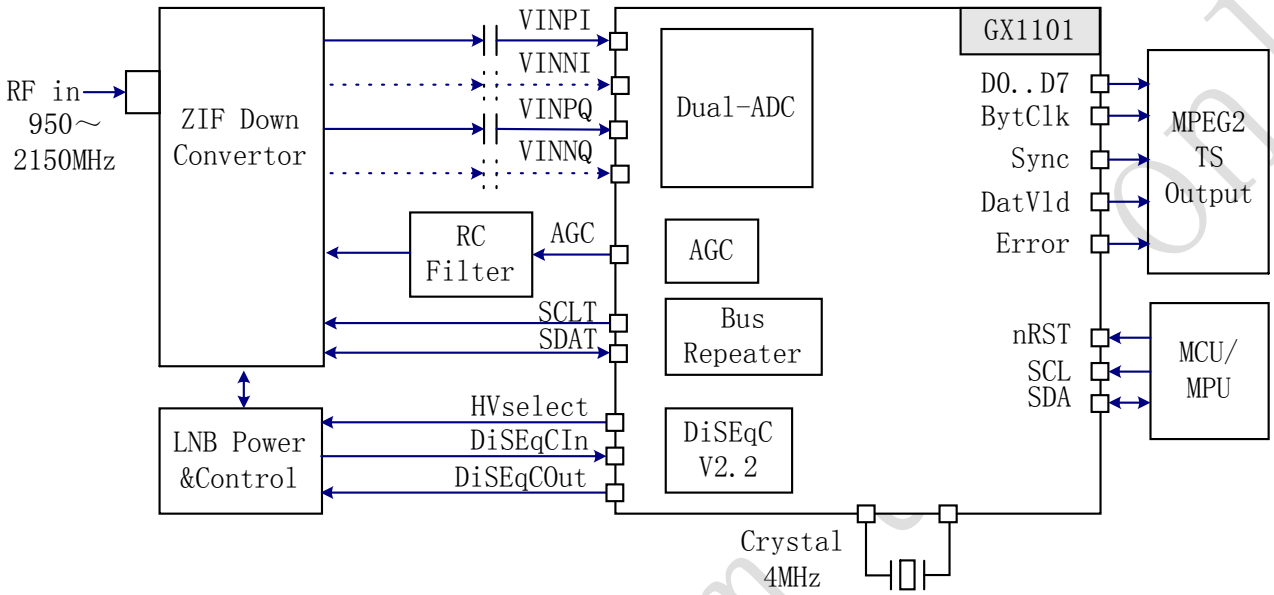
Addr: 5F East Software Park Innovation Building, No.99 Huaxing Road, Hangzhou P.R.China, 310012
Tel: +86-571-88156088 Fax: +86-571-88156081 http://www.nationalchip.com

9 Block Diagram



Addr: 5F East Software Park Innovation Building, No.99 Huaxing Road, Hangzhou P.R.China, 310012
Tel: +86-571-88156088 Fax: +86-571-88156081 http://www.nationalchip.com

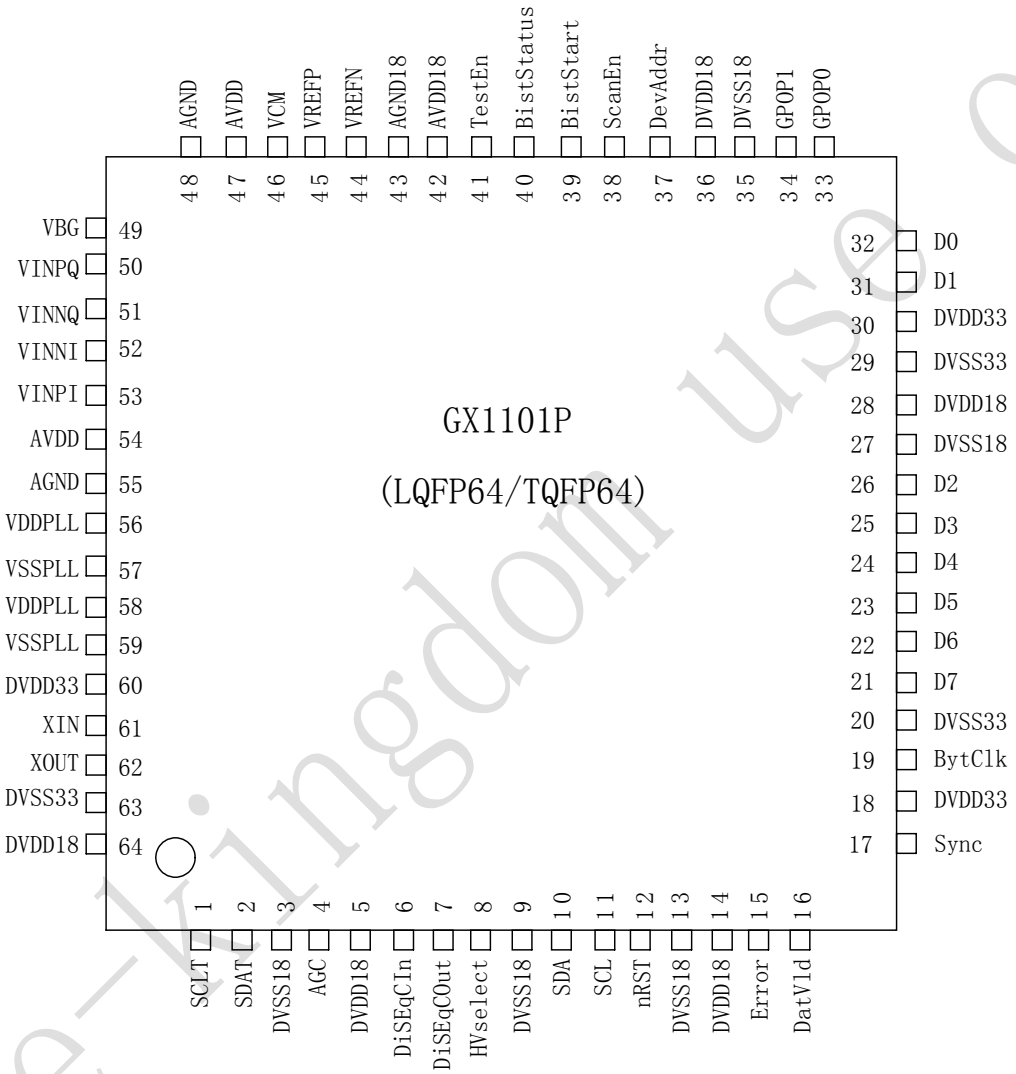
10 Application Diagram



Addr: 5F East Software Park Innovation Building, No.99 Huaxing Road, Hangzhou P.R.China, 310012
Tel: +86-571-88156088 Fax: +86-571-88156081 http://www.nationalchip.com

11 Pin Information

11.1 Pin Diagram



Addr: 5F East Software Park Innovation Building, No.99 Huaxing Road, Hangzhou P.R.China, 310012
Tel: +86-571-88156088 Fax: +86-571-88156081 http://www.nationalchip.com

11.2 Pin Description

PIN	NAME	DIR	DESCRIPTION
1	SCLT	OD	Serial Clock of the 2-wire bus for tuner, Open-Drain output, 5V tolerant.
2	SDAT	I/OD	Serial Data of the 2-wire bus for tuner, Open-Drain bi-direction, 5V tolerant.
10	SDA	I/OD	Serial Data of the 2-wire bus for GX1101P, Open-Drain bi-direction, 5V tolerant.
11	SCL	I	Serial Clock of the 2-wire bus for GX1101P, 5V tolerant.
37	DevAddr	I	Address select for 2-wire bus, 5V tolerant, Read address is: 110100A1, Write address is: 110100A0.
4	AGC	OD	PDM Output for AGC, Open-Drain output, 5V tolerant.
6	DiSEqCIn	I	DiSEqC Input signal, 5V tolerant.
7	DiSEqCOut	O	DiSEqC Output signal.
8	HVselect	O	Horizontal or Vertical polarization Select output for the LNB controller, refer to register 10H.
12	nRST	I	Chip Reset, active low, 5V tolerant. To get an effective reset, the low pulse width must be longer than 2us.
15	Error	O	Packet Error signal of MPEG2-TS.
16	DatVld	O	Data Valid signal of MPEG2-TS.
17	Sync	O	Packet Synchronize signal of MPEG2-TS.
19	BytClk	O	Byte Clock of MPEG2-TS, it is Bit Clock in serial output mode.
21-26, 31-32	D[7:0]	O	Data Output of MPEG2-TS, D[7] is serial data in serial output mode.
33	GPOP0	O	Programmable Output, refer to register 31H, 0 default.

Addr: 5F East Software Park Innovation Building, No.99 Huaxing Road, Hangzhou P.R.China, 310012
Tel: +86-571-88156088 Fax: +86-571-88156081 http://www.nationalchip.com

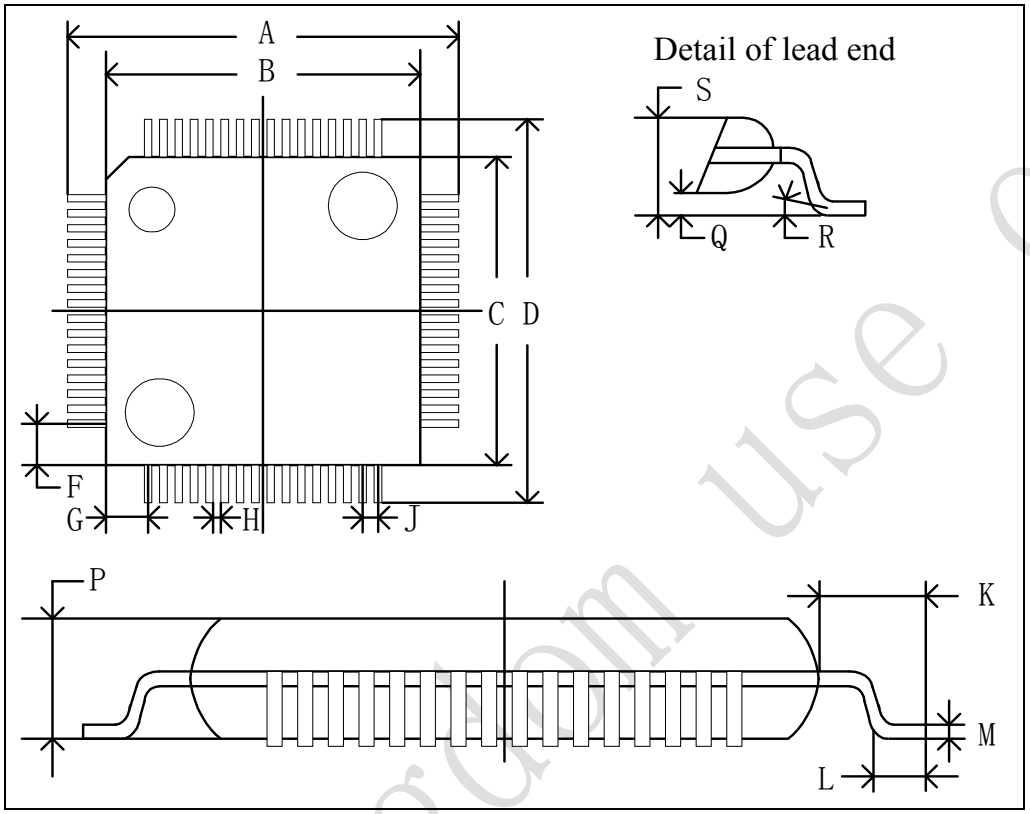
34	GPOP1	O	Programmable Output, refer to register 32H, 1 default.
38	ScanEn	I	Scan test Enable of Register Chain, active High, just for manufactory test and connect to 0 in normal operation mode.
39	BistStart	I	Built-In Self-Test (BIST) Start signal, active High, just for test and connect to 0 in normal operation mode.
40	BistStatus	O	Built-In Self-Test (BIST) Status output signal, just for test.
41	TestEn	I	Test Enable, active High, just for manufactory test and connect to 0 in normal operation mode.
42	AVDD18	Pow	Analog Positive Power Supply for ADC (1.8V)
43	AGND18	Pow	Analog Negative Power Supply for ADC (GND).
44	VREFN	O	Negative Reference Voltage output to be decoupled with external capacitors: 100nF between VREFN and AGND, and 2.2uF//100nF between VREFP and VREFN.
45	VREFP	O	Positive Reference Voltage output to be decoupled with external capacitors: 100nF between VREFP and AGND, and 2.2uF//100nF between VREFP and VREFN.
46	VCM	O	Common Mode Voltage output to be decoupled with external capacitors: 2.2uF//100nF between VCM and AGND.
47,54	AVDD	Pow	Analog Positive Power Supply for ADC (3.3V).
48,55	AGND	Pow	Analog Negative Power Supply for ADC (GND).
49	VBG	O	Band-Gap Voltage output to be decoupled with external capacitors: 2.2uF//100nF between VBG and AGND.
50	VINPQ	I	Voltage Input Positive of base-band signal Q.
51	VINNQ	I	Voltage Input Negative of base-band signal Q.
52	VINNI	I	Voltage Input Negative of base-band signal I.
53	VINPI	I	Voltage Input Positive of base-band signal I.
56,58	VDDPLL	Pow	Analog Positive Power Supply for PLL (1.8V).
57,59	VSSPLL	Pow	Analog Negative Power Supply for PLL (GND).

Addr: 5F East Software Park Innovation Building, No.99 Huaxing Road, Hangzhou P.R.China, 310012
Tel: +86-571-88156088 Fax: +86-571-88156081 http://www.nationalchip.com

61	XIN	I	Crystal Input.
62	XOUT	O	Crystal Output.
5,14,28,36,64	DVDD18	Pow	Digital Positive Power Supply for Core (1.8V).
3,9,13,27,35	DVSS18	Pow	Digital Negative Power Supply for Core(GND).
18,30,60	DVDD33	Pow	Digital Positive Power Supply for I/O(3.3V).
20,29,63	DVSS33	Pow	Digital Negative Power Supply for I/O (GND).

Addr: 5F East Software Park Innovation Building, No.99 Huaxing Road, Hangzhou P.R.China, 310012
Tel: +86-571-88156088 Fax: +86-571-88156081 http://www.nationalchip.com

12 Package Information



ITEM	MILLIMETERS	INCHES
A	12.0±0.4	0.472±0.016
B	10.0±0.2	0.394±0.008
C	10.0±0.2	0.394±0.008
D	12.0±0.4	0.472±0.016
F	1.25±0.1	0.049±0.004
G	1.25±0.1	0.049±0.004
H	0.2±0.1	0.008±0.004
I	0.13	0.005
J	0.5 (T.P.)	0.020 (T.P.)
K	1.0±0.2	0.039±0.008
L	0.5±0.2	0.020±0.008
M	+0.10 0.127 -0.05	+0.004 0.005 -0.002
N	0.10	0.004
P	1.4 (T.P.)	0.055 (T.P.)

Addr: 5F East Software Park Innovation Building, No.99 Huaxing Road, Hangzhou P.R.China, 310012
Tel: +86-571-88156088 Fax: +86-571-88156081 http://www.nationalchip.com

History

Date	Version	Note
2004-05	1.0	First version.
2004-07	1.3	Update registers: 59H, 69H, and add a clock drive circuit.
2004-08	1.4	Update according to NRE.
2004-12	1.5	Update register B1H
2005-02	1.6	Update pin list, 10uF ->2.2uF

杭州国芯科技有限公司
HANGZHOU GUOXIN SCIENCE AND TECHNOLOGY CO.,LTD

ADDRRESS: 5F East Software Park Innovation Building,
No.99 Huaxing Road, Hangzhou P.R.China,
ZIP CODE: 310012
TEL: +86-571-88156080, 88156088-858
FAX: +86-571-88156081, 88156083
E-mail: Marketing@nationalchip.com
Websit: http://www.nationalchip.com