High Speed CMOS 16-Bit Latch in QVSOP™

QS74FCT2X373T
QS74FCT2X2373T

FEATURES/BENEFITS

- 16-bit Function compatible to the 74F373 74ABT373 and 74FCT373T
- CMOS power levels: <15 mW static
- Available in 40-pin QVSOP
- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Undershoot clamp diodes on all inputs

FCT-T 2X373T

- JEDEC-FCT spec compatible
- Fastest CMOS logic family available
- A and C speed grades; 4.2 ns t_{PD} for C
- I_{OL} = 64 mA

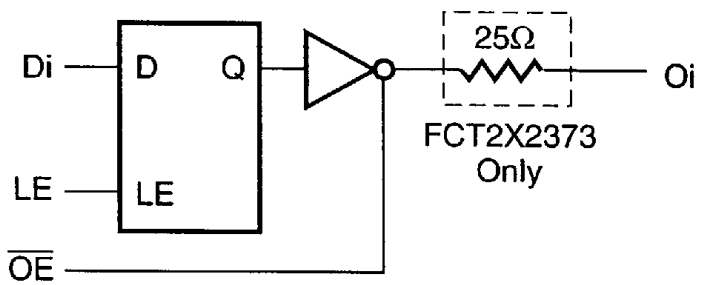
FCT-T 2X2373T (Advance Information)

- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- A and C speed grades; 4.2 ns t_{PD} for C
- I_{OL} = 12 mA

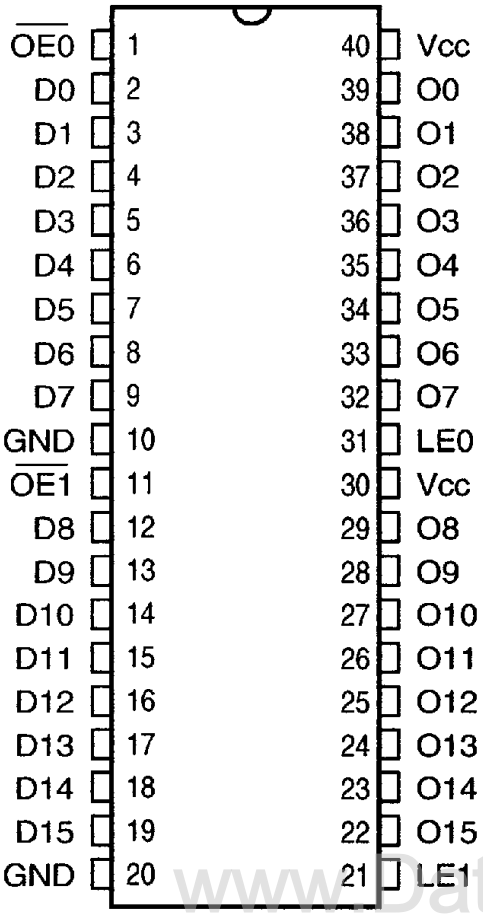
DESCRIPTION

The FCT2X373T and FCT2X2373T are 16-bit transparent latches with three-state outputs that are useful for bus-oriented applications. The Output Enable ($\overline{OE}$) and Latch Enable (LE) inputs are designed to operate as two 8-bit latches or one 16-bit latch. The FCT2X2373T is a 25Ω resistor output version useful for driving transmission lines and reducing system noise. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001), and outputs will no load an active bus when V_{CC} is removed from the device.

FUNCTIONAL BLOCK DIAGRAM



PINOUT



PIN DESCRIPTION

Name	I/O	Description
Di	I	Data Inputs
Oi	O	Data Outputs
LE0	I	Latch Enable, O7-O0
LE1	I	Latch Enable, O15-O8
$\overline{OE}$0	I	Output Enable, O7-O0
$\overline{OE}$1	I	Output Enable, O15-O8

FUNCTION TABLE

$\overline{OE}$n	LEn	Di	Internal Q Value	Outputs Oi	Function
H	X	X	X	Hi-Z	Disable Outputs
L L	X X	X X	H L	H L	Enable Outputs
X X	H H	L H	L H	X X	Pass Input Data
X	L	X	Q	X	Hold Prior Data

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground	–0.5V to +7.0V
DC Output Voltage V_{OUT}	–0.5V to +7.0V
DC Input Voltage V_{IN}	–0.5V to +7.0V
AC Input Voltage (for a pulse width ≤ 20 ns)	–3.0V
DC Input Diode Current with $V_{IN} < 0$	–20 mA
DC Output Diode Current with $V_{OUT} < 0$	–50 mA
DC Output Current Max. Sink Current/Pin	120 mA
Maximum Power Dissipation	1.2 watts
T_{STG} Storage Temperature	–65° to +150°C

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to this device resulting in functional or reliability type failures.

CAPACITANCE

T_A = 25°C, f = 1 MHz, V_{IN} = 0V, V_{OUT} = 0V

Pins	Typ	Unit
1-9, 11-19, 21, 31	4	pF
22-29, 32-39	6	pF

Note: Capacitance is characterized but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial T_A = 0°C to 70°C, Vcc = 5.0V ± 5%

Symbol	Parameter	Test Conditions	Min	Typ(1)	Max	Unit
V_{IH}	Input HIGH Voltage	Logic HIGH for All Inputs	2.0	—	—	V
V_{IL}	Input LOW Voltage	Logic LOW for All Inputs	—	—	0.8	V
ΔV_T	Input Hysteresis	$V_{TLH} - V_{THL}$ for All Inputs(3)	—	0.2	—	V
$\lvert I_{IH} \rvert$ $\lvert I_{IL} \rvert$	Input Current Input HIGH or LOW	Vcc = Max., 0 ≤ V_{IN} < Vcc	—	—	5	µA
$\lvert I_{OZ} \rvert$	Off-State Output Current (Hi-Z)	Vcc = Max., 0 ≤ V_{IN} ≤ Vcc	—	—	5	µA
I_{OS}	Short Circuit Current FCT2X373	Vcc = Max., V_{OUT} = GND(2,3)	–60	—	–225	mA
I_{OR}	Current Drive FCT2X2373 (25Ω)	Vcc = Max., V_{OUT} = 2.0V	50	—	—	mA
V_{IC}	Input Clamp Voltage	Vcc = Min., I_{IN} = –18 mA(3)	—	–0.7	–1.2	V
V_{OH}	Output HIGH Voltage	Vcc = Min., I_{OH} = –15 mA	2.4	—	—	V
V_{OL}	Output LOW Voltage FCT2X373	Vcc = Min., I_{OL} = 64 mA	—	—	0.55	V
V_{OL}	Output LOW Voltage FCT2X2373 (25Ω)	Vcc = Min., I_{OL} = 12 mA	—	—	0.50	V
R_{OUT}	Output Resistance FCT2X2373 (25Ω)	Vcc = Min., I_{OL} = 12 mA	20	28	40	Ω

Notes:
1. Typical values indicate Vcc = 5.0V and T_A = 25°C.
2. Not more than one output should be shorted and the duration is ≤1 second.
3. These parameters are guaranteed by design but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]	Min	Max	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., freq = 0 $0V \le V_{IN} \le 0.2V$ or $V_{CC}-0.2V \le V_{IN} \le V_{CC}$	—	3.0	mA
ΔI_{CC}	Supply Current per Input @ TTL HIGH	V_{CC} = Max., V_{IN} = 3.4V, freq = 0[2]	—	2.0	mA
Q_{CCD}	Supply Current per Input per MHz	V_{CC} = Max., Outputs Open and Enabled One Bit Toggling @ 50% Duty Cycle Other Inputs at GND or V_{CC}[3,4]	—	0.25	mA/ MHz

Notes:
1. For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
2. Per TTL driven input (V_{IN} = 3.4V).
3. For flip-flops, Q_{CCD} is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or teste capacitance. This parameter is guaranteed by design but not tested.
4. Ic can be computed using the above parameters as explained in the Technical Overview section.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

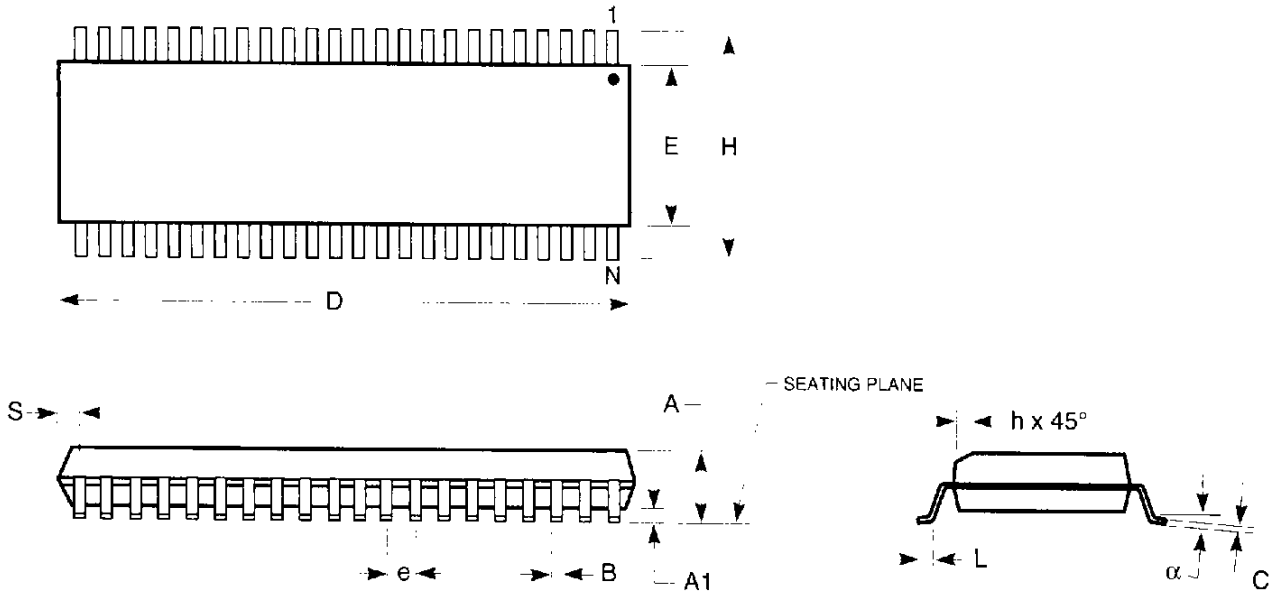
Commercial T_A = 0°C to 70°C, V_{CC} = 5.0V ± 5%
C_{LOAD} = 50 pF, R_{LOAD} = 500Ω unless otherwise noted.

Symbol	Description	2X373A 2X2373A Min	2X373A 2X2373A Max	2X373C 2X2373C Min	2X373C 2X2373C Max	Unit
t_{PHL} t_{PLH}	Propagation Delay[1] Di to Oi	1.5	5.2	1.5	4.2	ns
t_{PHLE} t_{PLHE}	Propagation Delay[1] LE HIGH to Oi	2.0	8.5	2.0	5.5	ns
t_{PZH} t_{PZL}	Output Enable Time[1] $\overline{OE}$ to Oi, FCT2X373	1.5	6.5	1.5	5.5	ns
t_{PZH} t_{PZL}	Output Enable Time[1] $\overline{OE}$ to Oi, FCT2X2373	1.5	6.5	1.5	6.2	ns
t_{PHZ} t_{PLZ}	Output Disable Time[2] $\overline{OE}$ to Oi	1.5	5.5	1.5	5.0	ns
t_S	Data Setup Time Di to LE, HIGH or LOW	2.0	—	2.0	—	ns
t_H	Data Hold Time Di to LE, HIGH or LOW	1.5	—	1.5	—	ns
t_W	Clock Pulse Width[2] HIGH or LOW	5.0	—	4.0	—	ns

Notes:
1. Minimums guaranteed but not tested. See Test Circuit and Waveforms.
2. This parameter is guaranteed but not tested.

150-MIL QVSOP™ - Package Code Q1/Q2

150-Mil Wide Plastic Small Outline Gull-Wing



JEDEC#	MO-154BB			MO-154AB		
DWG#	PSS-40A (Q2)			PSS-48A (Q1)		
Symbol	Min	Nom	Max	Min	Nom	Max
A	0.059	0.065	0.069	0.059	0.065	0.069
A1	0.004	0.006	0.008	0.004	0.006	0.008
B	0.0067	0.008	0.009	0.0051	0.0063	0.008
C	0.0075	0.008	0.0098	0.0075	0.008	0.0098
D	0.386	0.390	0.394	0.386	0.390	0.394
E	0.150	0.154	0.157	0.150	0.154	0.157
e	0.0197 BSC, 0.5mm			0.0157 BSC, 0.4mm		
H	0.228	0.236	0.244	0.228	0.236	0.244
h	0.010	0.013	0.016	0.010	0.013	0.016
L	0.020	0.024	0.030	0.020	0.024	0.030
N	40			48		
α	0°	5°	8°	0°	5°	8°
S	0.006	0.008	0.010	0.012	0.014	0.016

Notes:
1. Refer to applicable symbol list.
2. All dimensions are in inches.
3. N is the number of lead positions.
4. Dimensions D and E are to be measured at maximum material condition but do not include mold flash. Allowable mold flash is 0.006 in. per side.
5. Lead coplanarity is 0.003 in. maximum.