QPD0012

20 W / 40 W, 48 V, 2.5 – 2.7 GHz, Asymmetric Doherty

Product Overview

The QPD0012 is a dual-path discrete GaN on SiC HEMT in DFN package which operates from 2.5 to 2.7 GHz. The device is a single-stage power amplifier transistor for Doherty application.

QPD0012 can deliver P_{AVG} of 7.6 W at +48 V operation.

Lead-free and RoHS compliant.

6 Pin 7.0 x 6.5 mm DFN Package

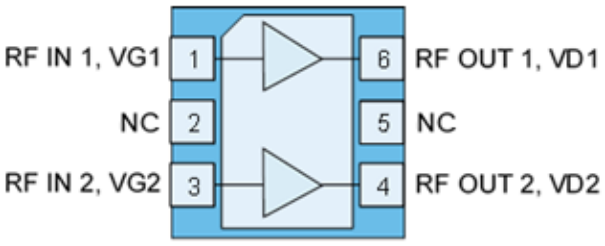
Key Features

- Operating Frequency Range: 2.5 – 2.7 GHz
- Operating Drain Voltage: +48 V
- Peak Doherty Output Power: 47.3 dBm
- Doherty Drain Efficiency at 38.8 dBm: 59%
- Doherty Gain at 38.8 dBm: 14.8 dB
- 7.0 x 6.5 mm DFN Package

Applications

- 5G Massive MIMO
- WCDMA / LTE
- Microcell Base Station
- Small Cell
- Active Antenna
- Asymmetric Doherty Applications

Functional Block Diagram



Ordering Information

Part Number	Description
QPD0012SR	7” Reel – 100 Pieces
QPD0012EVB2	Production Evaluation Board Kit

Absolute Maximum Ratings

Parameter	Rating
Breakdown Voltage (BV_{DG})	+165 V
Gate Voltage Range ($V_{G1,2}$)	−7 to +2 V
Drain Voltage ($V_{D1,2}$)	+55 V
Peak RF Input Power	34 dBm
VSWR Mismatch, P1dB Pulse (20% Duty Cycle, 100 µs Width), T = +25°C	10:1
Storage Temperature	−65 to +150°C

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to device may reduce device reliability.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Peaker Gate Voltage (V_{G2})		−4.5		V
Drain Voltage ($V_{D1,2}$)		+48		V
Carrier Quiescent Current (I_{DQ1})		40		mA

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Doherty Electrical Specifications

Parameter	Conditions	Min	Typ	Max	Units
Frequency Range		2500		2700	MHz
Quiescent Drain Current (Carrier)			40		mA
Doherty Gain	P_{AVG} = 38.8 dBm	12.8	14.8		dB
Doherty Peak Power	10 dB PAR, 20 MHz LTE	46.2	47.3		dBm
Doherty Drain Efficiency	P_{AVG} = 38.8 dBm	52	59		%
Carrier Amplifier Gate Leakage (I_{G1})	V_{G1} = −7 V, V_{D1} = +48 V	-1.5			mA
Peaking Amplifier Gate Leakage (I_{G2})	V_{G2} = −7 V, V_{D2} = +48 V	-3.0			mA

Test conditions unless otherwise noted: V_D = 48V, I_{DQ1} = 40 mA, V_{G2} = -4.5V, T = +25°C, using an 8 dB PAR, 20 MHz LTE signal at 2600 MHz on a 2500 – 2700 MHz reference fixture

Thermal Information

Parameter	Conditions	Values	Units
Thermal Resistance, Peak IR Surface Temperature at Average Power (θ_{JC})	T_{CASE} = +85°C, T_{CH} = 115°C CW: P_{DISS} = 3.82 W, P_{OUT} = 7.6 W	6.6	°C/W

Notes:

1. Based on expected carrier amplifier efficiency of Doherty.
2. P_{OUT} assumes 20% peaking amplifier contribution of total average Doherty rated power.
3. Thermal resistance is measured to package backside.
4. Refer to the following document: GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates

Carrier Amplifier Power-Matched Load Pull Performance

Frequency (MHz)	Source Impedance (Ω)	Load Impedance (Ω)	P3dB (dBm)	Drain Efficiency (%)	G3dB (dB)
2500	19.2 - j48.6	30.4 + j14.7	42.7	68.3	17.1
2600	19.3 - j51.7	27.8 + j8.3	42.7	64.7	17.1
2700	18.0 - j46.4	22.4 + j5.8	42.8	63.2	17.0

Test conditions unless otherwise noted: V_{D1} = +48 V, I_{DQ1} = 32.5 mA, T = +25°C, Pulsed (10% Duty Cycle, 100 µs Width), P3dB.

Carrier Amplifier Efficiency-Matched Load Pull Performance

Frequency (MHz)	Source Impedance (Ω)	Load Impedance (Ω)	P3dB (dBm)	Drain Efficiency (%)	G3dB (dB)
2500	19.2 - j48.6	17.5 + j27.4	41.1	77.9	19.2
2600	19.3 - j51.7	17.4 + j27.4	40.8	78.4	19.2
2700	18.0 - j46.4	17.7 + j22.9	41.1	76.9	18.6

Test conditions unless otherwise noted: V_{D1} = +48 V, I_{DQ1} = 32.5 mA, T = +25°C, Pulsed (10% Duty Cycle, 100 µs Width), P3dB.

Peaking Amplifier Power-Matched Load Pull Performance

Frequency (MHz)	Source Impedance (Ω)	Load Impedance (Ω)	P3dB (dBm)	Drain Efficiency (%)	G3dB (dB)
2500	19.0 - j47.6	13.9 - j3.1	46.3	61.4	18.1
2600	32.2 - j19.9	13.9 - j3.1	46.3	63.9	18.2
2700	16.7 - j12.5	10.7 - j6.1	46.2	57.8	17.5

Test conditions unless otherwise noted: V_{D2} = +48 V, I_{DQ2} = 81 mA, T = +25°C, Pulsed (10% Duty Cycle, 100 µs Width), P3dB.

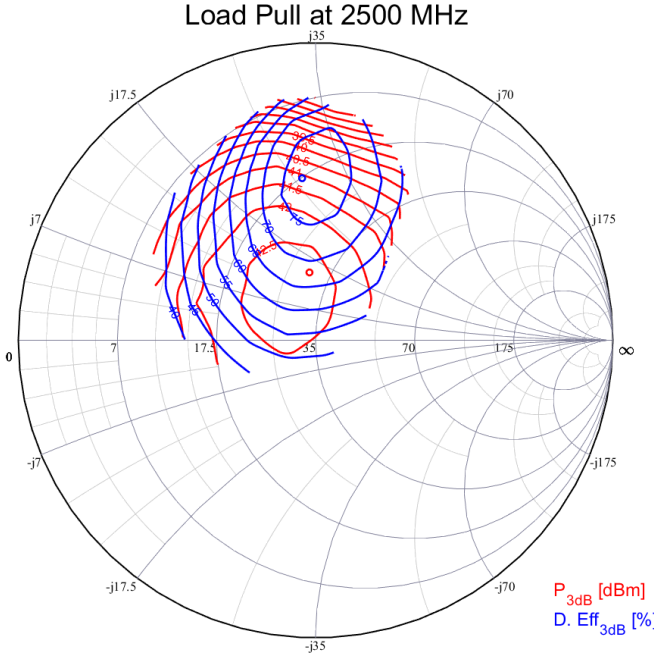
Peaking Amplifier Efficiency-Matched Load Pull Performance

Frequency (MHz)	Source Impedance (Ω)	Load Impedance (Ω)	P3dB (dBm)	Drain Efficiency (%)	G3dB (dB)
2500	19.0 - j47.6	11.0 + j7.7	44.6	77.6	20.5
2600	32.2 - j19.9	7.0 + j8.4	43.0	78.5	21.3
2700	16.7 - j12.5	10.4 + j5.4	44.5	77.6	20.0

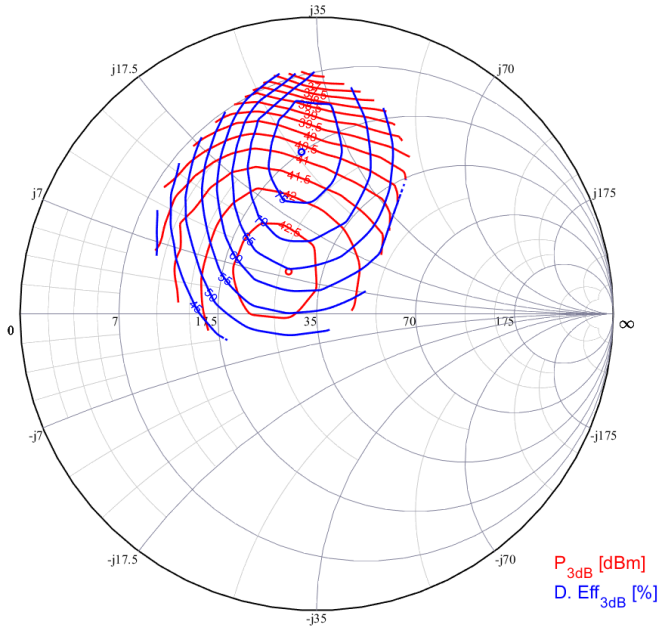
Test conditions unless otherwise noted: V_{D2} = +48 V, I_{DQ2} = 81 mA, T = +25°C, Pulsed (10% Duty Cycle, 100 µs Width), P3dB.

Carrier Amplifier Load Pull Plots

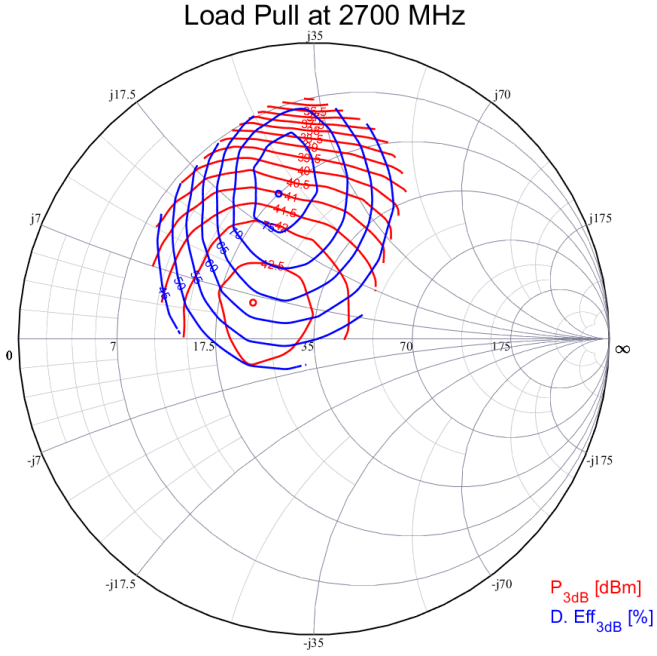
Load Pull at 2500 MHz



Load Pull at 2600 MHz



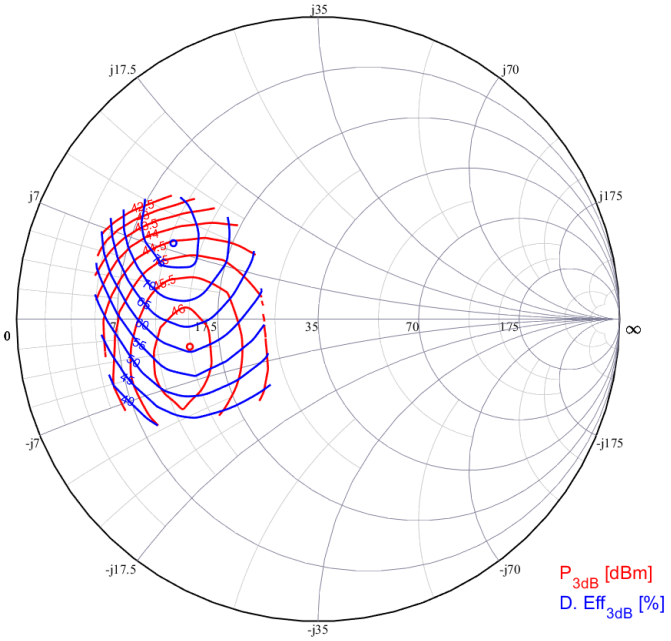
Load Pull at 2700 MHz



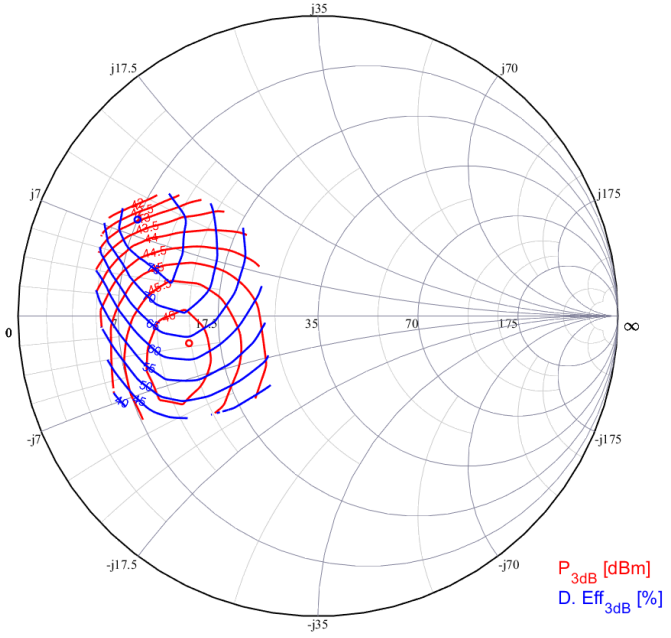
Test conditions unless otherwise noted: V_{D1} = +48 V, I_{DQ1} = 32.5 mA, T = +25°C, Pulsed (10% Duty Cycle, 100 µs Width), P3dB.

Peaking Amplifier Load Pull Plots

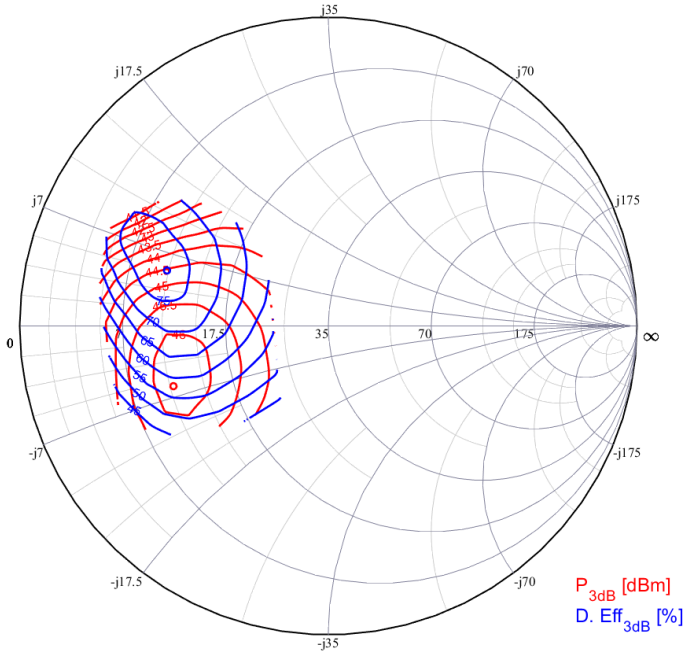
Load Pull at 2500 MHz



Load Pull at 2600 MHz



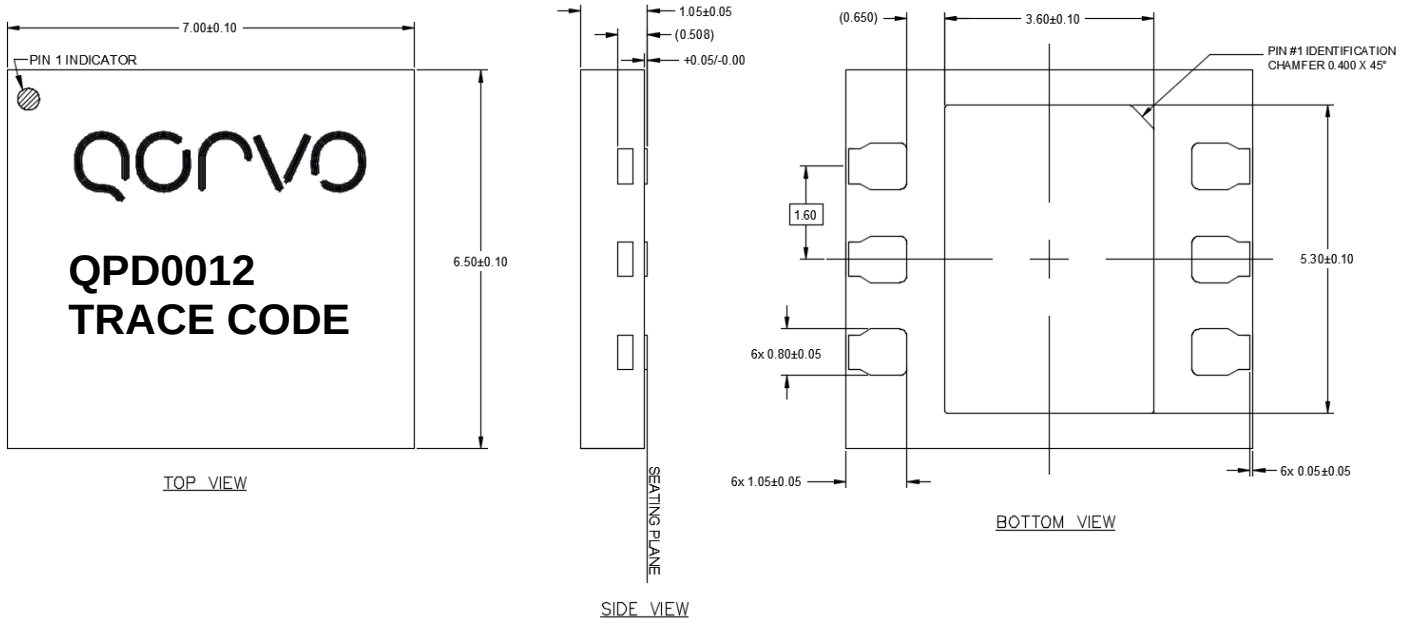
Load Pull at 2700 MHz



Test conditions unless otherwise noted: V_{D2} = +48 V, I_{DQ2} = 81 mA, T = +25°C, Pulsed (10% Duty Cycle, 100 µs Width), P3dB.

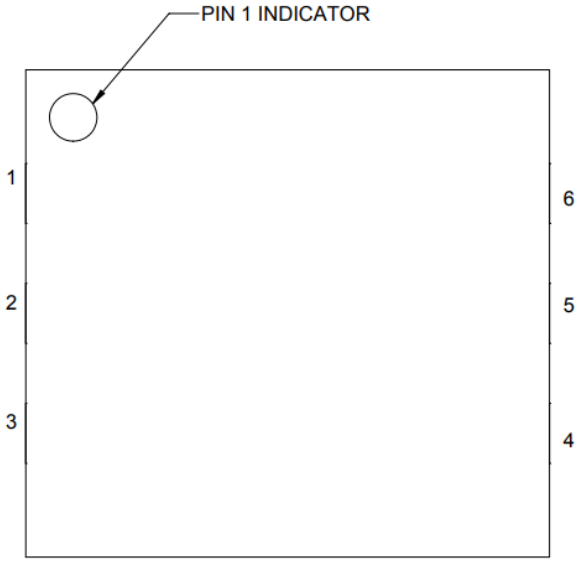
Package Marking and Dimensions

Marking: Qorvo Logo
Part Number – QPD0012
Trace Code – To be assigned by subcontractor

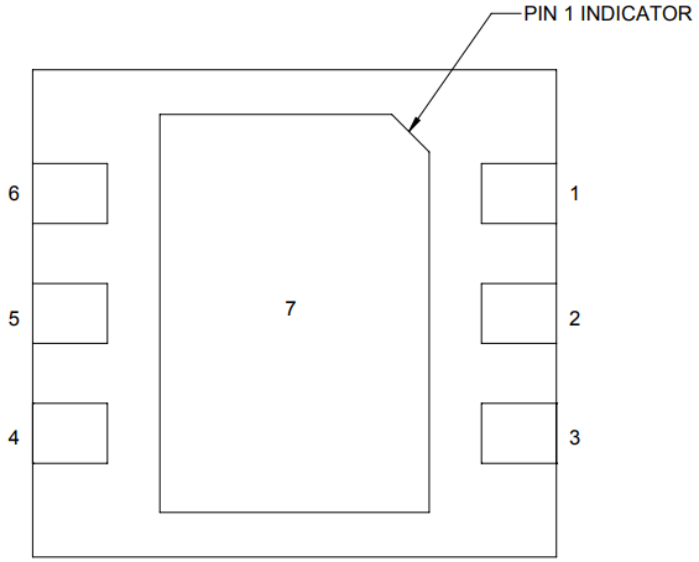


Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. Part is overmold encapsulated.
3. Contact plating is NiPdAu. Au thickness is 0.00254 to 0.01501 µm.

Pin Configuration and Description



Top View



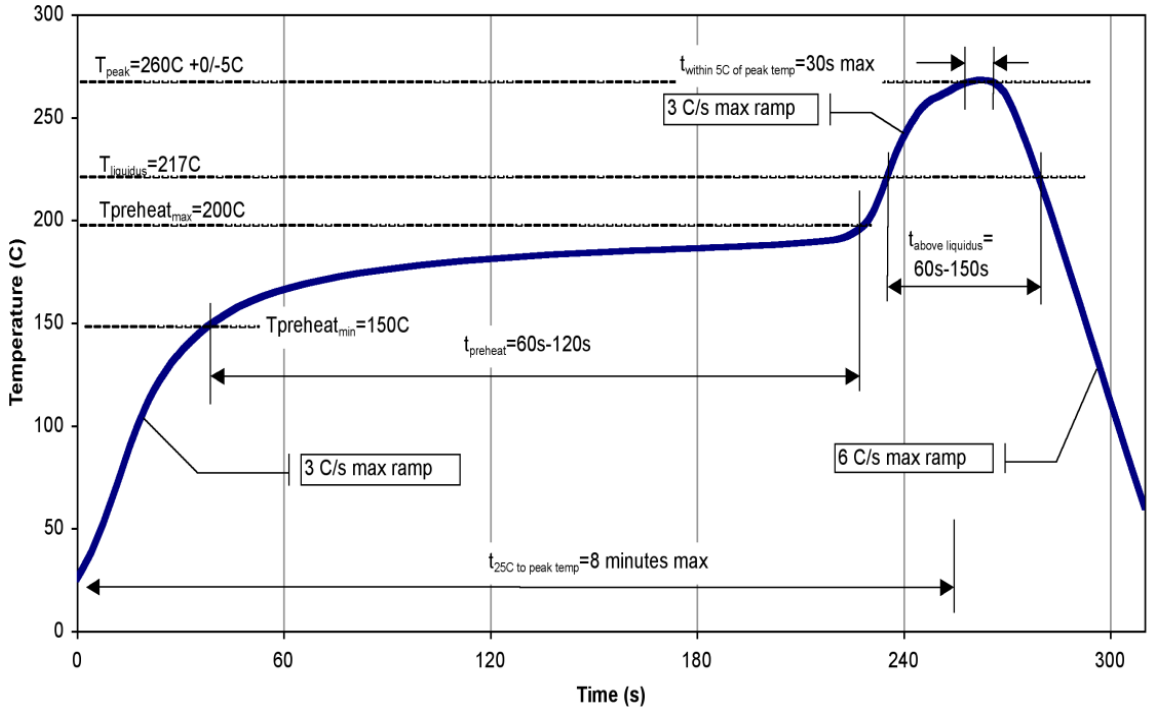
Bottom View

Pin Number	Label	Description
1	RF IN 1, V_{G1}	RF Input, Gate Bias
2	NC	No Connect
3	RF IN 2, V_{G2}	RF Input, Gate Bias
4	RF OUT 2, V_{D2}	RF Output, Drain Bias
5	NC	No Connect
6	RF OUT 1, V_{D1}	RF Output, Drain Bias
7 (Backside Paddle)	GND	Ground

Doherty Biasing Procedure

Bias On	Bias Off
1. Turn ON V_{G1} to −5 V. 2. Turn ON V_{G2} to −5 V. 3. Turn ON V_{D1} and V_{D2} to +48 V. 4. Slowly adjust V_{G1} until I_{D1} = 40 mA. 5. Set V_{G2} to −4.5 V. 6. Turn ON RF.	1. Turn OFF RF. 2. Adjust V_{G1} and V_{G2} to −5 V. 3. Turn OFF V_{D1} and V_{D2}. 4. Wait two (2) seconds to allow drain capacitors to discharge. 5. Turn OFF V_{G1} and V_{G2}.

Recommended Solder Temperature Profile



Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1B (500 V)	ANSI/ESDA/JEDEC Standard JS-001
ESD – Charged Device Model (CDM)	Class C3 (1000 V)	ANSI/ESDA/JEDEC Standard JS-002
MSL – Moisture Sensitivity Level	MSL 2	IPC/JEDEC Standard J-STD-020

Caution!
ESD-Sensitive Device

Solderability

Compatible with lead-free (260°C max. reflow temp.) soldering processes.

Package lead plating is NiPdAu. Au thickness is 0.00254 to 0.01501 µm.

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

Important Notice

The information contained herein is believed to be reliable; however, Qorvo makes no warranties regarding the information contained herein and assumes no responsibility or liability whatsoever for the use of the information contained herein. All information contained herein is subject to change without notice. Customers should obtain and verify the latest relevant information before placing orders for Qorvo products. The information contained herein or any use of such information does not grant, explicitly or implicitly, to any party any patent rights, licenses, or any other intellectual property rights, whether with regard to such information itself or anything described by such information. **THIS INFORMATION DOES NOT CONSTITUTE A WARRANTY WITH RESPECT TO THE PRODUCTS DESCRIBED HEREIN, AND QORVO HEREBY DISCLAIMS ANY AND ALL WARRANTIES WITH RESPECT TO SUCH PRODUCTS WHETHER EXPRESS OR IMPLIED BY LAW, COURSE OF DEALING, COURSE OF PERFORMANCE, USAGE OF TRADE OR OTHERWISE, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.**

Without limiting the generality of the foregoing, Qorvo products are not warranted or authorized for use as critical components in medical, life-saving, or life-sustaining applications, or other applications where a failure would reasonably be expected to cause severe personal injury or death.