QPA2640D

20 – 40 GHz 8 Watt GaN Power Amplifier

Product Overview

Qorvo's QPA2640D is a high power MMIC amplifier fabricated on Qorvo's production 0.15 um GaN on SiC process (QGaN15). The QPA2640D operates from 18 – 40 GHz, provides 8 W of saturated output power with 12 dB of large signal gain and 12% power–added efficiency. The operating frequency can extend to 18 – 40 GHz if desired.

To simplify system integration, the QPA2640D is fully matched to 50 ohms with integrated DC blocking caps on both I/O ports.

The QPA2640D is ideal for supporting communications and radar applications in both commercial and military markets.

The QPA2640D is 100% DC and RF tested on-wafer to ensure compliance to electrical specifications.

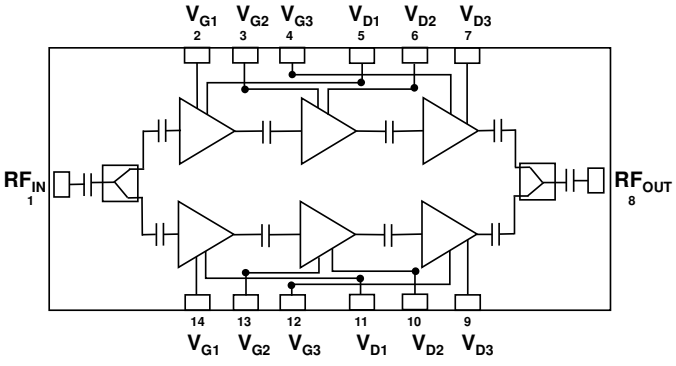
Lead-free and RoHS compliant

Key Features

- Frequency Range: 20 – 40 GHz
- Extended Frequency Range: 18 – 40 GHz
- P_{SAT} (P_{IN} = 27 dBm): 39 dBm
- PAE (P_{IN} = 27 dBm): 12 %
- Power Gain (P_{IN} = 27 dBm): 12 dB
- Small Signal Gain: 20 dB
- Return Losses: > 7 dB
- Bias: V_D = 18 V, I_{DQ} = 2040 mA, V_G ≈ -2.3 V typ.
- Die Dimensions: 5.87 x 3.50 x 0.05 mm

Performance is typical across frequency. Please reference electrical specification table and data plots for more details.

Functional Block Diagram



Applications

- Communications
- Radar
- Point-to-Point Radio
- Electronic Warfare

Ordering Information

Part No.	Description
QPA2640D	8 Watt GaN Amplifier
QPA2640DEVB01	Evaluation Board for QPA2640D

Absolute Maximum Ratings

Parameter	Value / Range
Drain Voltage (V_D)	29.5 V
Gate Voltage Range (V_G)	-4 V to 0 V
Drain Current, stage 1 (I_{D1})	1440 mA
Drain Current, stage 2 (I_{D2})	2030 mA
Drain Current, stage 3 (I_{D3})	3200 mA
Drain Current, total (I_D)	6670 mA
Gate Current (I_G)	See chart p. 17
Power Dissipation (P_{DISS}), T_{BASE} = 85 °C	74 W
Input Power (P_{IN}), 50 Ω, CW, V_D = 18 V, I_D = 2040 mA, T_{BASE} = 85 °C	33 dBm
Input Power (P_{IN}), 3:1 VSWR, CW, V_D = 18 V, I_D = 2040 mA, T_{BASE} = 85 °C	33 dBm
Mounting Temperature (30 seconds)	320 ºC
Storage Temperature	-55 to +150 ºC

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating Conditions

Parameter	Min	Typ.	Max	Units
Drain Voltage (V_D)		18	20	V
Drain Current, Quiescent (I_D)		2040		mA
Drain Current, RF (I_{D_Drive})	See charts p. 6, 10, 13, 16			mA
Gate Voltage Typ. Range (V_G)	–1.7 to -2.9			V
Gate Current, RF (I_{G_Drive})	See charts p. 6			mA
Input Power @ Saturation, (P_{IN})	T_{BASE} -40 °C: 27			dBm
	T_{BASE} +25 °C: 27			
	T_{BASE} +85 °C: 30			
Operating Temp. Range (T_{BASE} 1/)	–40		+85	ºC

1/ T_{BASE} is back side of 20 mil CuMo carrier plate with AuSn die attached.

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Parameter	Conditions (1) (2)	Min	Typ.	Max	Units
Operational Frequency Range		20 (3)		40 (3)	GHz
Output Power at Saturation, P_{SAT}	P_{IN} = +27 dBm, Frequency = 20 – 40 GHz		39		dBm
	P_{IN} = +27 dBm, Frequency = 18 – 19 GHz (3)		38.5		
Power Added Efficiency, PAE	P_{IN} = +27 dBm		12		%
Large Signal Gain	P_{IN} = +27 dBm		12		dB
Small Signal Gain, S21			20		dB
Input Return Loss, IRL			> 7		dB
Output Return Loss, ORL			> 7		dB
P_{SAT} Temperature Coefficient	T_{DIFF} = –40 ºC to +85 ºC; P_{IN} = +27 dBm		-0.03		dBm/ºC
S21 Temperature Coefficient	T_{DIFF} = –40 ºC to +85 ºC		-0.10		dB/ºC

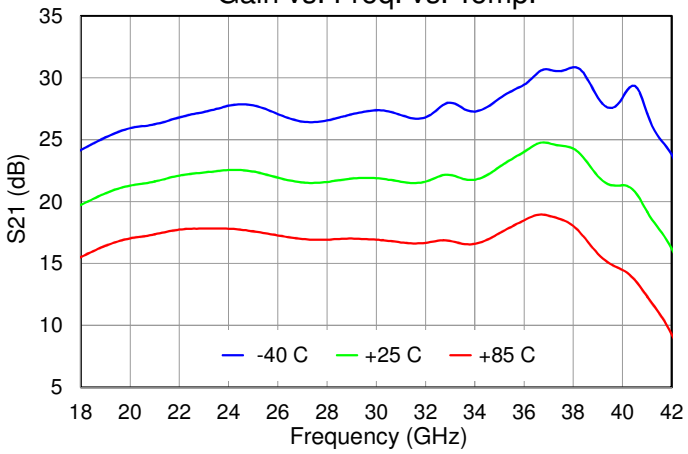
Notes:

1. Test conditions unless otherwise noted: CW, V_D = 18 V, I_D = 2040 mA, V_G = -2.3 V +/- 0.6V typical, T_{BASE} = +25ºC, Z_0 = 50 Ω
2. T_{BASE} is back side of 20 mil CuMo carrier plate with AuSn die attached
3. Extended frequency range: 18 – 40 GHz

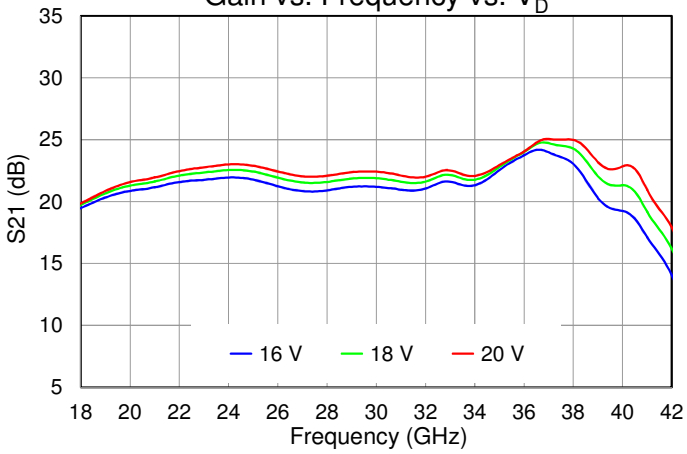
Performance Plots – Small Signal

Test conditions, unless otherwise noted: CW, V_D = 18 V, I_{DQ} = 2040 mA, T_{BASE} = 25 °C (T_{BASE} is backside of carrier plate)

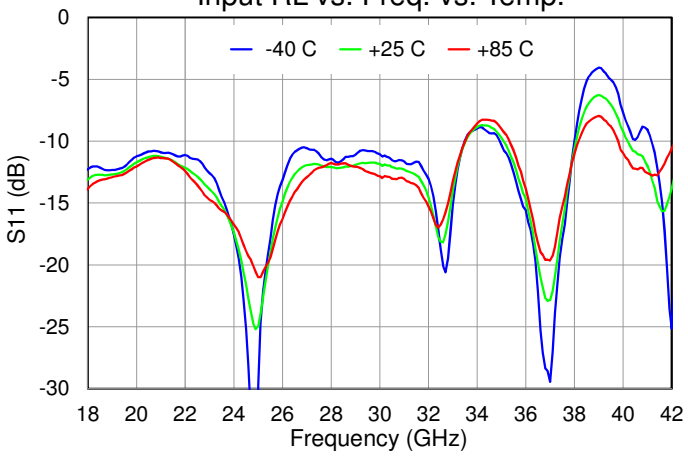
Gain vs. Freq. vs. Temp.



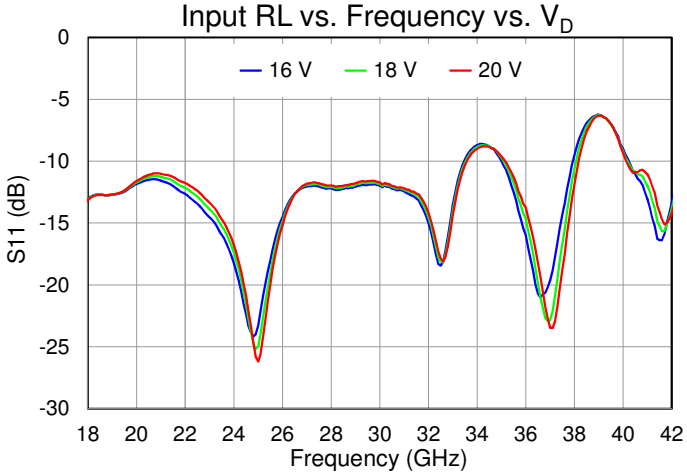
Gain vs. Frequency vs. V_D



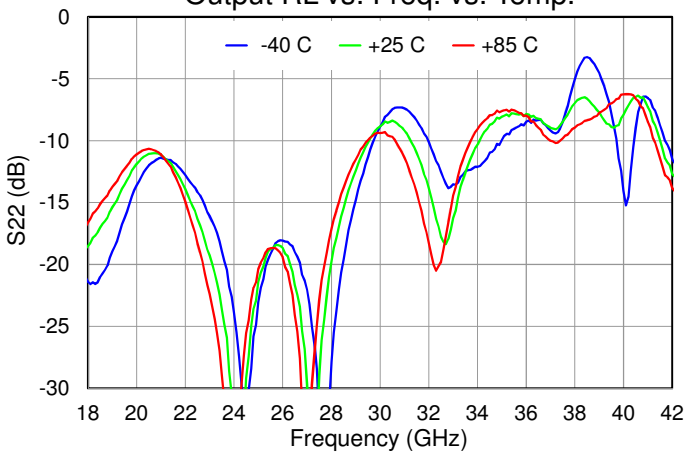
Input RL vs. Freq. vs. Temp.



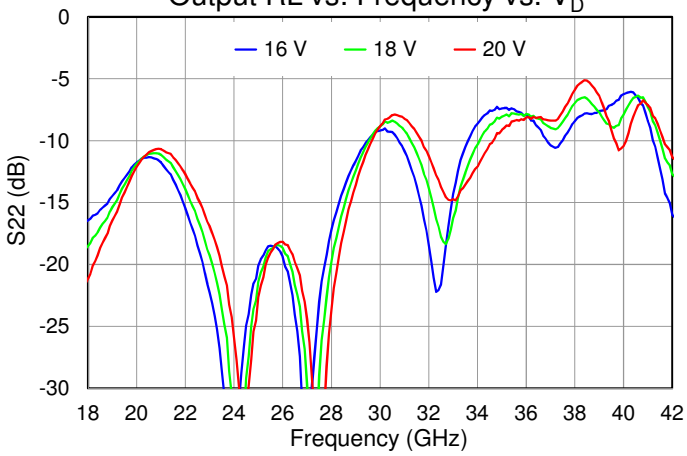
Input RL vs. Frequency vs. V_D



Output RL vs. Freq. vs. Temp.

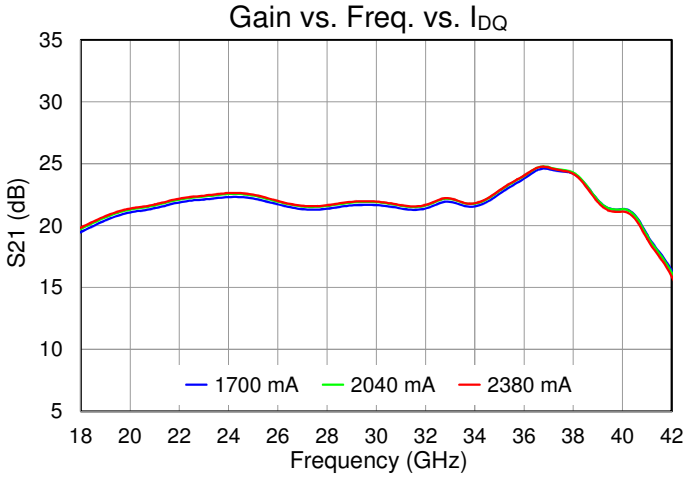


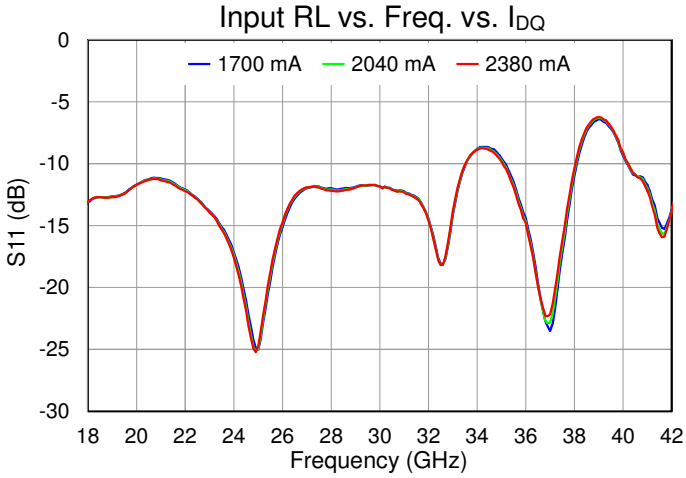
Output RL vs. Frequency vs. V_D

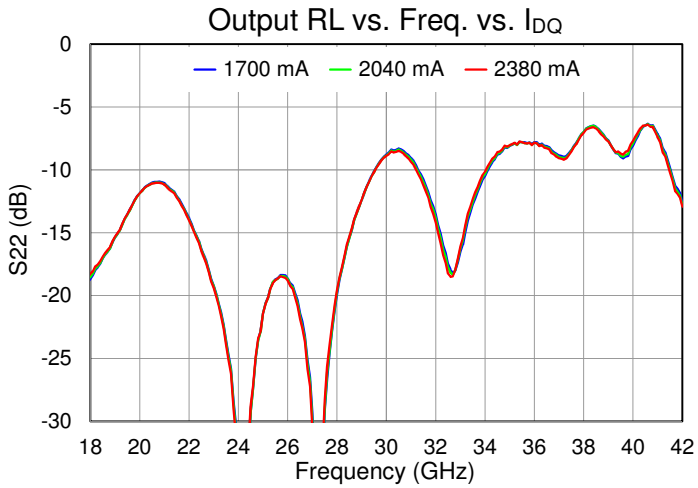


Performance Plots – Small Signal

Test conditions, unless otherwise noted: CW, V_D = 18 V, I_{DQ} = 2040 mA, T_{BASE} = 25 °C (T_{BASE} is backside of carrier plate)



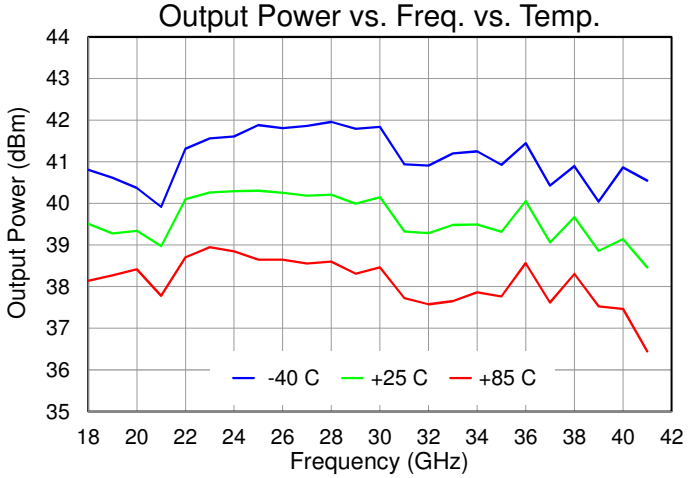




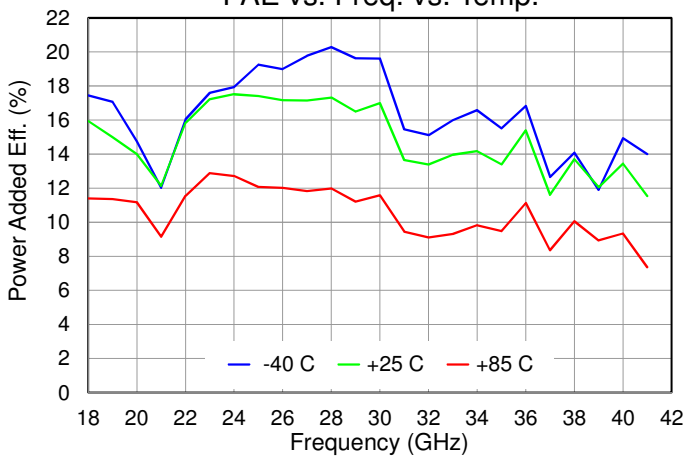
Performance Plots – Large Signal

Test conditions, unless otherwise noted: CW, V_D = 18 V, I_{DQ} = 2040 mA, P_{IN} = 27 dBm, T_{BASE} = 25 °C (T_{BASE} is backside of carrier plate)

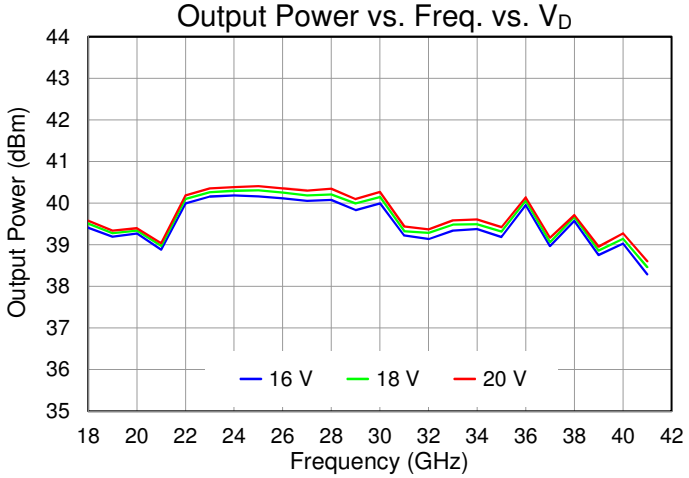
Output Power vs. Freq. vs. Temp.



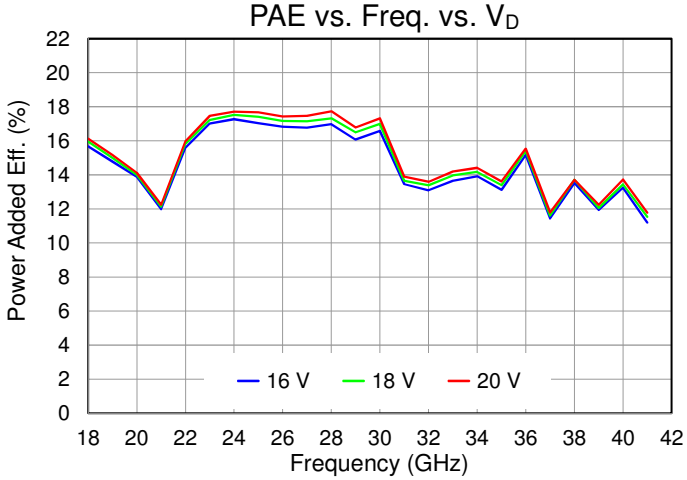
PAE vs. Freq. vs. Temp.



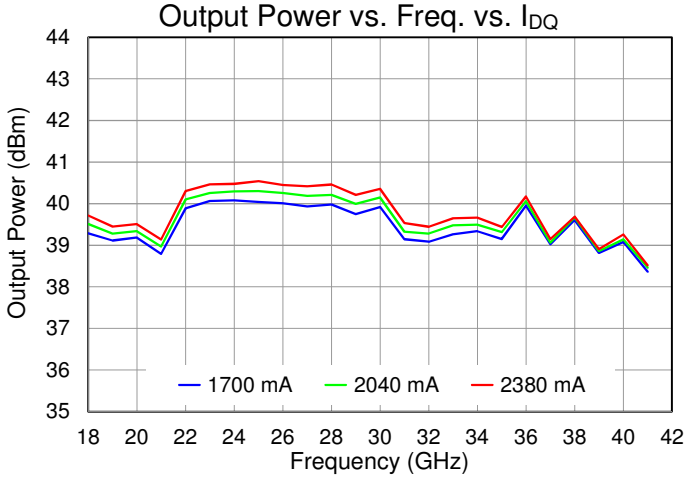
Output Power vs. Freq. vs. V_D



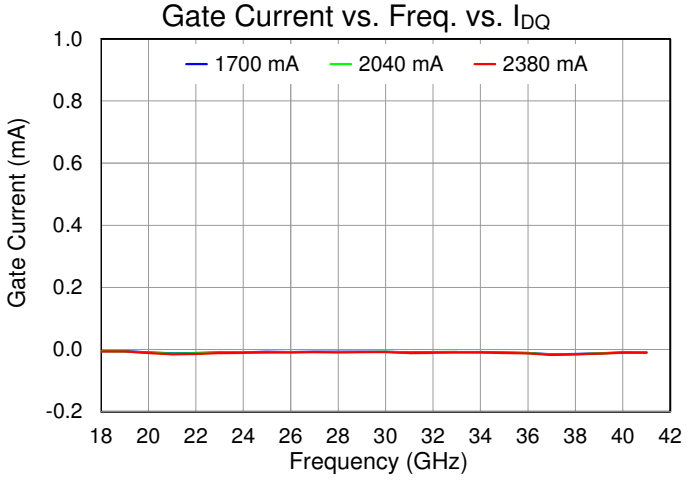
PAE vs. Freq. vs. V_D



Output Power vs. Freq. vs. I_{DQ}



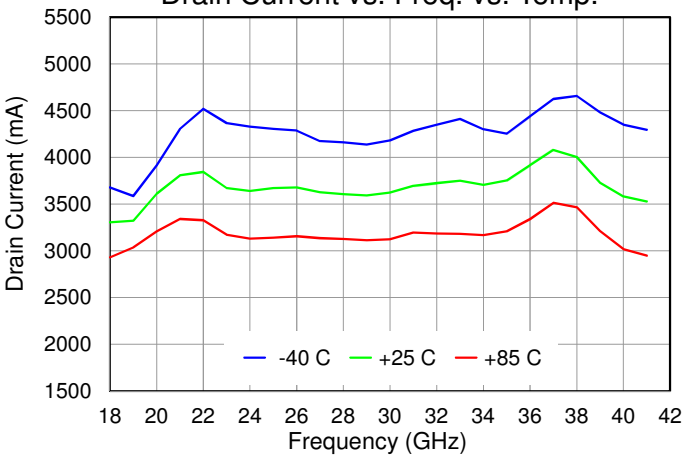
Gate Current vs. Freq. vs. I_{DQ}



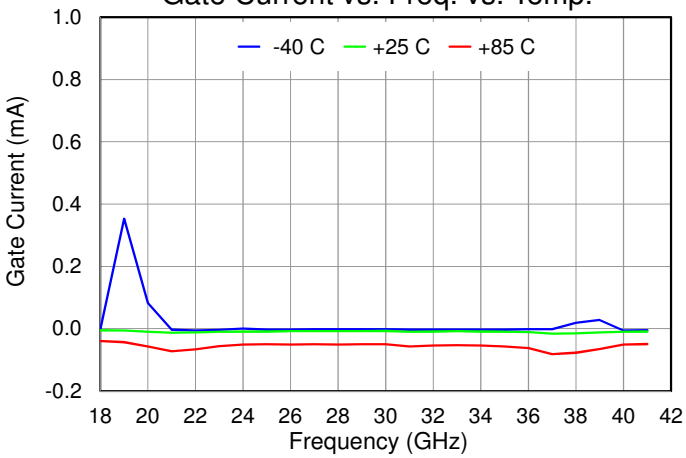
Performance Plots – Large Signal

Test conditions, unless otherwise noted: CW, V_D = 18 V, I_{DQ} = 2040 mA, P_{IN} = 27 dBm, T_{BASE} = 25 °C (T_{BASE} is backside of carrier plate)

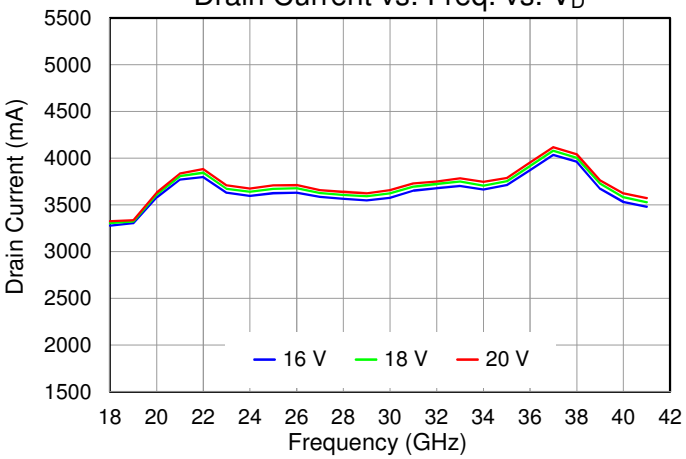
Drain Current vs. Freq. vs. Temp.



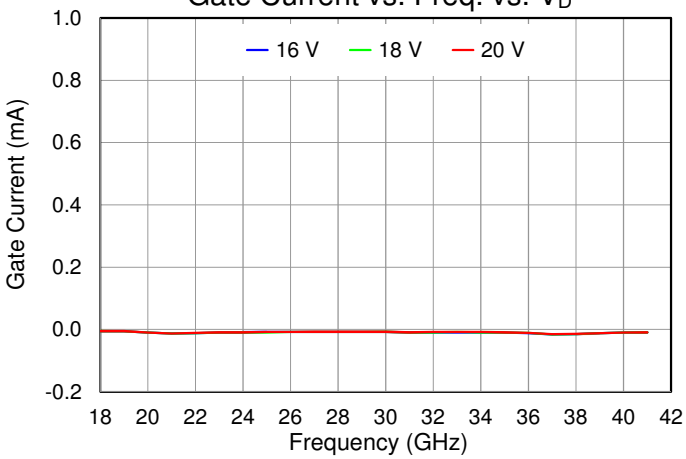
Gate Current vs. Freq. vs. Temp.



Drain Current vs. Freq. vs. V_D



Gate Current vs. Freq. vs. V_D



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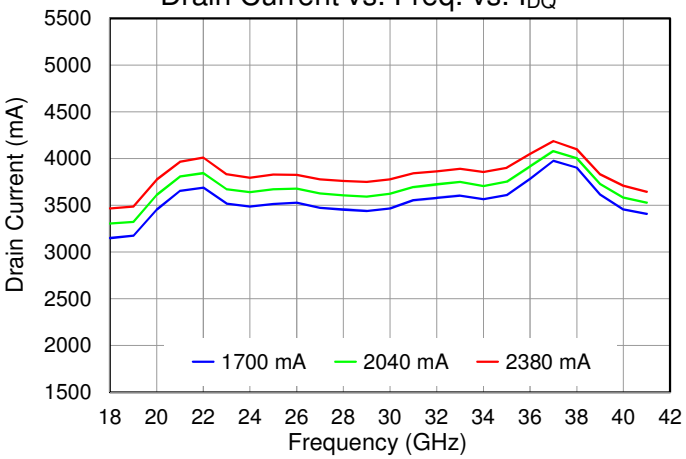

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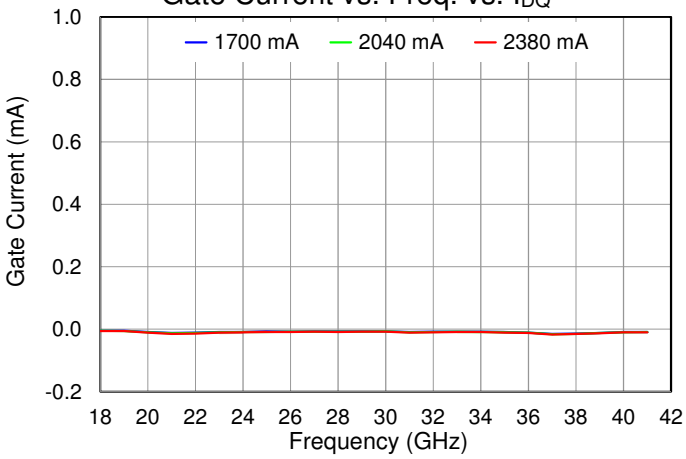

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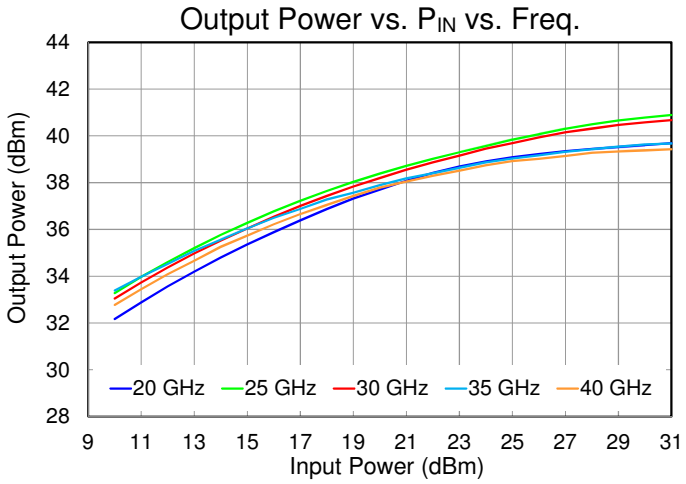

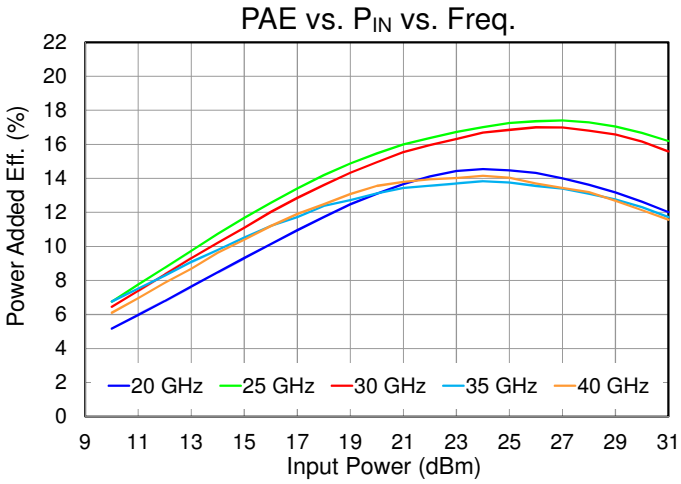

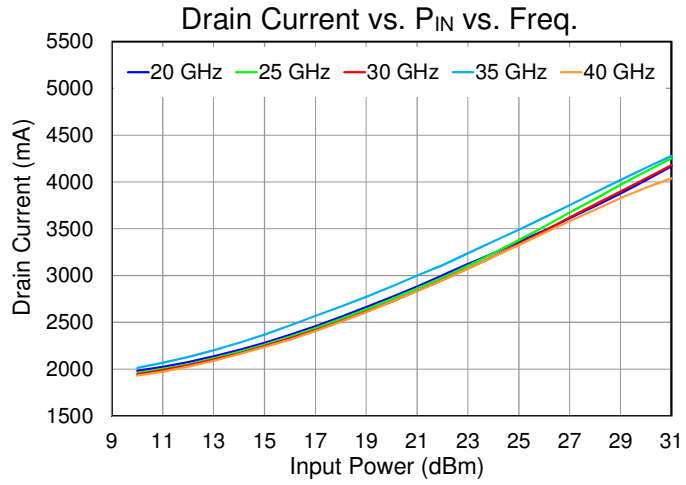

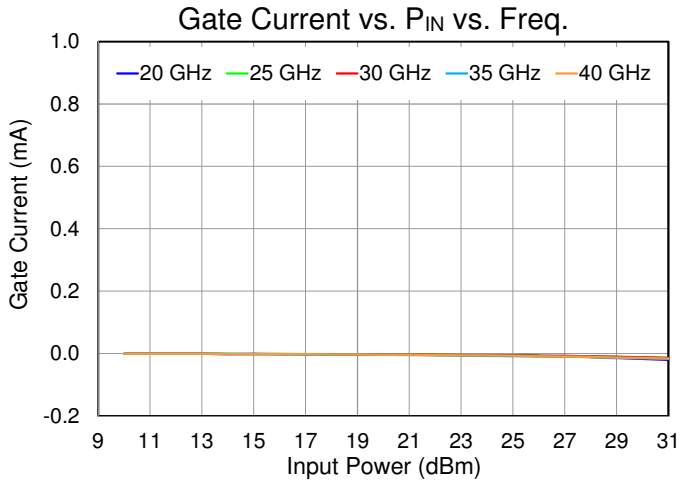

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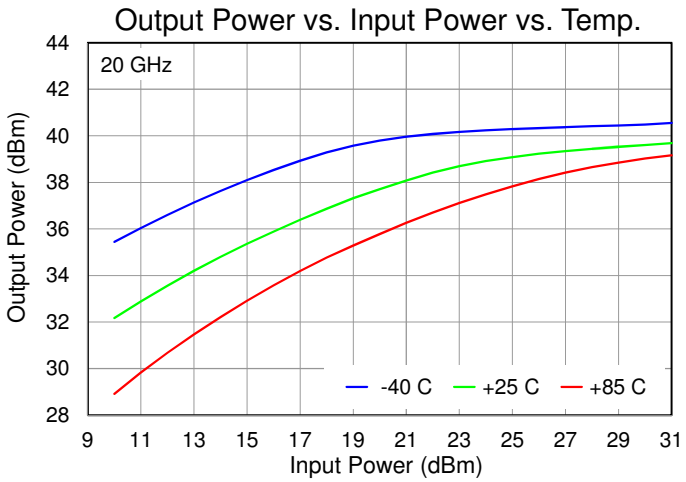

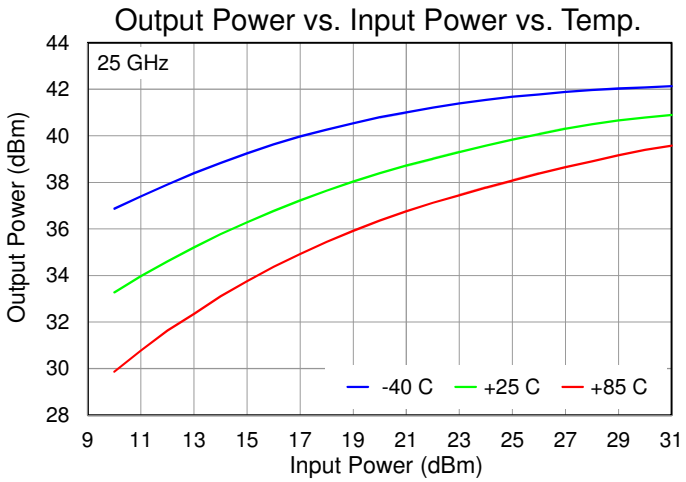

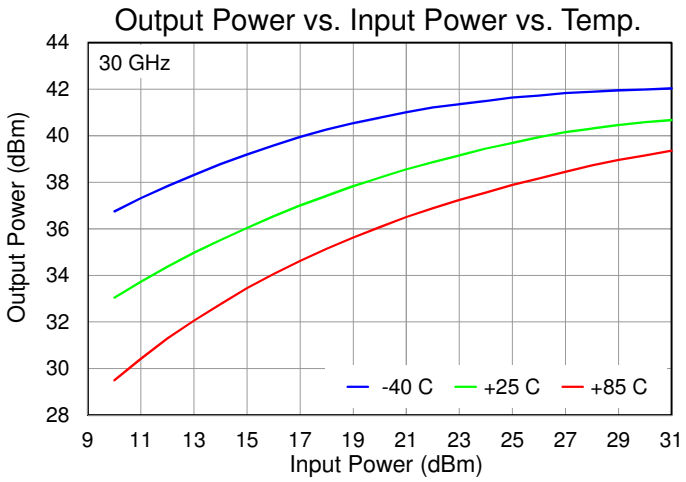

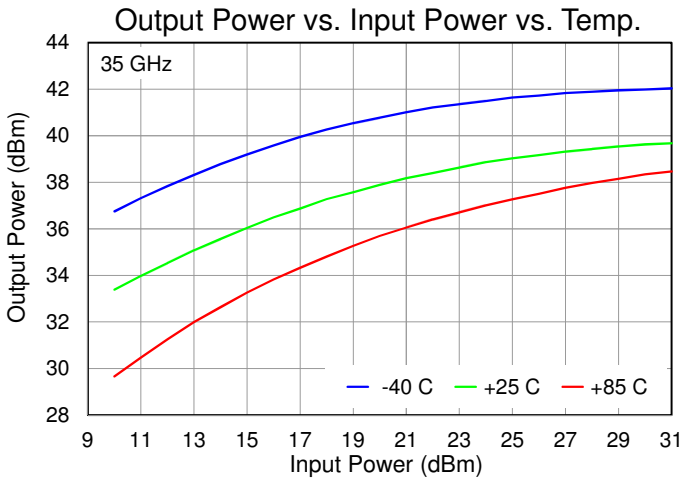

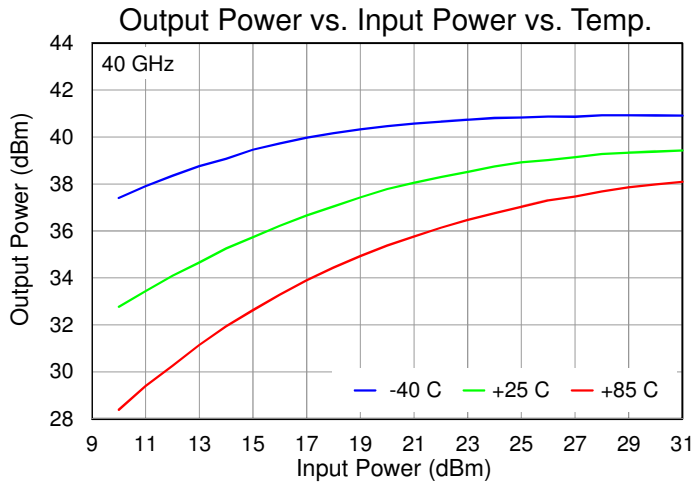

Performance Plots – Large Signal

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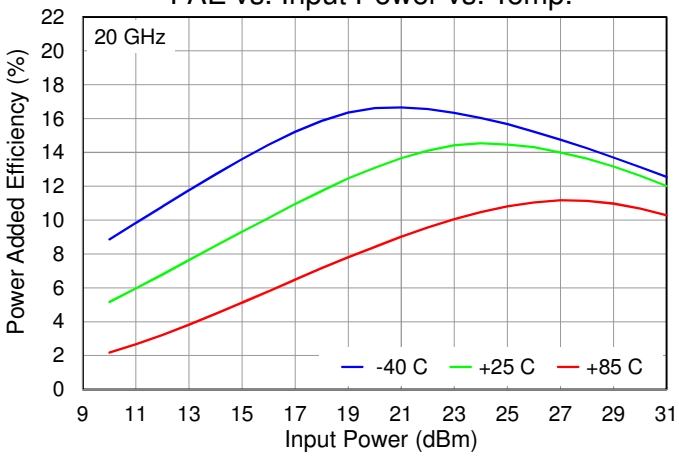
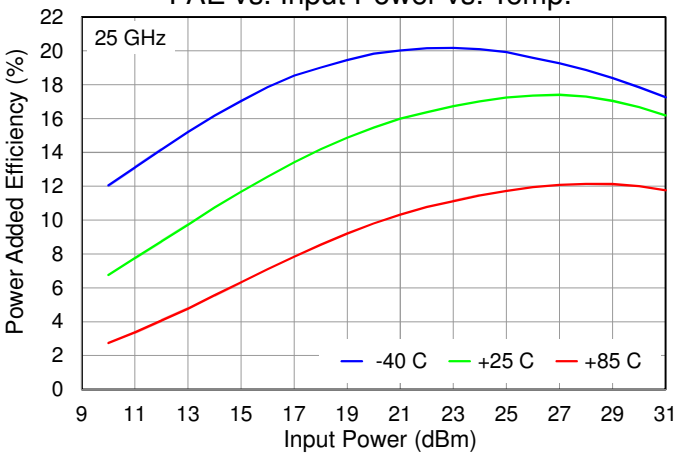
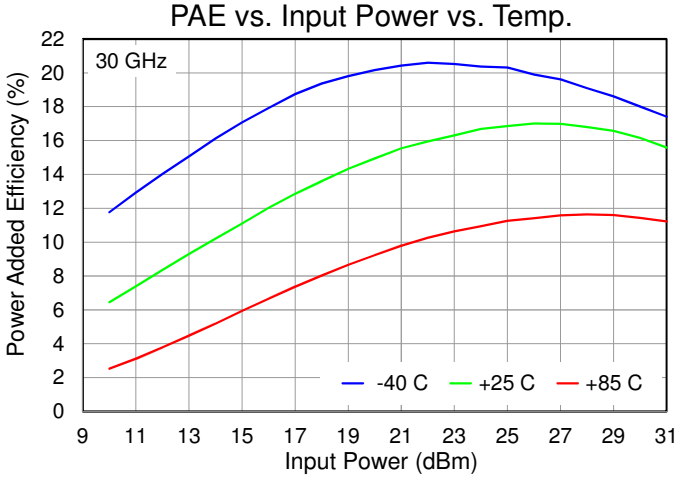
PAE vs. Input Power vs. Temp.



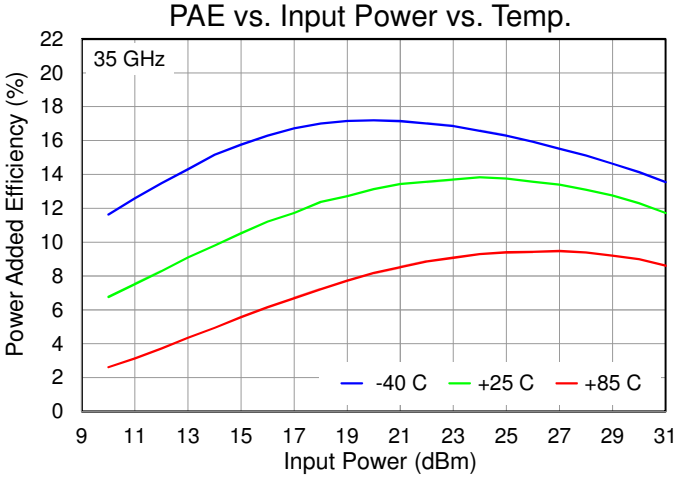
PAE vs. Input Power vs. Temp.



PAE vs. Input Power vs. Temp.



PAE vs. Input Power vs. Temp.



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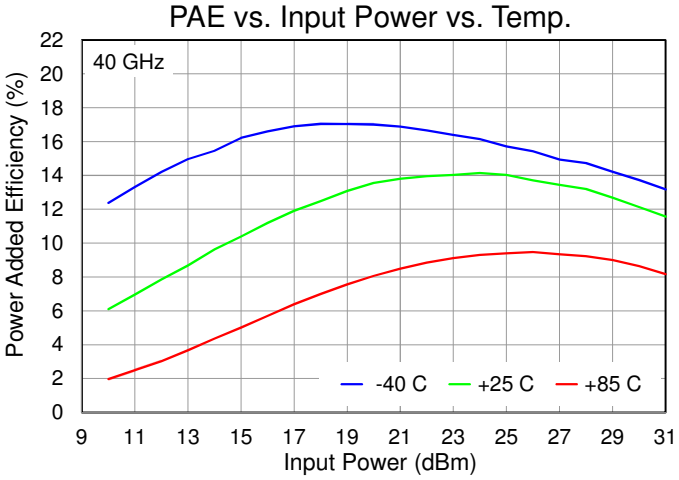

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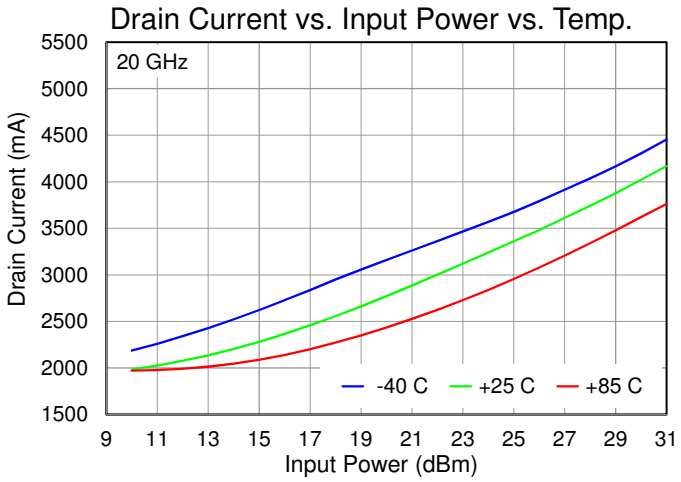

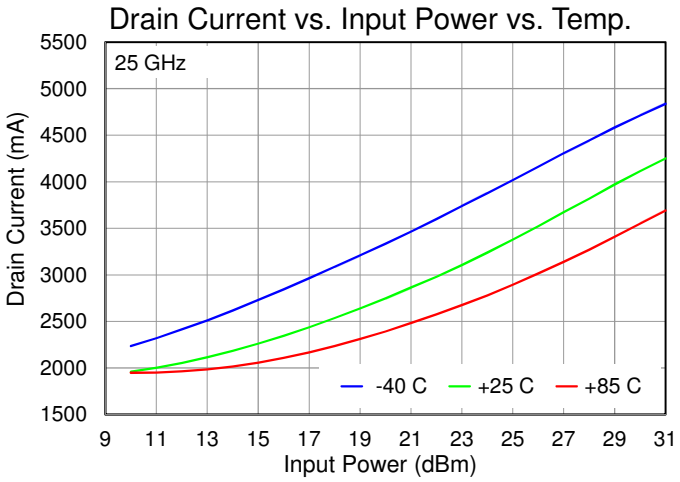

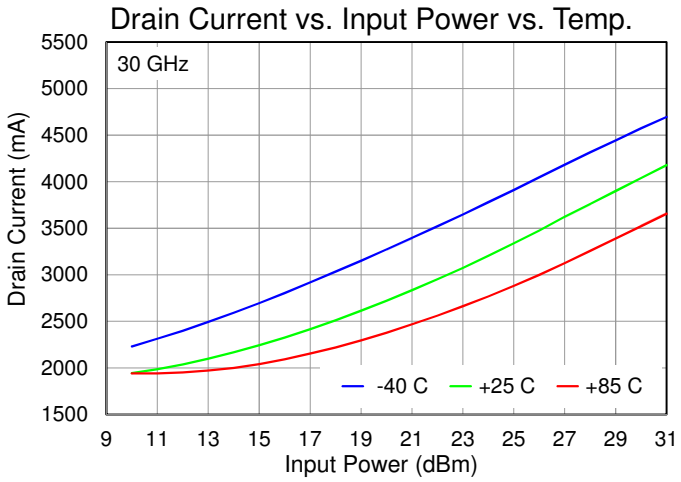

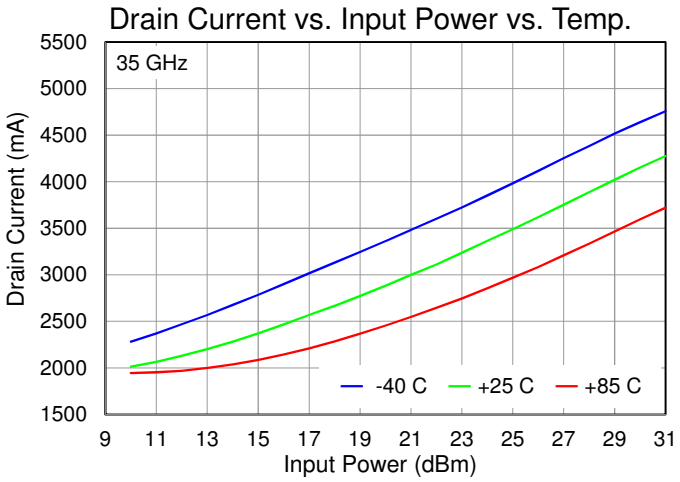

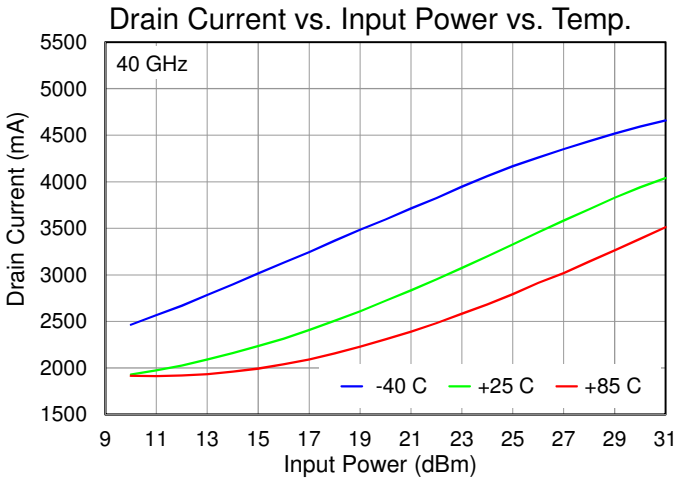

Performance Plots – Large Signal

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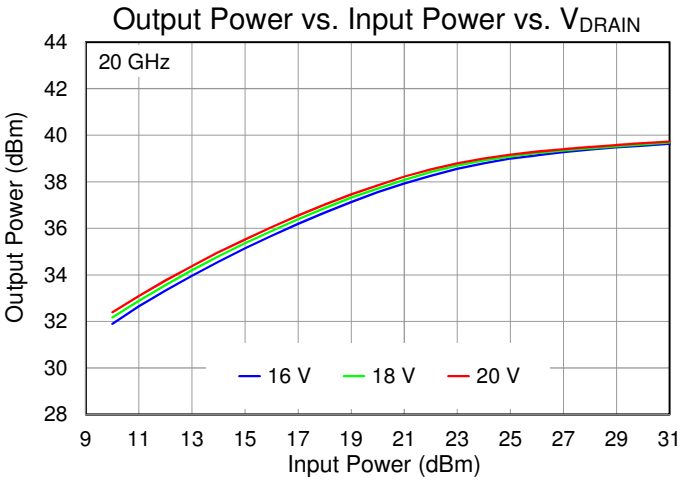
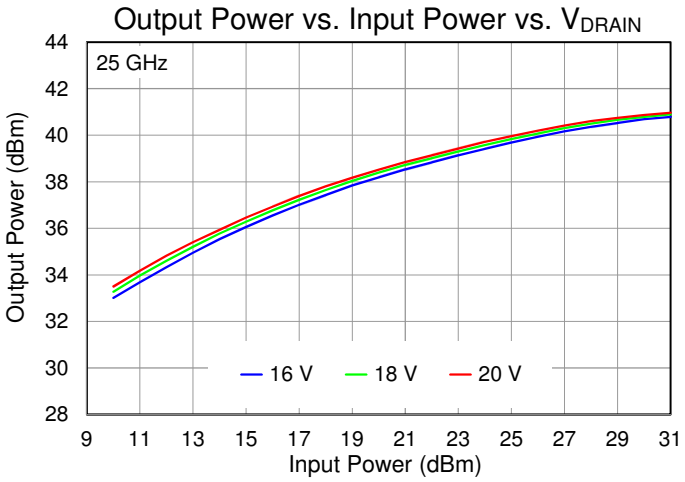
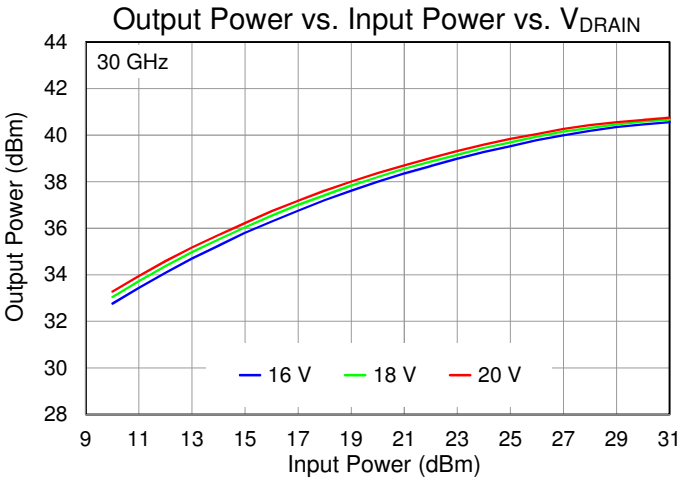
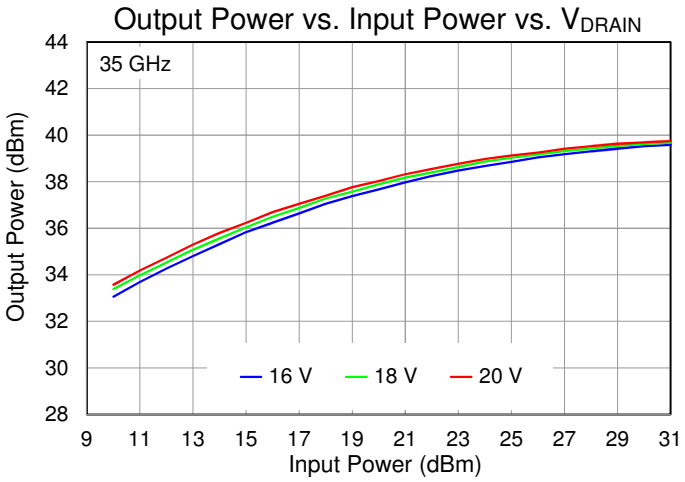
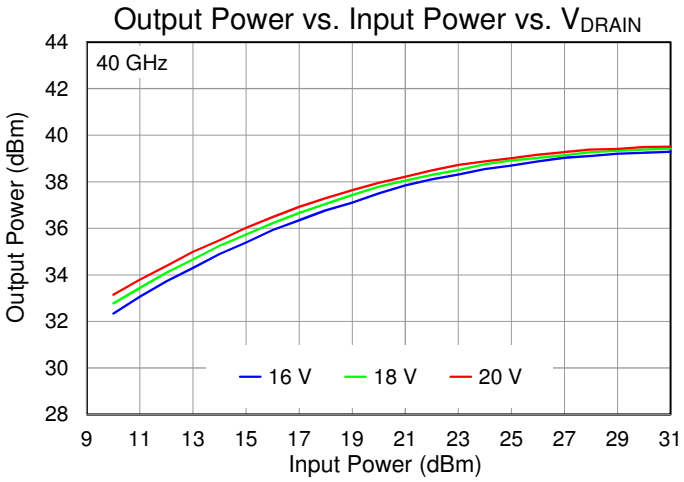






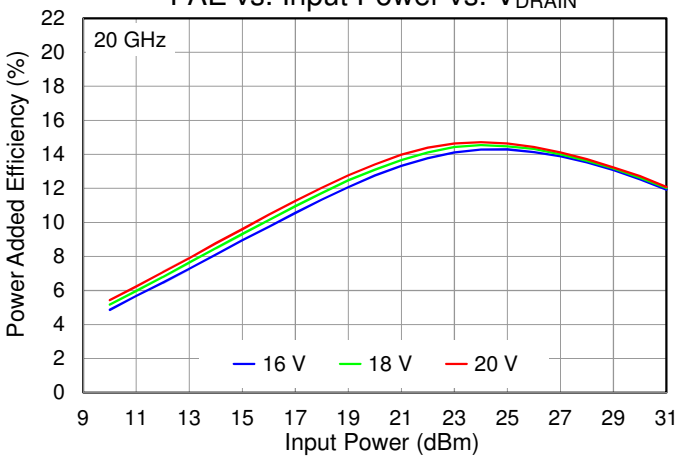




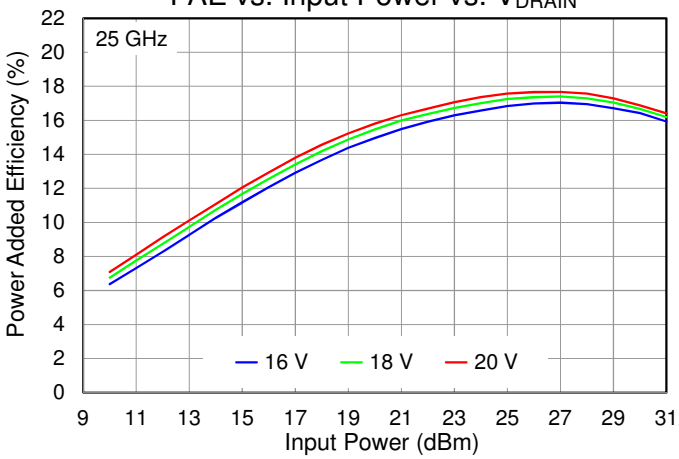
Performance Plots – Large Signal

Test conditions, unless otherwise noted: CW, V_D = 18 V, I_{DQ} = 2040 mA, P_{IN} = 27 dBm, T_{BASE} = 25 °C (T_{BASE} is backside of carrier plate)

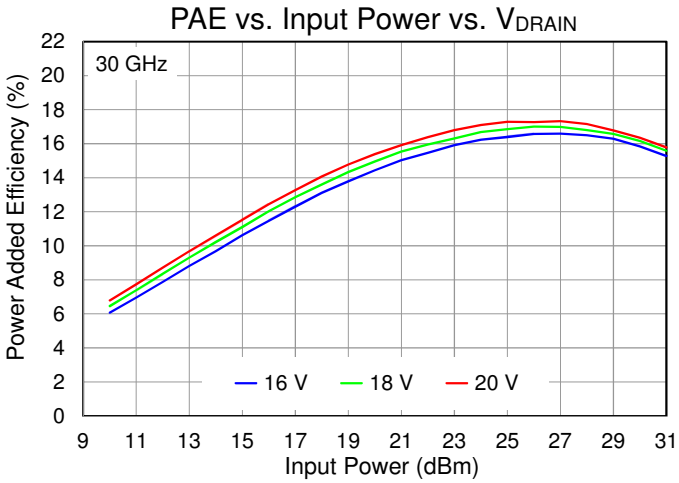
PAE vs. Input Power vs. V_{DRAIN}



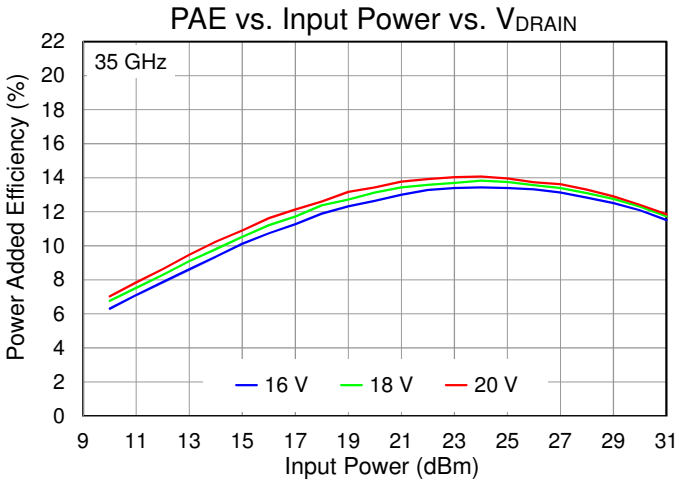
PAE vs. Input Power vs. V_{DRAIN}



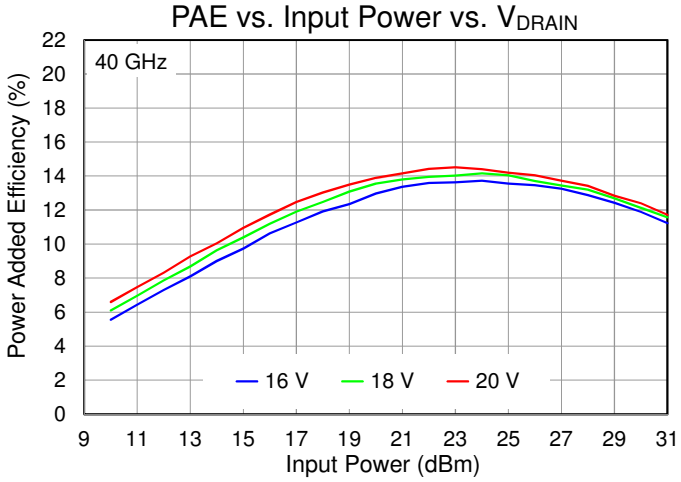
PAE vs. Input Power vs. V_{DRAIN}



PAE vs. Input Power vs. V_{DRAIN}



PAE vs. Input Power vs. V_{DRAIN}



Performance Plots – Large Signal

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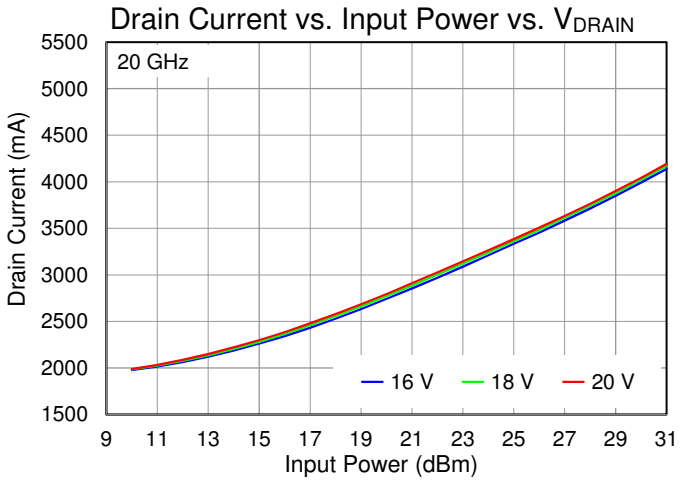
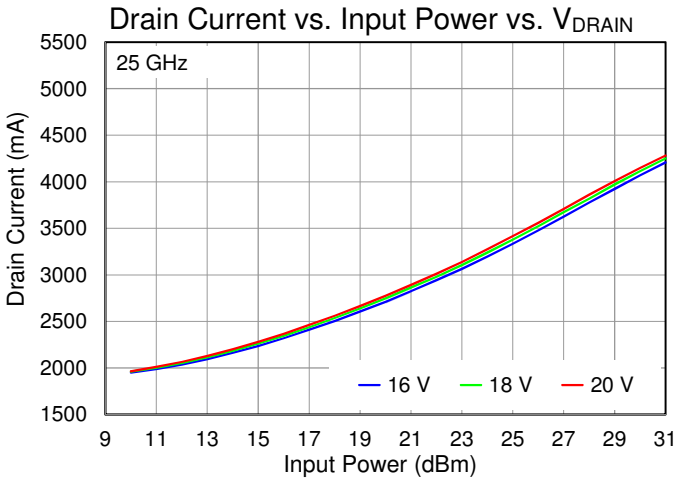
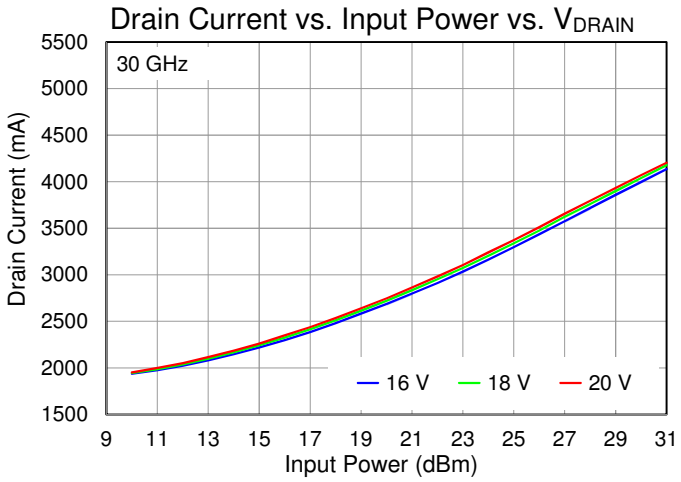
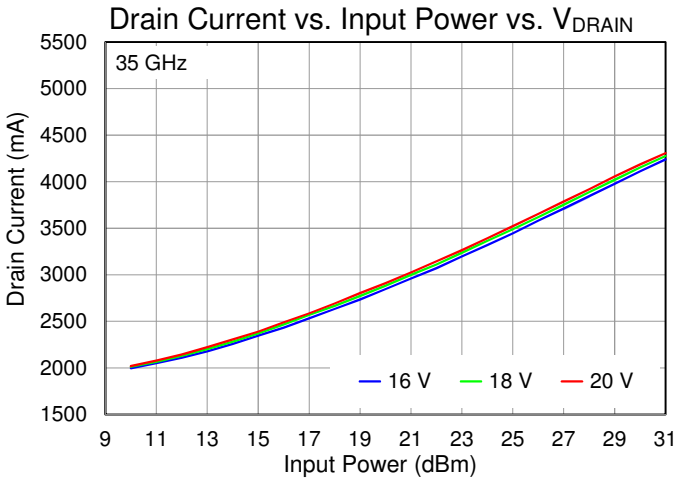
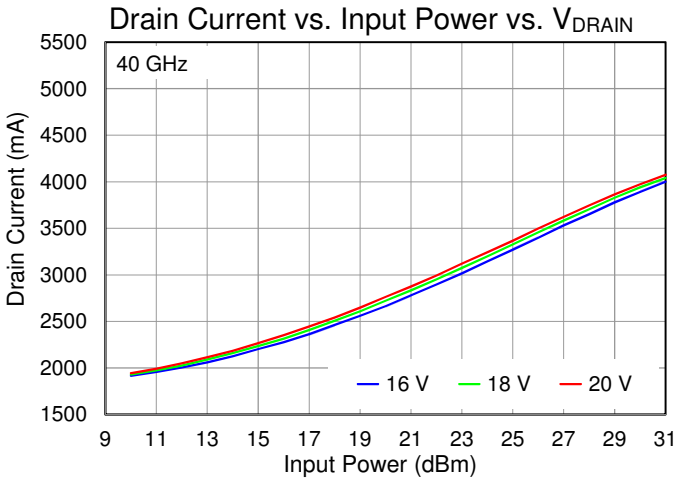




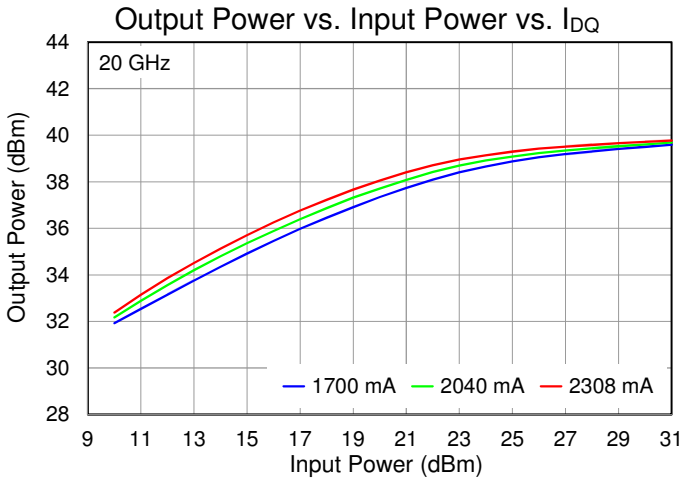


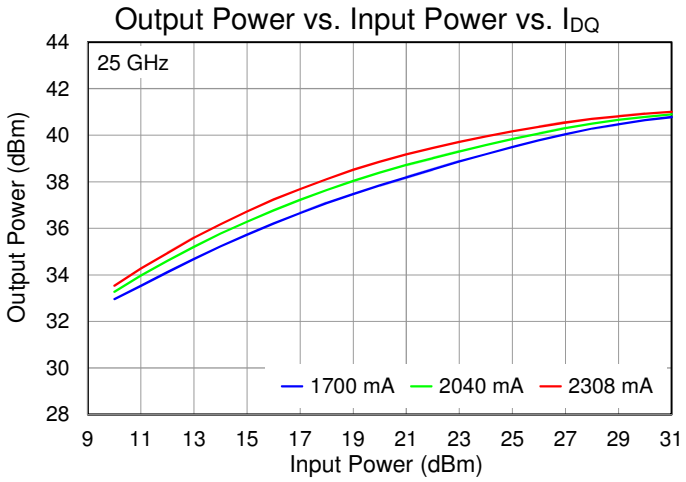


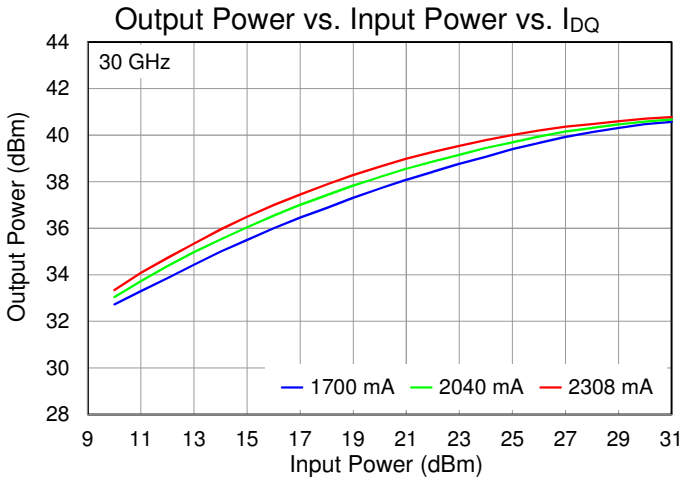


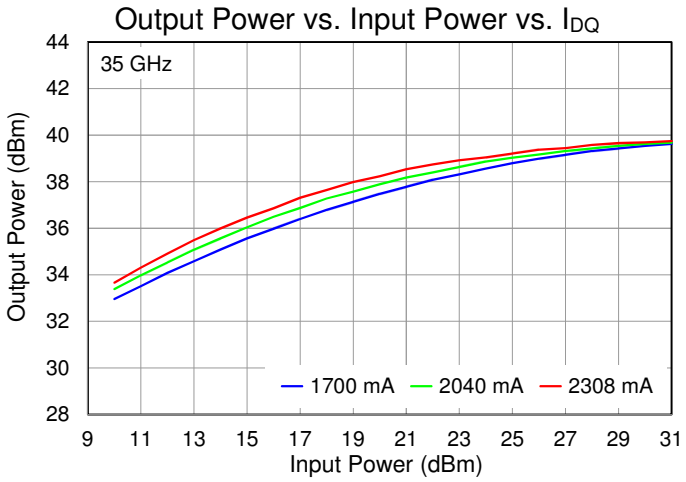
Performance Plots – Large Signal

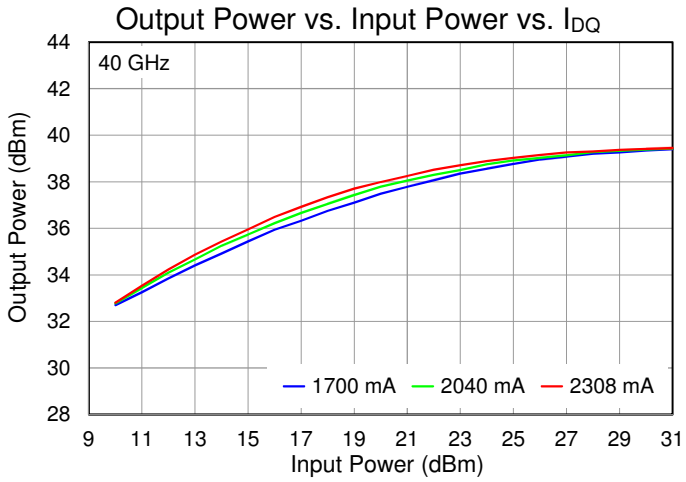
Test conditions, unless otherwise noted: CW, V_D = 18 V, I_{DQ} = 2040 mA, P_{IN} = 27 dBm, T_{BASE} = 25 °C (T_{BASE} is backside of carrier plate)





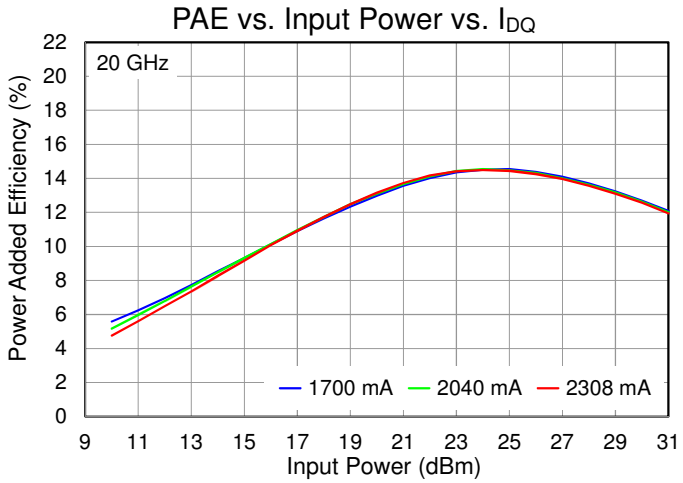


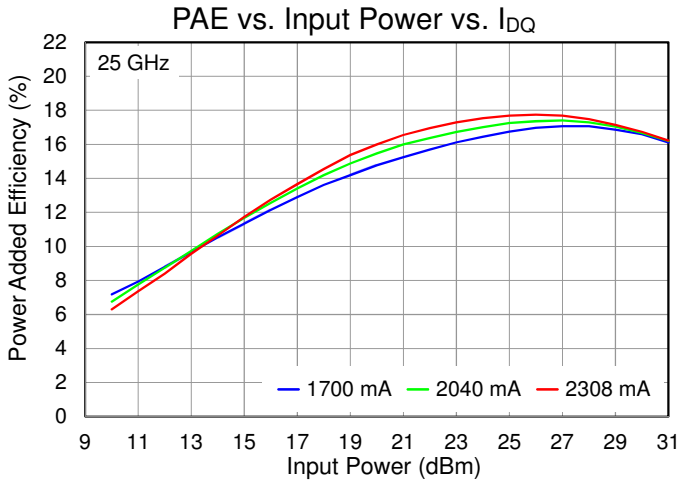


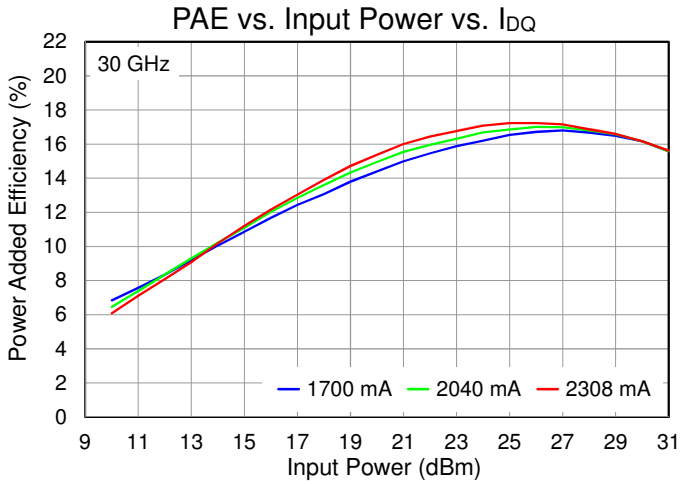


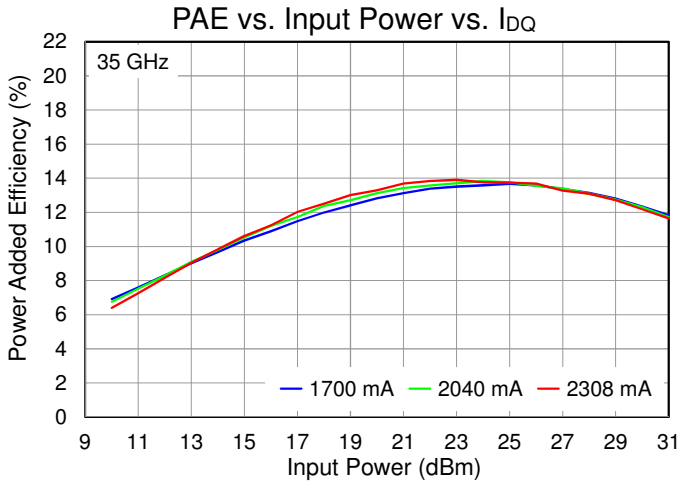
Performance Plots – Large Signal

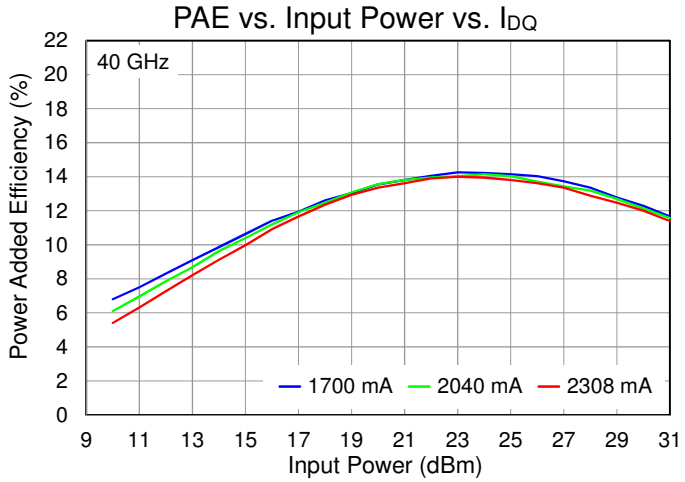
Test conditions, unless otherwise noted: CW, V_D = 18 V, I_{DQ} = 2040 mA, P_{IN} = 27 dBm, T_{BASE} = 25 °C (T_{BASE} is backside of carrier plate)





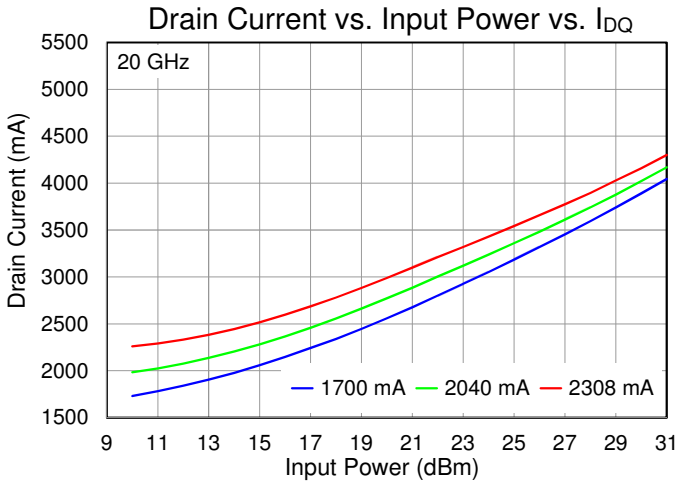


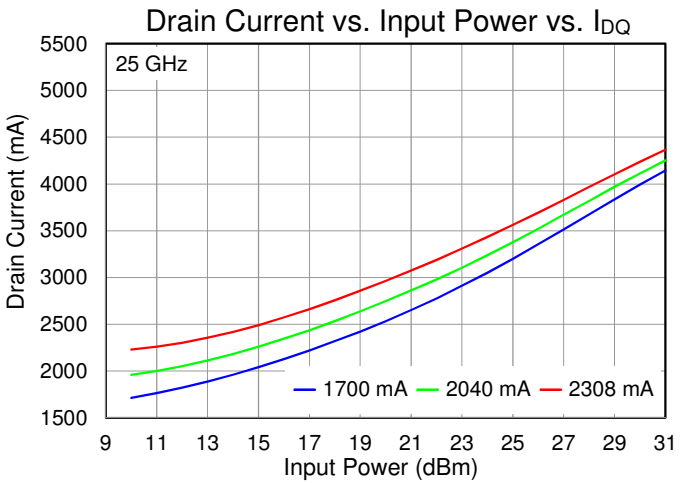


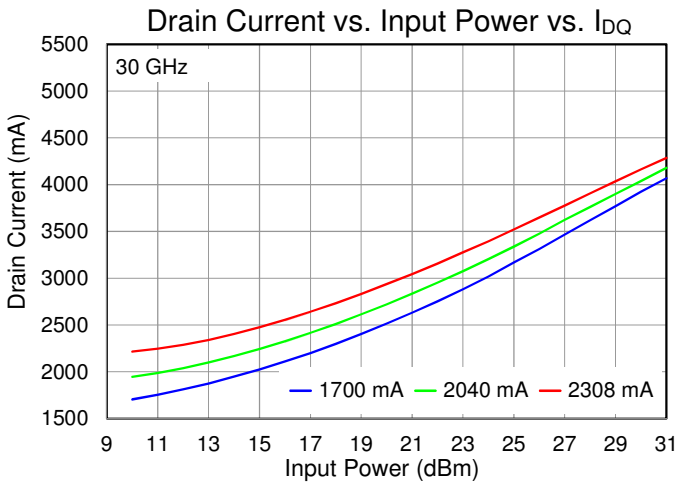


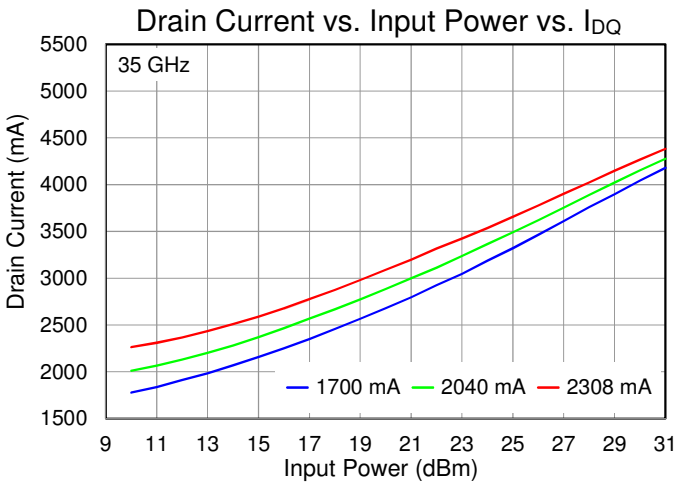
Performance Plots – Large Signal

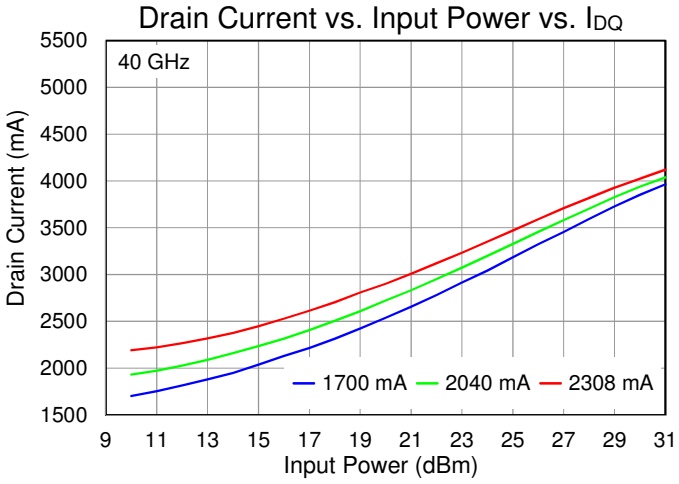
Test conditions, unless otherwise noted: CW, V_D = 18 V, I_{DQ} = 2040 mA, P_{IN} = 27 dBm, T_{BASE} = 25 °C (T_{BASE} is backside of carrier plate)











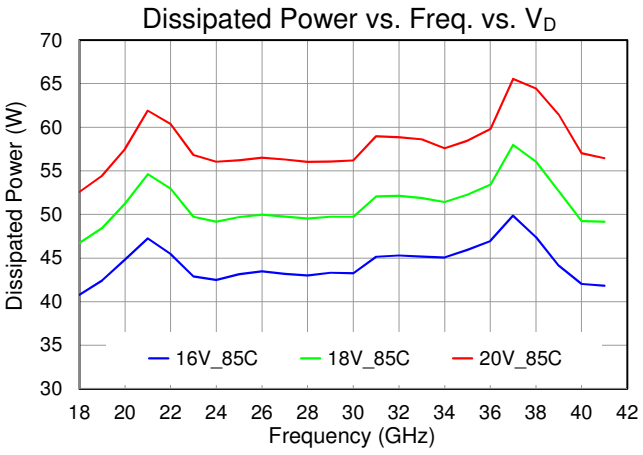
Thermal and Reliability Information

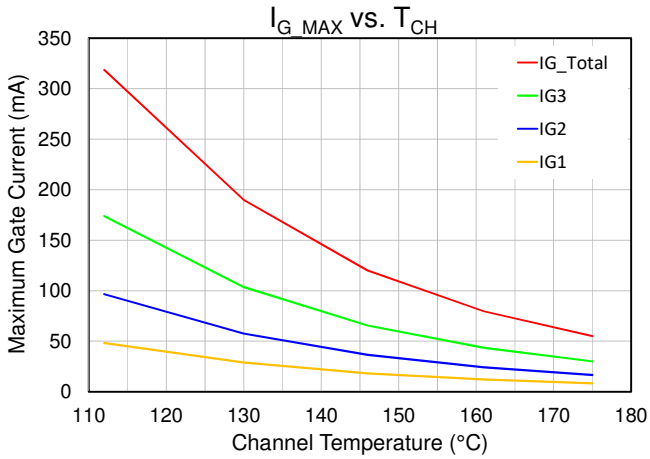
Parameter	Test Conditions	Value	Units
Thermal Resistance, θ_{JC} (1)	Quiescent T_{base} = 85 °C, V_D = 18 V, I_{DQ} = 2040 mA, P_{DISS} = 36.7 W	1.17	ºC/W
Channel Temperature, T_{CH} (2)		128	°C
Thermal Resistance, θ_{JC} (1)	CW, T_{base} = 85 °C, V_D = 18 V, I_{DQ} = 2040 mA, Freq = 37 GHz, I_{D_Drive} = 3515 mA, P_{IN} = 27 dBm, P_{OUT} = 37.6 dBm, P_{DISS} = 58 W	1.50	ºC/W
Channel Temperature, T_{CH} (2)		172	°C

Notes:

1. Thermal resistance determined to the back side of 20 mil CuMo carrier plate (T_{BASE} = 85 °C)
2. Channel temperature indicated is an IR scan equivalent temperature. Thermal resistance is calculated using this value. Additional information can be found in the Qorvo Applications Note “GaN Device TCHMAX Theta-JC and Reliability Estimates,” located here https://www.qorvo.com/products/d/da006480

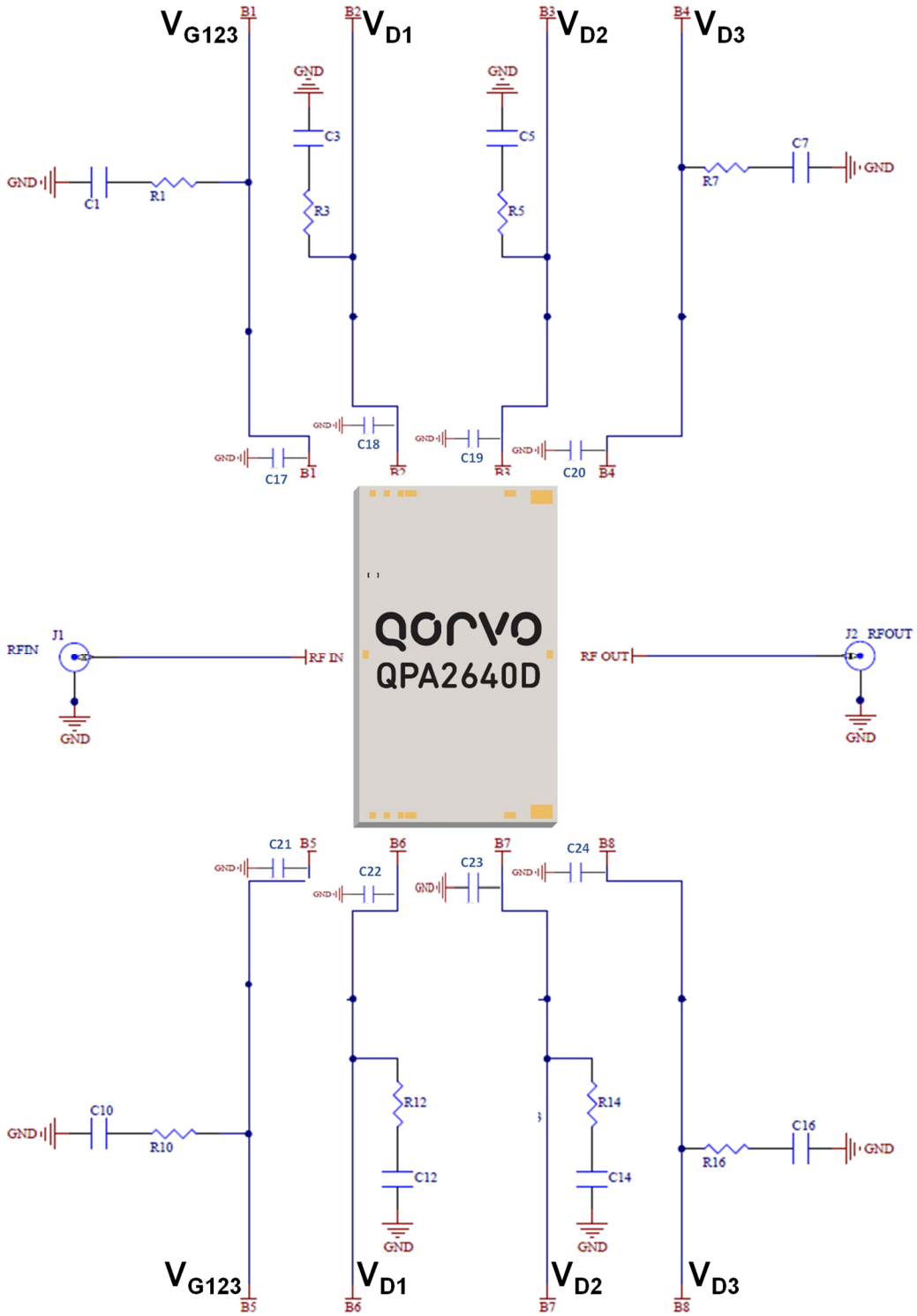
Dissipated Power and Maximum Gate Current





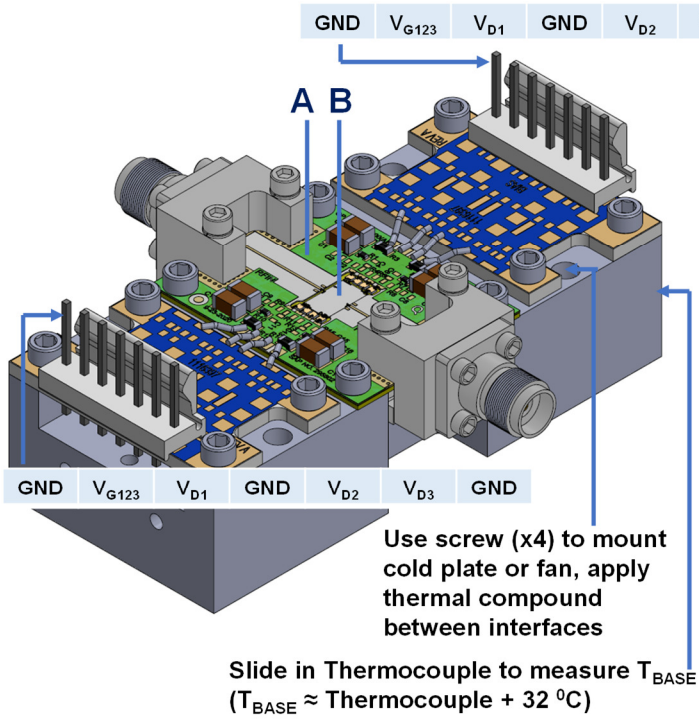
Test conditions, unless otherwise noted: CW, V_D = 18 V, I_{DQ} = 2040 mA, P_{IN} = 27 dBm, T_{BASE} = 85 ºC (T_{BASE} is backside of carrier plate)

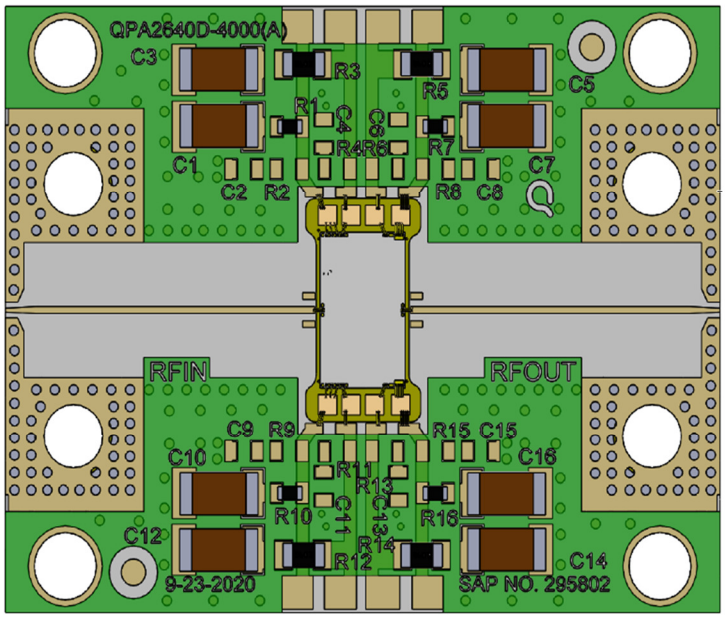
Applications Information



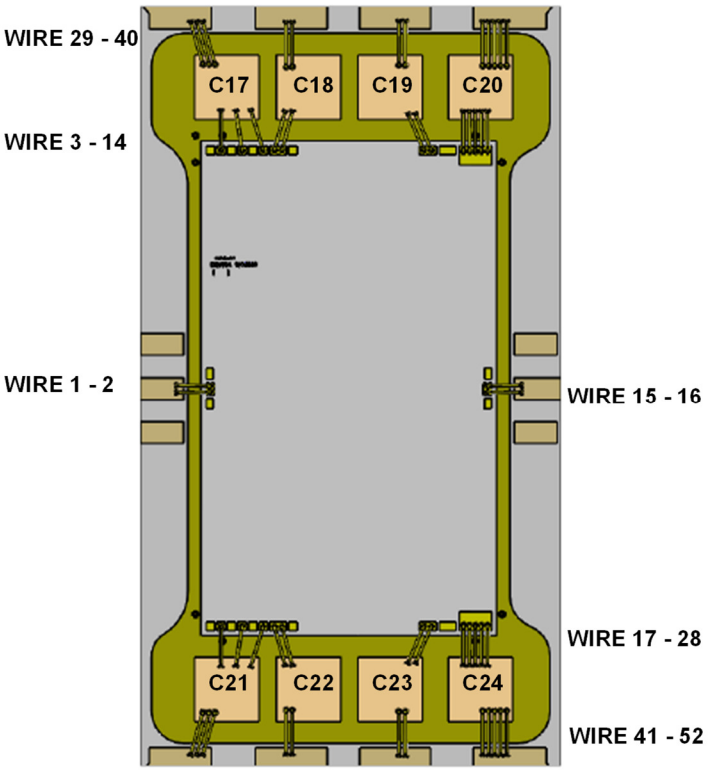
DC must be biased from both sides

Evaluation Board (EVB) Layout





DETAIL A



DETAIL B

Bill of Materials

Reference Des.	Qty	Value	Description	Part Number
C1, C3, C5, C7, C10, C12, C14, C16	8	10 uF	CAP, 10uF, 20%, 50V, 20%, X5R, 1206	
C17 – C24	8	10 nF	CAP, 10nF, ±15%, 30V, SLC, 0303	
R1, R7, R10, R16	4	0 Ω	RES, 0 Ohm, JMPR, 0402	
R3, R5, R12, R14	4	0 Ω	RES, 0 Ohm, 1/10W, 0603	
PCB_MMIC	1		PCB for MMIC, Taconics RF-35HTC 0.005", 0.5oz Ni/Pd/Au plating both sides, total thickness 0.009"	Qorvo, Custom
PCB,_Bias	2		PCB for DC Bias	Qorvo, Custom
H1, H2	2		CONN, HDR, Male-vert, 7 PIN, 1 RAW, MTA	
J1, J2	2		Connector, RF 2.4mm, F, Pin 0.005, Diel 0.029	Southwest Microwave 1492-04A-12
CP	1		Carrier Plate, CuMo, 0.9 x 1.15 x 0.02T	Qorvo, Custom
H-Block	1		H-Block, Copper C110, 1.14 x 2.49 x 0.59T	Qorvo, Custom
S1 – S4	12		Screw, Cap, Socket Head, 2-56X1/8"	
S5 – S12	8		Screw, Cap, Socket Head, 2-56X3/16"	
AuSn			AuSn Solder preform	
Epoxy			Epoxy preform	
Ablebond			Epoxy, Ablebond 84-1LMI	
Solder			Paste, solder, Syntech, Sn63/Pb37	
TC			Thermal Compound, Silver 5GR	Artic Silver 5 AS5-5G

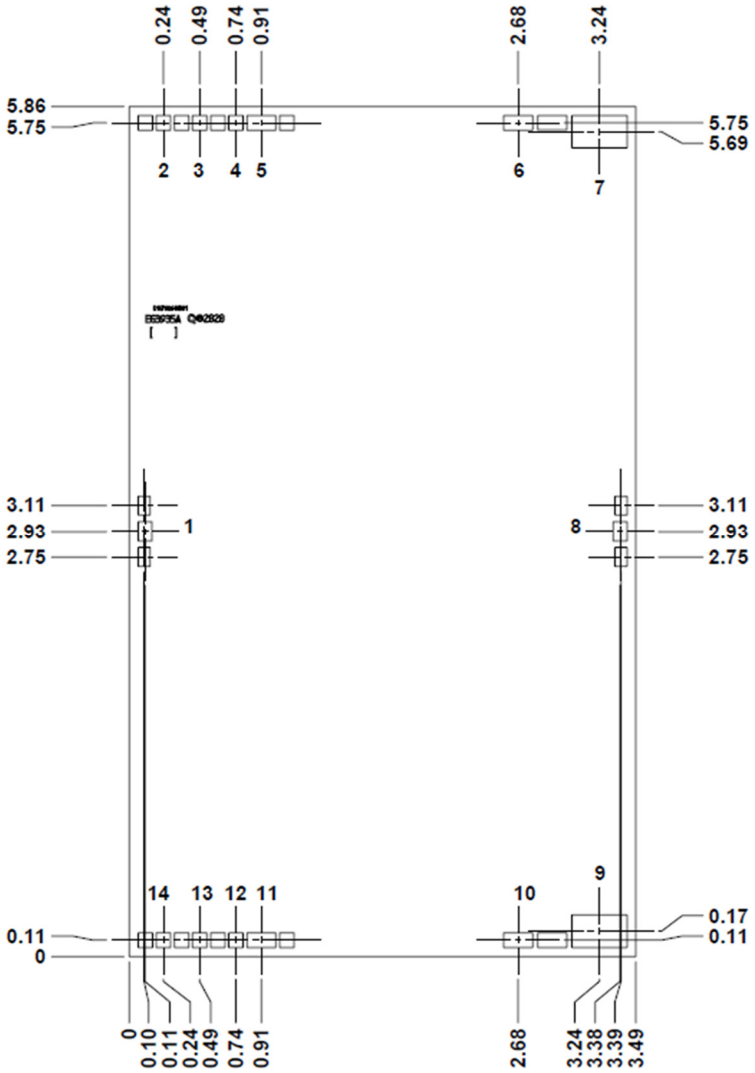
Bias-Up Procedure

1. Set I_D limit to 5 A, I_G limit to 50 mA
2. Set V_G to –3.8 V
3. Set V_D 18 V. Ensure I_{DQ} ~ 0 mA
4. Adjust V_G more positive until I_D = 2040 mA; $V_G \approx$ -2.3 V +/- 0.6V typical range
5. Apply RF signal

Bias-Down Procedure

1. Turn off RF signal
2. Reduce V_G to –3.8 V. Ensure I_{DQ} ~ 0 mA
3. Set V_D to 0 V
4. Turn off V_D supply
5. Turn off V_G supply

Mechanical Information



Dimensions: mm; Thickness: 0.05 mm; Die x, y size tolerance: ± 0.050; Ground is backside of die

Bond Pad Description

Pad No.	Symbol	Pad Size (mm)	Description
1	RF_{IN}	0.10 x 0.14	RF Input. Matched to 50 Ω, DC blocked
2, 14	V_{G1}	0.10 x 0.10	Gate voltage for stage 1*
3, 13	V_{G2}	0.10 x 0.10	Gate voltage for stage 2*
4, 12	V_{G3}	0.10 x 0.10	Gate voltage for stage 3*
5, 11	V_{D1}	0.20 x 0.10	Drain voltage for stage 1*
6, 10	V_{D2}	0.20 x 0.10	Drain voltage for stage 2*
7, 9	V_{D3}	0.30 x 0.22	Drain voltage for stage 3*
8	RF_{OUT}	0.10 x 0.14	RF Output. Matched to 50 Ω, DC blocked

* External bypassing required; refer to page 18 for recommendation

Assembly Notes

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.

Reflow process assembly notes:

- Use AuSn (80/20) solder and limit exposure to temperatures above 300 °C to 3 – 4 minutes, maximum.
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- Do not use any kind of flux.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonic are critical parameters.
- Aluminum wire should not be used.
- Devices with small pad sizes should be bonded with 0.0007-inch wire.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	1A	ANSI/ESD/JEDEC JS-001

Caution!

ESD-Sensitive Device

Solderability

Use only AuSn (80/20) solder, and limit exposure to temperatures above 300 °C to 3 – 4 minutes, maximum.

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

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