QP7C245A

October 12, 2007

2K x 8 Reprogrammable Registered PROM

Features

- 5V ±10% VCC, commercial, industrial and military
- Windowed Packages available for reprogrammability
- OTP (One-Time-Programmable) Packages available
- Programmable asynchronous register (INITbar)
- Programmable synchronous or asynchronous output enable
- High speed
  - 15 ns address set-up
  - 10 ns clock to output
- Slim, 300-mil, 24 pin hermetic DIP available
- Direct replacement for Cypress PROMs
- EPROM technology 100% programmable
- TTL-compatible I/O
- On-chip edge-triggered registers
- CMOS for optimum speed/power
- Low power
  - 660 mW (industrial & military)
  - 330 mW (commercial 25ns)
- Direct replacement for bipolar PROMs

General Description

The QP7C245A is a high-performance, 2K x 8, electrically programmable, read-only memory packaged in a variety of packages. The ceramic packages may be equipped with an erasure window; when exposed to UV light the PROM is erased and can then be reprogrammed. The memory cells utilize proven EPROM floating-gate technology and byte-wide intelligent programming algorithms.

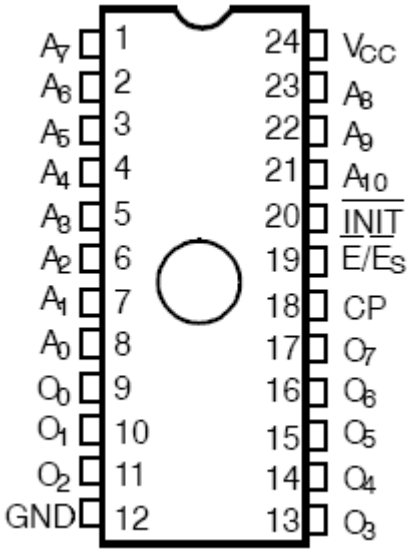
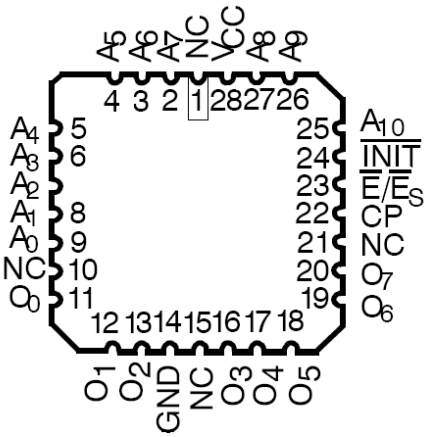
The QP7C245A replaces Cypress and bipolar devices. When replacing bipolar devices, it offers the advantages of lower power, reprogrammability, superior performance and high programming yield. The EPROM cell requires only 12.5V for the supervoltage, and low current requirements allow gang programming. The EPROM cells allow each memory location to be tested 100%, because each location is written into, erased, and exercised prior to assembly.

Each PROM is also tested for AC performance to guarantee that after customer programming the product will meet AC specification limits.

The QP7C245A has an asynchronous initialize function (INIT). This function acts as a 2049th 8-bit word loaded into the on-chip register. It is user programmable with any desired word, or may be used as a PRESET or CLEAR function on the outputs. A low level, not an edge, triggers INIT.

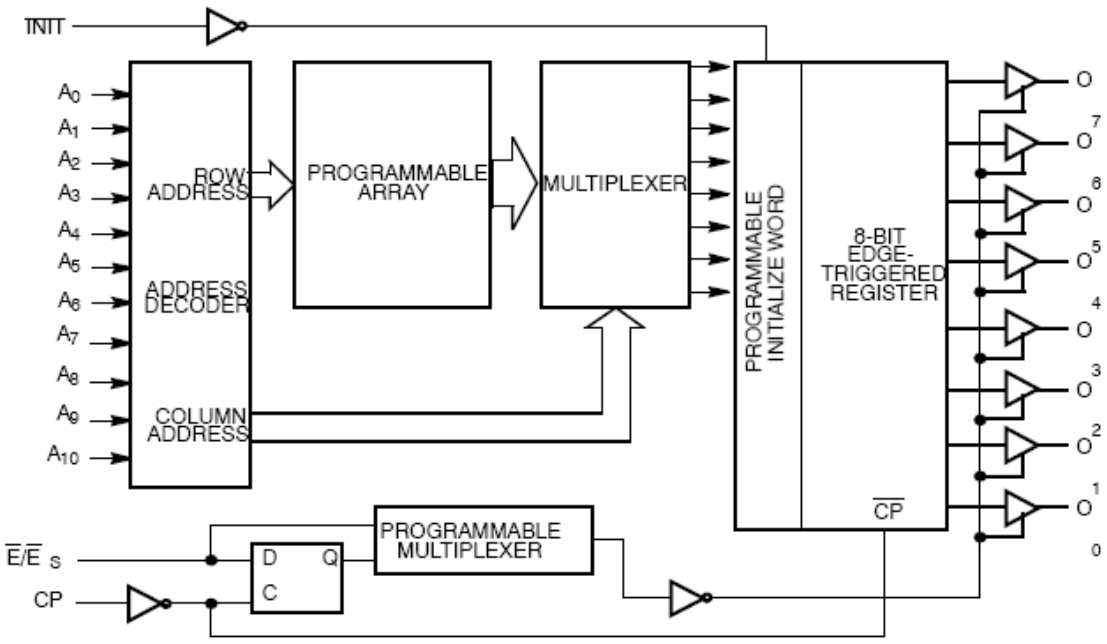
The devices are available in windowed packages (Erasable when exposed to UV light) and are also available in non-windowed OTP (One-Time-Programmable) hermetic and plastic packages.

Connection Diagrams

	CerDIP/PDIP/Cerpack 24 Lead	LLCC/LCC/PLCC
QP7C245A Hermetic Packages available in both Erasable (Windowed) and OTP – One-Time-Programmable (Non-Windowed) versions. Molded Plastic Packages (PDIP/PLCC) are only available as OTP (Non-Windowed).		

Block Diagram

QP7C245A



Absolute Maximum Ratings

Stresses above the AMR may cause permanent damage, extended operation at AMR may degrade performance and affect reliability

Condition		Units	Notes
Supply Voltage to Ground	-0.5 to 7.0	Volts	/1
DC Voltage Applied to Outputs in High Z State	-0.5 to 7.0	Volts	/1
DC Input Voltage	-3.0V to 7.0	Volts	/1
DC Program Voltage	13.0	Volts	
UV Exposure	7258	W_{SEC}/cm^2	
Storage Temperature	-65 to +155	ºC	
Ambient Temperature with Power Applied	-55 to +125	ºC	/2
Junction Temperature	150	ºC	/3 /4

Recommended Operating Conditions

Condition		Units	Notes
Supply Voltage Range	4.5 to 5.5	Volts DC	5V ± 10%
Case Operating Range (T_c)	-0C to +70	ºC	Commercial
Case Operating Range (T_c)	-40C to +85	ºC	Industrial
Case Operating Range (T_c)	-55 to +125	ºC	Military

Notes:

Apply to Absolute Maximum, Recommended Operating Conditions and Electrical Performance Characteristics.

/1 – The Voltage on any input or I/O pin cannot exceed the power pin during power-up.

/2 – T_A is the "instant on" case temperature.

/3– Applies to all versions, but is critical for molded plastic products. Tj above listed limits can activate mold compound flame retardant.

/4 – Maximum T_J is not to be exceeded.

/5 – V_{CC} 4.5 to 5.5 Volts

/6 – For devices using the synchronous enable, the device must be clocked after applying these voltages to perform this measurement.

/7 – For Test Purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

/8 – Applies only when the synchronous ($E_{S\ BAR}$) function is used.

/9 – Applies only when the asynchronous (E_{BAR})) function is used.

TABLE I – ELECTRICAL PERFORMANCE CHARACTERISTICS

Test	Symbol	Conditions /5 Case Operating Range (ºC)	Min	Max	Unit
Output Voltage High	V_{OH}	V_{CC}= 4.5V, I_{OH}=-4.0mA	2.4		V
Output Voltage Low	V_{OL}	V_{CC}= 4.5V, I_{OL}=16.0mA		0.4	V
Input High Voltage	V_{IH}	Guaranteed Input logical High for all inputs	2.0	V_{CC}	V
Input Low Voltage	V_{IL}	Guaranteed Input logical Low for all inputs		0.8	V
Input Load Current	I_{IX}	GND≤V_{OUT}≤V_{CC}	-10	10	µA
Output Leakage Current /6	I_{OZ}	GND≤V_{IN}≤V_{CC} Output Off	-10	10	µA

TABLE I – ELECTRICAL PERFORMANCE CHARACTERISTICS

Test	Symbol	Conditions /5 Case Operating Range (ºC)	Min	Max	Unit
Output Short Circuit Current /7	I_{OS}	V_{CC}= 5.5V, V_{OUT}=GND	-20	-90	mA
Operating Supply Current	I_{CC}	V_{CC}= 5.5V, I_{OUT}=0 mA			
		15ns Commercial		120	mA
		18ns Commercial		120	mA
		25ns Commercial		90	mA
		35ns Commercial		90	mA
		45ns Commercial		90	mA
		18ns Military		120	mA
		25ns Military		120	mA
		35ns Military		120	mA
		45ns Military		120	mA
Programming Supply Voltage	V_{PP}		12	13	V
Programming Supply Current	I_{PP}			50	mA
Input High Programming Voltage	V_{IHP}		3.0		V
Input Low Programming Voltage	V_{ILP}			0.4	V
Input Capacitance	C_{IN}	T_A=25ºC, f=1MHz, V_{CC}=5.0V		10	pF
Output Capacitance	C_{OUT}	T_A=25ºC, f=1MHz, V_{CC}=5.0V		10	pF
Address Set-up to Clock High	T_{SA}	QP7C245A - 15	15		nS
		QP7C245A - 18	18		nS
		QP7C245A - 25	25		nS
		QP7C245A - 35	35		nS
		QP7C245A - 45	45		nS
Address Hold from Clock High	T_{HA}	QP7C245A - 15	0		nS
		QP7C245A - 18	0		nS
		QP7C245A - 25	0		nS
		QP7C245A - 35	0		nS
		QP7C245A - 45	0		nS

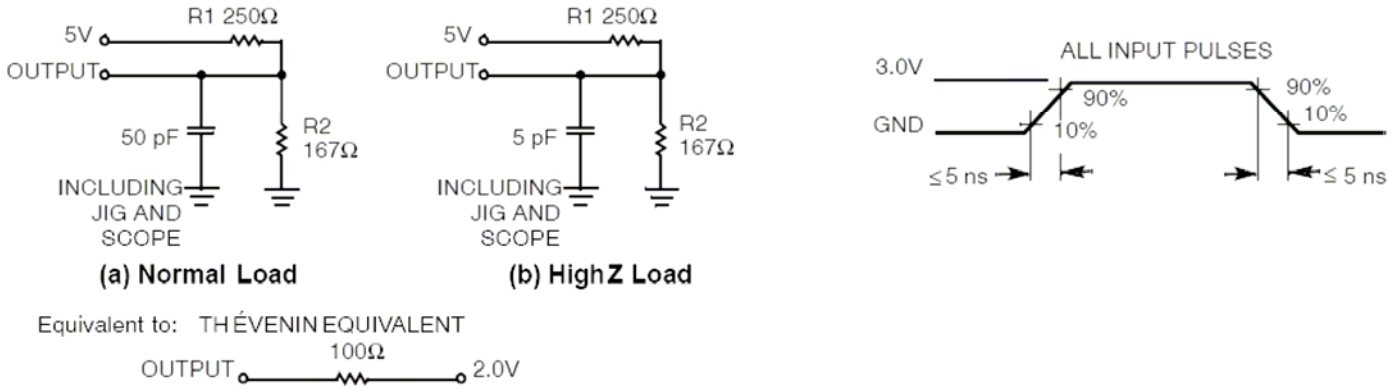
TABLE I – ELECTRICAL PERFORMANCE CHARACTERISTICS

Test	Symbol	Conditions /5 Case Operating Range (ºC)	Min	Max	Unit
Clock High to Valid Output	T_{CO}	QP7C245A - 15		10	nS
		QP7C245A - 18		12	nS
		QP7C245A - 25		12	nS
		QP7C245A - 35		15	nS
		QP7C245A - 45		25	nS
Clock Pulse Width	T_{PWC}	QP7C245A - 15	10		nS
		QP7C245A - 18	12		nS
		QP7C245A - 25	15		nS
		QP7C245A - 35	20		nS
		QP7C245A - 45	20		nS
$E_{S\ BAR}$ Set-up to Clock High	T_{SES}	QP7C245A - 15	10		nS
		QP7C245A - 18	10		nS
		QP7C245A - 25	12		nS
		QP7C245A - 35	15		nS
		QP7C245A - 45	15		nS
$E_{S\ BAR}$ Hold from Clock High	T_{HES}	QP7C245A - 15	5		nS
		QP7C245A - 18	5		nS
		QP7C245A - 25	5		nS
		QP7C245A - 35	5		nS
		QP7C245A - 45	5		nS
Delay $INIT_{BAR}$ to Valid Output	T_{DI}	QP7C245A - 15		15	nS
		QP7C245A - 18		20	nS
		QP7C245A - 25		20	nS
		QP7C245A - 35		20	nS
		QP7C245A - 45		35	nS
$INIT_{BAR}$ Recovery to Clock High	T_{RI}	QP7C245A - 15	10		nS
		QP7C245A - 18	12		nS
		QP7C245A - 25	15		nS
		QP7C245A - 35	20		nS
		QP7C245A - 45	20		nS

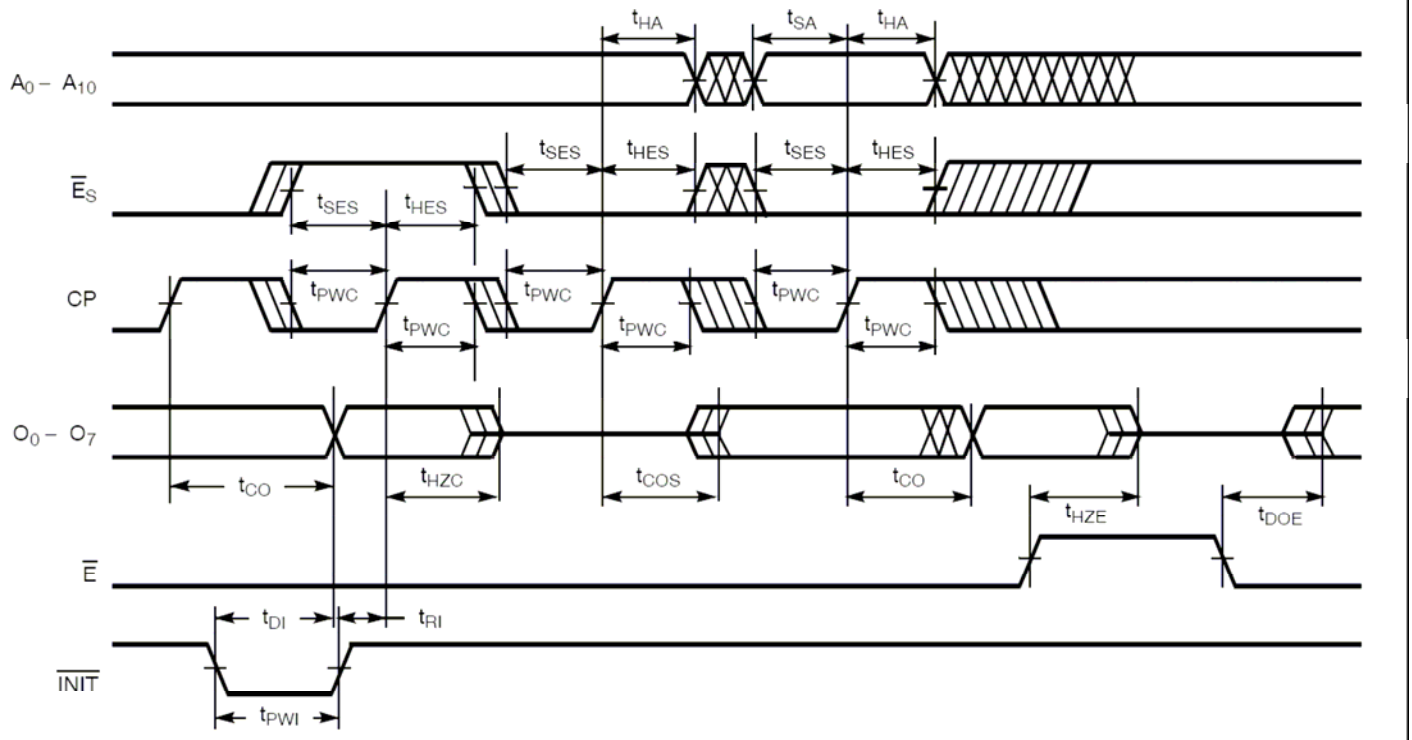
TABLE I – ELECTRICAL PERFORMANCE CHARACTERISTICS

Test	Symbol	Conditions /5 Case Operating Range (ºC)	Min	Max	Unit
$INIT_{BAR}$ Pulse Width	T_{PWI}	QP7C245A - 15	10		nS
		QP7C245A - 18	12		nS
		QP7C245A - 25	15		nS
		QP7C245A - 35	20		nS
		QP7C245A - 45	25		nS
Valid Output from Clock High /8	T_{COS}	QP7C245A - 15		15	nS
		QP7C245A - 18		15	nS
		QP7C245A - 25		15	nS
		QP7C245A - 35		20	nS
		QP7C245A - 45		30	nS
Inactive Output from Clock High /8	T_{HZC}	QP7C245A - 15		15	nS
		QP7C245A - 18		15	nS
		QP7C245A - 25		15	nS
		QP7C245A - 35		20	nS
		QP7C245A - 45		30	nS
Valid Output from E_{BAR} Low /9	T_{DOE}	QP7C245A - 15		12	nS
		QP7C245A - 18		15	nS
		QP7C245A - 25		15	nS
		QP7C245A - 35		20	nS
		QP7C245A - 45		30	nS
Inactive Output from E_{BAR} High /9	T_{HZE}	QP7C245A - 15		15	nS
		QP7C245A - 18		15	nS
		QP7C245A - 25		15	nS
		QP7C245A - 35		20	nS
		QP7C245A - 45		30	nS

AC Test Loads



Waveforms



Operating Modes

The QP7C245A is a CMOS electrically programmable read only memory organized as 2048 words x 8 bits and is a pin-for-pin replacement for bipolar TTL fusible link PROMs. The QP7C245A incorporates a D-type, master-slave register on chip, reducing the cost and size of pipelined microprogrammed systems and applications where accessed PROM data is stored temporarily in a register. Additional flexibility is provided with a programmable synchronous ($E_{bar}S$) or asynchronous (E_{bar}) output enable and asynchronous initialization ($INIT_{bar}$).

Upon power-up the state of the outputs will depend on the programmed state of the enable function ($E_{bar}S$ or E_{bar}). If the synchronous enable ($E_{bar}S$) has been programmed, the register will be in the set condition causing the outputs (O0–O7) to be in the OFF or high-impedance state. If the asynchronous enable (E_{bar}) is being used, the outputs will come up in the OFF or high-impedance state only if the enable (E_{bar}) input is at a HIGH logic level. Data is read by applying the memory location to the address inputs (A0–A10) and a logic LOW to the enable input. The stored data is accessed and loaded into the master flip-flops of the data register during the address set-up time. At the next LOW-to-HIGH transition of the clock (CP), data is transferred to the slave flip-flops, which drive the output buffers, and the accessed data will appear at the outputs (O0–O7).

If the asynchronous enable (E_{bar}) is being used, the outputs may be disabled at any time by switching the enable to a logic HIGH, and may be returned to the active state by switching the enable to a logic LOW.

If the synchronous enable ($E_{bar}S$) is being used, the outputs will go to the OFF or high-impedance state upon the next positive clock edge after the synchronous enable input is switched to a HIGH level. If the synchronous enable pin is switched to a logic LOW, the subsequent positive clock edge will return the output to the active state. Following a positive clock edge, the address and synchronous enable inputs are free to change since no change in the output will occur until the next low-to-high transition of the clock. This unique feature allows the QP7C245A decoders and sense amplifiers to access the next location while previously addressed data remains stable on the outputs.

System timing is simplified in that the on-chip edge triggered register allows the PROM clock to be derived directly from the system clock without introducing race conditions. The on-chip register timing requirements are similar to those of discrete registers available in the market.

The QP7C245A has an asynchronous initialize input ($INIT_{bar}$). The initialize function is useful during power-up and time-out sequences and can facilitate implementation of other sophisticated functions such as a built-in "jump start" address. When activated, the initialize control input causes the contents of a user-programmed 2049th 8-bit word to be loaded into the on-chip register. Each bit is programmable and the initialize function can be used to load any desired combination of 1s and 0s into the register. In the unprogrammed state, activating INIT will generate a register CLEAR (all outputs LOW). If all the bits of the initialize word are programmed, activating INIT performs a register PRESET (all outputs HIGH).

Applying a LOW to the $INIT_{bar}$ input causes an immediate load of the programmed initialize word into the master and slave flip-flops of the register, independent of all other inputs, including the clock (CP). The initialize data will appear at the device outputs after the outputs are enabled by bringing the asynchronous enable (E_{bar}) LOW.

Programmer Address		RAM Data
Decimal	Hex	Contents
0	000	Data
1	001	Data
.	.	.
.	.	.
2046	7FE	Data
2047	7FF	Data
2048	800	Init Byte
2049	801	Control Byte

Mode Selection	Pin Function /10							
Read or Output Disable	A_{10}-A_4	A_3	A_2-A_1	A_0	CP	E_{BAR}, $E_{S\ BAR}$	INIT	O_7-O_0
Other	A_{10}-A_4	A_3	A_2-A_1	A_0	PGM	VFY	V_{PP}	D_7-D_0
Read	A_{10}-A_4	A_3	A_2-A_1	A_0	V_{IL} / V_{IH}	V_{IL}	V_{IH}	O_7-O_0
Output Disable	A_{10}-A_4	A_3	A_2-A_1	A_0	X	V_{IH}	V_{IH}	High Z
Initialize	A_{10}-A_4	A_3	A_2-A_1	A_0	X	V_{IL}	V_{IL}	Init Byte
Program	A_{10}-A_4	A_3	A_2-A_1	A_0	V_{ILP}	V_{IHP}	V_{PP}	D_7-D_0
Program Verify	A_{10}-A_4	A_3	A_2-A_1	A_0	V_{IHP}	V_{ILP}	V_{PP}	O_7-O_0
Program Inhibit	A_{10}-A_4	A_3	A_2-A_1	A_0	V_{IHP}	V_{IHP}	V_{PP}	High Z
Intelligent Program	A_{10}-A_4	A_3	A_2-A_1	A_0	V_{ILP}	V_{IHP}	V_{PP}	D_7-D_0
Program Synchronous Enable	A_{10}-A_4	V_{IHP}	A_2-A_1	V_{PP}	V_{IHP}	V_{IHP}	V_{PP}	High Z
Program Initialization Byte	A_{10}-A_4	V_{IHP}	A_2-A_1	V_{PP}	V_{ILP}	V_{IHP}	V_{PP}	D_7-D_0
Blank Check Zeros	A_{10}-A_4	A_3	A_2-A_1	A_0	V_{IHP}	V_{ILP}	V_{PP}	Zeros

/10 – X = "Don't Care", but not to exceed VCC +5%

Erasure Characteristics:

Wavelengths of light less than 4000 Angstroms begin to erase these PROMs. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Angstroms for a minimum dose (UV intensity x exposure time of 25 Wsec/cm2. For an ultraviolet lamp with a 12 mW/cm2 power rating, the exposure time would be approximately 35 minutes. These PROMs need to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high-intensity UV light for an extended period of time.

7258 Wsec/cm2 is the recommended maximum dosage.

Programming Information:

The QP7C245A uses the same programming algorithm as Cypress 7C245A device. A variety of programming equipment currently supports the Cypress Algorithm. QP Semiconductor has verified that the devices program on Data I/O Unisite and on a programmer supplied by EETools.

Ordering Information

Temp Range	t_{AA} ns	Part Number	Package	Mil-Std-1835	Generic
Commerical	15	QP7C245A-15JC	28-Lead PLCC	-	7C245A
Commerical	15	QP7C245A-15PC	24-Lead 300-mil Plastic DIP	-	7C245A
Commerical	15	QP7C245A-15WC	24-Lead 300-mil Windowed CerDIP	GDIP3-T24	7C245A
Industrial	15	QP7C245A-15JI	28-Lead PLCC	-	7C245A
Industrial	15	QP7C245A-15PI	24-Lead 300-mil Plastic DIP	-	7C245A
Industrial	15	QP7C245A-15WI	24-Lead 300-mil Windowed CerDIP	GDIP3-T24	7C245A
Commerical	18	QP7C245A-18JC	28-Lead PLCC	-	7C245A
Commerical	18	QP7C245A-18PC	24-Lead 300-mil Plastic DIP	-	7C245A
Commerical	18	QP7C245A-18WC	24-Lead 300-mil Windowed CerDIP	GDIP3-T24	7C245A
Industrial	18	QP7C245A-18JI	28-Lead PLCC	-	7C245A
Industrial	18	QP7C245A-18PI	24-Lead 300-mil Plastic DIP	-	7C245A
Industrial	18	QP7C245A-18WI	24-Lead 300-mil Windowed CerDIP	GDIP3-T24	7C245A
Military	18	5962-89815033A	28-Lead Windowed LCC	CQCC1-N28	7C245A
Military	18	5962-8981503KA	24-Lead Windowed Flatpack	GDFP2-F24	7C245A
Military	18	5962-8981503LA	24-Lead 300-mil Windowed CerDIP	GDIP3-T24	7C245A
Military	18	QP7C245A-18DMB	24-Lead 300-mil CerDIP	GDIP3-T24	7C245A
Military	18	QP7C245A-18KMB	24-Lead Flatpack	GDFP2-F24	7C245A
Military	18	QP7C245A-18LMB	28-Lead LCC	CQCC1-N28	7C245A
Military	18	QP7C245A-18QMB	28-Lead Windowed LCC	CQCC1-N28	7C245A
Military	18	QP7C245A-18TMB	24-Lead Windowed Flatpack	GDFP2-F24	7C245A
Military	18	QP7C245A-18WMB	24-Lead 300-mil Windowed CerDIP	GDIP3-T24	7C245A
Commerical	25	QP7C245A-25JC	28-Lead PLCC	-	7C245A
Commerical	25	QP7C245A-25PC	24-Lead 300-mil Plastic DIP	-	7C245A
Commerical	25	QP7C245A-25WC	24-Lead 300-mil Windowed CerDIP	GDIP3-T24	7C245A
Industrial	25	QP7C245A-25JI	28-Lead PLCC	-	7C245A
Industrial	25	QP7C245A-25PI	24-Lead 300-mil Plastic DIP	-	7C245A
Industrial	25	QP7C245A-25WI	24-Lead 300-mil Windowed CerDIP	GDIP3-T24	7C245A
Military	25	5962-88735043A	28-Lead LCC	CQCC1-N28	7C245A
Military	25	5962-8873504KA	24-Lead Flatpack	GDFP2-F24	7C245A
Military	25	5962-8873504LA	24-Lead 300-mil CerDIP	GDIP3-T24	7C245A
Military	25	5962-89815023A	28-Lead Windowed LCC	CQCC1-N28	7C245A
Military	25	5962-8981502KA	24-Lead Windowed Flatpack	GDFP2-F24	7C245A
Military	25	5962-8981502LA	24-Lead 300-mil Windowed CerDIP	GDIP3-T24	7C245A

Temp Range	t_{AA} ns	Part Number	Package	Mil-Std-1835	Generic
Military	25	QP7C245A-25DMB	24-Lead 300-mil CerDIP	GDIP3-T24	7C245A
Military	25	QP7C245A-25KMB	24-Lead Flatpack	GDFP2-F24	7C245A
Military	25	QP7C245A-25LMB	28-Lead LCC	CQCC1-N28	7C245A
Military	25	QP7C245A-25QMB	28-Lead Windowed LCC	CQCC1-N28	7C245A
Military	25	QP7C245A-25TMB	24-Lead Windowed Flatpack	GDFP2-F24	7C245A
Military	25	QP7C245A-25WMB	24-Lead 300-mil Windowed CerDIP	GDIP3-T24	7C245A
Commerical	35	QP7C245A-35JC	28-Lead PLCC	-	7C245A
Commerical	35	QP7C245A-35PC	24-Lead 300-mil Plastic DIP	-	7C245A
Commerical	35	QP7C245A-35WC	24-Lead 300-mil Windowed CerDIP	GDIP3-T24	7C245A
Industrial	35	QP7C245A-35JI	28-Lead PLCC	-	7C245A
Industrial	35	QP7C245A-35PI	24-Lead 300-mil Plastic DIP	-	7C245A
Industrial	35	QP7C245A-35WI	24-Lead 300-mil Windowed CerDIP	GDIP3-T24	7C245A
Military	35	5962-87529023A	28-Lead Windowed LCC	CQCC1-N28	7C245A
Military	35	5962-87529023C	28-Lead Windowed LCC	CQCC1-N28	7C245A
Military	35	5962-8752902KA	24-Lead Windowed Flatpack	GDFP2-F24	7C245A
Military	35	5962-8752902LA	24-Lead 300-mil Windowed CerDIP	GDIP3-T24	7C245A
Military	35	5962-88735023A	28-Lead LCC	CQCC1-N28	7C245A
Military	35	5962-8873502KA	24-Lead Flatpack	GDFP2-F24	7C245A
Military	35	5962-8873502LA	24-Lead 300-mil CerDIP	GDIP3-T24	7C245A
Military	35	5962-88735033A	28-Lead LCC	CQCC1-N28	7C245A
Military	35	5962-8873503KA	24-Lead Flatpack	GDFP2-F24	7C245A
Military	35	5962-8873503LA	24-Lead 300-mil CerDIP	GDIP3-T24	7C245A
Military	35	5962-89815013A	28-Lead Windowed LCC	CQCC1-N28	7C245A
Military	35	5962-8981501KA	24-Lead Windowed Flatpack	GDFP2-F24	7C245A
Military	35	5962-8981501LA	24-Lead 300-mil Windowed CerDIP	GDIP3-T24	7C245A
Military	35	QP7C245A-35DMB	24-Lead 300-mil CerDIP	GDIP3-T24	7C245A
Military	35	QP7C245A-35KMB	24-Lead Flatpack	GDFP2-F24	7C245A
Military	35	QP7C245A-35LMB	28-Lead LCC	CQCC1-N28	7C245A
Military	35	QP7C245A-35QMB	28-Lead Windowed LCC	CQCC1-N28	7C245A
Military	35	QP7C245A-35TMB	24-Lead Windowed Flatpack	GDFP2-F24	7C245A
Military	35	QP7C245A-35WMB	24-Lead 300-mil Windowed CerDIP	GDIP3-T24	7C245A
Commerical	45	QP7C245A-45JC	28-Lead PLCC	-	7C245A
Commerical	45	QP7C245A-45PC	24-Lead 300-mil Plastic DIP	-	7C245A
Commerical	45	QP7C245A-45WC	24-Lead 300-mil Windowed CerDIP	GDIP3-T24	7C245A
Industrial	45	QP7C245A-45JI	28-Lead PLCC	-	7C245A
Industrial	45	QP7C245A-45PI	24-Lead 300-mil Plastic DIP	-	7C245A
Industrial	45	QP7C245A-45WI	24-Lead 300-mil Windowed CerDIP	GDIP3-T24	7C245A
Military	45	5962-87529013A	28-Lead Windowed LCC	CQCC1-N28	7C245A
Military	45	5962-87529013C	28-Lead Windowed LCC	CQCC1-N28	7C245A
Military	45	5962-8752901KA	24-Lead Windowed Flatpack	GDFP2-F24	7C245A
Military	45	5962-8752901LA	24-Lead 300-mil Windowed CerDIP	GDIP3-T24	7C245A
Military	45	5962-88735013A	28-Lead LCC	CQCC1-N28	7C245A
Military	45	5962-8873501KA	24-Lead Flatpack	GDFP2-F24	7C245A
Military	45	5962-8873501LA	24-Lead 300-mil CerDIP	GDIP3-T24	7C245A
Military	45	QP7C245A-45DMB	24-Lead 300-mil CerDIP	GDIP3-T24	7C245A
Military	45	QP7C245A-45KMB	24-Lead Flatpack	GDFP2-F24	7C245A
Military	45	QP7C245A-45LMB	28-Lead LCC	CQCC1-N28	7C245A
Military	45	QP7C245A-45QMB	28-Lead Windowed LCC	CQCC1-N28	7C245A
Military	45	QP7C245A-45TMB	24-Lead Windowed Flatpack	GDFP2-F24	7C245A
Military	45	QP7C245A-45WMB	24-Lead 300-mil Windowed CerDIP	GDIP3-T24	7C245A

* denotes Lead Free Lead Finish

In addition to those products listed above, QP Semiconductor supports Industrial Temperature Range, Source Control Drawing (SCD), and custom package development for this product family.

Notes:

Package outline information and specifications are defined by Mil-Std-1835 package dimension requirements.

Products manufactured by QP Semiconductor are compliant to the assembly, burn-in, test and quality conformance requirements of Test Methods 5004 & 5005 of Mil-Std-883 for Class B or Q devices as appropriate. The appropriate DSCC Detail Specifications define the electrical test requirements for each device.

The listed drawings, Mil-PRF-38535, Mil-Std-883 and Mil-Std-1835 are available online at http://www.dscc.dla.mil/

Additional information is available at our website http://www.qpsemi.com