QN8027

High Performance Digital FM Transmitter for Portable Devices

General Description

The QN8027 is a high performance, low power, full-featured single-chip stereo FM transmitter designed for portable audio/video players, automotive accessories, cell phones, and GPS personal navigation devices. The QN8027 covers frequencies from 76 MHz to 108 MHz in 50/100/200 kHz step sizes for worldwide FM band support. The QN8027 also supports RDS/RBDS data transmit.

The QN8027 integrates a complete transmitter function, from stereo audio input to RF antenna port, for worldwide FM band personal area broadcasting. It includes variable input gain programming, selectable pre-emphasis, precision low-spur MPX stereo encoding and pilot tone generation, low-noise PLL-based modulation, and an on-chip power amplifier with variable output level and RF band-pass filtering to ensure optimum transmit spectrum purity.

An integrated crystal oscillator and on-chip digital calibration circuits eliminate external tuning components and enable tuning-free manufacturing. Support for 12/24MHz reference clocks allows the chip to use readily available system clocks. Integrated saturation detection and a programmable audio interface eliminate distortion, optimize audio fidelity, and support a wide range of input audio levels. A low power IDLE mode extends battery life. An integrated LDO enables direct connection to the battery and provides high PSRR for superior noise suppression, in particular TDMA noise from GSM/GPRS phones.

The QN8027's small footprint, high integration with minimum external component count, and support for 12/24MHz clock frequencies make it easy to integrate into a variety of small form-factor low-power portable applications. Integrated low-phase noise digital synthesizers and extensive on-chip auto calibration ensures robust consistent performance over temperature and process variations. An integrated voltage regulator enables direct connection to a battery and provides high PSRR for superior noise suppression. A low-power IDLE mode extends battery life.

ESD protection is on all pins. The QN8027 is fabricated in highly reliable CMOS technology.

Key Features

- **Worldwide FM Band Transmit**
  - *76 MHz to 108 MHz full band tuning in 50/100/200 kHz step sizes*
  - *50/75μs pre-emphasis*
- **Ease of Integration**
  - *Small footprint, 3 x 3 x 0.95mm MSOP10*
  - *Only 2 external passive components required*
  - *Adaptive antenna tuning*
  - *Low cellular and GPS band spurs*
  - *High Immunity to TDMA (GSM/GPRS) burst noise*
  - *Multiple crystal frequencies supported*
  - *I^2C interface*
- **Low Power Consumption**
  - *7.0 mA of FCC output level*
  - *Integrated voltage regulator, direct connect to battery*
  - *Power saving IDLE-mode*
- **High Performance FM Transmitter (FMT)**
  - *65dB Stereo SNR, 0.04% THD*
  - *Maximum 119 dBμVp RF output level with 34dB adjustable range*
- **Automatic Input Audio Sensing**
  - *RF power automatically turned off if no input audio signal for 60s*
- **RDS/RBDS Transmit**
  - *Supports US and European data service, including TMC (Traffic Messaging Channel)*
- **Robust Operation**
  - *-25^0C to $+85^0C$ operation*
  - *ESD protection on all input and output pads*

Typical Applications

- Cell Phones / PDAs / Smart Phones
- Portable Audio & Media Players
- GPS Personal Navigation Devices
- Automotive and Accessories

CONTENTS

REVISION HISTORY

REVISION	CHANGE DESCRIPTION	DATE
0.1	Datasheet draft.	12/08/08
1.0	Modify Reg06h[3:0] 0000→0100	03/17/10
1.1	Update the I_{TX} value in Table 4	04/13/10
1.2	Update the Table 6 and Section 4.1	05/31/10
1.3	Update Section 5 and figure 5.	2010-7-21

STATEMENT:

Users are responsible for compliance with local regulatory requirements for low power unlicensed FM broadcast operation. Quintic is not responsible for any violations resulting from user's intentional or unintentional breach of regulatory requirements in personal or commercial use.

6.

1 FUNCTIONAL BLOCK DIAGRAM

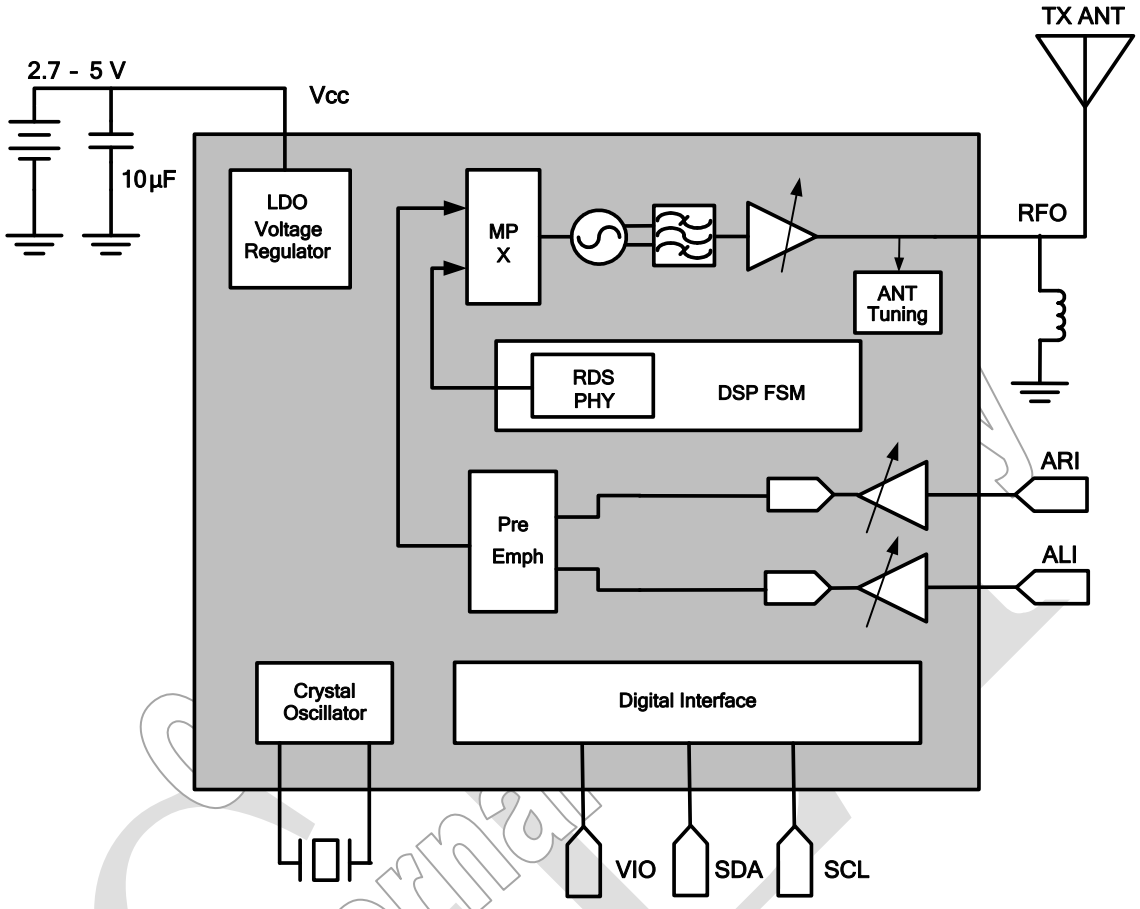
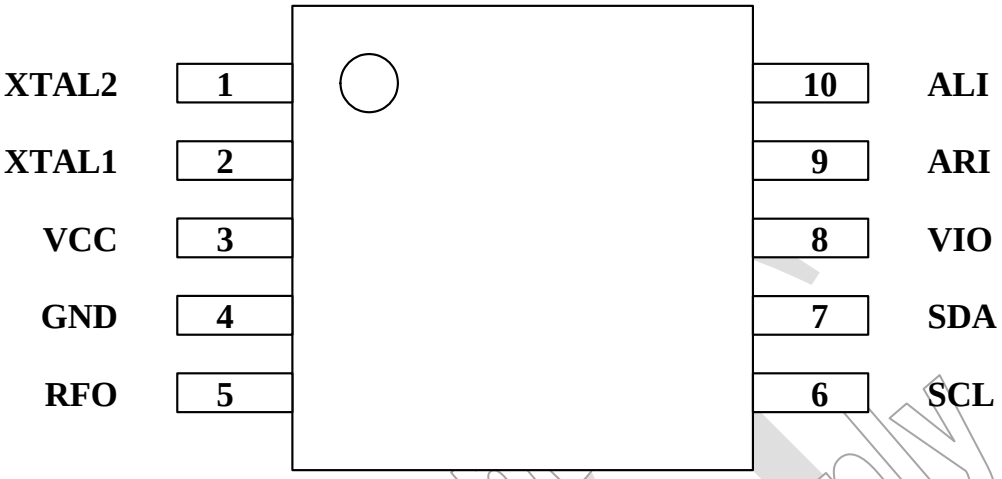


Figure 1: QN8027-SANC Functional Blocks

2 PIN ASSIGNMENTS



(Top View)

Figure 2: QN8027 Device Pin Out

Table 1: Pin Descriptions

PINS	NAME	DESCRIPTION
1	XTAL2	On-chip crystal driver port 2. If using an external clock source, connect this pin to ground.
2	XTAL1	On-chip crystal driver port 1. If using an external clock source, connect this pin to inject the clock.
3	VCC	Voltage supply
4	GND	Ground
5	RFO	Transmitter RF output – connect to matched antenna.
6	SCL	Clock for I^2C serial bus.
7	SDA	Bi-directional data line for I^2C serial bus.
8	VIO	IO voltage – specifies voltage limit for all digital pins.
9	ARI	Analog audio input – right channel
10	ALI	Analog audio input – left channel

3 ELECTRICAL SPECIFICATIONS

Table 2: Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{bat}	Supply voltage	VCC to GND	-0.3	5	V
V_{IO}	Logic signals	SCL, SDA to GND	-0.3	3.6	V
T_s	Storage temperature		-55	+150	^oC

Table 3: Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Vcc	Supply voltage	VCC to GND	2.7	3.3	5.0	V
T_A	Operating temperature		-25		+85	^oC
V_{ain}	L/R channel input signal level	Single ended peak to peak voltage		1000	1400	mV
V_{IO}	Digital I/O voltage		1.6		3.6	V

Table 4: DC Characteristics

(Vcc = 2.7 ~ 5.0 V, T_A = -25 ~ 85 °C, unless otherwise noticed. Typical values are at Vcc = 3.3.V, f carrier=88 MHz and T_A = 25°C).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
I_{TX}	Transmit mode supply current		7.0[1]		13.8[2]	mA
I_{IDLE}	Idle mode supply current	Idle mode		1.2		mA
Interface						
V_{OH}	High level output voltage		0.9*V_{IO}			V
V_{OL}	Low level output voltage				0.1*V_{IO}	V
V_{IH}	High level input voltage		0.7*V_{IO}			V
V_{IL}	Low level input voltage				0.4	V

Notes:
1. RFO output at Min level.
2. RFO output at Max level.

Table 5: AC Characteristics

(Vcc = 2.7 ~ 5.0 V, T_A = -25 ~ 85 °C, unless otherwise noticed. Typical values are at Vcc = 3.3V and T_A = 25°C).

SYMBOL	PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNIT
F_{xtal}[1]	Crystal or Clock frequency		12 or 24			MHz
F_{xtal_err}[2]	Crystal frequency accuracy	Over temperature, and aging	-20		20	ppm

Notes:
1. See also XSEL, R04[7].
2. Required by FCC standard.

Table 6: Transmitter Characteristics

(Vcc = 2.7 ~ 5.0 V, T_A = -25 ~ 85 °C, unless otherwise noticed. Typical values are at Vcc = 3.3V, f carrier=88 MHz and T_A = 25°C).

SYMBOL	PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNIT
R_{audio_in}	Audio input impedance[1]	At pin ALI and ARI	5		40	kΩ
C_{audio_in}	Audio input capacitance[1]	At pin ALI and ARI		2	5	pF
G_{audio_In}	Audio input gain	RIN[1:0] = 10	-9		6	dB
ΔG_{audio_In}	Audio gain step	For any gain setting	0.5	1	1.5	dB
τ_{emph}	Pre-emphasis time constant[1]	PETC = 1	71.3	75	78.7	μs
		PETC = 0	47.5	50	52.5	
SNR_{audio_tx}	Tx audio SNR[1, 2]	MONO, Δf = 22.5 kHz		64		dB
		STEREO, Δf = 67.5 kHz, Δf_{pilot} = 6.75 kHz		65		
THD_{audio_tx}	Tx audio THD[1, 2]	MONO, Δf = 75 kHz		0.04	0.1	%
		STEREO, Δf = 67.5 kHz, Δf_{pilot} = 6.75 kHz		0.04	0.1	
α_{LR_tx}	L/R separation [2]		35	42		dB
B_{LR_tx}	L/R channel imbalance [1]	L and R channel gain imbalance at 1 kHz offset from DC			1	dB
M_{pilot}	19 kHz pilot modulation [2, 5]	Relative to 75 kHz deviation	7	9.0	15	%
SUP_{sub}	38 kHz sub-carrier [2] suppression		70			dB
C_{tune}	Output capacitance tuning range[1]		5		30	pF
P_{out}	RF output voltage swing[3]	RF Channel frequency = 88 MHz	82		119	dBμVp
ΔG_{RF_Out}	Power gain step	Over process, temperature		0.62		dB
ΔP_{out}	Power gain flatness	Over 76 MHz ~ 108 MHz	-2		2	dB
P_{mask}	RF output spectrum mask[4]	120 kHz to 240 kHz offset		-50	-45	dBc
		240 kHz to 600 kHz offset		-45	-40	
		>600 kHz offset			-40	
F_{rf}	RF channel frequency		76		108	MHz
F_{ch}	Channel frequency step		50	100	200	kHz
F_{err}	Channel center frequency accuracy[6]		-2		2	kHz
F_{perr}	Pilot Tone frequency accuracy[1,6]		-2		2	Hz
F_{pk}	Modulation peak frequency deviation				75	kHz

SYMBOL	PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNIT

Notes:
1. Guaranteed by design.
2. 1000mVp-p, 1 kHz tone at ALI pin, no input signal at ARI pin.
3. Into matched antenna (see application note for details).
4. Within operating band 76 MHz to 108 MHz.
5. Value set with GAIN_TXPLT[3:0] (reg. 02h, bits 3:0). The user must conform to local regulatory requirements for low-power unlicensed FM broadcast operation when setting this value.
6. Required by FCC standard.

Table 7: Timing Characteristics

(Vcc = 2.7 ~ 5.0 V, T_A = -25 ~ 85 °C, unless otherwise noticed. Typical values are at Vcc = 3.3V and T_A = 25°C).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
τ_{pup}	Chip power-up time [1]	From rising edge of Power-On to PLL settled and transmitter ready for transmission.			0.1	Sec
τ_{chsw}	Channel switching time[1]	From any channel to any channel.			10	ms

Notes:
1. Guaranteed by design.

Table 8: I²C Interface Timing Characteristics

(Vcc = 2.7 ~ 5.0 V, T_A = -25 ~ 85 °C, unless otherwise noticed. Typical values are at Vcc = 3.3V and T_A = 25°C).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCL}	I²C clock frequency				400	kHz
t_{LOW}	Clock Low time		1.3			µs
t_{HI}	Clock High time		0.8			µs
t_{ST}	SCL input to SDA falling edge start [1,3]		0.6			µs
t_{STHD}	SDA falling edge to SCL falling edge start[3]		0.6			µs
t_{rc}	SCL rising edge[3]	Level from 30% to 70%			300	ns
t_{fc}	SCL falling edge[3]	Level from 70% to 30%			300	ns
t_{dtHD}	SCL falling edge to next SDA rising edge[3]		20			ns
t_{dtc}	SDA rising edge to next SCL rising edge[3]				900	ns
t_{stp}	SCL rising edge to SDA rising edge [2,3]		0.6			µs
t_w	Duration before restart[3]		1.3			µs
C_b	SCL, SDA capacitive loading[3]			10		pF

Notes:

1. Start signaling of I²C interface.
2. Stop signaling of I²C interface.
3. Guaranteed by design.

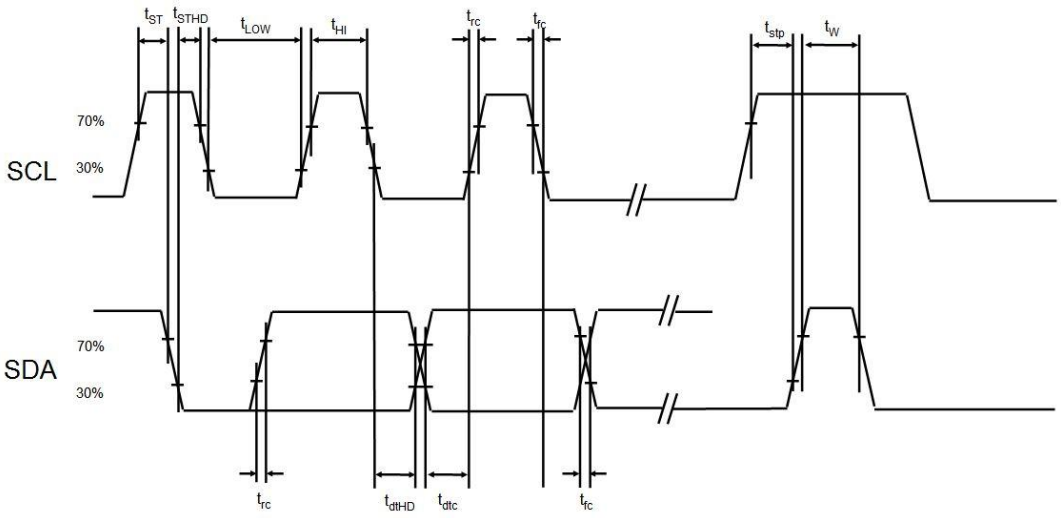


Figure 3: I²C Serial Control Interface Timing Diagram

4 FUNCTIONAL DESCRIPTION

The QN8027 is a high performance low power single chip FM transmitter IC that supports worldwide FM broadcast band operation. It has an IDLE mode for saving power. RDS/RBDS data service is also supported.

4.1 Transmit Mode

The QN8027 transmitter uses a highly digitized architecture. The input left and right analog audio signals are first adjusted by VGA, and then digitized by two high resolution ADCs into the digital domain. Pre-emphasis and MPX encoding are then performed. If RDS mode is enabled, the RDS signal will also be mixed with the MPX signal and the combined output will be fed into a high performance digital FM modulator which generates FM signal at RF carrier frequency. The FM signal is then filtered and amplified by the PA.

The QN8027 can deliver up to 119 dBμVp output signal to an external antenna and/or matching network. An RF VGA provides a 34dB output power control range in 0.62 dB steps and can be programmed through the serial control bus. Output power control and in-band power flatness can be easily achieved by a calibration circuit. This wide range of control allow for various antenna configurations such as loop, monopole, or meandering traces on PCB. An integrated RF bandpass filter ensures optimal output spectrum purity.

4.2 Idle Mode

The QN8027 features a low power IDLE mode for fast turn around and power savings. After power up, the QN8027 will enter IDLE mode automatically.

4.3 Audio Interface

The QN8027 has a highly flexible analog audio interface. For audio input, the signal is AC coupled with 3dB corner frequency less than 50Hz. It has 4 different input impedances and 15dB adjustable gain range. Digital gain provides more accurate gain control (in 1dB steps) to optimize the SNR and linearity. The gain setting can be manually set through the serial interface.

4.4 Audio Processing

The QN8027 supports audio AGC, programmable pre-emphasis. When there is no audio signal for a pre-determined period, AGC will power down the transmitter. A peak detector is also integrated to measure the input audio level. User can program VGA based on the peak value.

Stereo signal is generated by the MPX circuit. It combines the left and right channel signals in the following way:

$$m(t) = [L(t) + R(t)] + [L(t) - R(t)]\sin(4\pi ft + 2\theta_0) + \alpha\sin(2\pi ft + \theta_0) + d(t)\sin(6\pi ft + 3\theta_0)$$

Here, L(t) and R(t) correspond to the audio signals on left and right channels respectively, f = 19 kHz, θ is the initial phase of pilot tone and α is the magnitude of pilot tone, and d(t) is RDS signal. In mono mode, only the L+R portion of audio signal is transmitted. The 19 kHz pilot tone is generated by the MPX circuit which contributes 9% of peak modulation, and RDS signal will contribute 2.1% of peak modulation.

A pre-emphasis function is also integrated with both 75μs and 50μs time constants. The time constant can be programmed through the serial control interface.

4.5 Channel Setting

By programming channel index CH[9:0], the RF channel can be set to any frequency between 76 MHz ~ 108 MHz in 50 kHz steps. The channel index and RF frequency have the following relationship:

F_{RF} = *(76 + 0.05* x *Channel Index)*, where F_{RF} is the RF frequency in MHz.

The QN8027 has an integrated crystal oscillator and supports 12/24M Hz crystals. Alternatively, the QN8027 can be driven externally by clock source.

4.6 RDS/RBDS

The QN8027 supports RDS/RBDS data transmitting, including station ID, Meta data, TMC information, etc. RDS/RBDS data communicates with an external MCU through the serial control interface.

4.7 Power Setting

Reg 10H[6:0] 'PPA_TRGT' is used for PA output power control.

The PA output power expression of the PA output power is:

$$Power = (0.62 \times PA_{TRGT} + 71)\ dBuV$$

And the PA_TRRGT range is 20~75.

PA output power setting will not efficient immediately, it need to enter IDLE mode and re-enter TX mode, or when the frequency changed the PA output power setting will take effect.

5 CONTROL INTERFACE PROTOCOL

The QN8027 supports an I^{2}C serial interface. At power-on, all register bits are set to default values.

5.1 I^{2}C Serial Control Interface

QN8027 provides an I^{2}C-compatible serial interface. It consists of two wires; serial bi-directional data line (SDA) and input clock line (SCL). It operates as a slave on the bus and the slave address is 0101100c. The data transfer rate on the bus is up to 400 Kbit/s.

SDA must be stable during the high period of SCL, except for start and stop conditions. SDA can only change with SCL being low. A high-to-low transition on SDA while SCL is high indicates a start condition. A low-to-high transition on SDA while SCL is high indicates a stop condition.

An I^{2}C master initiates a data transfer by generating a start condition followed by the QN8027 slave address, MSB first, followed by a 0 to indicate a write cycle. After receiving an ACK from the QN8027 (by pulling SDA low), the master sends the sub-address of the register, or the first of a block of registers it wants to write, followed by one or more bytes of data, MSB first. The QN8027 acknowledges each byte after completion of each transfer. The I^{2}C master terminates the write operation by generating a stop condition (P).

The read operation consists of two phases. The first phase is the address phase. In this phase, an I^{2}C master initiates a write operation to the QN8027 by generating a start condition (S) followed by the QN8027 slave address, MSB first, followed by a 0 to indicate a write cycle. After receiving ACK from the QN8027, the master sends the sub-address of the register or the first of a block of registers it wants to read. After the cycle is acknowledged, the master terminates the cycle immediately by generating a stop condition (P).

The second phase is the data phase. In this phase, an I^{2}C master initiates a read operation to the QN8027 by generating a start condition followed by the QN8027 slave address, MSB first, followed by a 1 to indicate a read cycle. After an acknowledge from the QN8027, the I^{2}C master receives one or more bytes of data from the QN8027. The I^{2}C master acknowledges the transfer at the end of each byte. After the last data byte to be sent has been transferred from the QN8027 to the master, the master generates a NACK followed by a stop.

The timing diagrams below illustrate both write and read operations.

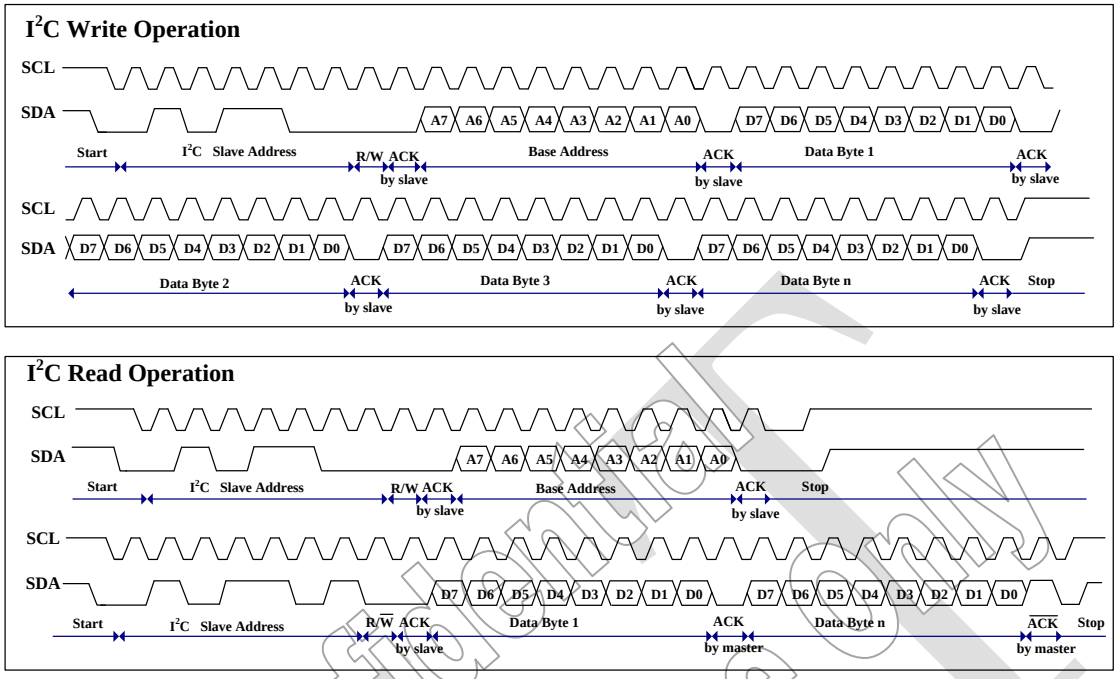


Figure 4: I²C Serial Control Interface Protocol

Notes:

1. The default IC address is 0101100.
2. "0x58" for a WRITE operation, "0x59" for a READ operation.

6 USER CONTROL REGISTERS

There are 19 user accessible control registers. All registers not listed below are for manufacturing use only.

Table 9: Summary of User Control Registers

REGISTER	NAME	USER CONTROL FUNCTIONS
00h	SYSTEM	Sets device modes, resets.
01h	CH1	Lower 8 bits of 10-bit channel index.
02h	GPLT	Audio controls, gain of TX pilot frequency deviation.
03h	REG_XTL	XCLK pin control.
04h	REG_VGA	TX mode input impedance, crystal frequency setting.
05h	CID1	Device ID numbers.
06h	CID2	Device ID numbers.
07h	STATUS	Device status indicators.
08h	RDSD0	RDS data byte 0.
09h	RDSD1	RDS data byte 1.
0Ah	RDSD2	RDS data byte 2.
0Bh	RDSD3	RDS data byte 3.
0Ch	RDSD4	RDS data byte 4.
0Dh	RDSD5	RDS data byte 5.
0Eh	RDSD6	RDS data byte 6.
0Fh	RDSD7	RDS data byte 7.
10h	PAC	PA output power target control.
11h	FDEV	Specify total TX frequency deviation.
12h	RDS	Specify RDS frequency deviation, RDS mode selection.

Register Bit R/W Status:

RO - *R*ead *O*nly: You can not program these bits.
WO - *W*rite *O*nly: You can write and read these bits; the value you read back will be the same as written.
R/W - *R*ead/*W*rite: You can write and read these bits; the value you read back can be different from the value written. Typically, the value is set by the chip itself.

Word: SYSTEM **Address: 00h**

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
swrst	recal	txreq	mono	mute	rdsrdy	ch[9]	ch[8]
r/w	wo	wo	wo	wo	wo	wo	wo

Bit	Symbol	Default	Description	
7	SWRST	0	Reset all registers to default values	
			0	Keep the current value.
			1	Reset to default values.
6	RECAL	0	Reset the state to initial states and recalibrate all blocks.	
			0	No reset. FSM runs normally.
			1	Reset the FSM. After this bit is de-asserted, FSM will go through all the power up and calibration sequence.
5	TXREQ	0	Transmission request:	
			0	Stay in IDLE mode.
			1	Enter Transmit mode.
4	MONO	0	Force MONO mode for transmission:	
			0	Stereo mode.
			1	MONO mode.
3	MUTE	0	Audio Mute enable:	
			0	Not Mute
			1	Mute
2	RDSRDY	0	RDS transmitting ready: If user want the chip transmitting all the 8 bytes in RDS0~RDS7, user should toggle this bit. Then the chip internally will fetch these bytes after completing transmitting of current group.	
1:0	CH[9:8]	01	Highest 2 bits of 10-bit channel index: Channel freq is (76+CH*0.05) MHz	

Word: CH1 **Address: 01h**

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
ch[7]	ch[6]	ch[5]	ch[4]	ch[3]	ch[2]	ch[1]	ch[0]
wo	wo	wo	wo	wo	wo	wo	wo

Bit	Symbol	Default	Description
7:0	CH[7:0]	0000 0000	Lower 8 bits of 10-bit Channel index. Channel used for TX.

Word: GPLT **Address: 02h**

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
tc	priv_en	T1m_sel[1]	T1m_sel[0]	gain_txplt[3]	gain_txplt[2]	gain_txplt[1]	gain_txplt[0]
wo	wo	wo	wo	wo	wo	wo	wo

Bit	Symbol	Default	Description	
7	TC	1	Pre-emphasis time constant.	
			TC	Time constant (us)
			0	50
			1	75
6	priv_en	0	Enable the privacy mode (audio scramble and RDS encryption)	
			priv_en	Privacy mode
			0	disabled
			1	enabled
5:4	t1m_sel[1:0]	10	Selection of 1 minute time for PA off when no audio. The real time is (58+t1m_sel) seconds	
			T1m_sel[1:0]	time
			00	58s
			01	59s
			10	60s
			11	Infinity (never)
3:0	GAIN_TXPLT[3:0]	1001	Gain of TX pilot to adjust pilot frequency deviation. Refer to peak frequency deviation of MPX signal when audio input is full scale.	
			GAIN_TXPLT[5:0]	value
			0111	7% * 75KHz
			1000	8% * 75KHz

			1001	9% * 75KHz
			1010	10% * 75KHz

Word: REG_XTL Address: 03h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
xinj[1]	xinj[0]	xisel[5]	xisel[4]	xisel[3]	xisel[2]	xisel[1]	xisel[0]
wo	wo	wo	wo	wo	wo	wo	wo

Bit	Symbol	Default	Description	
7:6	XINJ[1:0]	00	Select the reference clock source	
			XINJ[1:0]	Clock source
			00	Use crystal on XTAL1/XTAL2
			01	Inject digital clock from XTAL1
			10	Single end sine-wave injection on XTAL1
			11	Differential sine-wave injection on XTAL1/2
5:0	XISEL[5:0]	010000	Crystal oscillator current control. 6.25uA*XISEL[5:0], 0-400uA when use crystal on XTAL1/XTAL2.	

Word: REG_VGA Address: 04h

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
xsel	gvga[2]	gvga[1]	gvga[0]	GDB[1]	GDB[0]	rin[1]	rin[0]
wo	wo	wo	wo	wo	wo	wo	wo

Bit	Symbol	Default	Description				
7	XSEL	1	Crystal frequency selection				
			XSEL	XTAL frequency (MHz)			
			0	12			
			1	24			
6:4	GVGA[2:0]	011	TX input buffer gain (dB)				
			VGAG[2:0]	RIN[1:0]			
				00	01	10	11
			000	3	-3	-9	-15
			001	6	0	-6	-12
			010	9	3	-3	-9
			011	12	6	0	-6

			100	15	9	3	-3
			101	18	12	6	0
			11X	Reserved			
3:2	GDB[1:0]	00	TX digital gain				
			GDB[1:0]	Digital gain			
			00	0 dB			
			01	1 dB			
			10	2 dB			
			11	reserved			
1:0	RIN[1:0]	10	TX mode input impedance for both L/R channels.				
			RIN[1:0]	Input impedance (KΩ)			
			00	5			
			01	10			
			10	20			
			11	40			

Word: CID1 **Address: 05h (RO)**

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
cid0[2]	cid0[1]	cid0[0]	cid1[2]	cid1[1]	cid1[0]	cid2[1]	cid2[0]
ro	ro	ro	ro	ro	ro	ro	ro

Bit	Symbol	Default	Description	
7:5	CID0[2:0]	rrr	reserved	
4:2	CID1[2:0]	rrr 000	Chip ID for product family	
			CID1[2:0]	Product Family
			000	FM
			001-111	reserved
1:0	CID2[1:0]	rr 01	Chip ID for minor revision	
			CID2[1:0]	Minor revision
			00	1
			01	2
			10	3
			11	4

Word: CID2 **Address: 06h (RO)**

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
cid3[3]	cid3[2]	cid3[1]	cid3[0]	cid4[3]	cid4[2]	cid4[1]	cid4[0]
ro	ro	ro	ro	ro	ro	ro	ro

Bit	Symbol	Default	Description	
7:4	CID3[3:0]	rrrr 0100	Chip ID for product ID	
			CID3[2:0]	Product
			0100	QN8027
			others	reserved
3:0	CID4[3:0]	rrrr 0100	Chip ID for major revision is 1+CID4	
			CID4[3:0]	Revision number
			0000-1111	reserved

Word: STATUS **Address: 07h**

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
aud_pk[3]	aud_pk[2]	aud_pk[1]	aud_pk[0]	rds_upd	fsm[2]	fsm[1]	fsm[0]
ro	ro	ro	ro	ro	ro	ro	ro

Bit	Symbol	Default	Description	
7:4	aud_pk[3:0]	rrrr	Audio peak value at ADC input is aud_pk[3:0]*45mV	
3	RDS_UPD	r	RDS TX: To transmit the 8 bytes in RDS0~RDS7, the user should toggle the register bit RDSRDY. Then the chip internally fetches these bytes after completing transmitting the current group. Once the chip has internally fetched these bytes, it will toggle this bit, and the user can write in another group.	
2:0	FSM[2:0]	rrr	Top FSM state code	
			FSM[2:0]	FSM status
			000	RESET
			001	CALI
			010	IDLE

			011	TX_RSTB
			100	PA calibration
			101	Transmit
			110	PA_OFF
			111	reserved

Word: RDSD0 **Address: 08h**

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
rdsd0[7]	rdsd0[6]	rdsd0[5]	rdsd0[4]	rdsd0[3]	rdsd0[2]	rdsd0[1]	rdsd0[0]
wo	wo	wo	wo	wo	wo	wo	wo

Bit	Symbol	Default	Description
7:0	RDSD0	00000000	RDS data byte0 to be sent: Data written into RDSD0~RDSD7 can not be sent out if user didn't toggle RDSRDY to allow the data to be loaded into the internal transmitting buffer.

Word: RDSD1 **Address: 09h**

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
rdsd1[7]	rdsd1[6]	rdsd1[5]	rdsd1[4]	rdsd1[3]	rdsd1[2]	rdsd1[1]	rdsd1[0]
wo	wo	wo	wo	wo	wo	wo	wo

Bit	Symbol	Default	Description
7:0	RDSD1[7:0]	0000 0000	RDS data byte 1

Word: RDSD2 **Address: 0Ah**

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
rdsd2[7]	rdsd2[6]	rdsd2[5]	rdsd2[4]	rdsd2[3]	rdsd2[2]	rdsd2[1]	rdsd2[0]
wo	wo	wo	wo	wo	wo	wo	wo

Bit	Symbol	Default	Description
7:0	RDSD2[7:0]	0000 0000	RDS data byte 2

Word: RDSD3 **Address: 0Bh**

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
rdsd3[7]	rdsd3[6]	rdsd3[5]	rdsd3[4]	rdsd3[3]	rdsd3[2]	rdsd3[1]	rdsd3[0]
wo	wo	wo	wo	wo	wo	wo	wo

Bit	Symbol	Default	Description
7:0	RDSD3[7:0]	0000 0000	RDS data byte 3

Word: RDSD4 **Address: 0Ch**

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
rdsd4[7]	rdsd4[6]	rdsd4[5]	rdsd4[4]	rdsd4[3]	rdsd4[2]	rdsd4[1]	rdsd4[0]
wo	wo	wo	wo	wo	wo	wo	wo

Bit	Symbol	Default	Description
7:0	RDSD4[7:0]	0000 0000	RDS data byte 4

Word: RDSD5 **Address: 0Dh**

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
rdsd5[7]	rdsd5[6]	rdsd5[5]	rdsd5[4]	rdsd5[3]	rdsd5[2]	rdsd5[1]	rdsd5[0]
wo	wo	wo	wo	wo	wo	wo	wo

Bit	Symbol	Default	Description
7:0	RDSD5[7:0]	0000 0000	RDS data byte 5

Word: RDSD6 **Address: 0Eh**

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
rdsd6[7]	rdsd6[6]	rdsd6[5]	rdsd6[4]	rdsd6[3]	rdsd6[2]	rdsd6[1]	rdsd6[0]
wo	wo	wo	wo	wo	wo	wo	wo

Bit	Symbol	Default	Description
7:0	RDSD6[7:0]	0000 0000	RDS data byte 6

Word: RDSD7 **Address: 0Fh**

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
rdsd7[7]	rdsd7[6]	rdsd7[5]	rdsd7[4]	rdsd7[3]	rdsd7[2]	rdsd7[1]	rdsd7[0]
wo	wo	wo	wo	wo	wo	wo	wo

Bit	Symbol	Default	Description
7:0	RDSD7[7:0]	0000 0000	RDS data byte 7

Word: PAC **Address: 10h**

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
txpd_clr	pa_trgt[6]	pa_trgt[5]	pa_trgt[4]	pa_trgt[3]	pa_trgt[2]	pa_trgt[1]	pa_trgt[0]
wo	wo	wo	wo	wo	wo	wo	wo

Bit	Symbol	Default	Description
7	TXPD_CLR	0	TX aud_pk clear signal: Audio peak value is max-hold and stored in aud_pk[3:0]. Once TXPD_CLR is toggled, the aud_pk value is cleared and restarted again.
6:0	PA_TRGT[6:0]	111 1111	PA output power target is 0.62*PA_TRGT+71dBu. Valid values are 20-75.

Word: FDEV **Address: 11h**

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
tx_fdev[7]	tx_fdev[6]	tx_fdev[5]	tx_fdev[4]	tx_fdev[3]	tx_fdev[2]	tx_fdev[1]	tx_fdev[0]
wo	wo	wo	wo	wo	wo	wo	wo

Bit	Symbol	Default	Description	
7:0	TX_FDEV[7:0]	10000001	Specify total TX frequency deviation: TX frequency deviation = 0.58 kHz*TX_FDEV.	
			TX_FDEV[7:0]	value
			0000 0000 - 1111 1111	0 ~ 255

Word: RDS **Address: 12h**

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
rdsen	rdsfdev[6]	rdsfdev[5]	rdsfdev[4]	rdsfdev[3]	rdsfdev[2]	rdsfdev[1]	rdsfdev[0]
wo	wo	wo	wo	wo	wo	wo	wo

Bit	Symbol	Default	Description	
7	RDSEN	0	RDS enable:	
			0	RDS disable
			1	RDS enable
6	RDSFDEV[6:0]	000 0110	Specify RDS frequency deviation: RDS frequency deviation = 0.35KHz*RDSFDEV.	
			RDSFDEV[6:0]	Value
			000 0000 – 111 1111	0~127

7 ORDERING INFORMATION

Part Number	Description	Package
QN8027-SANC	The QN8027 is a high performance, low power, full-featured single-chip stereo FM transmitter designed for portable audio/video players, automotive accessories, cell phones, and GPS personal navigation devices.	3x3 mm Body [MSOP10]

8 PACKAGE DESCRIPTION

10-Lead plastic package – 3x3 mm Body [MSOP]

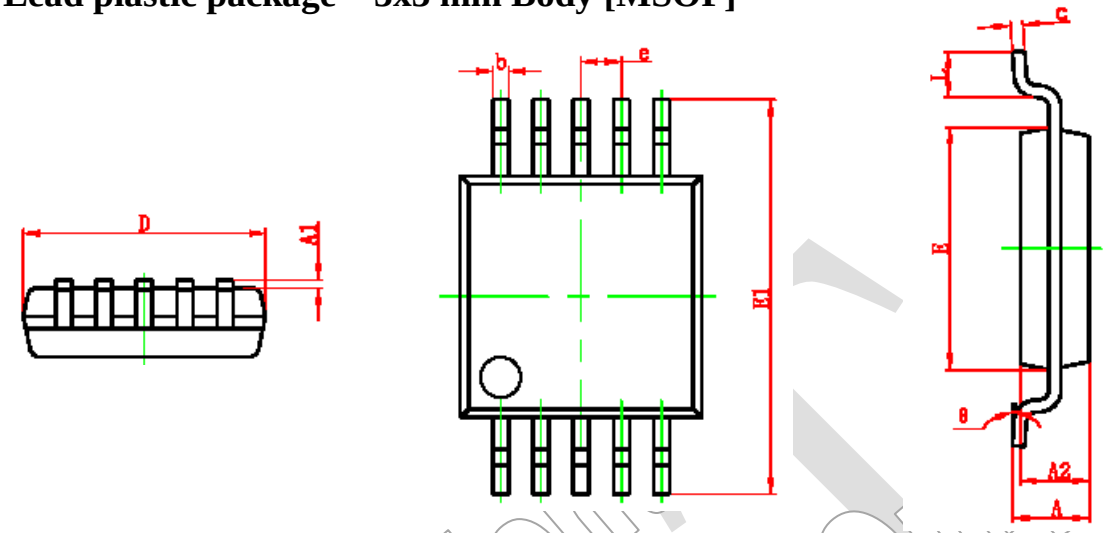


Figure 5: MSOP10 Package Outline Dimensions

Symbol	Description	Millimeters		
		Minimum	Nominal	Maximum
A	Overall package height	0.820	0.95	1.100
A1	Board standoff	0.020	-	0.150
A2	Package thickness	0.750	0.85	0.950
b	Lead width	0.180	0.23	0.280
c	Lead thickness	0.090	-	0.230
D	Package's outside, X-axis	2.900	3.00	3.100
e	Lead pitch		0.50 (BSC)	
E	Package's outside, Y-axis	2.900	3.00	3.100
E1	Lead to lead, Y-axis	4.750	4.90	5.050
L	Foot length	0.400	0.60	0.800
θ	Foot to board angle	0°	-	6°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the area indicated in the drawing.
2. Dimensioning and tolerance per ASME Y 14.5M.
   BSC: Basic Dimension. The theoretically exact value is shown without tolerance.

Carrier Tape Dimensions

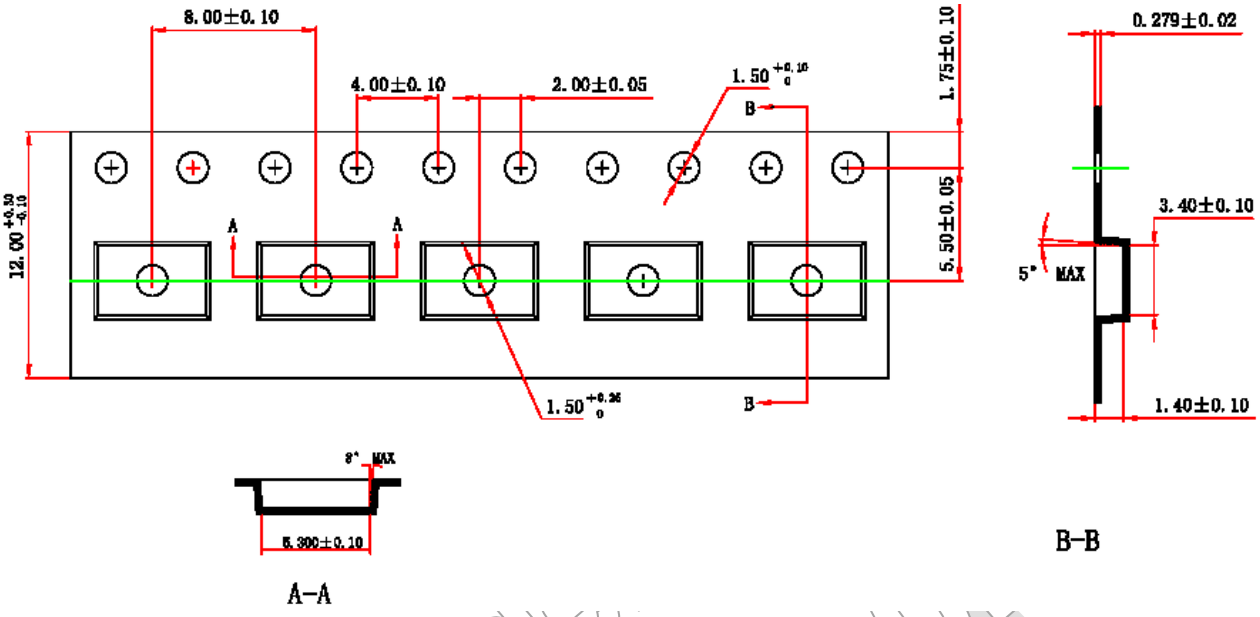


Figure 6: MSOP10 Carrier Tape Drawing

NOTES:

1. 10 sprocket hole pitch cumulative tolerance ±0.2mm maximum.
2. Camber not to exceed 1mm in 100mm: ≤1mm/100mm.
3. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

9 SOLDER REFLOW PROFILE

9.1 Package Peak Reflow Temperature

QN8027 is assembled in a lead-free MSOP package. Since the geometrical size of QN8027 is 3 mm × 3 mm × 0.95 mm, the volume and thickness is in the category of volume<350 mm^3 and thickness<1.6 mm in Table 4-2 of IPC/JEDEC J-STD-020C. The peak reflow temperature is:

$$T_p = 260^o C$$

The temperature tolerance is +0°C and -5°C. Temperature is measured at the top of the package.

9.2 Classification Reflow Profiles

Profile Feature		Specification*
Average Ramp-Up Rate (tsmax to tP)		3°C/second max.
Pre-heat:	Temperature Min (Tsmin)	150°C
	Temperature Max (Tsmax)	200°C
	Time (ts)	60-180 seconds
Time maintained above:	Temperature (T_L)	217°C
	Time (t_L)	60-150 seconds
Peak/Classification Temperature (Tp)		260°C
Time within 5°C of Actual Peak Temperature (tp)		20-40 seconds
Ramp-Down Rate		6°C/second max.
Time 25°C to Peak Temperature		8 minutes max.

*Note: All temperatures are measured at the top of the package.

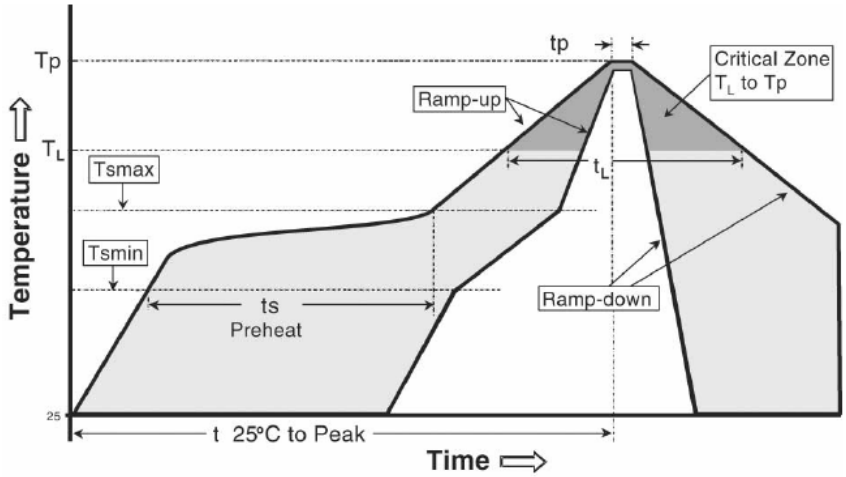


Figure 7: Reflow Temperature Profile

9.3 Maximum Reflow Times

All package reliability tests were performed and passed with a pre-condition procedure that repeat a reflow profile, which conforms to the requirements in **Section 9.2, three (3)** times.

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