QuickLogic PolarPro™ Data Sheet

QUICKLOGIC®

Combining Low Power, Performance, Density, and Embedded RAM

Device Highlights

Flexible Programmable Logic

- 0.18 µm, six layer metal CMOS process
- 1.8 V core voltage, 1.8/2.5/3.3 V drive capable I/Os
- Up to 202 kilobits of SRAM
- Up to 292 I/Os available
- Up to one million system gates
- Nonvolatile, instant-on
- IEEE 1149.1 boundary scan testing compliant

Embedded Dual Port SRAM

- Up to eight dual-port 4-kilobit high performance SRAM blocks
- Embedded synchronous/asynchronous FIFO controller
- Configurable and cascadable aspect ratio

Programmable I/O

- Bank programmable drive strength
- Bank programmable slew rate control
- Independent I/O banks capable of supporting multiple I/O standards in one device
- Native support for DDR I/Os
- Bank programmable I/O standards: LVTTL, LVCMOS, and LVCMOS18

Advanced Clock Network

- Multiple low skew clock networks
  - 1 dedicated global clock network
  - 4 programmable global clock networks
- Quadrant-based segmentable clock networks
  - 20 quad clock networks per device
  - 4 quad clock networks per quadrant
  - 1 dedicated clock network per quadrant
- Two user Configurable Clock Managers (CCMs)

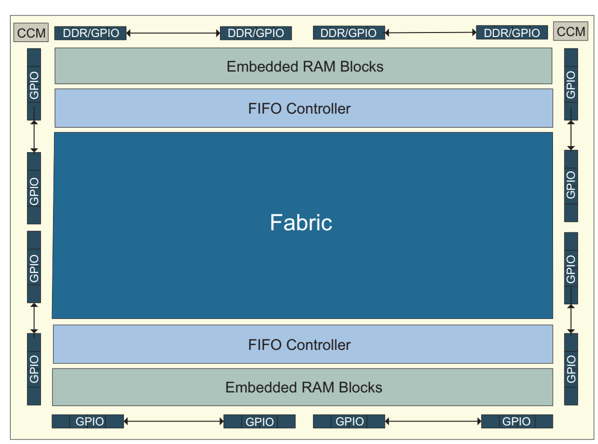
Very Low Power (VLP) Mode

- QuickLogic PolarPro has a special VLP pin which can enable a low power sleep mode that significantly reduces the overall power consumption of the device.
- Enter VLP mode from normal operation in less than 250 µs
- Exit from VLP mode to normal operation in less than 250 µs

Security Links

There are several security links to disable JTAG access to the device. Programming these optional links completely disables access to the device from the outside world and provides an extra level of design security not possible in SRAM-based FPGAs.

Figure 1: QuickLogic PolarPro Block Diagram



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Ultra-Low Power FPGA Combining Performance, Density, and Embedded RAM

Table 1: PolarPro Product Family Members

Features		QL1P075	QL1P100	QL1P150	QL1P300	QL1P600	QL1P1000
Max Gates		75,000	100,000	150,000	300,000	600,000	1,000,000
Logic Cells		512	640	1,536	1,920	4,224	7,680
Max I/O		172	188	292	302	508	652
RAM Modules		8	8	12	12	22	22
FIFO Controllers		8	8	12	12	22	22
RAM bits		36,864	36,864	55,296	55,296	202,752	202,752
CCMs		2	2	2	2	2	2
Packages	TFBGA (0.8 mm)	196	196	-	-	-	-
	TQFP (0.5 mm)	144	144	-	-	-	-
	LBGA (1.0 mm)	256	256	256, 324	256, 324	256, 324	256, 324

Process Data

QuickLogic PolarPro is fabricated on a 0.18 μ, six layer metal CMOS process. The core voltage is 1.8 V. The I/O voltage input tolerance and output drive can be set as 1.8 V, 2.5 V, and 3.3 V.

Programmable Logic Architectural Overview

The QuickLogic PolarPro logic cell structure presented in **Figure 2** is a single register, multiplexer-based logic cell. It is designed for wide fan-in and multiple, simultaneous output functions. The cell has a high fan-in, fits a wide range of functions with up to 24 simultaneous inputs (including register control lines), and four outputs (three combinatorial and one registered). The high logic capacity and fan-in of the logic cell accommodates many user functions with a single level of logic delay.

The QuickLogic PolarPro logic cell can implement:

- Two independent 3-input functions
- Any 4-input function
- 8 to 1 mux function
- Independent 2 to 1 mux function
- Single dedicated register with clock enable, active high set and reset signals
- Direct input selection to the register, which allows combinatorial and register logic to be used separately
- Combinatorial logic that can also be configured as an edge-triggered master-slave D flip-flop

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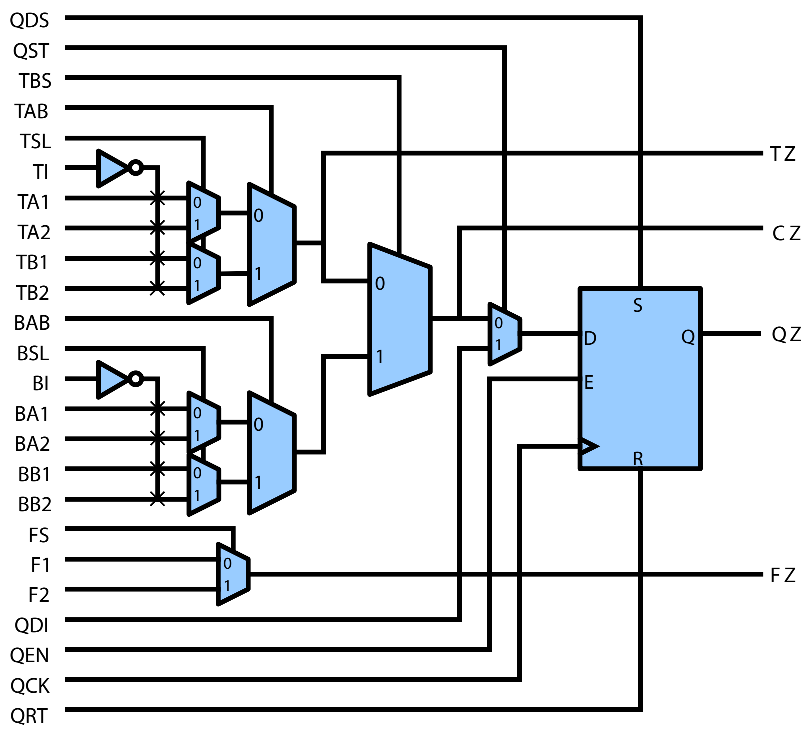
Figure 2: PolarPro Logic Cell



RAM Modules

The QuickLogic PolarPro family of devices includes up to eight 4-kilobit of dual-port RAM modules for implementing RAM and FIFO functions as shown in **Figure 3**.

The RAM features include:

- Independently configurable read and write data bus widths
- Independent read and write clocks
- Horizontal and vertical concatenation
- Write byte enables
- Selectable pipelined or non-pipelined read data

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Figure 3: 4-Kilobit Dual-Port RAM Block

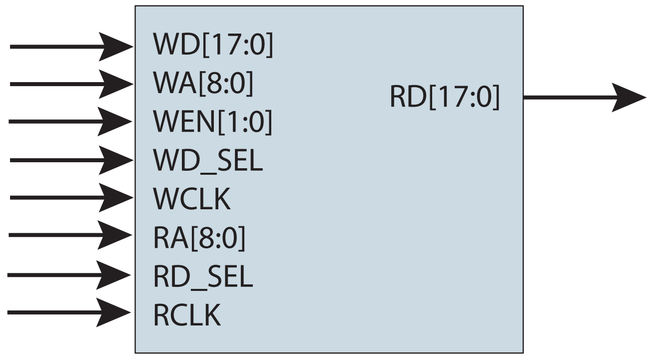

Table 2: RAM Interface Signals

Signal Name	Function
Inputs	
WD [17:0]	Write Data
WA [8:0]	Write Address
WEN [1:0]	Write Enable (two 9-bit enables)
WD_SEL	Write Chip Select
WCLK	Write Clock
RA [8:0]	Read Address
RD_SEL	Read Chip Select
RCLK	Read Clock
Output	
RD [17:0]	Read Data

The read and write data buses of a RAM block can be arranged to variable bus widths. The bus widths can be configured using the RAM Wizard available in QuickWorks, QuickLogic's development software. The selection of the RAM depth and width determines how the data is addressed.

The RAM blocks also support data concatenation. Designers can cascade multiple RAM modules to increase the depth or width by connecting corresponding address lines together and dividing the words between modules. Generally, this requires the use of additional programmable logic resources. However, when concatenating only two 4-kilobit RAM blocks, they can be concatenated horizontally or vertically without using any additional programmable fabric resources.

For example, two internal dual-port RAM blocks concatenated vertically to create a 512x18 RAM block or horizontally to create a 256x36 RAM block. A block diagram of horizontal and vertical concatenation is displayed in **Figure 4**.

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Figure 4: Horizontal and Vertical Concatenation Examples

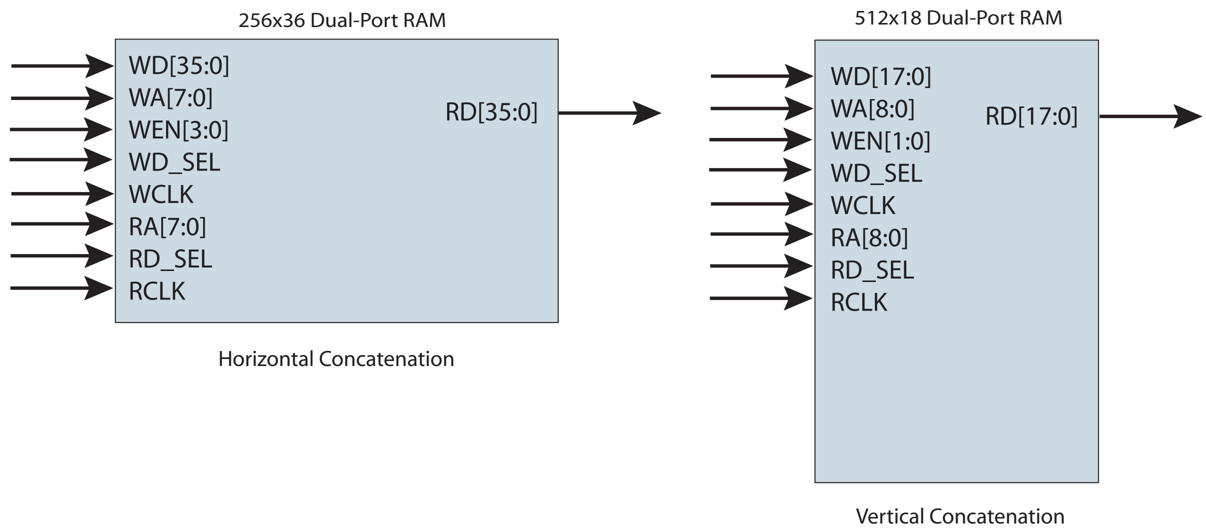

Table 3 shows the various RAM configurations supported by the PolarPro RAM modules.

Table 3: Available Dual-Port RAM Configurations

Number of RAM Blocks	Depth	Width
1	256	1 to 18
1	512	1 to 9
2	256	1 to 36
2	512	1 to 18
2	1024	1 to 9

True Dual-Port RAM

PolarPro dual-port RAM modules can also be concatenated to generate true dual-port RAMs. The true dual-port RAM module's Port1 and Port2 have completely independent read and write ports, and separate read and write clocks. This allows Port1 and Port2 to have different data widths and clock domains. It is important to note that there is no circuitry preventing a write and read operation to the same address space at the same time. Therefore, it is up to the designer to ensure that the same address is not read from and written to simultaneously, otherwise the data is considered invalid. Likewise, the same address must not be written to from both ports at the same time. However, it is possible to read from the same address. **Figure 5** shows an example of a 512x18 true dual-port RAM.

Figure 5: 512x18 True Dual-Port RAM Block

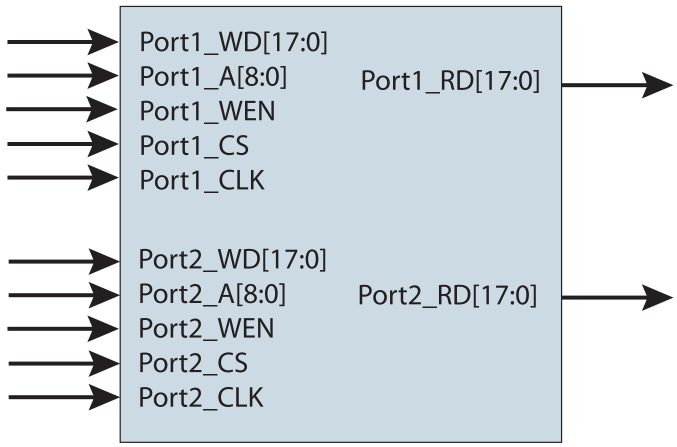

Table 4: True Dual-Port RAM Interface Signals

Port	Signal Name	Function
Port1	**Inputs**	
	Port1_WD[17:0]	Write Data
	Port1_A[8:0]	Write Address
	Port1_WEN	Write Enable
	Port1_CS	Chip Select
	Port1_CLK	Clock
	Output	
	Port1_RD[17:0]	Read Data
Port2	**Inputs**	
	Port2_WD[17:0]	Write Data
	Port2_A[8:0]	Write Address
	Port2_WEN	Write Enable
	Port2_CS	Chip Select
	Port2_CLK	Clock
	Output	
	Port2_RD[17:0]	Read Data

Table 5: Available True Dual-Port RAM Configurations

Number of RAM Blocks	Depth	Width
2	512	1 to 18
2	1024	1 to 9

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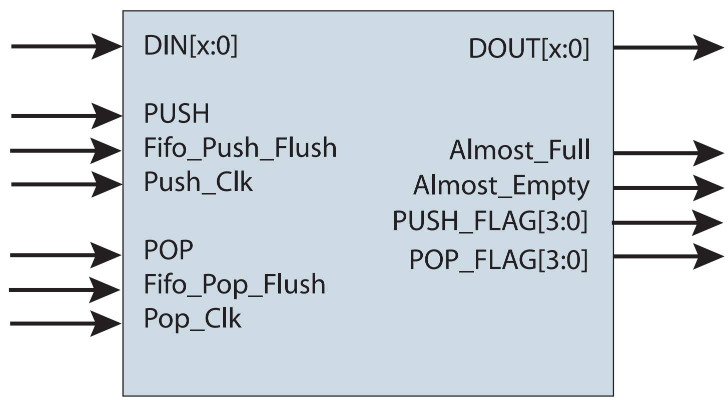
Embedded FIFO Controllers

Every 4-kilobit RAM block can be implemented as a synchronous or asynchronous FIFO. There are built-in FIFO controllers that allow for varying depths and widths without requiring programmable fabric resources.

The PolarPro FIFO controller features include:

- x9, x18 and x36 data bus widths
- Independent PUSH and POP clocks
- Independent programmable data width on PUSH and POP sides
- Configurable synchronous or asynchronous FIFO operation
- 4-bit PUSH and POP level indicators to provide FIFO status outputs for each port
- Pipelined read data to improve timing

Figure 6: FIFO Module



NOTE: x = {1,2,3,...35}.

Table 6: Available FIFO Configurations

Number of RAM Blocks Used	Depth	Supported Widths
1	256	1 to 18 bits
1	512	1 to 9 bits
2	256	1 to 36 bits
2	512	1 to 18 bits
2	1024	1 to 9 bits

Table 7 lists the FIFO controller interface signals.

Table 7: FIFO Interface Signals

Signal Name	Width (bits)	Direction	Function
PUSH Signals			
DIN	1 to 36	I	Data bus input
PUSH	1	I	Initiates a data push
Fifo_Push_Flush	1	I	Empties the FIFO
Push_Clk	1	I	Push data clock
POP Signals			
DOUT	1 to 36	O	Data bus output
POP	1	I	Initiates a data pop
Fifo_Pop_Flush	1	I	Empties the FIFO
Pop_Clk	1	I	Pop data clock
Status Flags			
Almost_Full	1	O	Asserted when FIFO has one location available
Almost_Empty	1	O	Asserted when FIFO has one location used
PUSH_FLAG[3:0]	4	O	FIFO PUSH level indicator
POP_FLAG[3:0]	4	O	FIFO POP level indicator

Table 8 and **Table 9** highlight the corresponding FIFO level indicator for each 4-bit value of the PUSH_FLAG and POP_FLAG outputs.

Table 8: FIFO PUSH Level Indicator Values

Value	Status
0000	Full
0001	Empty
0010	Room for more than one-half
0011	Room for more than one-forth
1000	Room for 8 or more
1001	Room for 7
1010	Room for 6
1011	Room for 5
1100	Room for 4
1101	Room for 3
1110	Room for 2
1111	Room for 1
Others	Reserved

Table 9: FIFO POP Level Interface Signals

Value	Status
0000	Empty
0001	1 entry in FIFO
0010	2 entries in FIFO
0011	3 entries in FIFO
1000	4 entries in FIFO
1010	5 entries in FIFO
1100	6 entries in FIFO
1110	7 entries in FIFO
1000	8 or more entries in FIFO
1101	One-forth or more full
1110	One-half or more full
1111	Full
Others	Reserved

FIFO Flush Procedure

Both PUSH and POP domains are provided with a flush input signal synchronized to their respective clocks. When a flush is triggered from one side of the FIFO, the signal propagates and re-synchronizes internally to the other clock domain. During a flush operation, the values of the FIFO flags are invalid for a specific number of cycles (see **Figure 7** and **Figure 8**).

As shown in **Figure 7**, when the **Fifo_Push_Flush** asserts, the **Almost_Full** and **PUSH_FLAG** signals become invalid until the FIFO can flush the data with regards to the Push clock domain as well as the Pop clock domain. After the **Fifo_Push_Flush** is asserted, the next rising edge of the Pop clock starts the Pop flush routine.

Figure 7 illustrates a FIFO Flush operation. After the **Fifo_Push_Flush** is asserted at 2 (**PUSH_Clk**), four POP clock cycles (12 through 15) are required to update the **POP_FLAG**, and **PUSH_FLAG** signals. The **Almost_Empty** signal is asserted to indicate that the push flush operation has been completed. On the following rising edge of the **PUSH_Clk** (8), the **PUSH_FLAG** is accordingly updated to reflect the successful flush operation.

Figure 7: FIFO Flush from PUSH Side

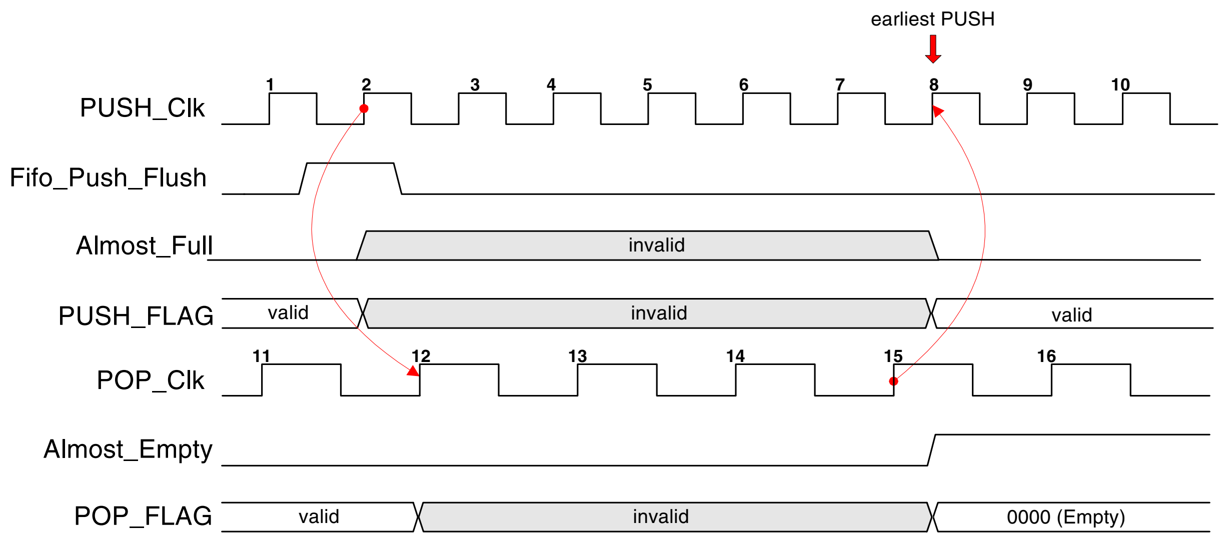


Figure 8 illustrates a POP flush operation. After the **Fifo_Pop_Flush** is asserted at 2 (**POP_Clk**), four PUSH clock cycles (12 through 15) are required to update the **POP_FLAG**, and **PUSH_FLAG** signals. The **Almost_Empty** signal is asserted to indicate that the pop flush operation has been completed. On the following rising edge of the **POP_Clk** (8), the **POP_FLAG** is updated accordingly to reflect the successful flush operation.

Figure 8: FIFO Flush from POP Side

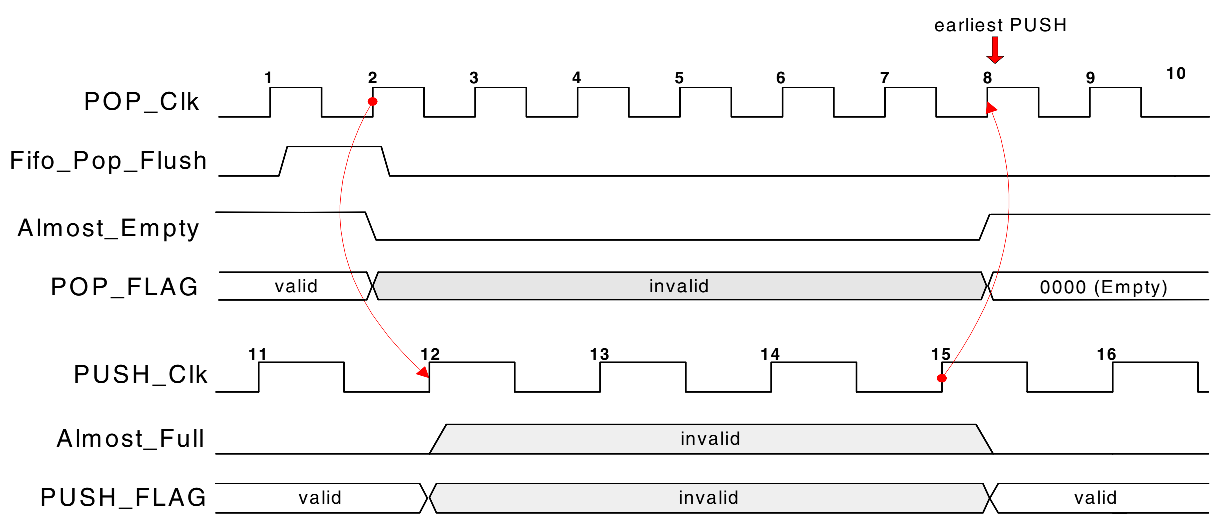


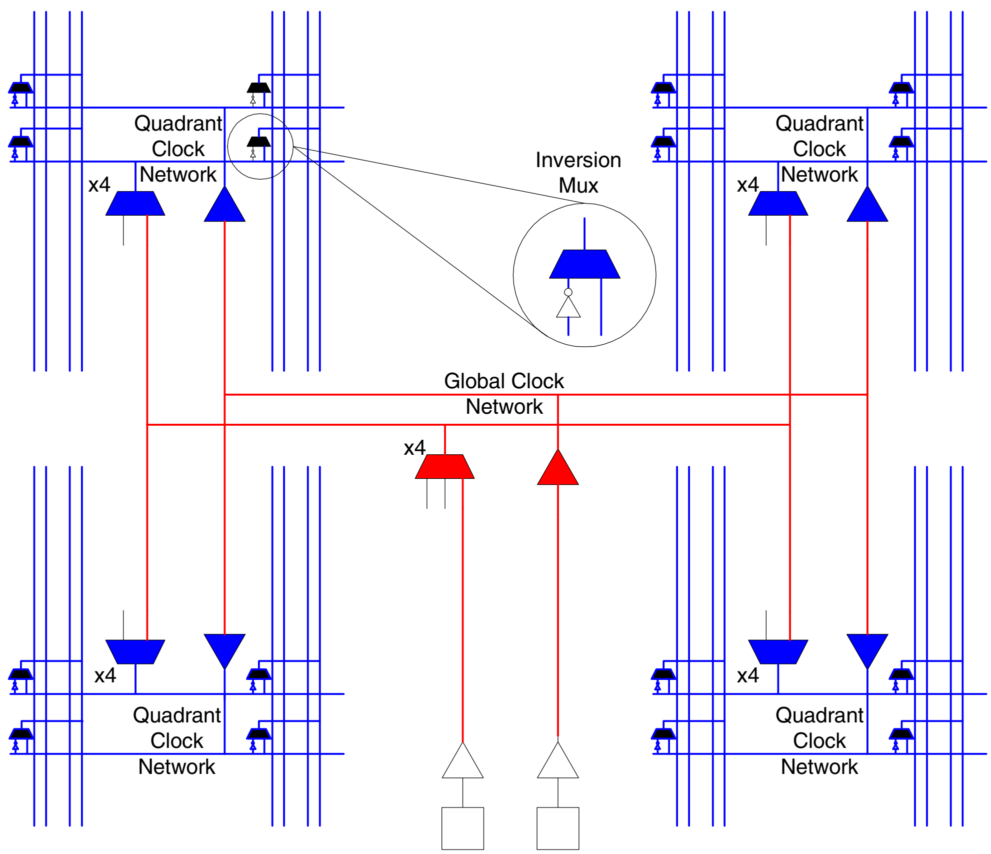
Figure 7 and **Figure 8** are only true for this particular PUSH-POP clock frequency combination. The clock frequency and phase difference between POP_Clk and PUSH_Clk can cause an additional flush delay of one clock cycle in either domain because of the asynchronous relationship between the two clocks.

Distributed Clock Networks

Global Clocks

The PolarPro clock network architecture consists of a 2-level H-tree network as shown in **Figure 9**. The first level of each clock tree (high-lighted in red) spans from the clock input pad to the global clock network and to the center of each quadrant of the chip. The second level (high-lighted in blue) spans from the quadrant clock network to every logic cell inside that quadrant. There are five global clocks in the global clock network, and five quadrant clocks in each quadrant clock network. All global clocks drive the quadrant clock network inputs. The quadrant clocks output to clock inversion muxes, which pass either the original input clock or an inverted version of the input clock to the logic cells in that quadrant. The clock networks can drive RAM block clock inputs and reset, set, enable, and clock inputs to I/O registers. Furthermore, the quadrant clock outputs can be routed to all logic cell inputs.

Figure 9: Global Clock Architecture



Of the five global clock networks, four can be either driven directly by clock pads, Configurable Clock Manager (CCM) outputs, or internally generated signals. These four clock nets go through 3-input global clock muxes located in the middle of the die. See **Figure 10** for a diagram of a 3-input global clock mux. The fifth is a dedicated global clock network that goes directly to the quadrant quad-net clock network and is used as a dedicated fast clock.

Figure 10: Global Clock Structure

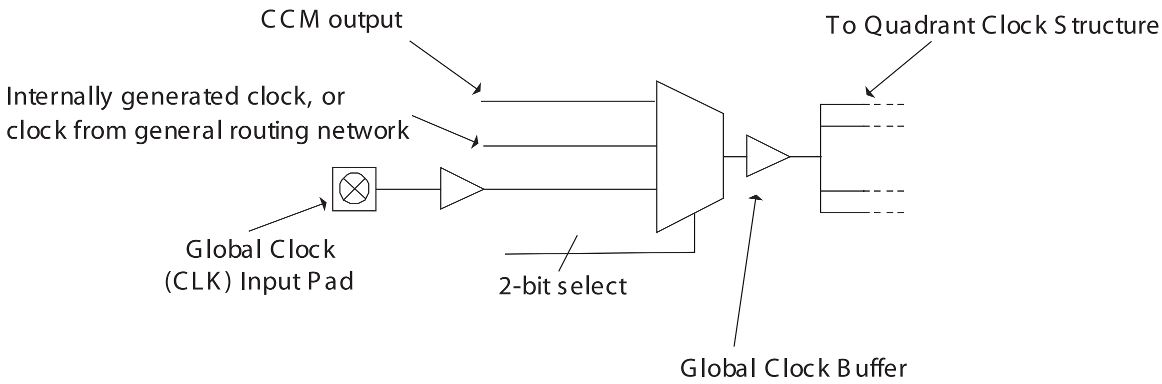
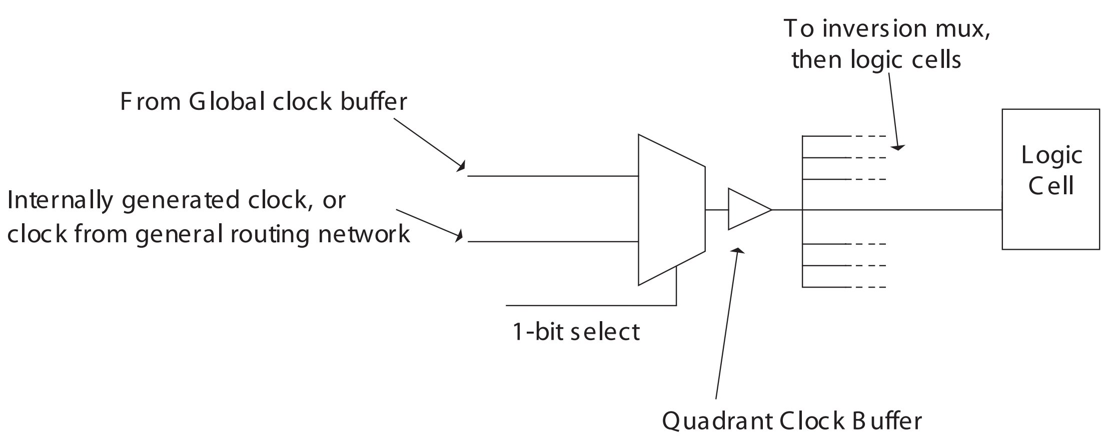


Figure 11 illustrates the quadrant clock 2-input mux.

Figure 11: Quadrant Clock Structure



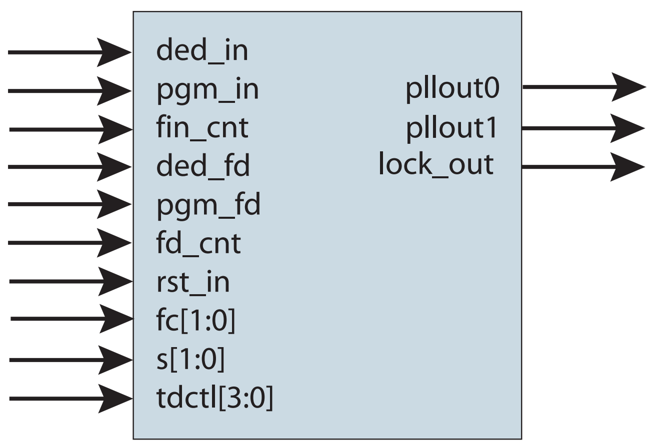
It is important to note that the select lines for the global clock and quad-net muxes are static signals and cannot be changed dynamically during device operation. For more information about global and quad-net clock networks and how to use them, refer to *Application Note 85 Clock Networks in PolarPro Devices* at http://www.quicklogic.com/images/appnote85.pdf.

Configurable Clock Managers

The CCM features include:

- Input frequency range from 25 MHz to 150 MHz
- Output frequency range from 25 MHz to 300 MHz
- Output jitter is less than 200 ps
- Two outputs: pullout0 (with 0° phase shift), and pullout1 (with an option of 0°, 90°, 180°, or 270° phase shift plus a programmable delay).
- Programmable delay allows delays up to 2.5 ns at 250 ps intervals
- CCM inputs can be driven from either a clock input pad or internal routing
- Programmable or fixed feedback path

Figure 12: Configurable Clock Manager



The reset signal can be routed from a clock pad or generated using internal logic. The lock_out signal can be routed to internal logic and/or an output pad. Both CCM clock outputs can drive the global clock networks, as well as any general purpose I/O pin. Once the CCM has synchronized the output clock to the incoming clock, the lock_out signal will be asserted to indicate that the output clock is valid. Lock detection requires at least 2 µs after reset to assert lock_out. The PolarPro CCMs have three modes of operation, based on the input frequency and desired output frequency. **Table 10** indicates the features of each mode.

Table 10: CCM PLL Mode Frequencies

Output Frequency	Input Frequency Range	Output Frequency Range	PLL Mode
x1	25 MHz to150 MHz	25 MHz to 150 MHz	PLL_MULT1
x2	25 MHz to 150 MHz	50 MHz to 300 MHz	PLL_MULT2
x4	25 MHz to 75 MHz	100 MHz to 300 MHz	PLL_MULT4

CCM Signals

Table 11 provides the name, direction, function and description of the CCM ports.

Table 11: CCM Signals

Signal Name	Direction	Function	Description
Routable Ports			
ded_in	I	Dedicated Input	Clock pad CCM input source.
pgm_in	I	Programmable Input	Internal logic CCM input source.
ded_fd	I	Dedicated Feedback	Automatically calculated and routed by the software tools.
pgm_fd	I	Programmable Feedback	Routed from internal logic. Configured by the user.
rst_in	I	Reset	Active high reset: If rst_in is asserted, pllout0 and pllout1 are reset to 0. This signal must be asserted and then released for lock_out to assert.
pllout0	O	0° Phase Clock	0° phase clock output.
pllout1	O	Configurable Phase Clock	0°, 90°,180°, or 270° phase clock output with programmable delay.
lock_out	O	Lock Detect	Active high lock detection signal. Active when the pllout signals correctly output the configured functionality.
Static Ports			
fin_cnt	I	Clock Input Control	Mux signal that selects between the dedicated or programmable clock input.
fd_cnt	I	Feedback Control	Mux signal that selects between the dedicated or programmable feedback input.
fc[1:0]	I	Phase Shift Control	Determines whether pllout1 is 0°, 90°, 180°, or 270° degrees out of phase with pllout0.
s[1:0]	I	Set Mode	Determines pllout1 and pllout0 frequency multiplier (x1, x2, or x4).
tdctl[3:0]	I	Time Delay Control	Pllout1 programmable delay, configurable in 250 ps increments up to a maximum of 2.5 ns. NOTE: 205 ps can vary depending on process variation.

Table 12, **Table 13**, and **Table 14** give the values used to configure the Set Mode, Phase Shift Control and Time Delay Control bits.

Table 12: Set Mode Values

pllout0/ pllout1	Multiplier
00	x1
01	x2
10	x4
11	Reserved

Table 13: Phase Shift Control Values

fc[1:0]	Phase Shift (Deg.)
00	0
01	90
10	180
11	270

Table 14: Time Delay Control Values

tdctl[3:0]	Time Delay (ps)
0000	0
0001	250
0010	500
0011	750
0100	1000
0101	1250
0110	1500
0111	1750
1000	2000
1001	2250
1010	2500
1011	Reserved
1100	Reserved
1101	Reserved
1110	Reserved
1111	Reserved

CCM Configurations

The main purpose of the CCM is to align the clock arrival times of two separate clock destinations, whether it is within the FPGA or external to the chip. The difference between the two clock destinations is referred to as clock skew. To correct for clock skew the CCMs can be configured to shift the phase and/or delay of the pllout1 clock output.

In most cases the desired phase or added delay can be accomplished by configuring both the clock source input and feedback input as dedicated. In the case of a dedicated clock source and dedicated feedback, the QuickLogic development software calculates and generates all of the required routing delays to produce the requested configuration. However, if a more specific delay is required, the programmable feedback path can be configured to generate the desired pllout0 and pllout1 output.

To accomplish this task the relationship between the CCM input clock source and feedback path must be understood. Specifically, the delay from the clock source to the CCM input, the delay from the CCM to the destination, and the delay from the destination to the CCM feedback input must all be taken into account. For the purpose of this document these delays are defined as:

Δ A = Delay from the source clock or clock I/O pad to the input of the CCM

Δ B = Delay from the output of the CCM to the destination logic element

Δ C = Delay from internal or external destination to the CCM

Figure 13 shows a representation of the corresponding delays. In **Figure 13** the combination of the various delays associated from one location to another are graphically represented by a single buffer.

Figure 13: CCM Routing

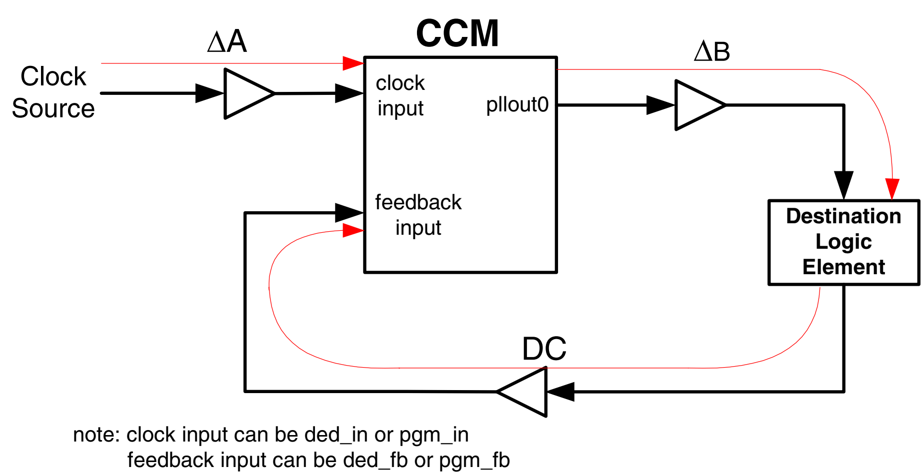


Table 15: Available Configurations

CCM Case	Clock	Feedback	Example Usage	Comments
1	Dedicated clock pad	Dedicated feedback	Standard PLL application. Reduce set-up and hold time requirements.	If the clock pad and destination are in phase, then $\Delta A = \Delta C$
2	Dedicated clock pad	Programmable feedback from logic	Generate an early or late clock (in regards to the clock input pad) to remove skew, or synchronize arrival times.	If $\Delta C > \Delta A$, pllout0 = early clock If $\Delta C < \Delta A$, pllout0 = late clock
3	Dedicated clock pad	Programmable feedback from I/O	Reduce FPGA or external component delays (set-up and hold times)	pllout will drive out through an I/O pad and connect back to the feedback pad. If $\Delta C > \Delta A$, pllout0 = early clock If $\Delta C < \Delta A$, pllout0 = late clock
4	Programmable input from logic or I/O	Programmable feedback from logic	Clock signal manipulation on internally derived clocks.	Useful for clock derivation.
5	Programmable input from logic or I/O	Programmable feedback from I/O	Operate on clock signal internally or externally.	Requires knowledge of off-chip delays.

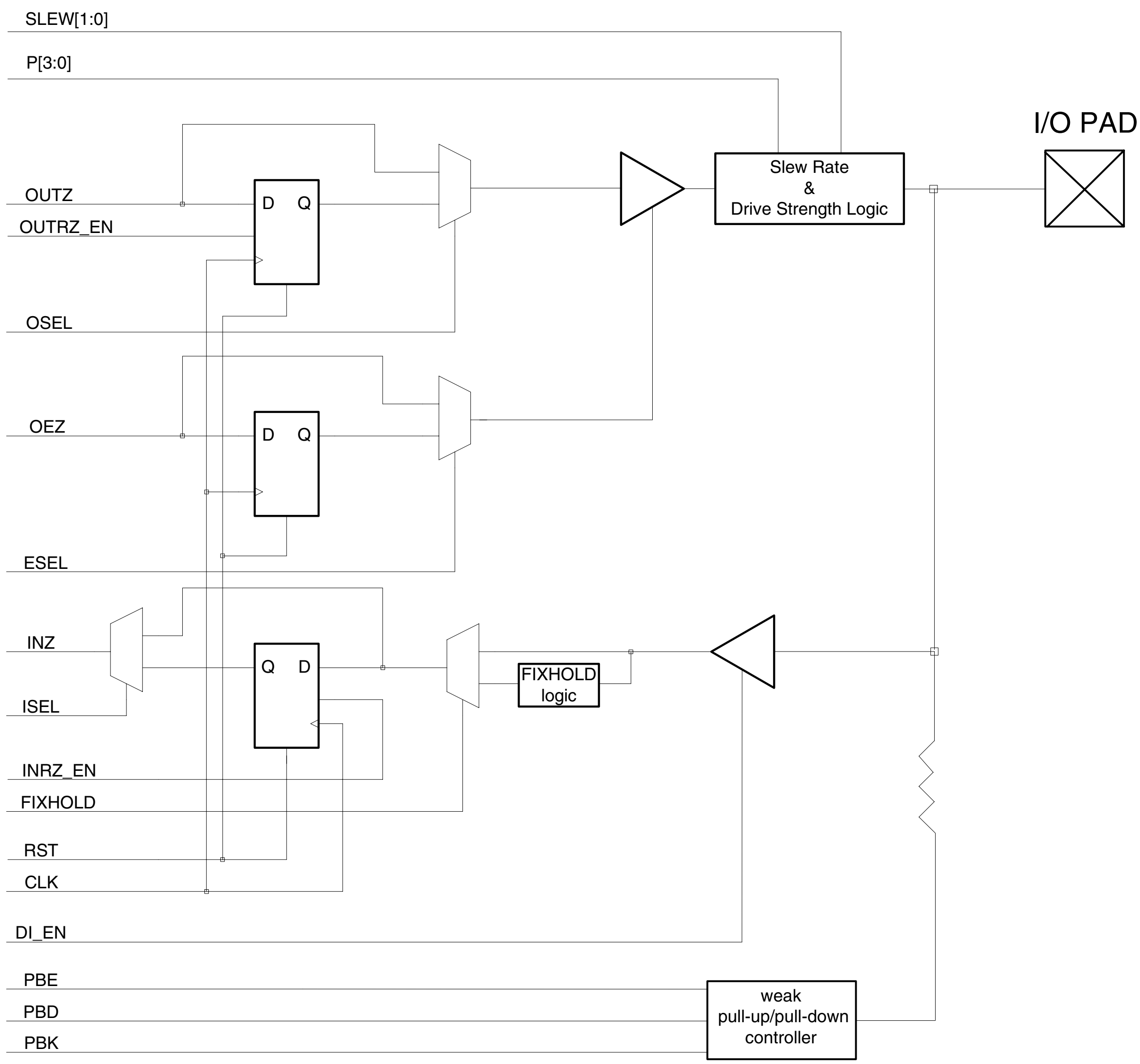
For more information on CCMs and how to use them in QuickWorks, refer to *Application Note 87 Configurable Clock Managers* at http://www.quicklogic.com/images/appnote87.pdf.

General Purpose Input Output (GPIO) Cell Structure

The GPIO features include:

- Direct or registered input with input path select
- Direct or registered output with output path select
- Direct or registered output enable with OE path select
- Input buffer enable to reduce power
- Programmable weak keeper, programmable pull-up/pull-down control
- Programmable drive strength
- Configurable slew rate
- Support for JTAG boundary scan

Figure 14: PolarPro GPIO Cell



With bi-directional I/O pins and global clock input pins, the PolarPro device maximizes I/O performance, functionality, and flexibility. All input and I/O pins are 1.8 V, 2.5 V, and 3.3 V tolerant and comply with the specific I/O standard selected. For single-ended I/O standards, the corresponding VCCIO bank input specifies the input tolerance and the output drive voltage. Drive strength and slew rate are configured for an entire bank. Weak keeper, pull-up, and pull-down functions can be configured for individual I/O.

Table 16: GPIO Interface Signals

Signal Name	Direction	Function
Routable Signals		
OUTZ	I	Data out from internal logic
OUTRZ_EN	I	Enable for registered OUTZ
OEZ	I	Tristate enable for the output signal
INZ	O	Input signal to the internal logic
INRZ_EN	I	Enable for registered INZ
RST	I	Reset for optional registers
CLK	I	Clock signal for optional registers
DI_EN	I	Enable for I/O input signal. Drives a 1 to internal logic when disabled.
Static Signals		
SLEW[1:0]	I	2-bit slew rate control
P[3:0]	I	Programmable drive strength
OSEL	I	Select signal for registered or flow through OUTZ
ESEL	I	Select signal for registered or flow-through OEZ
ISEL	I	Select signal for registered or flow-through INZ
FIXHOLD	I	Enable control for I/O input delay for hold fixing
PBE	I	Input signals for the weak keeper, pull-up/pull-down controller, see **Table 17** for functional behavior
PBD	I	
PBK	I	

Programmable Weak Keeper, Pull-Up, and Pull-Down

A programmable Weak Keeper, Pull-Up or Pull-Down controller is also available on each General Purpose I/O bank. When implementing the Weak Keeper, Pull-Up, and Pull-Down functions, each I/O can be configured separately. The I/O Weak Pull-Up and Pull-Down eliminates the need for external resistors. When PBK=1 the keeper block is placed into keeper mode. In the keeper mode, the pad pin (if the driver is tristated), will be kept at whichever level it was last forced, either by the driver itself, or by an external driver.

Table 17: Weak Pull-Up, and Pull-Down Controller

PBK	PBD	PBE	Function
0	0	0	Tristate (floating)
0	0	1	Weak Pull-Down
0	1	1	Weak Pull-Up
1	X	X	Weak Keeper (retains state)
0	1	0	Reserved

Programmable Drive Strength

Table 18 lists the worst case process (T_J=125×C) output currents (in mA) across the output driver at three levels of I/O voltages. The GPIO output current drive strength is guaranteed to be the specified amount in **Table 18** or better.

Table 18: Programmable Drive Strength

P[3:0]	Drive Strength	Worst Case Output Current (mA) at VCCIO =		
		1.62 V	2.25 V	2.97 V
0001	x1	1.6	2.5	3.1
0010	x2	3.2	5.0	6.2
0011	x3	4.8	7.5	9.3
0100	x4	6.4	10.0	12.4
0101	x5	8.0	12.5	15.5
0110	x6	9.6	15.0	18.6
0111	x7	11.2	17.5	21.7
1000	x8	12.8	20.0	24.8
1001	x9	14.4	22.5	27.9
1010	x10	16.0	25.0	31.0
1011	x11	17.8	27.5	34.1
1111	x12	19.4	29.0	35.7
Others	N/A	Reserved		

Programmable Slew Rate

Each I/O has programmable slew rate capability. The PolarPro GPIOs allow up to four different slew rate speeds. Slower slew rates can be used to reduce noise caused by I/O switching. **Table 19** lists the typical output slew rates (in V/ns) with various levels of output voltages and a load capacitor of 10 pF.

Table 19: Output Slew Rate Control

Slew[1:0]	Typical Output Slew Rate (V/ns) at VCCIO =		
	1.8V	2.5V	3.3V
00	0.13	0.25	0.50
01	0.25	0.50	1.00
10	0.50	1.00	2.00
11	1.00	2.00	4.00

I/O interface standards are programmable on a per bank basis. **Table 20** illustrates the I/O bank configurations available. Each I/O bank is independent of other I/O banks and each I/O bank has its own VCCIO supply inputs. A mixture of different I/O standards can be used on a PolarPro device. However, there is a limitation as to which I/O standards can be supported within a given bank. Only standards that share a common VCCIO can be shared within the same bank (e.g., PCI and LVTTL).

Table 20: I/O Standards and Applications

I/O Standard	VCCIO Voltage	Application
LVTTL	3.3 V	General Purpose
LVCMOS25	2.5 V	General Purpose
LVCMOS18	1.8 V	General Purpose
PCI	3.3 V	PCI Bus Applications

DDRIO Cell Structure

QuickLogic PolarPro devices support DDRIOs, which allows clocking data on both the positive and negative clock edges. All PolarPro devices have one I/O bank (Bank D) that can be configured in either a GPIO bank or a DDRIO mode. When bank D is configured to DDRIO mode, it is further divided into DDRIO sets. Each set contains 12 I/Os, which include 8 DQs, 1 DQM, 1 DQS, 1 DQCK_N and 1 DQCK_P (for the differential clocks, refer to **Table 21**).

Figure 15: PolarPro DDRIO Block Diagram

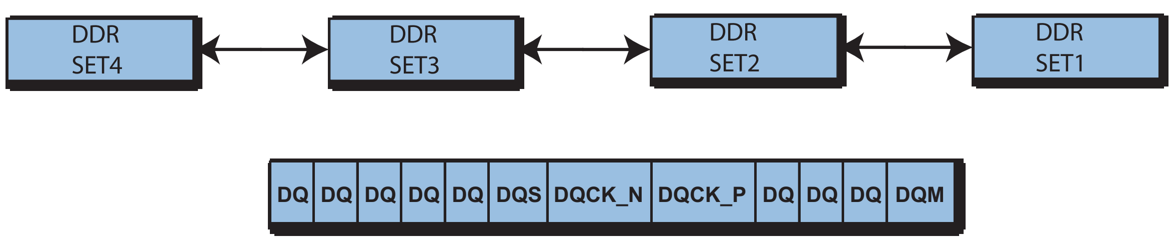


Table 21: Available DDR Sets

PolarPro Device	Package	Number of DDR Sets
QL1P075	PF144	2
	PT196	4
	PS256	4
QL1P100	PF144	2
	PT196	4
	PS324	4
QL1P150	PS256	4
	PS324	4
QL1P300	PS256	4
	PS324	4
QL1P600	PS256	4
	PS324	4
QL1P1000	PS256	4
	PS324	4

Double Data Rate (DDR) I/O

The DDR features include:

- Programmable slew rate
- Programmable drive strength
- Programmable pull-up

Figure 16: DDRIO DQ Configuration

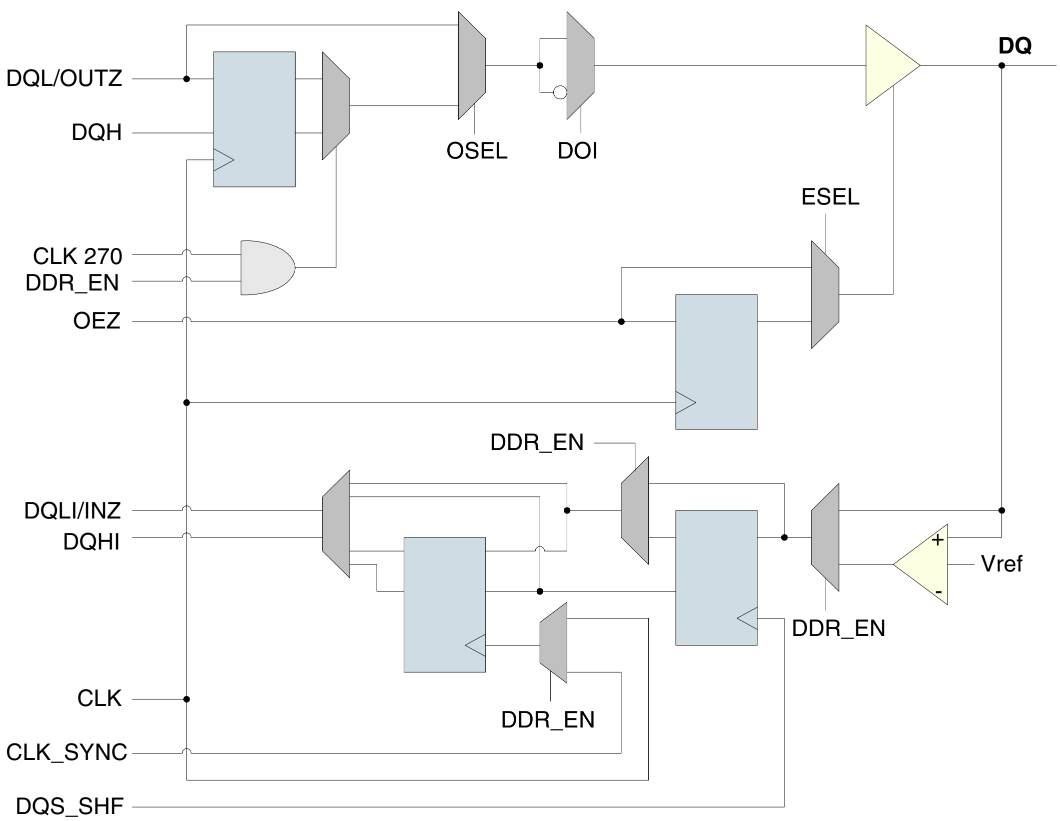


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Figure 17: DDRIO DQS Configuration

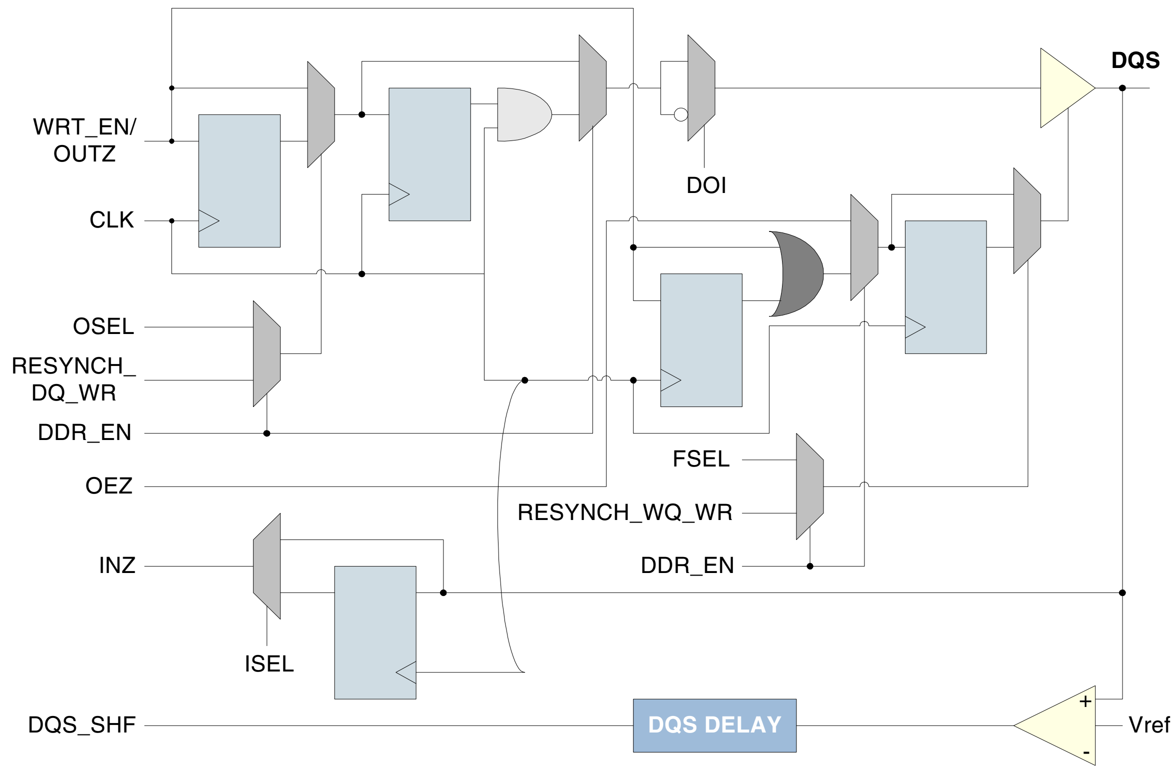

Table 22: DDR DQ Fabric Interface Signals

Signal Name	Direction	Function
Routable Signals		
DDR_EN	I	Enable DDR function, otherwise function will be that of GPIO.
CLK270	I	Shifted clock used in center-aligning data with DQS in writing out data.
PDB	I	Used as control for differential power-down.
CLK	I	System clock signal from the programmable fabric.
RST	I	Reset signal for registers inside the I/O.
INRZ_EN	I	Enable for registered DQLI / INZ.
DQH	I	Higher bit DQ signal output from core.
OUTRZ_EN	I	GPIO: enable for registered OUTZ signal.
DQL / OUTZ	I	DDR(DQL): lower bit DQ signal output from core. GPIO(OUTZ): data out from core with optional register.
OEZ	I	Tristate enable for the output signal with optional register.
DQHI	O	Higher bit DQ signal input to core with optional register for resynchronization.
DQLI / INZ	O	DDR(DQLI): lower bit DQ signal input to core with optional register for resynchronization. GPIO(INZ): data in signal to core with optional register.

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Table 22: DDR DQ Fabric Interface Signals *(Continued)*

Signal Name	Direction	Function
Static Signals		
resync_DQ_rd	I	Signal to enable resynching of DQ being read to avoid setup violations inside the programmable fabric.
resync_DQ_wr	I	Signal to enable resynching of DQ being written to avoid setup violations inside the I/O.
SLEW[1:0]	I	2-bit slew rate control.
P[3:0]	I	Pull-up programmable drive strength.
N[3:0]	I	Pull-down programmable drive strength.
FIXHOLD	I	Enable control for I/O input delay for hold fixing.
PBE	I	Input signal for weak pull-up controller.
DOI	I	Used as control for data out inversion.
ISEL	I	Select signal for registered or flow through INZ.
OSEL	I	Select signal for registered or flow through OUTZ.
ESEL	I	Select signal for registered or flow through OEZ.

Table 23: DDR DQS Interface Signals

Signal Name	Direction	Function
Routable Signals		
CLK_SYNC	I	Optional resynchronization clock to sync incoming data with the programmable fabric system clock.
PDB	I	Control for differential power-down.
CLK	I	System clock signal from the programmable fabric.
RST	I	Reset signal for registers inside the I/O.
INRZ_EN	I	GPIO: enable for registered INZ.
INZ	O	GPIO: data in signal to core with optional register.
DQS_BR_REL	I	A read burst signal used to mask the end of DQS pulses to avoid unnecessary glitches that will result in clocking-in unwanted data.
OEZ	I	Tristate enable for the output signal with optional register.
OUTRZ_EN	I	Enable for registered or flow-through WRT_EN/OUTZ.
WRT_EN	I	DDR(WRT_EN): write enable signal. GPIO(OUTZ): data out from core with optional register.
Static Signals		
CLK_SYNC_DEL_CTRL[4:0]	I	Setting to program delay for CLK_SYNC.
CLK_SYNC_INV	I	Option to invert CLK_SYNC.
resync_DQ_wr	I	Signal to enable resynching of DQ being written to avoid setup violations inside I/O.
DDR_EN	I	Enable DDR function, otherwise function will be that of GPIO.
FIXHOLD	I	Enable control for I/O input delay for hold fixing.

Table 23: DDR DQS Interface Signals *(Continued)*

Signal Name	Direction	Function
PBE	I	Input signal for weak pull-up controller.
SLEW[1:0]	I	Slew rate control setting.
P[3:0]	I	Pull-up programmable drive strength.
N[3:0]	I	Pull-down programmable drive strength.
DOI	I	Control for data out inversion.
ISEL	I	DDR: selects between VREF (ISEL=0) or PADI (ISEL=1), to connect to the inverting-input of a differential amplifier inside the DDR I/O driver. GPIO: Select signal for registered or flow-through INZ.
OSEL	I	Select signal for registered or flow-through WRT_EN/OUTZ.
ESEL	I	Select signal for registered or flow-through DQS_OE/OEZ.
DQS_DEL_ CTRL[3:0]	I	Setting to program delay of DQS signal.

Very Low Power Mode

The QuickLogic PolarPro devices have a unique feature, referred to as VLP mode, which reduces power consumption by placing the device in standby. Specifically, VLP mode can bring the total standby current down to less than 10 µA at room temperature when no incoming signals are toggled. VLP mode is controlled by the VLP pin. The VLP pin is active low, so VLP mode is activated by pulling the VLP pin to ground. Conversely, the VLP pin must be pulled to 3.3 V for normal operation.

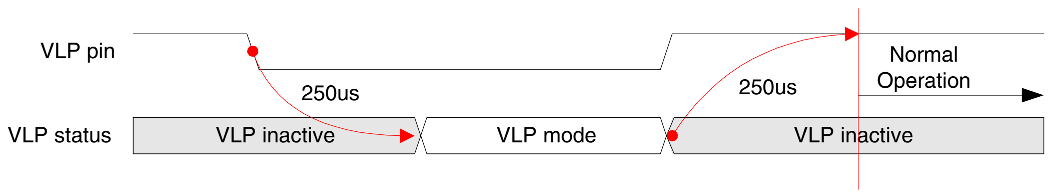
When a PolarPro device goes into VLP mode, the following occurs:

- All logic cell registers and GPIO registers values are held
- All RAM cell data is retained
- The outputs from all GPIO to the internal logic are tied to a weak ‘1’
- GPIO outputs drive the previous values
- GPIO output enables retain the previous values
- DDRIO outputs are pulled down through a weak pull down circuit
- Clock pad inputs are gated
- CCMs are held in the reset state

The entire operation from normal mode to VLP mode requires 250µs. Since the output of the GPIO to the internal logic is a weak ‘1’, the GPIO should not be used to drive any asynchronous active high signal, like set or reset. If the GPIO is an active high set or reset, then the registers may be cleared or set prior to entering VLP mode, hence replacing the previous register values.

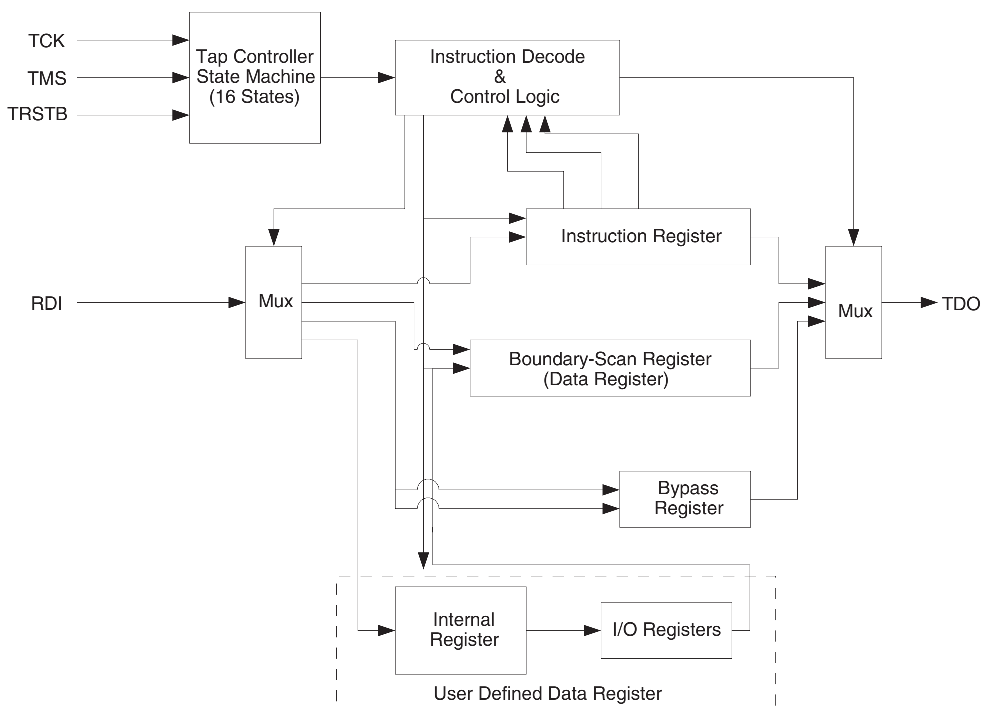
As the device exits out of VLP mode, the data from the registers, RAM, and GPIO will be used to recover the functionality of the device. Furthermore, since the CCMs were in a reset state during VLP mode, they will have to re-acquire the correct output signals before asserting lock_out. The time required to go from VLP mode to normal operation is 250 µs. **Figure 18** displays the delays associated with entering and exiting VLP mode.

Figure 18: VLP Mode Timing



Joint Test Access Group (JTAG) Information

Figure 19: JTAG Block Diagram



QuickLogic's PolarPro family complies with IEEE standard 1149.1, the Standard Test Access Port and Boundary Scan Architecture. The JTAG boundary scan test methodology allows complete observation and control of the boundary pins of a JTAG-compatible device through JTAG software. A Test Access Port (TAP) controller works in concert with the Instruction Register (IR), which allow users to run three required tests along with several user-defined tests. JTAG tests allow users to reduce system debug time, reuse test platforms and tools, and reuse subsystem tests for comprehensive verification of higher level system elements.

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The 1149.1 standard requires the following three tests:

- **Extest Instruction.** The Extest Instruction performs a printed circuit board (PCB) interconnect test. This test places a device into an external boundary test mode, selecting the boundary scan register to be connected between the TAP Test Data In (TDI) and Test Data Out (TDO) pins. Boundary scan cells are preloaded with test patterns (through the Sample/Preload Instruction), and input boundary cells capture the input data for analysis.
- **Sample/Preload Instruction.** The Sample/Preload Instruction allows a device to remain in its functional mode, while selecting the boundary scan register to be connected between the TDI and TDO pins. For this test, the boundary scan register can be accessed through a data scan operation, allowing users to sample the functional data entering and leaving the device.
- **Bypass Instruction.** The Bypass Instruction allows data to skip a device boundary scan entirely, so the data passes through the bypass register. The Bypass instruction allows users to test a device without passing through other devices. The bypass register is connected between the TDI and TDO pins, allowing serial data to be transferred through a device without affecting the operation of the device.

JTAG BSDL Support

- Boundary Scan Description Language (BSDL)
- Machine-readable data for test equipment to generate testing vectors and software
- BSDL files available for all device/package combinations from QuickLogic
- Extensive industry support available and ATVG (Automatic Test Vector Generation)

Electrical Specifications

DC Characteristics

The DC Specifications are provided in **Table 24** through **Table 27**.

Table 24: Absolute Maximum Ratings

Parameter	Value	Parameter	Value
VCC Voltage	-0.5 V to 2.0 V	Latch-up Immunity	±100 mA
VCCIO Voltage	-0.5 V to 4.0 V	ESD Pad Protection	
VREF Voltage	0.5 V to VCCIO	Leaded Package Storage Temperature	-65° C to + 150° C
Input Voltage	-0.5 V to VCCIO + 0.5 V	Laminate Package (BGA) Storage Temperature	-55° C to + 125° C

Table 25: Recommended Operating Range

Symbol	Parameter		Military		Industrial		Commercial		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
VCC	Supply Voltage		1.71	1.89	1.71	1.89	1.71	1.89	V
VCCIO	I/O Input Tolerance Voltage		1.71	3.60	1.71	3.60	1.71	3.60	V
TJ	Junction Temperature		-55	125	-40	100	0	85	°C
K	Delay Factor	-6 Speed Grade	0.49	1.57	0.50	1.51	0.54	1.47	n/a
		-7 Speed Grade	0.48	1.40	0.50	1.34	0.53	1.31	n/a
		-8 Speed Grade	0.45	1.32	0.47	1.26	0.50	1.23	n/a

NOTE: VI characteristics, drive current, and quiescent current data will be supplied once characterization has been completed.

Table 26: DC Characteristics

Symbol	Parameter	Conditions	Min.	Max.	Units
I_I	I or I/O Input Leakage Current	VI = VCCIO or GND	-1	1	µA
I_{OZ}	3-State Output Leakage Current	VI = VCCIO or GND	-	1	µA
C_I	I/O Input Capacitance	-	-	8	pF
C_{CLOCK}	Clock Input Capacitance	-	-	8	pF
I_{OS}	Output Short Circuit Current[a]	VO = GND VO = VCC	-15 40	-180 210	mA mA
I_{REF}	Quiescent Current on VREF	-	-10	10	µA
I_{PD}	Current on programmable pull-down	VCC = 1.8 V	-	50	µA
I_{PLL}	Quiescent Current on each VCCPLL	2.5 V 3.3 V	-	3	mA
I_{VCCIO}	Quiescent Current on VCCIO	VCCIO = 3.6 V VCCIO = 2.5 V VCCIO = 1.8 V	-	20 10 10	µA

a. The data provided in **Table 26** represents the JEDEC and PCI specifications.

Table 27: DC Input and Output Levels[a]

Symbol	INREF		V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V_{MIN}	V_{MAX}	V_{MIN}	V_{MAX}	V_{MIN}	V_{MAX}	V_{MAX}	V_{MIN}	mA	mA
LVTTL	n/a	n/a	-0.3	0.8	2.2	VCCIO + 0.3	0.4	2.4	2.0	-2.0
LVCMOS2	n/a	n/a	-0.3	0.7	1.7	VCCIO + 0.3	0.7	1.7	2.0	-2.0
LVCMOS18	n/a	n/a	-0.3	0.63	1.2	VCCIO + 0.3	0.7	1.7	2.0	-2.0
GTL+	0.88	1.12	-0.3	INREF - 0.2	INREF + 0.2	VCCIO + 0.3	0.6	n/a	40	n/a
PCI	n/a	n/a	-0.3	0.3 x VCCIO	0.6 x V_{CCIO}	VCCIO + 0.5	0.1 x VCCIO	0.9 x VCCIO	1.5	-0.5
SSTL2	1.15	1.35	-0.3	INREF - 0.18	INREF + 0.18	VCCIO + 0.3	0.74	1.76	7.6	-7.6
SSTL3	1.3	1.7	-0.3	INREF - 0.2	INREF + 0.2	VCCIO + 0.3	1.10	1.90	8	-8

a. The data provided in **Table 27** represents the JEDEC and PCI specification. QuickLogic devices either meet or exceed these requirements.

NOTE: All CLK and CCM pins are clamped to the VCC rail. Therefore, these pins can be driven up to VCC. All JTAG inputs are clamped to the VCC rail. These JTAG input pins can only be driven up to VCC.

AC Characteristics

NOTE: The AC specifications will be provided in **Table 28** through **Table 38** once production silicon has been characterized.

Logic cell diagrams and waveforms are provided in **Figure 20** through **Figure 33**.

Figure 20: PolarPro Logic Cell

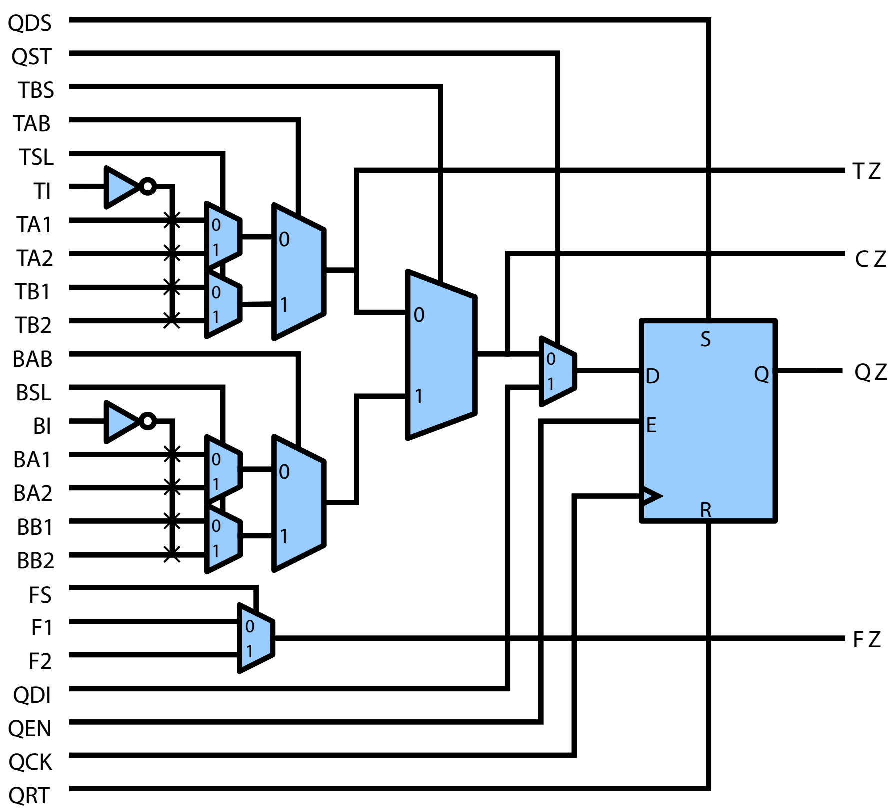

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Table 28: Logic Cell Delays

Symbol	Parameter	Value	
		Min.	Max.
t_{PD}	Combinatorial Delay of the longest path: time taken by the combinatorial circuit to output	TBD	TBD
t_{SU}	Setup time: time the synchronous input of the flip-flop must be stable before the active clock edge	TBD	TBD
t_{HL}	Hold time: time the synchronous input of the flip-flop must be stable after the active clock edge	TBD	TBD
t_{CO}	Clock-to-out delay: the amount of time taken by the flip-flop to output after the active clock edge.	TBD	TBD
t_{CWHI}	Clock High Time: required minimum time the clock stays high	TBD	TBD
t_{CWLO}	Clock Low Time: required minimum time that the clock stays low	TBD	TBD
t_{SET}	Set Delay: time between when the flip-flop is "set" (high) and when the output is consequently "set" (high)	TBD	TBD
t_{RESET}	Reset Delay: time between when the flip-flop is "reset" (low) and when the output is consequently "reset" (low)	TBD	TBD
t_{SW}	Set Width: time that the SET signal must remain high/low	TBD	TBD
t_{RW}	Reset Width: time that the RESET signal must remain high/low	TBD	TBD

Figure 21: Logic Cell Flip-Flop Timings—First Waveform

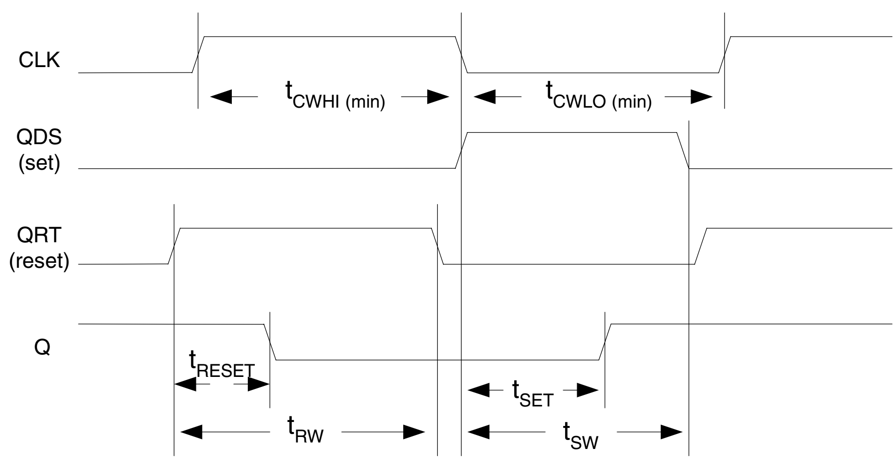

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Figure 22: Logic Cell Flip-Flop Timings—Second Waveform

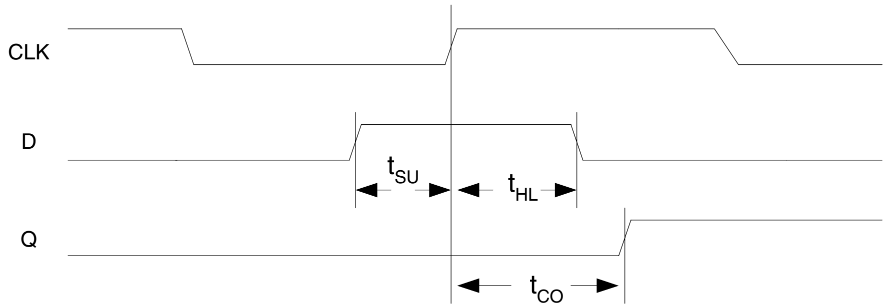

Figure 23: PolarPro Clock Network

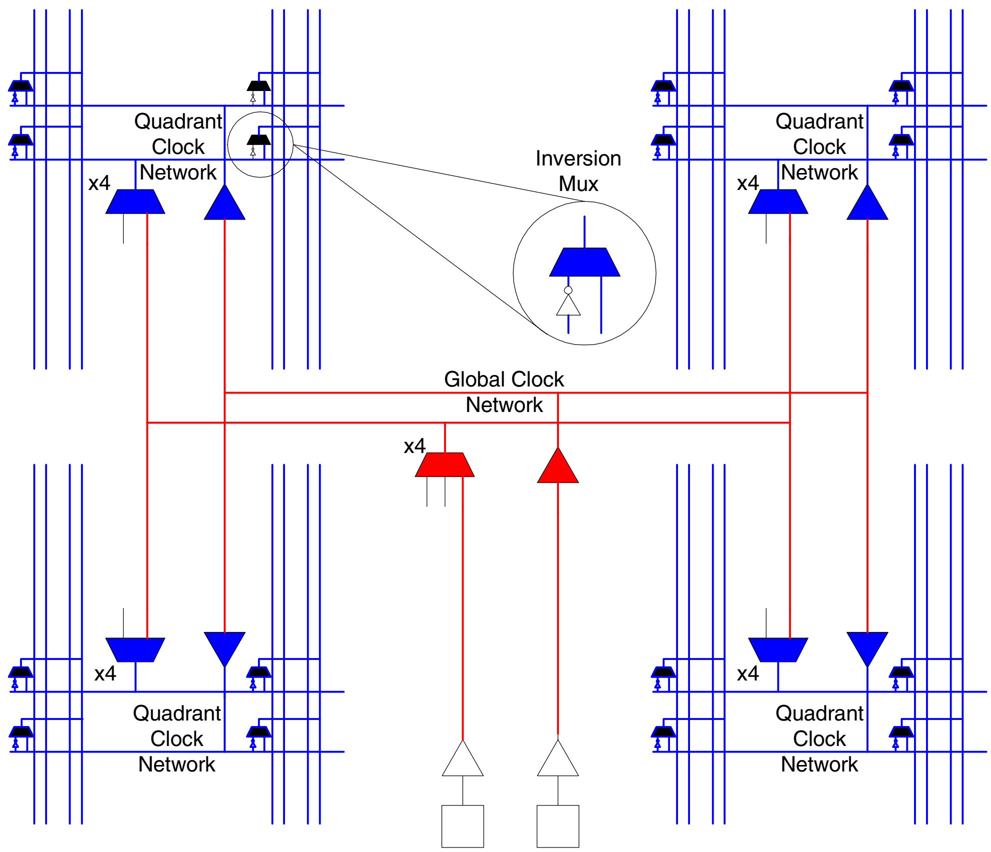

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Table 29: PolarPro Clock Network Delay

Clock Segment	Parameter	Value	
		Min.	Max.
t_{PGCK}	Global clock pin delay to quad net	TBD	TBD
t_{BGCK}	Global clock tree delay (quad net to flip-flop)	TBD	TBD
t_{DPD}	Dedicated clock pad	TBD	TBD
t_{GSKEW}	Global delay clock skew	TBD	TBD
t_{DSKEW}	Dedicated clock skew	TBD	TBD

RAM Timing

Figure 24: RAM Module

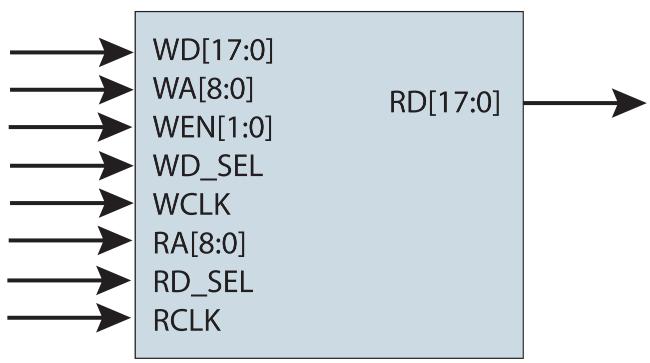

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Table 30: RAM Cell Write Timing

Symbol	Parameter	Value	
		Min.	Max.
RAM Cell Synchronous Write Timing			
t_{SWA}	WA setup time to WCLK: time the WRITE ADDRESS must be stable before the active edge of the WRITE CLOCK	TBD	TBD
t_{HWA}	WA hold time to WCLK: time the WRITE ADDRESS must be stable after the active edge of the WRITE CLOCK	TBD	TBD
t_{SWD}	WD setup time to WCLK: time the WRITE DATA must be stable before the active edge of the WRITE CLOCK	TBD	TBD
t_{HWD}	WD hold time to WCLK: time the WRITE DATA must be stable after the active edge of the WRITE CLOCK	TBD	TBD
t_{SWE}	WE setup time to WCLK: time the WRITE ENABLE must be stable before the active edge of the WRITE CLOCK	TBD	TBD
t_{HWE}	WE hold time to WCLK: time the WRITE ENABLE must be stable after the active edge of the WRITE CLOCK	TBD	TBD
t_{WCRD}	WCLK to RD (WA = RA): time between the active WRITE CLOCK edge and the time when the data is available at RD	TBD	TBD

Figure 25: RAM Cell Write Timing

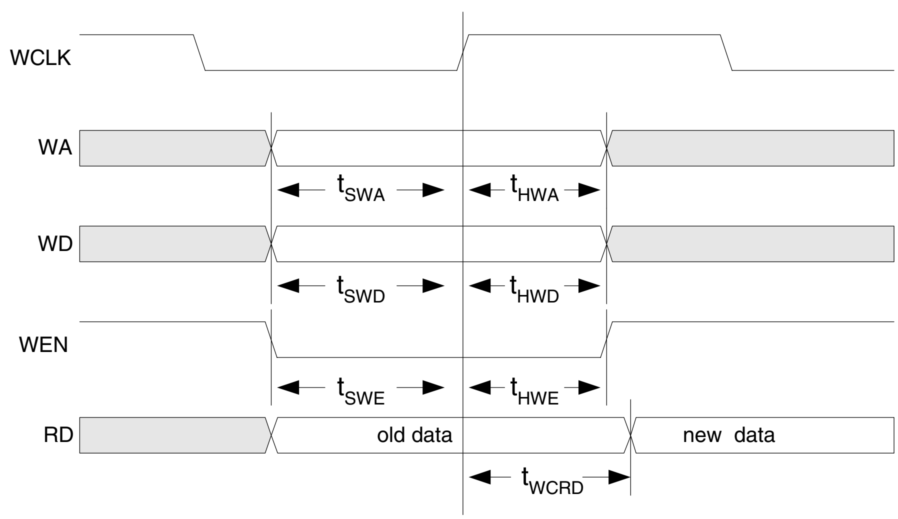
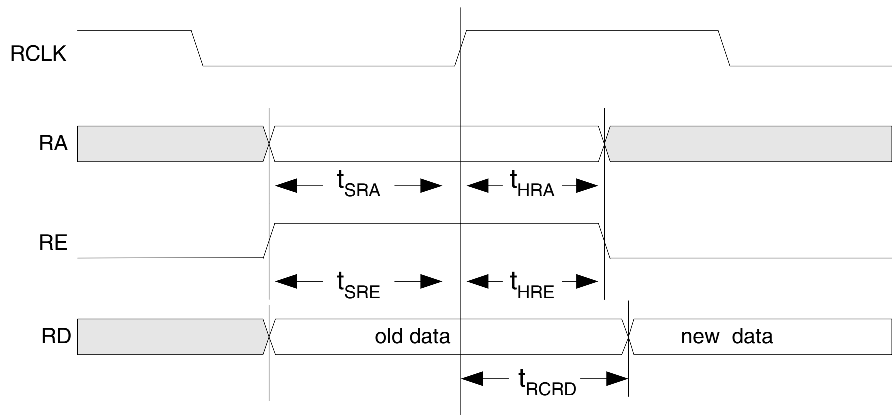


Table 31: RAM Cell Read Timing

Symbol	Parameter	Value	
		Min.	Max.
t_{SRA}	RA setup time to RCLK: time the READ ADDRESS must be stable before the active edge of the READ CLOCK	TBD	TBD
t_{HRA}	RA hold time to RCLK: time the READ ADDRESS must be stable after the active edge of the READ CLOCK	TBD	TBD
t_{SRE}	RE setup time to WCLK: time the READ ENABLE must be stable before the active edge of the READ CLOCK	TBD	TBD
t_{HRE}	RE hold time to WCLK: time the READ ENABLE must be stable after the active edge of the READ CLOCK	TBD	TBD
t_{RCRD}	RCLK to RD: time between the active READ CLOCK edge and the time when the data is available at RD	TBD	TBD

Figure 26: RAM Cell Read Timing



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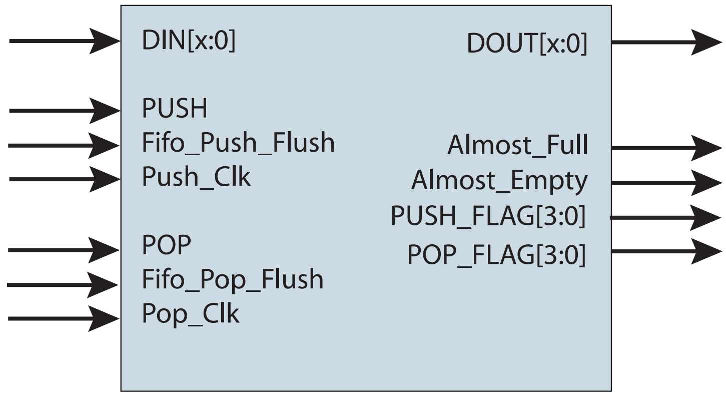
FIFO Timing

Figure 27: FIDO Module



NOTE: x = {1,2,3,...35}.

Table 32: FIFO PUSH Timing

Symbol	Parameter	Value	
		Min.	Max.
t_{SPUSHD}	WD setup time to Clk1: time WD must be stable before the active edge of the FIFO clock	TBD	TBD
t_{HPUSHD}	WD hold time to Clk1: time WD must be stable after the active edge of the FIFO clock	TBD	TBD
$t_{SPUSHEN}$	WEN setup time to Clk1: time WEN must be stable before the active edge of the FIFO clock	TBD	TBD
$t_{HPUSHEN}$	WEN hold time to Clk1: time WEN must be stable after the active edge of the FIFO clock	TBD	TBD
$t_{SPUSHFLUSH}$	FLUSH setup time to Clk1: time CS1 must be stable before the active edge of the FIFO clock	TBD	TBD
$t_{HPUSHFLUSH}$	FLUSH hold time to Clk1: time CS1 must be stable after the active edge of the FIFO clock	TBD	TBD
t_{FPUSH}	Clk1 to Push: time between the active FIFO CLOCK edge and the time when the data is pushed to the FIFO	TBD	TBD
t_{COAF}	Clock-to-out of Almost Full	TBD	TBD
$t_{COPUSHFLAG}$	Clock-to-out of FIFO Push level indicator	TBD	TBD

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Figure 28: FIFO PUSH Timing

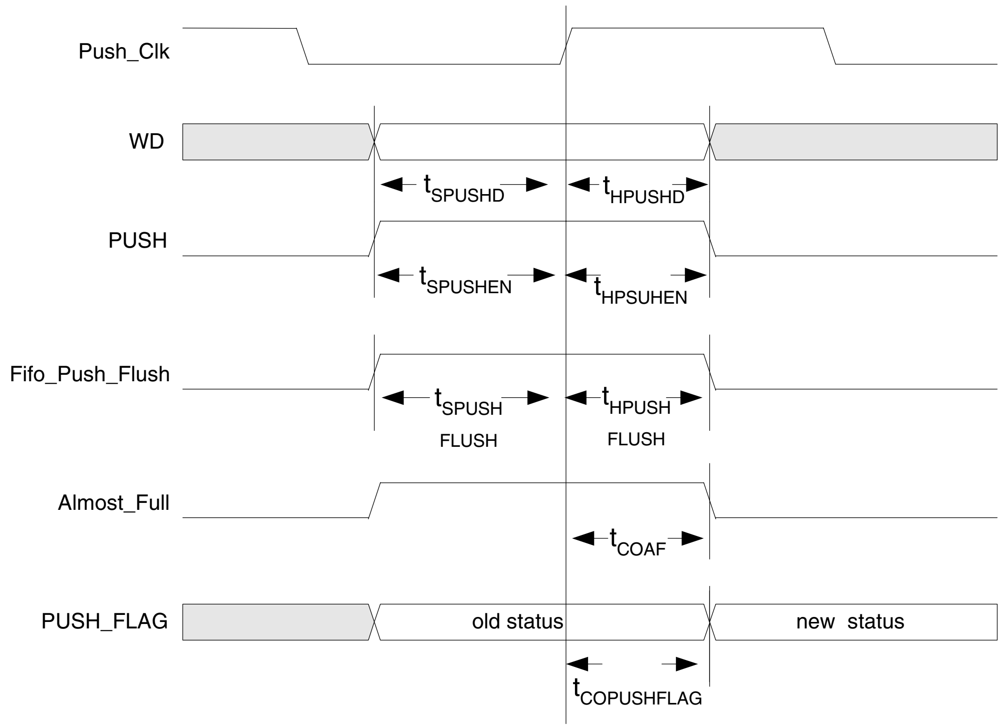
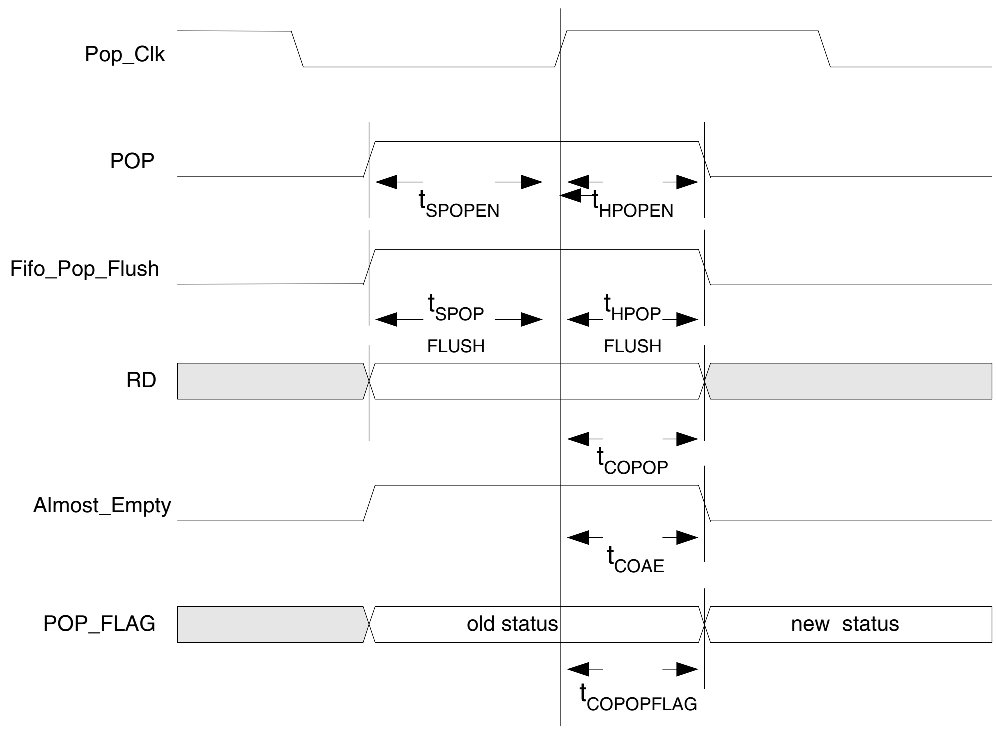


Table 33: FIFO POP Timing

Symbol	Parameter	Value	
		Min.	Max.
t_{SPOPEN}	POP setup time to Clk2: time POP must be stable before the active edge of the FIFO clock	TBD	TBD
t_{HPOPEN}	POP hold time to Clk2: time POP must be stable after the active edge of the FIFO clock	TBD	TBD
$t_{SPOPFLUSH}$	FLUSH setup time to Clk2: time CS2 must be stable before the active edge of the FIFO clock	TBD	TBD
$t_{HPOPFLUSH}$	FLUSH hold time to Clk2: time CS2 must be stable after the active edge of the FIFO clock	TBD	TBD
t_{FPOP}	Clk2 to Pop: time between the active FIFO CLOCK edge and the time when the data is popped from the FIFO	TBD	TBD
t_{COPOP}	Clock-to-out of RD	TBD	TBD
t_{COAE}	Clock-to-out of Almost Empty	TBD	TBD
$t_{COPOPFLAG}$	Clock-to-out of FIFO Pop level indicator	TBD	TBD

Figure 29: FIFO POP Timing



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GPIO Cell Timing

Figure 30: PolarPro I/O Cell Output Path

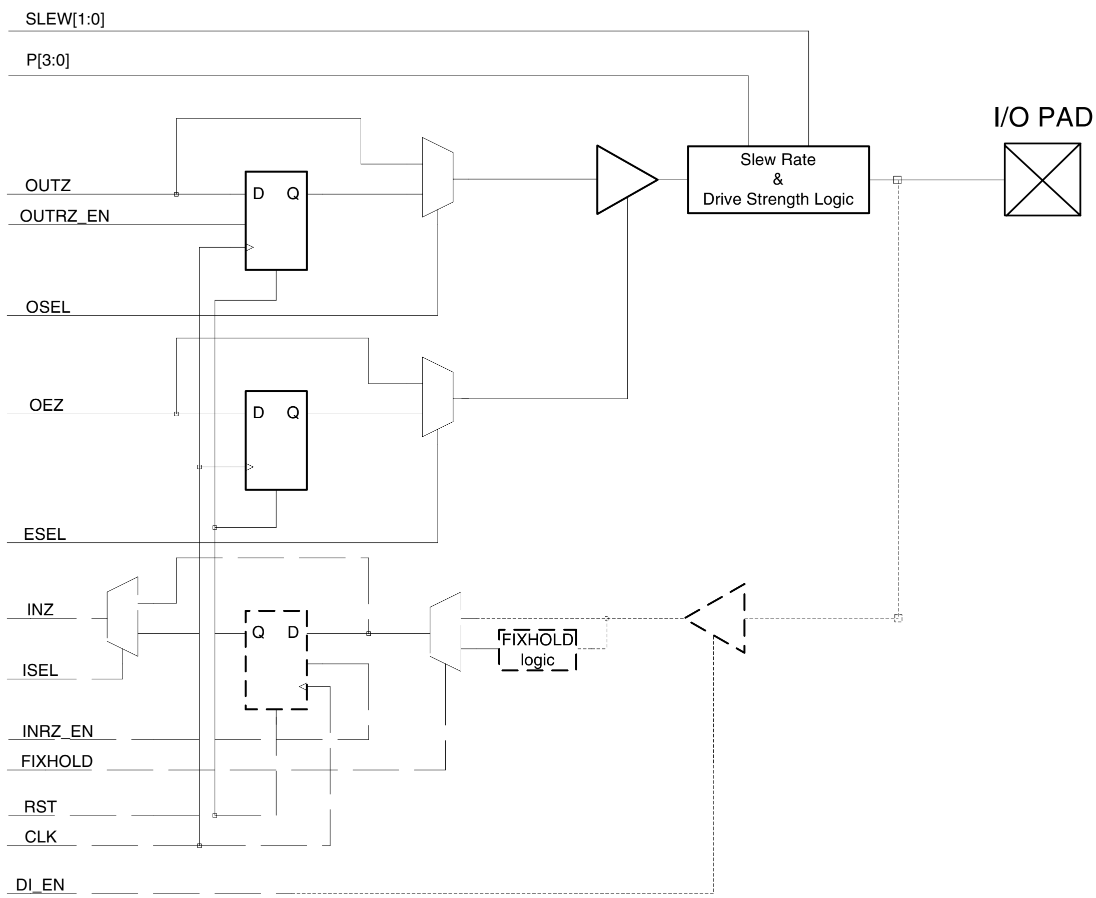
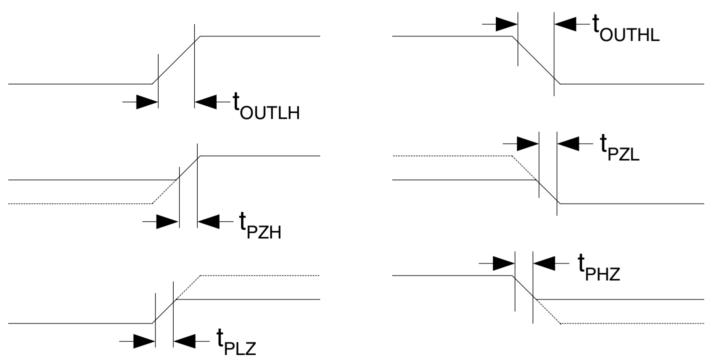


Figure 31: PolarPro I/O Cell Output Enable Timing



PRELIMINARY

Table 34: PolarPro I/O Cell Output Timing

Symbol	Parameter	Value (ns)	
Output Register Cell Only		Slow Slew Max	Fast Slew Max
t_{OUTLH}	Output Delay low to high (90% of H)	TBD	TBD
t_{OUTHL}	Output Delay high to low (10% of L)	TBD	TBD
t_{PZH}	Output Delay tri-state to high (90% of H)	TBD	TBD
t_{PZL}	Output Delay tri-state to low (10% of L)	TBD	TBD
t_{PHZ}	Output Delay high to tri-state	TBD	TBD
t_{PLZ}	Output Delay low to tri-state	TBD	TBD
t_{COP}	Clock-to-out delay (does not include clock tree delays)	TBD	TBD

Table 35: Output Slew Rates @ VCCIO = 3.3 V, T = 25° C

	Fast Slew	Slow Slew
Rising Edge	TBD	TBD
Falling Edge	TBD	TBD

Table 36: Output Slew Rates @ VCCIO = 2.5 V, T = 25° C

	Fast Slew	Slow Slew
Rising Edge	TBD	TBD
Falling Edge	TBD	TBD

Table 37: Output Slew Rates @ VCCIO = 1.8 V, T = 25° C

	Fast Slew	Slow Slew
Rising Edge	TBD	TBD
Falling Edge	TBD	TBD

Figure 32: PolarPro I/O Cell Input Path

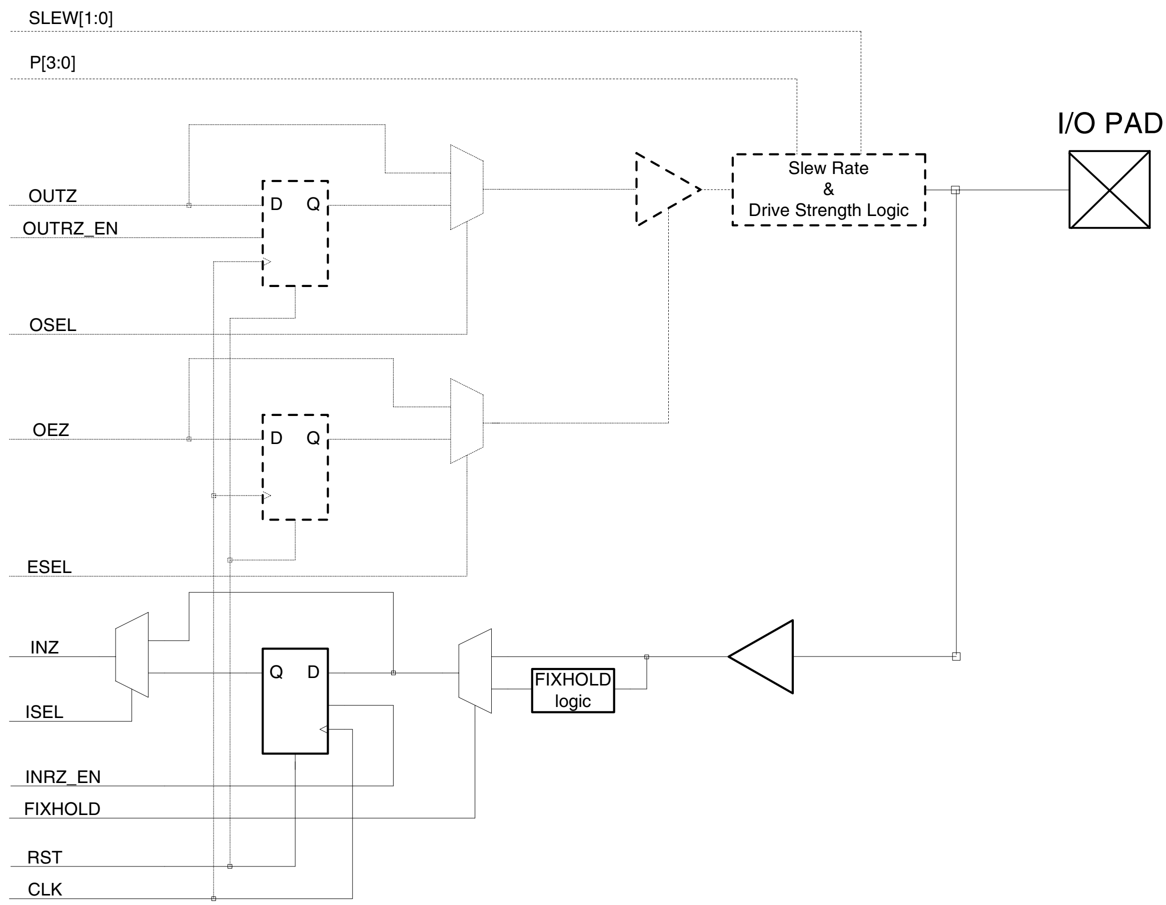


Figure 33: PolarPro Input Register Cell Timing

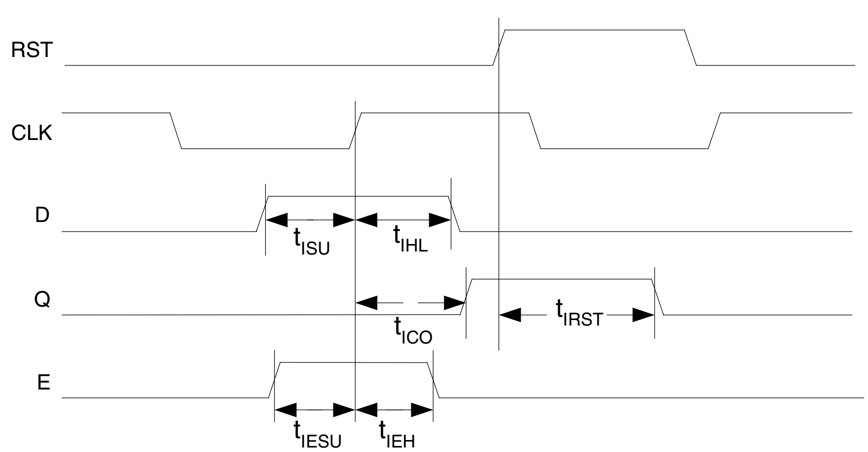


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Table 38: I/O Input Register Cell Timing

Symbol	Parameter	Value	
		Min.	Max.
t_{ISU}	Input register setup time: time the synchronous input of the flip-flop must be stable before the active clock edge	TBD	TBD
t_{IHL}	Input register hold time: time the synchronous input of the flip-flop must be stable after the active clock edge	TBD	TBD
t_{ICO}	Input register clock-to-out: time taken by the flip-flop to output after the active clock edge	TBD	TBD
t_{IRST}	Input register reset delay: time between when the flip-flop is “reset” (low) and when the output is consequently “reset” (low)	TBD	TBD
t_{IESU}	Input register clock enable setup time: time “enable” must be stable before the active clock edge	TBD	TBD
t_{IEH}	Input register clock enable hold time: time “enable” must be stable after the active clock edge	TBD	TBD

Table 39: I/O Input Buffer Delays

Symbol	Parameter	Value	
	To get the total input delay add this delay to t_{ISU}	Min.	Max.
t_{SID} (LVTTL)	LVTTL input delay: Low Voltage TTL for 3.3 V applications	TBD	TBD
t_{SID} (LVCMOS2)	LVCMOS2 input delay: Low Voltage CMOS for 2.5 V and lower applications	TBD	TBD
t_{SID} (LVCMOS18)	LVCMOS18 input delay: Low Voltage CMOS for 1.8 V applications	TBD	TBD
t_{SID} (GTL+)	GTL+ input delay: Gunning Transceiver Logic	TBD	TBD
t_{SID} (SSTL3)	SSTL3 input delay: Stub Series Terminated Logic for 3.3 V	TBD	TBD
t_{SID} (SSTL2)	SSTL2 input delay: Stub Series Terminated Logic for 2.5 V	TBD	TBD
t_{SID} (PCI)	PCI input delay: Peripheral Component Interconnect for 3.3 V	TBD	TBD

DDR Cell Timing

TBD

Package Thermal Characteristics

The PolarPro device is available for Commercial (0°C to 85°C Junction), Industrial (-40°C to 100°C Junction), and Military (-55°C to 125°C Junction) temperature ranges.

Thermal Resistance Equations:

θ_{JC} = $(T_J - T_C)/P$
θ_{JA} = (TJ - TA)/P
P_{MAX} = $(T_{JMAX} - T_{AMAX})/\theta_{JA}$

Parameter Description:

θ_{JC}: Junction-to-case thermal resistance

θ_{JA}: Junction-to-ambient thermal resistance

T_J: Junction temperature

T_A: Ambient temperature

P: Power dissipated by the device while operating

P_{MAX}: The maximum power dissipation for the device

T_{JMAX}: Maximum junction temperature

T_{AMAX}: Maximum ambient temperature

NOTE: Maximum junction temperature (T_{JMAX}) is 125°C. To calculate the maximum power dissipation for a device package look up θ_{JA} from **Table 40**, pick an appropriate T_{AMAX} and use:

$P_{MAX} = (125°C - T_{AMAX})/ \theta_{JA}$

Table 40: Package Thermal Characteristics

Device	Package Description			θ_{JA} (º C/W)		
	Package Code	Package Type	Pin Count	0 LFM	200 LFM	400 LFM
QL1P1000	PS	LBGA	256	TBD	TBD	TBD
	PS	LBGA	324	TBD	TBD	TBD
QL1P600	PS	LBGA	256	TBD	TBD	TBD
	PS	LBGA	324	TBD	TBD	TBD
QL1P300	PS	LBGA	256	TBD	TBD	TBD
	PS	LBGA	324	TBD	TBD	TBD
QL1P150	PS	LBGA	256	TBD	TBD	TBD
	PS	LBGA	324	TBD	TBD	TBD
QL1P100	PF	TQFP	144	TBD	TBD	TBD
	PT	TFBGA	196	TBD	TBD	TBD
	PS	LBGA	256	TBD	TBD	TBD
QL1P075	PF	TQFP	144	TBD	TBD	TBD
	PT	TFBGA	196	TBD	TBD	TBD
	PS	LBGA	256	TBD	TBD	TBD

Table 41: Maximum Junction and Maximum Body Temperature

Package Type	θ_{JA} (°C)	Tbody (°C)
TFBGA	TBD	TBD
TQFP	TBD	TBD
LBGA	TBD	TBD
TFBGA - Pb-free	TBD	TBD
TQFP - Pb-free	TBD	TBD
LBGA - Pb-free	TBD	TBD

Moisture Sensitivity Level

All PolarPro devices are Moisture Sensitivity Level 3.

Table 42: Solder and Lead Finish Composition

	Lead Included	Lead-free
BGA Solder	73% Pb, 37% Sn	Sn3AgCu:Sn4AgCu[a]
QFP Lead Finish	85% Pb, 15% Sn	Sn (matte)

a. Sn3AgCu:Sn4AgCu means that Ag can range from 3% to 4%. Cu is always 0.5%.

Power Vs. Operating Frequency

The basic power equation which best models power consumption is given below:

$$P_{TOTAL} = 0.350 + f[0.0031\ \eta_{LC} + 0.0948\ \eta_{CKBF} + 0.01\ \eta_{CLBF} + 0.0263\ \eta_{CKLD} + 0.543\ \eta_{RAM} + 0.20\ \eta_{PLL} + 0.0035\ \eta_{INP} + 0.0257\ \eta_{OUTP}]\ (mW)$$

Where:

η_{LC} = number of logic cells in the design

η_{CKBF} = number of clock buffers

η_{CLBF} = number of column clock buffers

η_{CKLD} = number of loads connected to the column clock buffers

η_{RAM} = number of RAM blocks

η_{PLL} = number of PLLs

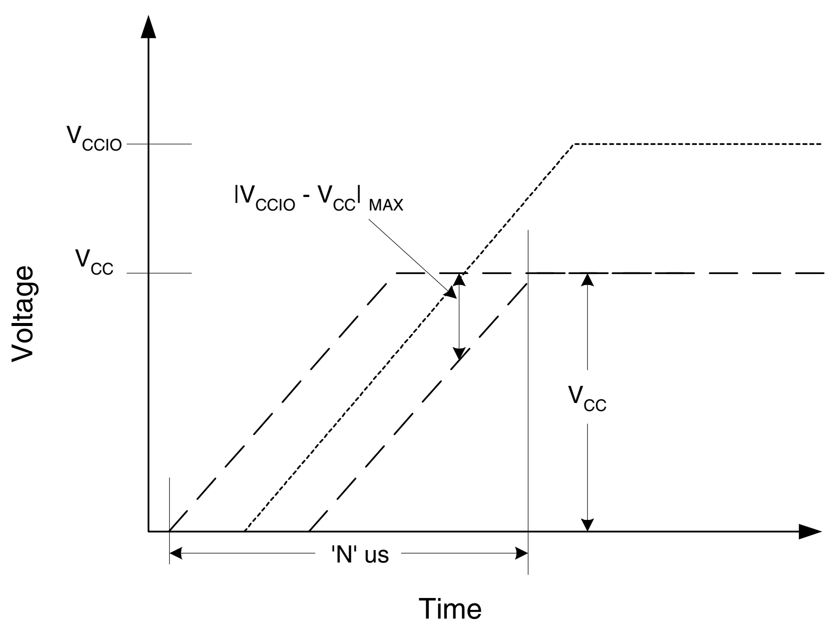
η_{INP} = number of input pins

η_{OUTP} = number of output pins

NOTE: To learn more about power consumption, see QuickLogic Application Note 60 at http://www.quicklogic.com/images/appnote60.pdf.

Power-Up Sequencing

Figure 34: Power-Up Sequencing



NOTE: Power-up sequencing timing will be provided once production silicon characterization is completed.

Pin Descriptions

Table 43: Pin Descriptions

Pin	Direction	Function	Description
Dedicated Pin Descriptions			
GPIO(C:A)	I/O	General purpose input/output pin	The I/O pin is a bi-directional pin, configurable to either an input-only, output-only, or bi-directional pin. The letter inside the parenthesis means that the I/O is located in the bank with that letter. If an I/O is not used, the development software provides the option of tying that pin to GND, VCCIO, or Hi-Z.
CLK(D:A)	I	Global clock network pin low skew global clock	This pin provides access to a distributed network capable of driving the CLOCK, SET, RESET, all inputs to the Logic Cell, READ and WRITE CLOCKS, Read and Write Enables of the Embedded RAM Blocks, and I/O inputs. The voltage tolerance of this pin is specified by VCCIO.
CCMIN(1:0)	I	CCM clock input	Input clock for CCM. The voltage tolerance for this pin is specified by the VCCIO of the same bank.
CCMVCC (1:0)	I	Power supply pin for CCM	CCM input voltage level. Configurable as 1.8 V only. If CCMVCC is grounded, then the CCM is disabled.
CCMGND(1:0)	I	Ground pin for CCM	Connect to ground.
VLP	I	Voltage low power	Active low. Therefore, when VLP pin is low, the device will go into low power mode. Tie VLP to 3.3 V to disable low power mode.
VCC	I	Power supply pin	Connect to 1.8 V supply.
VCCIO(D:A)	I	Input voltage tolerance pin	This pin provides the flexibility to interface the device with either a 3.3 V, 2.5 V, or 1.8 V device. The letter inside the parenthesis means that the VCCIO is located in the bank with that letter. Every I/O pin in the same bank will be tolerant of the same VCCIO input signals and will drive VCCIO level output signals. This pin must be connected to either 3.3 V, 2.5 V, or 1.8 V.
GND	I	Ground pin	Connect to ground.
DQ/ GPIO(D)	I/O	Configurable pin can be declared as either a DDRIO DQ or as a general purpose I/O	The D inside the parenthesis means that the I/O is located in Bank D. If an I/O is not used, the development software provides the option of typing that pin to GND, VCCIO, or Hi-Z.
DQS/ GPIO(D)	I/O	Configurable pin can be declared as either a DDRIO DQS or as a general purpose I/O	The D inside the parenthesis means that the I/O is located in Bank D. If an I/O is not used, the development software provides the option of typing that pin to GND, VCCIO, or Hi-Z.
DQCK_N/ GPIO(D)	I/O	Configurable pin can be declared as either a DDRIO DQ, DDR negative clock, or as a general purpose I/O.	The D inside the parenthesis means that the I/O is located in Bank D. If an I/O is not used, the development software provides the option of typing that pin to GND, VCCIO, or Hi-Z.

Table 43: Pin Descriptions *(Continued)*

Pin	Direction	Function	Description
DQCK_P/ GPIO(D)	I/O	Configurable pin can be declared as either a DDRIO DQ, DDR positive clock, or as a general purpose I/O.	The D inside the parenthesis means that the I/O is located in Bank D. If an I/O is not used, the development software provides the option of typing that pin to GND, VCCIO, or Hi-Z.
VREF(D)	I	Differential reference voltage	The INREF is the reference voltage pin for the SSTL1.8 and SSTL2 standards. The D inside the parenthesis means that INREF is located in Bank D. Tie this pin to GND if voltage referenced standards are not used.
POR	I	Power-on reset	Active high reset used during power-up sequence. Drive to VCCIO(B) during power-up. Pull low after power-up to begin normal operation.
JTAG Pin Descriptions			
TDI/RSI	I	Test data in for JTAG/RAM init. serial data in	Hold HIGH during normal operation. Connect to VCCIO(B) if unused.
TRSTB	I	Active low reset for JTAG	Hold LOW during normal operation. Connect to GND if unused. During JTAG, a high voltage is based on VCCIO(B).
TMS	I	Test mode select for JTAG	Hold HIGH during normal operation. Connect to VCCIO(B) if not used for JTAG.
TCK	I	Test clock for JTAG	Hold HIGH or LOW during normal operation. Connect to VCCIO(B) or GND if not used for JTAG.
TDO	O	Test data out for JTAG	Must be left unconnected if not used for JTAG. The output voltage drive is specified by VCCIO(B).

Recommended Unused Pin Terminations for PolarPro Devices

All unused, general purpose I/O pins can be tied to VCC, GND, or Hi-Z (high impedance) internally.

Terminate the rest of the pins at the board level as recommended in **Table 44**.

Table 44: Recommended Unused Pin Terminations

Signal Name	Recommended Termination
VREF	If an I/O bank does not require the use of the INREF signal, connect the pin to GND.
CLK <x>[a]	Connect to GND or VCCIO(x) if unused.
VLP	Tie VLP to 3.3 V to disable low power mode.
TDI	Connect to VCCIO(B) if not used for JTAG.
TRSTB	Connect to GND if not used for JTAG.
TMS	Connect to VCCIO(B) if not used for JTAG
TCK	Connect to VCCIO(B) or GND if not used for JTAG.
TDO	Must be left unconnected if not used for JTAG.

a. x represents A, B, C or D.

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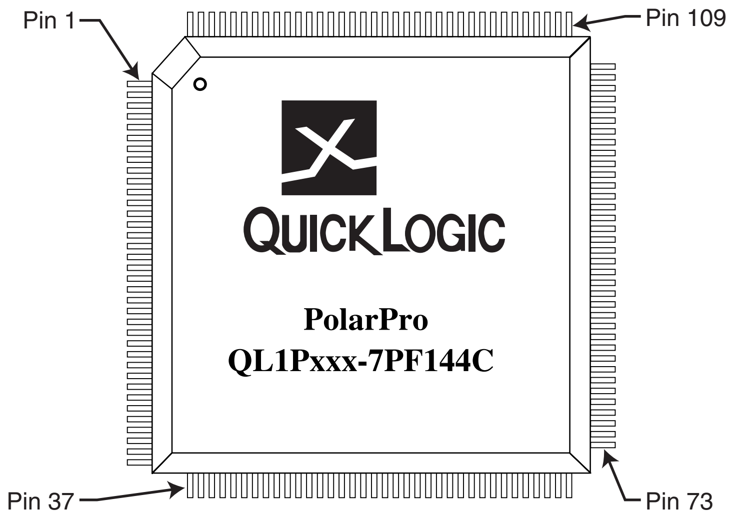
Packaging Pinout Diagrams and Tables

PolarPro QL1Pxxx - 144 TQFP Pinout Diagram



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PolarPro QL1Pxxx - 144 TQFP Pinout Table

Table 45: QL1P050 – 144 TQFP Pinout Table

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	VCCIO(C)	37	GND	73	VCCIO(A)	109	VCCIO(D)
2	GPIO(C)	38	GPIO(B)	74	GPIO(A)	110	VREF(D)
3	GPIO(C)	39	GPIO(B)	75	GPIO(A)	111	DQ/GPIO(D)
4	GPIO(C)	40	TDO	76	GPIO(A)	112	DQ/GPIO(D)
5	GPIO(C)	41	VCCIO(B)	77	GPIO(A)	113	DQ/GPIO(D)
6	GPIO(C)	42	GPIO(B)	78	GPIO(A)	114	DQ/GPIO(D)
7	GPIO(C)	43	GPIO(B)	79	VCC	115	DQCK_N/GPIO(D)
8	GPIO(C)	44	GPIO(B)	80	GPIO(A)	116	DQCK_P/GPIO(D)
9	GPIO(C)	45	GPIO(B)	81	TRSTB	117	DQS/GPIO(D)
10	GPIO(C)	46	GPIO(B)	82	GPIO(A)	118	DQ/GPIO(D)
11	GPIO(C)	47	GPIO(B)	83	GPIO(A)	119	DQ/GPIO(D)
12	GPIO(C)	48	GPIO(B)	84	CLK(A)/CCMIN(1)	120	DQ/GPIO(D)
13	VCC	49	GPIO(B)	85	GPIO(A)	121	TMS
14	GPIO(C)	50	GPIO(B)	86	VCCIO(A)	122	DQ/GPIO(D)
15	GPIO(C)	51	GPIO(B)	87	GPIO(A)	123	DQ/GPIO(D)
16	VCC	52	TDI	88	GPIO(A)	124	VCC
17	GPIO(C)	53	CLK(B)	89	GPIO(A)	125	CLK(D)
18	GPIO(C)	54	VCCIO(B)	90	VCC	126	VCCIO(D)
19	VCCIO(C)	55	VCC	91	GPIO(A)	127	DQ/GPIO(D)
20	GPIO(C)	56	CLK(B)	92	GPIO(A)	128	DQ/GPIO(D)
21	GPIO(C)	57	GPIO(B)	93	VCC	129	DQ/GPIO(D)
22	GPIO(C)	58	VCC	94	GPIO(A)	130	DQ/GPIO(D)
23	CLK(C)	59	GPIO(B)	95	GPIO(A)	131	DQCK_N/GPIO(D)
24	TCK	60	GPIO(B)	96	GPIO(A)	132	DQCK_P/GPIO(D)
25	GPIO(C)	61	GPIO(B)	97	GPIO(A)	133	DQS/GPIO(D)
26	GPIO(C)	62	GPIO(B)	98	GPIO(A)	134	DQ/GPIO(D)
27	VCCIO(B)	63	GPIO(B)	99	GPIO(A)	135	DQ/GPIO(D)
28	GPIO(C)	64	GPIO(B)	100	GPIO(A)	136	DQ/GPIO(D)
29	GPIO(C)	65	GPIO(B)	101	GPIO(A)	137	DQ/GPIO(D)
30	GPIO(C)	66	GPIO(B)	102	GPIO(A)	138	VREF(D)
31	GPIO(C)	67	GPIO(B)	103	GPIO(A)	139	DQ/GPIO(D)
32	GPIO(C)	68	GPIO(B)	104	CCMVCC(1)	140	VCCIO(D)
33	GPIO(C)	69	VCCIO(B)	105	VCCIO(A)	141	VCC
34	VCCIO(C)	70	VLP	106	CCMGND(1)	142	VCCIO(D)
35	GND	71	POR	107	GND	143	GND
36	GND	72	GND	108	GND	144	GND

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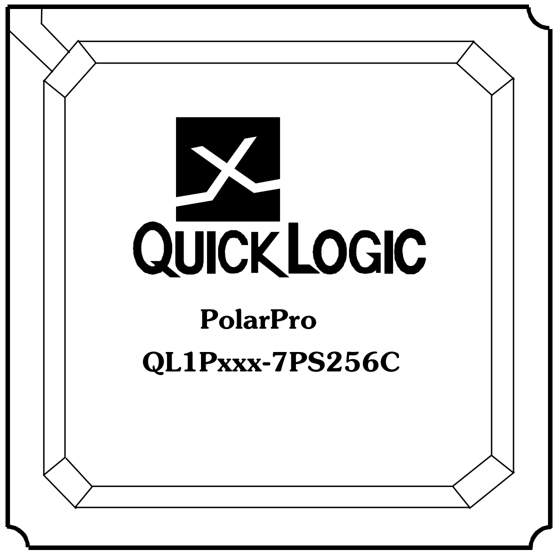
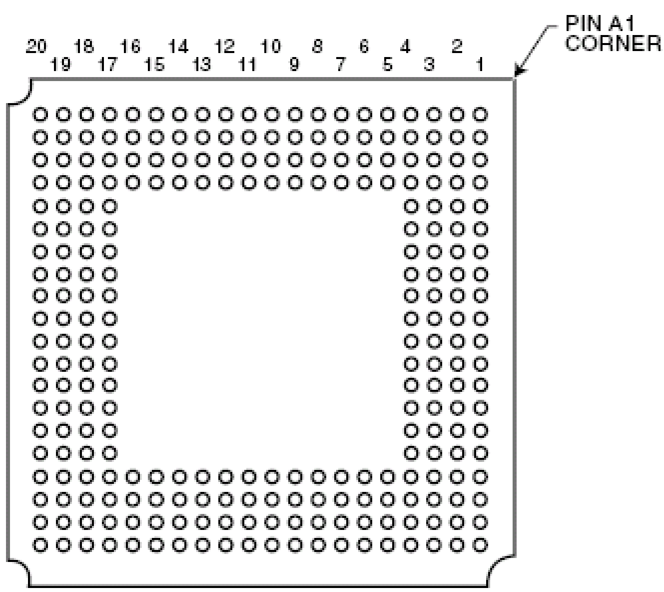
PolarPro QL1Pxxx - 256 LBGA Pinout Diagram

Top



Bottom



PRELIMINARY

PolarPro QL1Pxxx - 256 LBGA Pinout Table

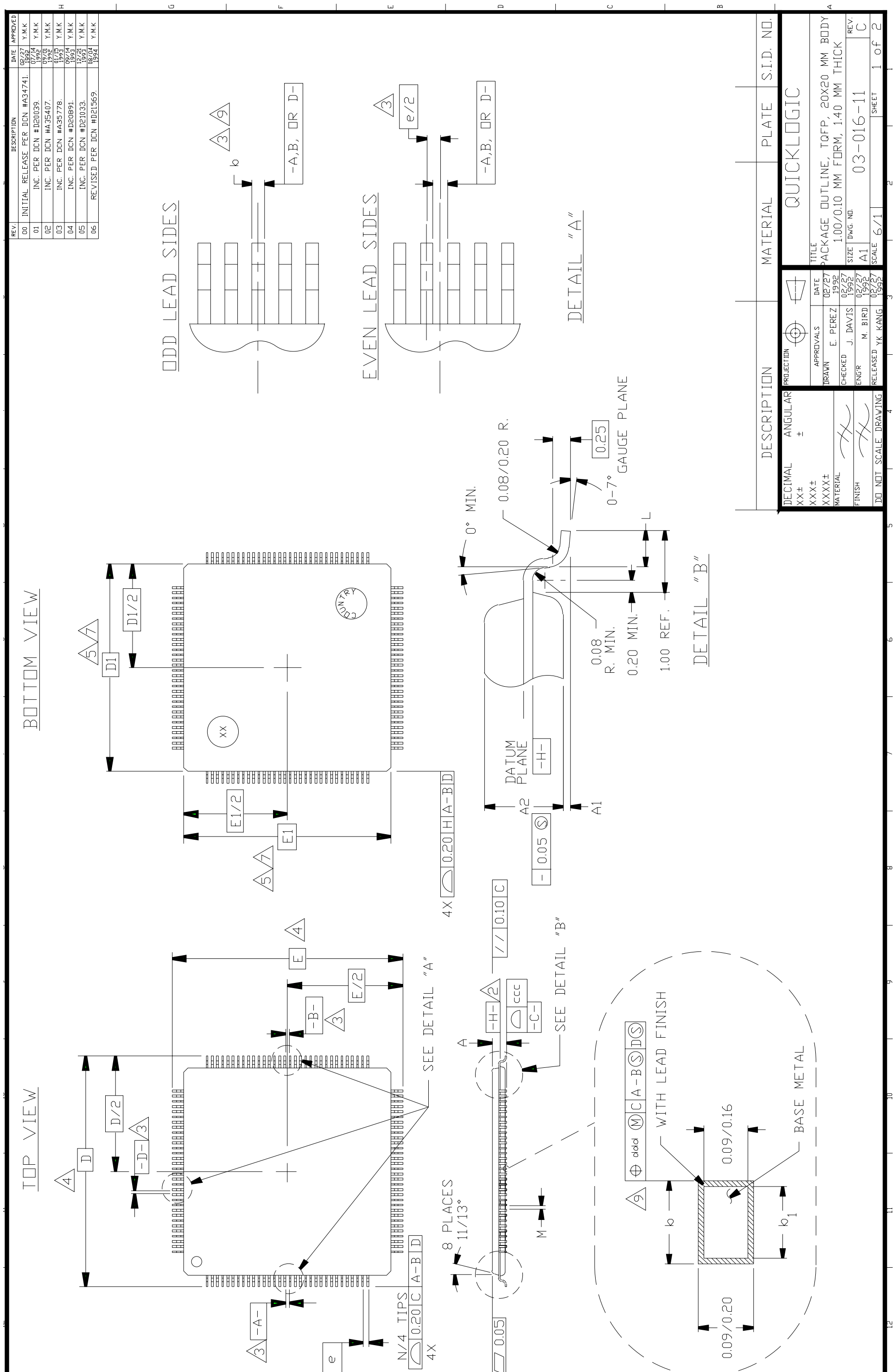
Table 46: QL1P050 – 256 LBGA Pinout Table

Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function
A1	GND	C12	DQCK/GPIO(D)	F7	VCC	J2	GPIO(C)	L13	GPIO(A)	P8	GPIO(B)
A2	DQ/GPIO(D)	C13	DQCK/GPIO(D)	F8	GND	J3	GPIO(C)	L14	GPIO(A)	P9	GPIO(B)
A3	DQ/GPIO(D)	C14	GND	F9	TMS	J4	GPIO(C)	L15	GPIO(A)	P10	GPIO(B)
A4	DQ/GPIO(D)	C15	DQ/GPIO(D)	F10	VCC	J5	VCCIO(C)	L16	GPIO(A)	P11	GPIO(B)
A5	DQ/GPIO(D)	C16	DQ/GPIO(D)	F11	DQ/GPIO(D)	J6	GND	M1	GPIO(C)	P12	GPIO(B)
A6	DQ/GPIO(D)	D1	GPIO(C)	F12	CCMVCC(1)	J7	GND	M2	GPIO(C)	P13	GPIO(B)
A7	DQS/GPIO(D)	D2	GPIO(C)	F13	GPIO(A)	J8	VCC	M3	GPIO(B)	P14	GND
A8	DQ/GPIO(D)	D3	GPIO(C)	F14	GPIO(A)	J9	VCC	M4	GPIO(B)	P15	GPIO(B)
A9	CLK(D)	D4	GPIO(C)	F15	GPIO(A)	J10	GND	M5	GPIO(B)	P16	GPIO(B)
A10	DQ/GPIO(D)	D5	VREF(D)	F16	GPIO(A)	J11	TRSTB	M6	VCCIO(B)	R1	GPIO(B)
A11	DQ/GPIO(D)	D6	DQS/GPIO(D)	G1	GPIO(C)	J12	VCCIO(A)	M7	VCCIO(B)	R2	GPIO(B)
A12	DQ/GPIO(D)	D7	DQ/GPIO(D)	G2	GPIO(C)	J13	GPIO(A)	M8	VCCIO(B)	R3	GPIO(B)
A13	DQ/GPIO(D)	D8	DQ/GPIO(D)	G3	GPIO(C)	J14	GPIO(A)	M9	VCCIO(B)	R4	GPIO(B)
A14	DQ/GPIO(D)	D9	DQ/GPIO(D)	G4	GPIO(C)	J15	GPIO(A)	M10	VCCIO(B)	R5	TDO
A15	GPIO(A)	D10	DQCK/GPIO(D)	G5	GPIO(C)	J16	CLK(A) CCMIN(1)	M11	VCCIO(B)	R6	GPIO(B)
A16	GND	D11	DQ/GPIO(D)	G6	VCC	K1	GPIO(C)	M12	GPIO(B)	R7	GPIO(B)
B1	DQ/GPIO(D)	D12	VREF(D)	G7	GND	K2	GPIO(C)	M13	GPIO(A)	R8	GPIO(B)
B2	DQ/GPIO(D)	D13	DQ/GPIO(D)	G8	GND	K3	GPIO(C)	M14	GPIO(A)	R9	GPIO(B)
B3	DQ/GPIO(D)	D14	GPIO(A)	G9	GND	K4	GPIO(C)	M15	GPIO(A)	R10	GPIO(B)
B4	DQ/GPIO(D)	D15	GPIO(A)	G10	GND	K5	GPIO(C)	M16	GPIO(A)	R11	GPIO(B)
B5	DQ/GPIO(D)	D16	GPIO(A)	G11	VCC	K6	VCC	N1	GPIO(B)	R12	GPIO(B)
B6	DQ/GPIO(D)	E1	GPIO(C)	G12	GPIO(A)	K7	GND	N2	GPIO(B)	R13	GPIO(B)
B7	DQCK/GPIO(D)	E2	GPIO(C)	G13	GPIO(A)	K8	GND	N3	GPIO(B)	R14	GPIO(B)
B8	DQCK/GPIO(D)	E3	GPIO(C)	G14	GPIO(A)	K9	GND	N4	GPIO(B)	R15	GPIO(B)
B9	DQ/GPIO(D)	E4	GPIO(C)	G15	GPIO(A)	K10	GND	N5	GPIO(B)	R16	GPIO(B)
B10	DQ/GPIO(D)	E5	CCMGND(0)	G16	GPIO(A)	K11	VCC	N6	GPIO(B)	T1	GND
B11	DQ/GPIO(D)	E6	VCCIO(D)	H1	CLK(C)/ CCMIN(0)	K12	GPIO(A)	N7	GPIO(B)	T2	GPIO(B)
B12	DQ/GPIO(D)	E7	VCCIO(D)	H2	GPIO(C)	K13	GPIO(A)	N8	GPIO(B)	T3	GPIO(B)
B13	DQ/GPIO(D)	E8	VCCIO(D)	H3	GPIO(C)	K14	GPIO(A)	N9	GPIO(B)	T4	GPIO(B)
B14	DQ/GPIO(D)	E9	VCCIO(D)	H4	GPIO(C)	K15	GPIO(A)	N10	GPIO(B)	T5	GPIO(B)
B15	DQ/GPIO(D)	E10	VCCIO(D)	H5	VCCIO(C)	K16	GPIO(A)	N11	GPIO(B)	T6	GPIO(B)
B16	DQS/GPIO(D)	E11	VCCIO(D)	H6	TCK	L1	GPIO(C)	N12	GPIO(B)	T7	CLK(B)
C1	GPIO(C)	E12	CCMGND(1)	H7	GND	L2	GPIO(C)	N13	GPIO(B)	T8	GPIO(B)
C2	GPIO(C)	E13	GPIO(A)	H8	VCC	L3	GPIO(C)	N14	GPIO(B)	T9	CLK(B)
C3	GND	E14	GPIO(A)	H9	VCC	L4	GPIO(C)	N15	GPIO(A)	T10	GPIO(B)
C4	DQ/GPIO(D)	E15	GPIO(A)	H10	GND	L5	GPIO(C)	N16	GPIO(B)	T11	GPIO(B)
C5	DQCK/GPIO(D)	E16	GPIO(A)	H11	GND	L6	STM	P1	GPIO(B)	T12	GPIO(B)
C6	DQCK/GPIO(D)	F1	GPIO(C)	H12	VCCIO(A)	L7	VCC	P2	GPIO(B)	T13	GPIO(B)
C7	DQ/GPIO(D)	F2	GPIO(C)	H13	GPIO(A)	L8	TDI	P3	GND	T14	GPIO(B)
C8	DQ/GPIO(D)	F3	GPIO(C)	H14	GPIO(A)	L9	POR	P4	GPIO(B)	T15	GPIO(B)
C9	DQ/GPIO(D)	F4	GPIO(C)	H15	GPIO(A)	L10	VCC	P5	GPIO(B)	T16	GND
C10	DQCK/GPIO(D)	F5	CCMVCC(0)	H16	GPIO(A)	L11	VCCIO(B)	P6	GPIO(B)		
C11	DQ/GPIO(D)	F6	VCC	J1	GPIO(C)	L12	VLP	P7	GPIO(B)		

PRELIMINARY

Package Mechanical Drawings

144 TQFP Packaging Drawing



PRELIMINARY

144 TQFP Packaging Drawing (Continued)

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. DATUM PLANE -H- LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DATUMS A-B AND -D- TO BE DETERMINED AT CENTERLINE BETWEEN LEADS WHERE LEADS EXIT PLASTIC BODY AT DATUM PLANE -H- .
4. TO BE DETERMINED AT SEATING PLANE -C- .
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.254 MM ON D1 AND E1 DIMENSIONS.
6. "N" IS THE TOTAL NUMBER OF TERMINALS.
7. THESE DIMENSIONS TO BE DETERMINED AT DATUM PLANE -H- .
8. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15 MILLIMETERS, AND THE TOP OF THE PACKAGE WILL NOT OVERHANG THE BOTTOM OF THE PACKAGE.
9. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
10. CONTROLLING DIMENSION: MILLIMETER.
11. MAXIMUM ALLOWABLE DIE THICKNESS TO BE ASSEMBLED IN THIS PACKAGE FAMILY IS 0.38 MILLIMETERS.
12. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-136, VARIATION BT.

(JEDEC VARIATION)

ALL DIMENSIONS IN MILLIMETERS

SYMBOL	BT MIN.	BT NOM.	BT MAX.	NOTE
A	—	—	1.60	
A_1	0.05	0.10	0.15	
A_2	1.35	1.40	1.45	
D		22.00 BSC.		4
D_1		20.00 BSC.		7,8
E		22.00 BSC.		4
E_1		20.00 BSC.		7,8
L	0.45	0.60	0.75	
M	0.14	—	—	
N		*128, 144		
e		0.50 BSC.		
b	0.17	0.22	0.27	9
b1	0.17	0.20	0.23	
ccc	—	—	0.08	
ddd	—	—	0.08	

* NOTE: THE 128 LEAD IS A COMPLIANT DEPOPULATION OF THE 144 LEAD MO-136 VARIATION BT.

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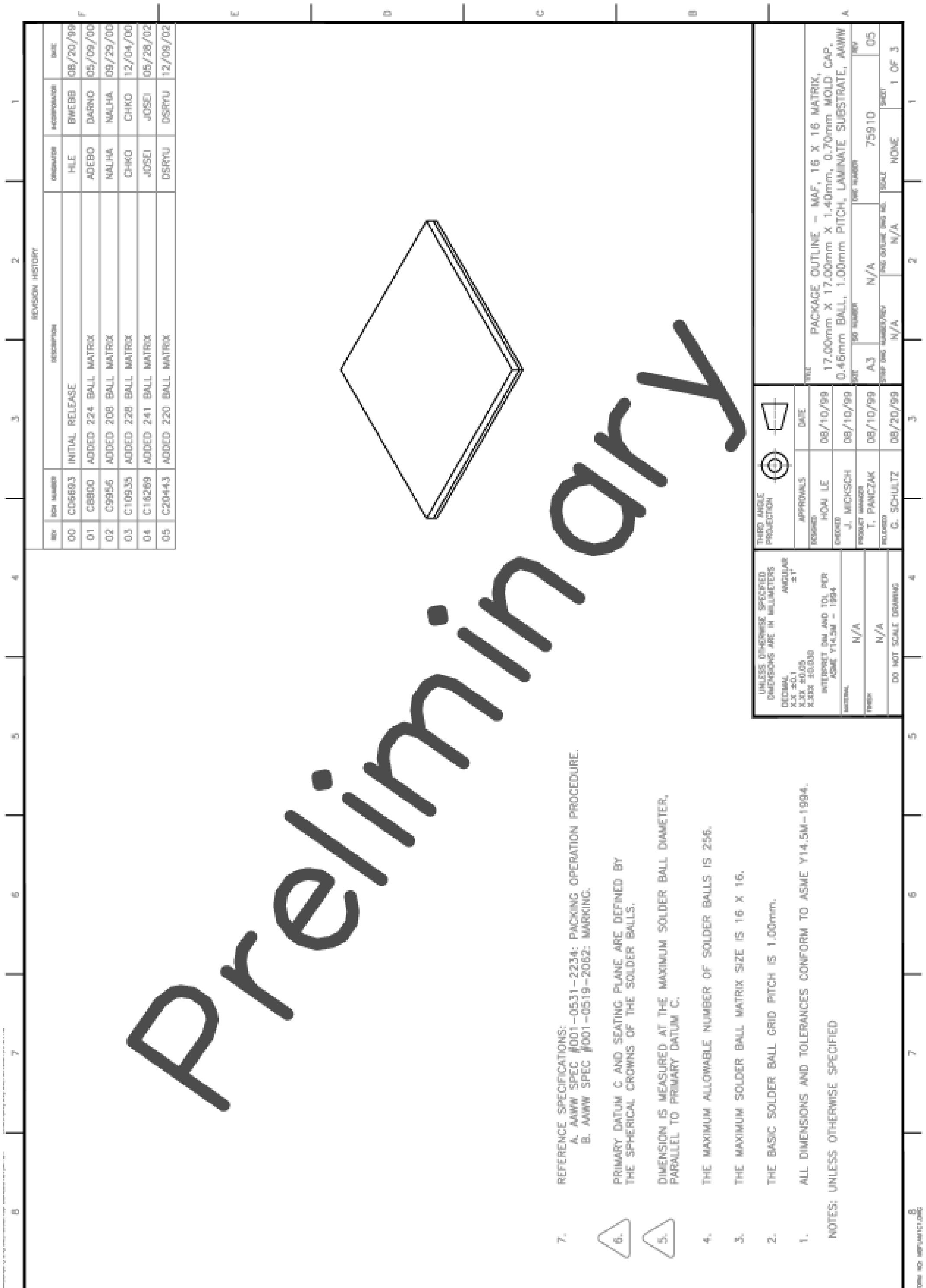
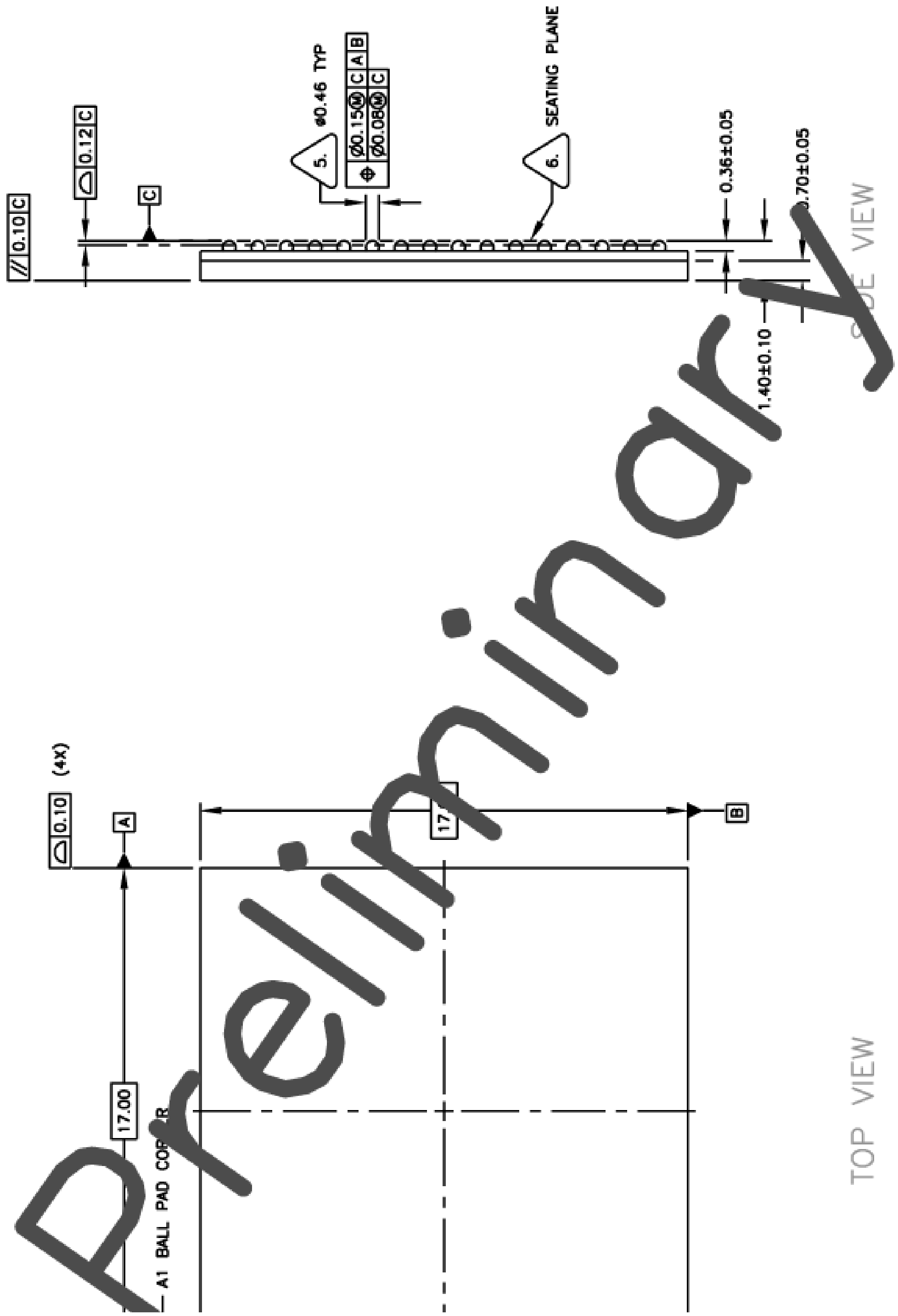
PRELIMINARY

256 LBGA Package Drawing



256 LBGA Package Drawing (Continued)



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PRELIMINARY

Packaging Information

The PolarPro product family packaging information is presented in **Table 47**.

Table 47: Packaging Options

Device Information	Device			
	QL1P075 / QL1P100		QL1P150 / QL1P300 / QL1P600 / QL1P1000	
	Pin	Pitch	Pin	Pitch
Package Definitions[a]	144 TQFP	0.50 mm		
	196 TFBGA	0.80 mm		
	256 LBGA	1.0 mm	256 LBGA	1.0 mm
			324 LBGA	1.0 mm

a. TFBGA = Thin Profile Fine Pitch Ball Grid Array
LBGA = Low Profile Ball Grid Array
TQFP = Thin Quad Flat Pack

Ordering Information

QL 1P075 -6 PF144 C

Operating Range:
C = Commercial
I = Industrial
M = Military

Package Lead Count:
PF144 (PFN144)* = 144-pin TQFP (0.5 mm)
PT196 (PTN196)* = 196-pin TFBGA (0.8 mm)
PS256 (PSN256)* = 256-pin LBGA (1.0 mm)
PS324 (PSN324)* = 324-pin LBGA (1.0 mm)

Speed Grade:
-6 - fast
-7 - faster
-8 - fastest

Part Number:
1P075
1P100
1P150
1P300
1P600
1P1000

QuickLogic Device

* Lead-free packaging is available, contact QuickLogic regarding availability (see Contact Information).

Contact Information

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Revision History

Revision	Date	Originator and Comments
A	November 2005	Jason Lew and Kathleen Murchek First release

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