

# PXN011-100QL

N-channel 100 V, 11 mOhm, logic level Trench MOSFET in MLPAK33

21 September 2023

Product data sheet

# 1. General description

General purpose MOSFET for standard applications, 56 A, logic level N-channel enhancement mode Power MOSFET in MLPAK33 package.

# 2. Features and benefits

- Logic level compatibility
- Trench MOSFET technology
- Thermally efficient package in a small form factor (3.3 mm x 3.3 mm footprint)

# 3. Applications

- Secondary side synchronous rectification
- DC-to-DC converters
- Home appliance
- Motor drive
- Load switching
- LED lighting

# 4. Quick reference data

#### Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Мах	Unit
V <sub>DS</sub>	drain-source voltage	25 °C ≤ T <sub>j</sub> ≤ 150 °C		-	-	100	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 25 °C; <u>Fig. 2</u>		-	-	56	А
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <u>Fig. 1</u>		-	-	66	W
Tj	junction temperature			-55	-	150	°C
Static chara	acteristics						
R <sub>DSon</sub>	drain-source on-state	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 10 A; T <sub>j</sub> = 25 °C; <u>Fig. 9</u>		-	8.3	11	mΩ
	resistance	$V_{GS}$ = 4.5 V; I <sub>D</sub> = 10 A; T <sub>j</sub> = 25 °C; <u>Fig. 9</u>		-	10.4	14	mΩ
Dynamic ch	naracteristics	·		•			
Q <sub>GD</sub>	gate-drain charge	$I_D$ = 10 A; $V_{DS}$ = 50 V; $V_{GS}$ = 4.5 V;		-	7.5	-	nC
Q <sub>G(tot)</sub>	total gate charge	T <sub>j</sub> = 25 °C; <u>Fig. 11; Fig. 12</u>		-	18	-	nC
Avalanche ı	ruggedness	·					
E <sub>DS(AL)S</sub>	non-repetitive drain- source avalanche energy	$\label{eq:ID} \begin{array}{l} I_D = 9.2 \text{ A}; \ V_{sup} \leq \ 100 \text{ V}; \ V_{GS} = 10 \text{ V}; \\ T_{j(init)} = 25 \ ^\circ\text{C}; \ unclamped \end{array}$	[1]	-	-	168.9	mJ

# nexperia

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Symbol	Parameter	Conditions		Min	Тур	Мах	Unit
Source-drain d	iode						
Qr		$I_{S} = 10 \text{ A}; \text{ d}I_{S}/\text{d}t = -100 \text{ A}/\mu\text{s}; \text{ V}_{GS} = 0 \text{ V}; \\ \text{V}_{DS} = 50 \text{ V}; \text{ T}_{j} = 25 ^{\circ}\text{C}; \text{ Fig. 15}$	[2]	-	19	-	nC

[1] Protected by 100% test

[2] includes capacitive recovery

# 5. Pinning information

#### Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	1 2 3 4	
2	S	source	رف ف ف ف	
3	S	source		D
4	G	gate		
5	D	drain		G C C C C C C C C C C C C C C C C C C C
6	D	drain	Цеее	mbb076 S
7	D	drain		
8	D	drain	MLPAK33 (SOT8002-1)	

# 6. Ordering information

# Table 3. Ordering information Type number Package Name Description Version PXN011-100QL MLPAK33 plastic thermal enhanced surface mounted package; mini leads; 8 terminals; pitch 0.65 mm; 3.3 x 3.3 x 0.8 mm body SOT8002-1

# 7. Marking

Table 4. Marking codes	
Type number	Marking code
PXN011-100QL	9AL

# 8. Limiting values

#### Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Tj = 25 °C unless otherwise stated.

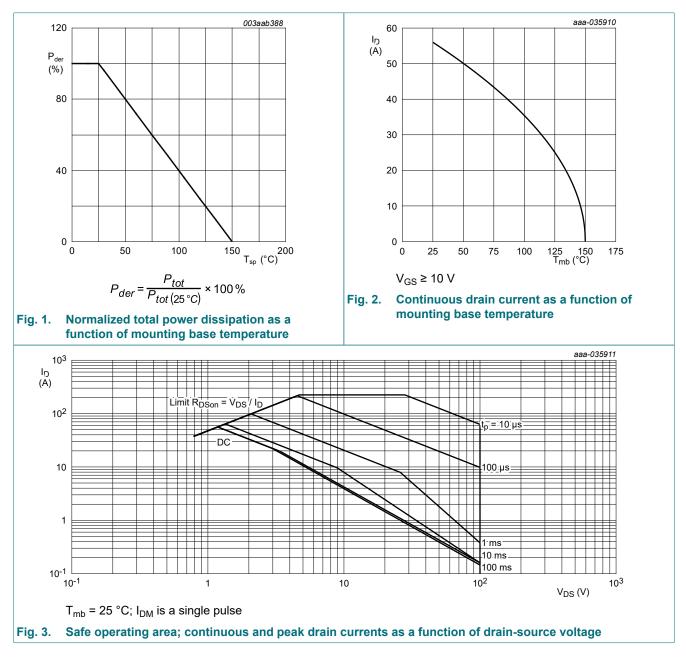
Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DS</sub>	drain-source voltage	25 °C ≤ T <sub>j</sub> ≤ 150 °C	-	100	V
V <sub>GS</sub>	gate-source voltage		-20	20	V
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <u>Fig. 1</u>	-	66	W
I <sub>D</sub>	drain current	V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 25 °C; <u>Fig. 2</u>	-	56	А
		V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 100 °C; <u>Fig. 2</u>	-	35	A
I <sub>DM</sub>	peak drain current	pulsed; $t_p \le 10 \ \mu s$ ; $T_{mb} = 25 \ ^{\circ}C$ ; Fig. 3	-	224	А
T <sub>stg</sub>	storage temperature		-55	150	°C

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Symbol	Parameter	Conditions		Min	Max	Unit
Tj	junction temperature			-55	150	°C
T <sub>sld(M)</sub>	peak soldering temperature			-	260	°C
Source-drai	n diode				-	
Is	source current	T <sub>mb</sub> = 25 °C		-	55	А
I <sub>SM</sub>	peak source current	pulsed; $t_p \le 10 \ \mu s$ ; $T_{mb} = 25 \ ^{\circ}C$		-	224	А
Avalanche r	ruggedness					
E <sub>DS(AL)S</sub>	non-repetitive drain- source avalanche energy	$\begin{split} I_D &= 9.2 \text{ A};  \text{V}_{\text{sup}} \leq \ 100  \text{V};  \text{V}_{\text{GS}} = 10  \text{V}; \\ \text{T}_{j(\text{init})} &= 25 ^{\circ}\text{C}; \text{ unclamped} \end{split}$	[1]	-	168.9	mJ
I <sub>AS</sub>	non-repetitive avalanche current	T <sub>j(init)</sub> = 25 °C	[1]	-	9.2	A

[1] Protected by 100% test



PXN011-100QL

# 9. Thermal characteristics

#### **Table 6. Thermal characteristics** Conditions Symbol Parameter Min Тур Max Unit 1.57 K/W thermal resistance from Fig. 4 1.89 $R_{th(j-mb)}$ junction to mounting base aaa-035912 10 Z<sub>th(i-mb)</sub> (K/W) 1 δ\_= 0.5 ŧ 0:2-TT Ш 0:1<sup>.</sup> 10<sup>-1</sup> 0.05 0.02 tp Р δ= т single shot 10<sup>-2</sup> t t<sub>p</sub> |≁− т 10<sup>-3</sup> 10<sup>-6</sup> 10<sup>-2</sup> 10<sup>-5</sup> 10<sup>-3</sup> 10-4 10<sup>-1</sup> 1 t<sub>p</sub> (s) Transient thermal impedance from junction to mounting base as a function of pulse duration Fig. 4.

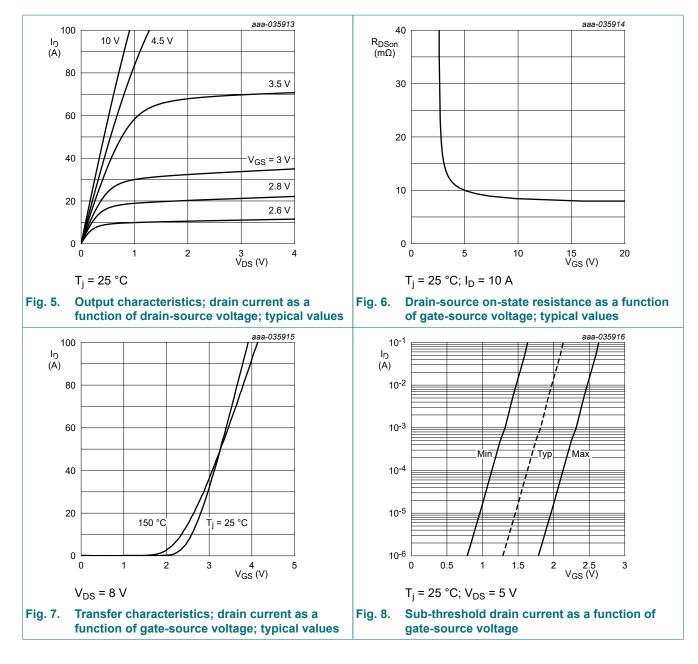
# **10. Characteristics**

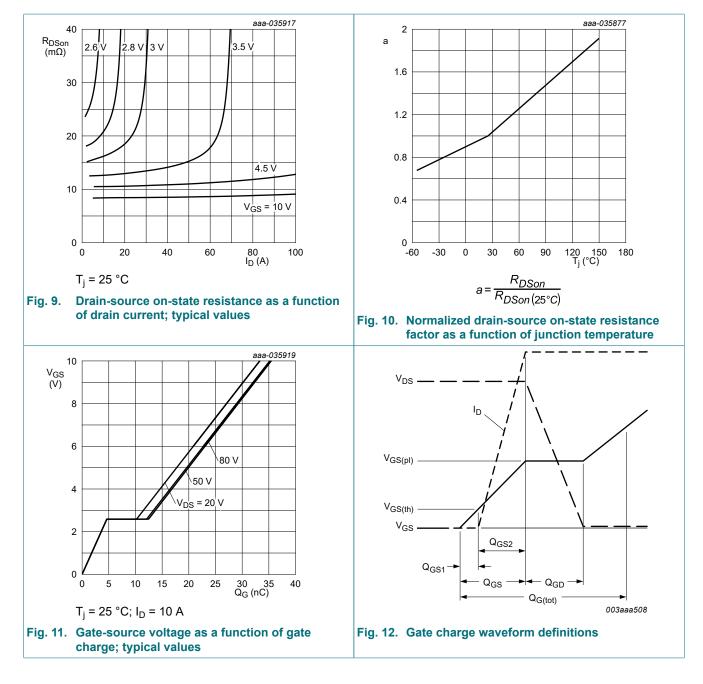
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static charac	teristics					
V <sub>(BR)DSS</sub>	drain-source	I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C	100	-	-	V
	breakdown voltage	I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V; T <sub>j</sub> = -55 °C	-	100	-	V
V <sub>GS(th)</sub>	gate-source threshold voltage	$I_D = 0.25 \text{ mA}; V_{DS}=V_{GS}; T_j = 25 \text{ °C};$ Fig. 8	1.2	1.53	2.2	V
		I <sub>D</sub> = 0.25 mA; V <sub>DS</sub> =V <sub>GS</sub> ; T <sub>j</sub> = 150 °C	-	0.8	-	V
		I <sub>D</sub> = 0.25 mA; V <sub>DS</sub> =V <sub>GS</sub> ; T <sub>j</sub> = -55 °C	-	1.9	-	V
$\Delta V_{GS(th)} / \Delta T$	gate-source threshold voltage variation with temperature	25 °C ≤ T <sub>j</sub> ≤ 150 °C	-	-6.1	-	mV/K
I <sub>DSS</sub>	drain leakage current	V <sub>DS</sub> = 100 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	0.02	1	μA
		V <sub>DS</sub> = 100 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 150 °C	-	22	-	μA
I <sub>GSS</sub>	gate leakage current	$V_{GS}$ = 20 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C	-	2	100	nA
		V <sub>GS</sub> = -20 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	2	100	nA
R <sub>DSon</sub>	drain-source on-state	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 10 A; T <sub>j</sub> = 25 °C; <u>Fig. 9</u>	-	8.3	11	mΩ
	resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 10 A; T <sub>j</sub> = 150 °C; Fig. 10	-	-	21	mΩ
		V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 10 A; T <sub>j</sub> = 25 °C; <u>Fig. 9</u>	-	10.4	14	mΩ
		V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 10 A; T <sub>j</sub> = 150 °C; Fig. 10	-	-	27	mΩ

#### PXN011-100QL

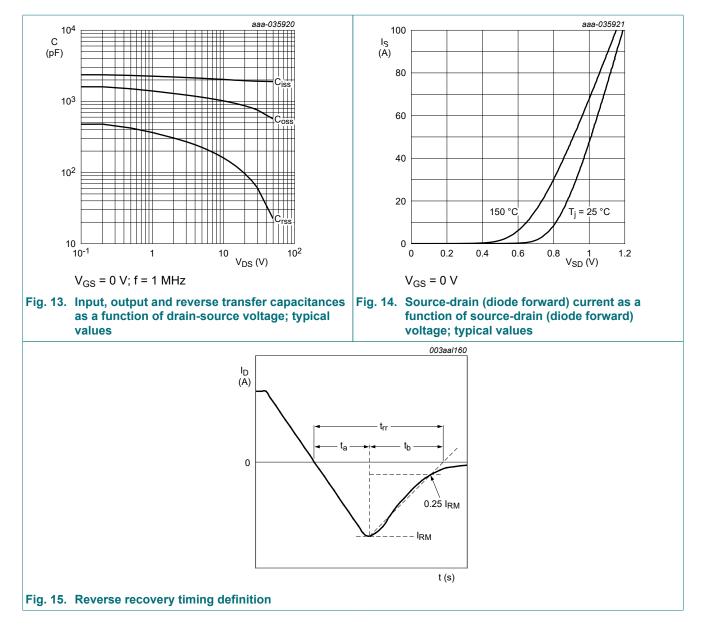
Symbol	Parameter	Conditions	Mi	in Typ	Мах	Unit
R <sub>G</sub>	gate resistance	f = 1 MHz; T <sub>j</sub> = 25 °C	-	1	-	Ω
Dynamic ch	naracteristics	· · ·		I		
Q <sub>G(tot)</sub>	total gate charge	$    I_D = 10 \text{ A}; \text{ V}_{DS} = 50 \text{ V}; \text{ V}_{GS} = 4.5 \text{ V}; \\ \text{T}_j = 25 \text{ °C}; \text{ Fig. 11}; \text{ Fig. 12}                                   $	-	18	-	nC
		$\label{eq:ID} \begin{array}{l} I_D = 10 \text{ A};  \text{V}_{DS} = 50  \text{V};  \text{V}_{GS} = 10  \text{V}; \\ \text{T}_j = 25 ^\circ\text{C}; \begin{array}{l} \text{Fig. 11}; \\ \text{Fig. 12} \end{array}$	-	35	-	nC
		$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V};$ $T_j = 25 \text{ °C}$	-	30	-	nC
Q <sub>GS</sub>	gate-source charge	I <sub>D</sub> = 10 A; V <sub>DS</sub> = 50 V; V <sub>GS</sub> = 4.5 V;	-	4.6	-	nC
Q <sub>GS(th)</sub>	pre-threshold gate- source charge	T <sub>j</sub> = 25 °C; <u>Fig. 11; Fig. 12</u>	-	3	-	nC
Q <sub>GS(th-pl)</sub>	post-threshold gate- source charge		-	1.6	-	nC
Q <sub>GD</sub>	gate-drain charge	_	-	7.5	-	nC
V <sub>GS(pl)</sub>	gate-source plateau voltage	I <sub>D</sub> = 10 A; V <sub>DS</sub> = 50 V; T <sub>j</sub> = 25 °C; Fig. 11; Fig. 12	-	2.6	-	V
C <sub>iss</sub>	input capacitance	V <sub>DS</sub> = 50 V; V <sub>GS</sub> = 0 V; f = 1 MHz;	-	1898	-	pF
C <sub>oss</sub>	output capacitance	T <sub>j</sub> = 25 °C; <u>Fig. 13</u>	-	567	-	pF
C <sub>rss</sub>	reverse transfer capacitance	-	-	22	-	pF
t <sub>d(on)</sub>	turn-on delay time	$V_{DS}$ = 50 V; $R_{L}$ = 5 $\Omega$ ; $V_{GS}$ = 4.5 V;	-	13	-	ns
t <sub>r</sub>	rise time	R <sub>G(ext)</sub> = 5 Ω; T <sub>j</sub> = 25 °C	-	21	-	ns
t <sub>d(off)</sub>	turn-off delay time	_	-	22	-	ns
t <sub>f</sub>	fall time	1	-	18	-	ns
Q <sub>oss</sub>	output charge	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 50 V; f = 1 MHz; T <sub>j</sub> = 25 °C	-	42	-	nC
Source-drai	in diode			I		
V <sub>SD</sub>	source-drain voltage	$I_{S}$ = 10 A; $V_{GS}$ = 0 V; $T_{j}$ = 25 °C; <u>Fig. 14</u>	-	0.8	1.2	V
t <sub>rr</sub>	reverse recovery time	$I_{S} = 10 \text{ A}; \text{ d}I_{S}/\text{d}t = -100 \text{ A}/\mu\text{s}; \text{ V}_{GS} = 0 \text{ V};$	-	29	-	ns
Q <sub>r</sub>	recovered charge	V <sub>DS</sub> = 50 V; T <sub>j</sub> = 25 °C; <u>Fig. 15</u>	[1] -	19	-	nC

[1] includes capacitive recovery



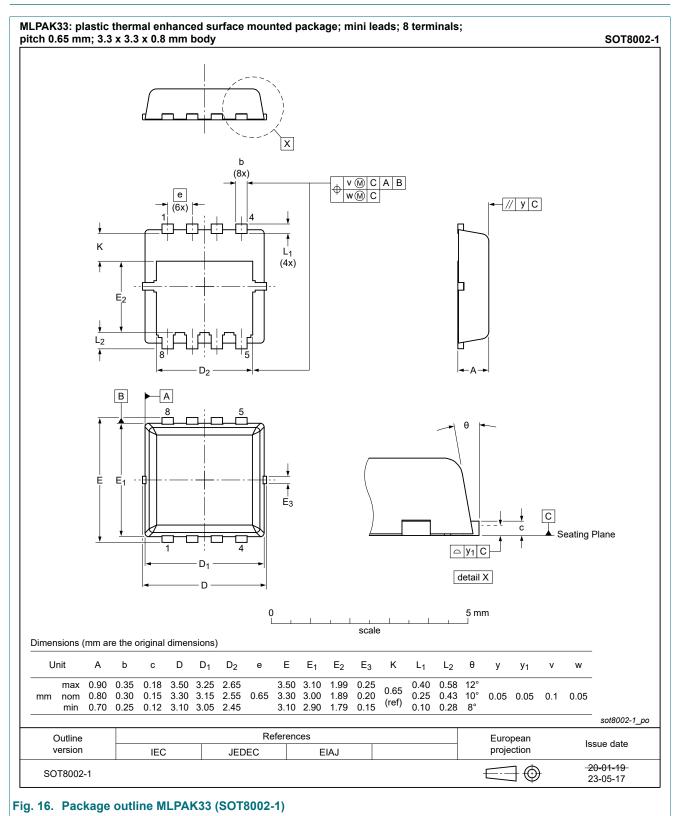


**Product data sheet** 

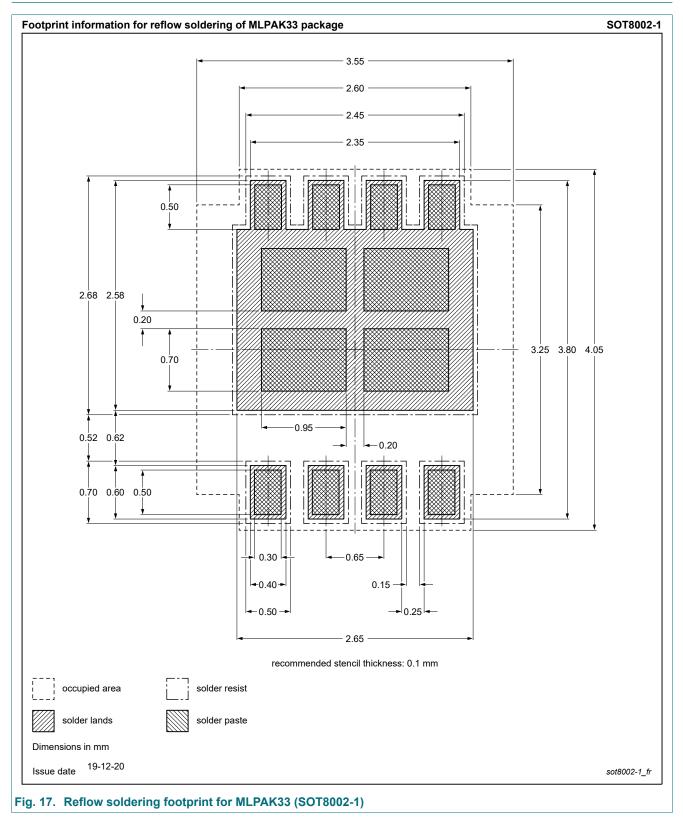


**Product data sheet** 

# 11. Package outline



# 12. Soldering



# 13. Legal information

#### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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