Rockchip PX5 Datasheet

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Chapter 1 Introduction

1.1 Overview

PX5 is a low power, high performance processor for in-vehicle infotainment system, support Android based on the ARM Cortex architecture,, and integrates octa-core Cortex-A53 with separately NEON coprocessor.

Many embedded powerful hardware engines provide optimized performance for high-end application. PX5 supports almost full-format H.264 decoder by 4Kx2K@30fps, H.265 decoder by 4Kx2K@60fps, also support H.264/MVC/VP8 encoder by 1080p@30fps, high-quality JPEG encoder/decoder, and special image preprocessor and postprocessor.

Embedded 3D GPU makes PX5 completely compatible with OpenGL ES3.1, OpenCL1.2 and DirectX 9.3. Special 2D hardware engine with MMU will maximize display performance and provide very smoothly operation.

PX5 has high-performance external memory interface (DDR3/DDR3L /LPDDR2/LPDDR3) capable of sustaining demanding memory bandwidths, also provides a complete set of peripheral interface to support very flexible applications.

1.2 Features

The features listed below which may or may not be present in actual product, may be subject to the third party licensing requirements. Please contact Rockchip for actual product feature configurations and licensing requirements.

1.2.1 Processor

- Octa-core ARM Cortex-A53 MP Core processor, a high-performance, low-power and cached application processor
- Two CPU clusters, with four CPU core for each cluster, One cluster is optimized for high-performance(big cluster) and the other is optimized for low power(little cluster)
- Full implementation of the ARM architecture v8-A instruction set, ARM Neon Advanced SIMD (single instruction, multiple data) support for accelerated media and signal processing computation
- ARMv8 Cryptography Extensions
- In-order pipeline with symmetric dual-issue of most instructions.
- Harvard Level 1 (L1) memory system with a Memory Management Unit (MMU).
- Level 2 (L2) memory system providing cluster memory coherency, including an L2 cache.
- Include VFP v3 hardware to support single and double-precision add, subtract, divide, multiply and accumulate, and square root operations
- SCU ensures memory coherency between the four CPUs for each cluster
- CCI400 ensures the memory coherency between the two clusters
- Integrated 32KB L1 instruction cache , 32KB L1 data cache with 4-way set associative
- 512KB unified L2 Cache for big cluster, 256KB unified L2 Cache for little cluster
- Trustzone technology support
- Full coresight debug solution
  - Debug and trace visibility of whole systems
  - ETM trace support
  - Invasive and non-invasive debug
- Ten separate power domains for CPU core system to support internal power switch and externally turn on/off based on different application scenario
  - PD_A53_L0: 1st Cortex-A53 + Neon + FPU + L1 I/D Cache of little cluster
  - PD_A53_L1: 2nd Cortex-A53 + Neon + FPU + L1 I/D Cache of little cluster
  - PD_A53_L2: 3rd Cortex-A53 + Neon + FPU + L1 I/D Cache of little cluster
  - PD_A53_L3: 4th Cortex-A53 + Neon + FPU + L1 I/D Cache of little cluster

- PD_SCU_L: SCU + L2 Cache controller, and including PD_A53_L0, PD_A53_L1, PD_A53_L2, PD_A53_L3, debug logic of little cluster
- PD_A53_B0: 1st Cortex-A53 + Neon + FPU + L1 I/D Cache of big cluster
- PD_A53_B1: 2nd Cortex-A53 + Neon + FPU + L1 I/D Cache of big cluster
- PD_A53_B2: 3rd Cortex-A53 + Neon + FPU + L1 I/D Cache of big cluster
- PD_A53_B3: 4th Cortex-A53 + Neon + FPU + L1 I/D Cache of big cluster
- PD_SCU_B: SCU + L2 Cache controller, and including PD_A53_B0, PD_A53_B1, PD_A53_B2, PD_A53_B3, debug logic of big cluster

- One isolated voltage domain to support DVFS

1.2.2 Memory Organization

- Internal on-chip memory
  - BootRom
  - Internal SRAM for security and non-security access
- External off-chip memory①
  - DDR3/DDR3L
  - LPDDR2
  - LPDDR3
  - Async Nand Flash(include LBA Nand)
  - Sync ONFI/toggle Nand Flash

1.2.3 Internal Memory

- Internal BootRom
  - Size : 20KB
  - Support system boot from the following device :
    - 8bits Async Nand Flash
    - 8bits toggle Nand Flash
    - SFC interface
    - eMMC interface
    - SDMMC interface
  - Support system code download by the following interface:
    - USB OTG interface
- Internal SRAM
  - Size : 68KB
  - Support security and non-security access
  - Security or non-security space is software programmable
  - Security space can be 0KB,4KB,8KB,12KB,16KB, … up to 64KB by 4KB step

1.2.4 External Memory or Storage device

- Dynamic Memory Interface (DDR3-1066/DDR3L/LPDDR2/LPDDR3)
  - Compatible with JEDEC standard DDR3-1600/DDR3L/LPDDR2/LPDDR3 SDRAM
  - Support one channel, with 16 or 32bits data widths
  - Support up to 2 ranks (chip selects), totally 4GB(max) address space
  - 16bits/32bits data width is software programmable
  - 7 host ports with 64bits/128bits AXI bus interface for system access, AXI bus clock is asynchronous with DDR clock
  - Programmable timing parameters to support DDR3-1600/DDR3L/LPDDR2/LPDDR3 SDRAM from various vendor
  - Advanced command reordering and scheduling to maximize bus utilization
  - Low power modes, such as power-down and self-refresh for DDR3-1600/LPDDR2/LPDDR3 SDRAM; clock stop and deep power-down for LPDDR2/LPDDR3 SDRAM
  - Embedded dynamic drift detection in the PHY to get dynamic drift compensation with the controller
  - Programmable output and ODT impedance with dynamic PVT compensation
  - Support one low-power work mode: power down DDR PHY digital logic power, make

SDRAM still in self-refresh state to prevent data missing.

- Nand Flash Interface
  - Support async nand flash, each channel 8bits, up to 4 banks
  - Support sync DDR nand flash, each channel 8bits, up to 4 banks
  - Support LBA nand flash in async or sync mode
  - Up to 60bits hardware ECC
  - For async nand flash, support configurable interface timing , maximum data rate is 16bit/cycle
  - Embedded special DMA interface to do data transfer
  - Also support data transfer together with general PERI_DMAC in SoC system

- eMMC Interface
  - Compatible with standard iNAND interface
  - Support MMC4.5.1 protocol
  - Provide eMMC boot sequence to receive boot data from external eMMC device
  - Support FIFO over-run and under-run prevention by stopping card clock automatically
  - Support CRC generation and error detection
  - Embedded clock frequency division control to provide programmable baud rate
  - Support block size from 1 to 65535Bytes
  - 8bits data bus width

- SD/MMC Interface
  - Compatible with SD3.0, MMC ver4.5
  - Support FIFO over-run and under-run prevention by stopping card clock automatically
  - Support CRC generation and error detection
  - Embedded clock frequency division control to provide programmable baud rate
  - Support block size from 1 to 65535Bytes
  - Data bus width is 4bits

1.2.5 System Component

- CRU (clock & reset unit)
  - Support clock gating control for individual components inside PX5
  - One oscillator with 24MHz clock input and 6 embedded PLLs
  - Up to 2.2GHz clock output for all PLLs
  - Support global soft-reset control for whole SOC, also individual soft-reset for every components

- PMU(power management unit)
  - Multiple configurable work modes to save power by different frequency or automatical clock gating control or power domain on/off control
  - Lots of wakeup sources in different mode
  - 3 separate voltage domains
  - 16 separate power domains, which can be power up/down by software based on different application scenes

- Timer
  - 12 on-chip 64bits Timers in SoC with interrupt-based operation for non-secure application
  - 2 on-chip 64bits Timers in SoC with interrupt-based operation for secure application
  - Provide two operation modes: free-running and user-defined count
  - Support timer work state checkable
  - Fixed 24MHz clock input

- PWM
  - Four on-chip PWMs with interrupt-based operation
  - Programmable pre-scaled operation to bus clock and then further scaled

- Embedded 32-bit timer/counter facility
- Support capture mode
- Support continuous mode or one-shot mode
- Provides reference mode and output various duty-cycle waveform

- WatchDog
  - 32 bits watchdog counter width
  - Counter clock is from APB bus clock
  - Counter counts down from a preset value to 0 to indicate the occurrence of a timeout
  - WDT can perform two types of operations when timeout occurs:
    - Generate a system reset
    - First generate an interrupt and if this is not cleared by the service routine by the time a second timeout occurs then generate a system reset
  - Programmable reset pulse length
  - Totally 16 defined-ranges of main timeout period

- Bus Architecture
  - 128bit/64-bit/32-bit multi-layer AXI/AHB/APB composite bus architecture
  - CCI400 embedded to support two Cortex-A53 cluster cache coherency
  - 5 embedded AXI interconnect
    - CPU interconnect with four 64-bits AXI masters, one 64-bits AXI slaves, one 32-bits AHB master and lots of 32-bits AHB/APB slaves
    - PERI interconnect with two 64-bits AXI masters, one 64-bits AXI slave, five 32-bits AHB masters and lots of 32-bits AHB/APB slaves
    - Display interconnect with three 128-bits AXI master, four 64-bits AXI masters and one 32-bits AHB slave
    - GPU interconnect with one 128-bits AXI master with point-to-point AXI-lite architecture and 32-bits APB slave
    - VCODEC interconnect also with two 64-bits AXI master and two 32-bits AHB slave, they are point-to-point AXI-lite architecture
  - For each interconnect with AXI/AHB/APB composite bus, clocks for AXI/AHB/APB domains are always synchronous, and different integer ratio is supported for them.
  - Flexible different QoS solution to improve the utility of bus bandwidth

- Interrupt Controller
  - Support 3 PPI interrupt source and 160 SPI interrupt sources input from different components inside PX5
  - Support 16 software-triggered interrupts
  - Input interrupt level is fixed , only high-level sensitive
  - Two interrupt outputs (nFIQ and nIRQ) separately for each Cortex-A53, both are low-level sensitive
  - Support different interrupt priority for each interrupt source, and they are always software-programmable

- DMAC
  - Micro-code programming based DMA
  - The specific instruction set provides flexibility for programming DMA transfers
  - Linked list DMA function is supported to complete scatter-gather transfer
  - Support internal instruction cache
  - Embedded DMA manager thread
  - Support data transfer types with memory-to-memory, memory-to-peripheral, peripheral-to-memory
  - Signals the occurrence of various DMA events using the interrupt output signals
  - Mapping relationship between each channel and different interrupt outputs is software-programmable
  - Two embedded DMA controller , BUS_DMAC is for bus system, PERI_DMAC is for peripheral system

- BUS_DMAC features:
  - 6 channels totally
  - 8 hardware request from peripherals
  - 2 interrupt output
  - Dual APB slave interface for register config, designated as secure and non-secure
  - Support trustzone technology and programmable secure state for each DMA channel
- PERI_DMAC features:
  - 7 channels totally
  - 17 hardware request from peripherals
  - 2 interrupt output
  - Not support trustzone technology

- Security system
  - Support trustzone technology for the following components inside PX5
    - Cortex-A53, support security and non-security mode, switch by software
    - BUS_DMAC, support some dedicated channels work only in security mode
    - eFuse, only accessed by Cortex-A53 in security mode
    - Internal memory , part of space is addressed only in security mode, detailed size is software-programmable together with TZMA(trustzone memory adapter)
  - Embedded encryption and decryption engine
    - Support AES-128/192/256 with ECB, CBC, OFB, CTR, CBC-MAC, CMAC, XCBC-MAC, XTS and CCM modes
    - Supports the DES (ECB and CBC modes) and TDES (EDE and DED) algorithms
    - Supports SHA-1, SHA-256 and SHA-512 modes, as well as HMAC
    - Support all mathematical operations required to implement the PKA supported cryptosystems between 128 bits and 3136 bits in size (in steps of 32 bits)
    - Support random bits generator from the ring oscillator
    - Control the AIB interface to the OTP memory and providing an interface for the CPU to access to the non-confidential trusted data
    - Set the device's security lifecycle state according to the values of various flag words in the OTP memory
    - Provide an firmware interface for secure boot, secure debug
    - Provide a security processor sub-system based on an internal 32-bit CPU
  - Support security boot
  - Support security debug

1.2.6 Video CODEC

- Shared internal memory and bus interface for video decoder and encoder②
- Embedded memory management unit(MMU)
- Video Decoder
  - Real-time video decoder of MPEG-1, MPEG-2, MPEG-4, H.263, H.264, AVS, VC-1, VP8, MVC
  - Error detection and concealment support for all video formats
  - Output data format is YUV420 semi-planar, and YUV400(monochrome) is also supported for H.264
  - H.264 up to HP level 5.2 : 4Kx2K@30fps (4096x2304)®
  - MPEG-4 up to ASP level 5 : 1080p@60fps (1920x1088)
  - MPEG-2 up to MP : 2160p@30fps (3840x2160)
  - MPEG-1 up to MP : 1080p@60fps (1920x1088)
  - H.263 : 576p@60fps (720x576)
  - VC-1 up to AP level 3 : 1080p@30fps (1920x1088)
  - VP8 : 2160p@24fps (3840x2160)
  - AVS : 1080p@60fps (1920x1088)
  - MVC : 2160p@30fps (3840x2160)
  - For AVS, 4:4:4 sampling not supported
  - For H.264, image cropping not supported

- For MPEG-4, GMC(global motion compensation) not supported
- For VC-1, up scaling and range mapping are supported in image post-processor
- For MPEG-4 SP/H.263k, using a modified H.264 in-loop filter to implement deblocking filter in post-processor unit

- Video Encoder
  - Support video encoder for H.264 (BP@level4.0, MP@level4.0, HP@level4.0), MVC and VP8
  - Only support I and P slices, not B slices
  - Support error resilience based on constrained intra prediction and slices
  - Input data format:
    - YCbCr 4:2:0 planar
    - YCbCr 4:2:0 semi-planar
    - YCbYCr 4:2:2
    - CbYCrY 4:2:2 interleaved
    - RGB444 and BGR444
    - RGB555 and BGR555
    - RGB565 and BGR565
    - RGB888 and BRG888
    - RGB101010 and BRG101010
  - Image size is from 96x96 to 1920x1088(Full HD)
  - Maximum frame rate is up to 30fps@1920x1080[3]
  - Bit rate supported is from 10Kbps to 20Mbps

1.2.7 HEVC Decoder

- Main HEVC/H.265 decoder by 4k@60FPS
- Support up to 4096x2304 resolution
- Support up to 100Mbps bit rate
- Embedded memory management unit(MMU)
- Stream error detector (28 IDs)
- Internal 128k cache for bandwidth reduction
- Multi-clock domains and auto clock-gating design for power saving

1.2.8 JPEG CODEC

- JPEG decoder
  - Input JPEG file : YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 sampling formats
  - Output raw image : YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 semi-planar
  - Decoder size is from 48x48 to 8176x8176(66.8Mpixels)
  - Support JPEG ROI(region of image) decode
  - Maximum data rate[4] is up to 76million pixels per second
  - Embedded memory management unit(MMU)

- JPEG encoder
  - Input raw image :
    - YCbCr 4:2:0 planar
    - YCbCr 4:2:0 semi-planar
    - YCbYCr 4:2:2
    - CbYCrY 4:2:2 interleaved
    - RGB444 and BGR444
    - RGB555 and BGR555
    - RGB565 and BGR565
    - RGB888 and BRG888
    - RGB101010 and BRG101010
  - Output JPEG file : JFIF file format 1.02 or Non-progressive JPEG
  - Encoder image size up to 8192x8192(64million pixels) from 96x32
  - Maximum data rate[4] up to 90million pixels per second

- Embedded memory management unit(MMU)

1.2.9 Image Enhancement

- Image pre-processor
  - Only used together with HD video encoder inside PX5, not support stand-alone mode
  - Provides RGB to YCbCr 4:2:0 color space conversion, compatible with BT601, BT709 or user defined coefficients
  - Provides YCbCr4:2:2 to YCbCr4:2:0 color space conversion
  - Support cropping operation from 8192x8192 to any supported encoding size
  - Support rotation with 90 or 270 degrees
- Video stabilization
  - Work in combined mode with HD video encoder inside PX5 and stand-alone mode
  - Adaptive motion compensation filter
  - Support scene detection from video sequence, encodes key frame when scene change noticed
- Image Post-Processor (embedded inside video decoder)
  - Combined with HD video decoder and JPEG decoder, post-processor can read input data directly from decoder output to reduce bus bandwidth
  - Also work as a stand-alone mode, its input data is from image data stored in external memory
  - Input data format:
    - Any format generated by video decoder in combined mode
    - YCbCr 4:2:0 semi-planar
    - YCbCr 4:2:0 planar
    - YCbYCr 4:2:2
    - YCrYCb 4:2:2
    - CbYCrY 4:2:2
    - CrYCbY 4:2:2
  - Output data format:
    - YCbCr 4:2:0 semi-planar
    - YCbYCr 4:2:2
    - YCrYCb 4:2:2
    - CbYCrY 4:2:2
    - CrYCbY 4:2:2
    - Fully configurable ARGB channel lengths and locations inside 32bits, such as ARGB8888, RGB565, ARGB4444 etc.
  - Input image size:
    - Combined mode: from 48x48 to 8176x8176 (66.8Mpixels)
    - Stand-alone mode: width from 48 to 8176,height from 48 to 8176, and maximum size limited to 16.7Mpixels
    - Step size is 16 pixels
  - Output image size: from 16x16 to 1920x1088 (horizontal step size 8,vertical step size 2)
  - Support image up-scaling:
    - Bicubic polynomial interpolation with a four-tap horizontal kernel and a two-tap vertical kernel
    - Arbitrary non-integer scaling ratio separately for both dimensions
    - Maximum output width is 3x input width
    - Maximum output height is 3x input height
  - Support image down-scaling:
    - Arbitrary non-integer scaling ratio separately for both dimensions
    - Unlimited down-scaling ratio
  - Support YUV to RGB color conversion, compatible with BT.601-5, BT.709 and user definable conversion coefficient
  - Support dithering (2x2 ordered spatial dithering) for 4/5/6bit RGB channel precision
  - Support programmable alpha channel and alpha blending operation with the following overlay input formats:

- 8bit alpha + YUV444, big endian channel order with AYUV8888
- 8bit alpha + 24bit RGB, big endian channel order with ARGB8888

- Support deinterlacing with conditional spatial deinterlace filtering, only compatible with YUV420 input format
- Support RGB image contrast/brightness/color saturation adjustment
- Support image cropping & digital zoom only for JPEG or stand-alone mode
- Support picture in picture
- Support image rotation (horizontal flip, vertical flip, rotation 90,180 or 270 degrees)

- Image Enhancement-Processor (IEP)
  - Image format
    - Input data: XRGB/RGB565/YUV420/YUV422
    - Output data: ARGB/RGB565/YUV420/YUV422
    - The format ARGB/XRGB/RGB565/YUV support swap
    - Support YUV semi-planar/planar
    - Support BT601_l/BT601_f/BT709_l/BT709_f color space conversion
    - Support RGB dither up/down conversion
    - Support YUV up/down sampling conversion
    - Max source image resolution: 8192x8192
    - Max scaled image resolution: 4096x4096
  - Enhancement
    - Gamma adjustment with programmable mapping table
    - Hue/Saturation/Brightness/Contrast enhancement
    - Color enhancement with programmable coefficient
    - Detail enhancement with filter matrix up to 9x9
    - Edge enhancement with filter matrix up to 9x9
    - Programmable difference table for detail enhancement
    - Programmable distance table for detail and edge enhancement
  - Noise reduction
    - Compression noise reduction with filter matrix up to 9x9
    - Programmable difference table for compression noise reduction
    - Programmable distance table for compression noise reduction
    - Spatial sampling noise reduction
    - Temporal sampling noise reduction
    - Optional coefficient for sampling noise reduction
  - Scaling
    - Horizontal down-scaling with vertical down-scaling
    - Horizontal down-scaling with vertical up-scaling
    - Horizontal up-scaling with vertical down-scaling
    - Horizontal up-scaling with vertical up-scaling
    - Arbitrary non-integer scaling ratio, from 1/16 to 16
  - Deinterlace
    - Input 4 fields, output 2 frames mode
    - Input 4 fields, output 1 frames mode
    - Input 2 fields, output 1 frames mode
    - Programmable motion detection coefficient
    - Programmable high frequency factor
    - Programmable edge interpolation parameter
    - Source width up to 1920
  - Max resolution for dynamic image
    - Deinterlace: 1920x1080
    - Sampling noise reduction: 1920x1080
    - Compression noise reduction: 4096x2304
    - Enhancement: 4096x2304
  - Interface

- Programmable direct path to VOP
- Embedded memory management unit(MMU)

1.2.10 Graphics Engine

- 3D Graphics Engine :
  - Base handheld architecture fully Microsoft® DirectX™ 9.3, OpenGL® 3.1, and OpenGL ES 3 compliant
  - Support for pull-model attribute evaluation
  - Tile-based deferred rendering architecture with concurrent processing of multiple tiles
  - Multi-threaded Unified Shading Cluster (USC) engine incorporating pixel shader, vertex shader, and GP-GPU (compute shader) functionality
  - USC incorporates an ALU architecture with high SIMD efficiency
  - Fully virtualized memory addressing (up to 1 TB address space), supporting unified memory architecture
  - Fine-grained task switching, workload balancing and power management
  - Dedicated processor for Rogue core firmware execution

- 2D Graphics Engine :
  - BitBlit with Stretch Blit, Simple Blit and Filter Blit
  - Color fill with gradient fill, and pattern fill
  - Line drawing with anti-aliasing and specified width
  - High-performance stretch and shrink
  - Monochrome expansion for text rendering
  - ROP2, ROP3, ROP4
  - Alpha blending modes including global alpha, per pixel alpha, porter-duff and fading
  - 8K x 8K input and 2K x 2K output raster 2D coordinate system
  - Arbitrary degrees rotation with anti-aliasing on every 2D primitive
  - Blending, scaling and rotation are supported in one pass for Bitbilt
  - Source format:
    - ABGR8888, XBGR888, ARGB8888, XRGB888
    - RGB888, RGB565
    - RGBA5551, RGBA4444
    - YUV420 planar, YUV420 semi-planar
    - YUV422 planar, YUV422 semi-planar
    - BPP8, BPP4, BPP2, BPP1
  - Destination formats:
    - ABGR8888, XBGR888, ARGB8888, XRGB888
    - RGB888, RGB565
    - RGBA5551, RGBA4444
    - YUV420 planar, YUV420 semi-planar only in filter and pre-scale mode
    - YUV422 planar, YUV422 semi-planar only in filter and pre-scale mode

1.2.11 Video IN/OUT

- Camera Interface(interface only)
  - Support up to 5M pixels
  - 8bits BT656(PAL/NTSC) interface
  - 16bits BT601 DDR interface
  - 8bits/10bits/12bits raw data interface
  - YUV422 data input format with adjustable YUV sequence
  - YUV422,YUV420 output format with separately Y and UV space
  - Support picture in picture (PIP)
  - Support simple image effects such as Arbitrary(sepia), Negative, Art freeze, Embossing etc.
  - Support static histogram statistics and white balance statistics
  - Support image crop with arbitrary windows
  - Support scale up/down from 1/8 to 8 with arbitrary non-integer ratio

- Camera Interface and Image Processer(Interface and Image Processing)
  - Maximum input resolution of 8M(3264x2448) pixels
  - Main scaler with pixel-accurate up- and down-scaling to any resolution between 3264x2448 and 32x16 pixel in processing mode
  - Self scaler with pixel-accurate up- and down-scaling to any resolution between 1920x1080 and 32x16 pixel in processing mode
  - support of semiplanar NV21 color storage format
  - support of independent image cropping on main and self path
  - ITU-R BT 601/656 compliant video interface supporting YCbCr or RGB Bayer data
  - 12 bit camera interface
  - 12 bit resolution per color component internally
  - YCbCr 4:2:2 processing
  - quantization and Huffman tables
  - Windowing and frame synchronization
  - Macro block line, frame end, capture error, data loss interrupts and sync. (h_start, v_start) interrupts
  - Luminance/chrominance and chrominance blue/red swapping for YUV input signals
  - Continuous resize support
  - Color processing (contrast, saturation, brightness, hue, offset, range)
  - Display-ready RGB output in self-picture path (RGB888, RGB666 and RGB565)
  - Rotation unit in self-picture path (90°, 180°, 270° and h/v flipping) for RGB output
  - Read port provided to read back a picture from system memory
  - Simultaneous picture read back, resizing and storing through self path while main
  - path captures the camera picture
  - Black level compensation
  - Four channel Lens shade correction (Vignetting)
  - Auto focus measurement
  - White balancing and black level measurement
  - Auto exposure support by brightness measurement in 5x5 sub windows
  - Defect pixel cluster correction unit (DPCC) supports on the fly and table based pixel correction
  - De-noising pre filter (DPF)
  - Enhanced color interpolation (RGB Bayer demosaic)
  - Chromatic aberration correction
  - Combined edge sensitive Sharpening / Blurring filter (Noise filter)
  - Color correction matrix (cross talk matrix)
  - Global Tone Mapping with wide dynamic range unit (WDR)
  - Image Stabilization support and Video Stabilization Measurement
  - Flexible Histogram calculation
  - Digital image effects (Emboss, Sketch, Sepia, B/W (Grayscale), Color Selection, Negative image, sharpening)
  - Solarize effect through gamma correction

- Display Interface
  - Embedded one channel display interface.
  - Parallel Display interface
    - Parallel RGB LCD Interface:
      - 24-bit(RGB888),18-bit(RGB666), 15-bit(RGB565)
    - dither down:
      - allegro, FRC
      - gamma after dither
    - Max output resolution: 4096x2304
    - Scaning timing 8192x4096
  - IFDBC
    - decompress FB generated by GPU FBC
    - support 2048x1536 UI

- support ARGB888,RGB888,RGB565
- output for one layer among WIN0/1/2/3
- only support one IFDBC block which can used for WIN0/1/2/3 by configuration

- Display process
  - Background layer:
    - programmable 24-bit color
  - Win0 (Video0) layer:
    - RGB888, ARGB888, RGB565, YCbCr422, YCbCr420, YCbCr444
    - Support virtual display
    - 1/8 to 8 scaling-down and scaling-up engine:
      - Scale up using bicubic or bilinear;
      - Scale down using bilinear or average;
      - 4 Bicubic tables : precise, spline, catrom, mitchell;
      - coord 8bit, coe 8bit signed
    - x-mirror,y-mirror
  - Win1 (Video1) layer:
    - RGB888, ARGB888, RGB565, YCbCr422, YCbCr420, YCbCr444
    - Support virtual display
    - 1/8 to 8 scaling-down and scaling-up engine
      - Scale up using bicubic or bilinear;
      - Scale down using bilinear otraverage;
      - 4 Bicubic tables : precise,spline,catrom,mitchell;
      - coord 8bit, coe 8bit signed
    - x-mirror, y-mirror
  - Win2 (UI 0) layer:
    - RGB888, ARGB888, RGB565, 1/2/4/8bpp
    - Support virtual display
    - 4 display regions
    - x-mirror, y-mirror
  - Win3 (UI 1) layer:
    - RGB888, ARGB888, RGB565, 1/2/4/8bpp
    - Support virtual display
    - 4 display regions
    - x-mirror, y-mirror
  - Hardware cursor:
    - RGB888, ARGB888, RGB565, 1/2/4/8bpp
    - Support two size: 32x32,64x64,or 128x128
  - Overlay:
    - Win0/Win1/Win2/Win3 256 level alpha blending (support pre-multiplied alpha)
    - Win0/Win1/Win2/Win3 overlay position exchangeable
    - Win0/Win1/Win2/Win3 Transparency color key
    - Win0/Win1/Win2/Win3 global/per-pixel alpha
    - HWC 256 level alpha blending
    - HWC global/per-pixel alpha
- Others
  - 3 x 256 x 8 bits display LUTs
  - YcbCr2RGB(rec601-mpeg/rec601-jpeg/rec709/BT2020)and RGB2YcbCr
  - Support BCSH function
  - Support CABC function
  - QoS request signals
  - Gather transfer (Max 8)
  - Y/UV scheduler
  - Addr alignment
  - Support IEP direct path(win0/1/2/3)
  - Embedded memory management unit(MMU)
  - Support MIPI flow control

1.2.12 HDMI

- Single Physical Layer PHY with support for HDMI 1.4 and 2.0 operation
- For HDMI operation, support for the following:
  - Up to 1080p at 120 Hz and 4k x 2k at 60 Hz HDTV display resolutions and up to QXGA graphic display resolutions
  - 3-D video formats
  - Up to 10-bit Deep Color modes
  - Up to 18 Gbps aggregate bandwidth
  - 13.5–600 MHz input reference clock
  - HPD input analog comparator
- Link controller flexible interface with 30-, 60- or 120-bit SDR data access
- Support HDCP 1.4/HDCP2.2

1.2.13 MIPI_DSI/LVDS/TTL combo PHY

- MIPI_TX
  - Support 4 data lane, providing up to 4Gbps data rate
  - Support 1080p @ 60fps output
- LVDS
  - Comply with the TIA/EIA-644-A LVDS standard
  - Combine LVTTL IO, support LVDS/LVTTL data output
  - Support reference clock frequency range from 10Mhz to 148.5Mhz
  - Support LVDS RGB 24/18bits color data transfer
  - Support VESA/JEIDA LVDS data format transfer
- TTL
  - Combine LVTTL IO, support LVDS/LVTTL data output

1.2.14 MIPI_CSI PHY

- Embedded one MIPI_CSI PHY
- Support 4 data lane, providing up to 4Gbps data rate

1.2.15 eDP PHY

- Support 4Kx2K @ 30fps
- Compliant with eDP TM Specification, version 1.1
- Up to 4 physical lanes of 2.7/1.62 Gbps/lane(HBR2/HBR/RBR)
- RGB, YCbCr 4:4:4, YCbCr 4:2:2 and 8/10/12 bit per component video format
- Encoded bit stream (Dolby Digital) – IEC61937 compliant
- Support VESA DMT and CVT timing standards
- Fully support EIA/CEA-861D video timing and Info Frame structure
- Hot plug and unplug detection and link status monitor
- Support DDC/CI and MCCS command transmission when the monitor includes a display controller.

1.2.16 Audio Interface

- I2S/PCM with 8ch
  - Up to 8 channels (4xTX, 2xRX)
  - Audio resolution from 16bits to 32bits
  - Sample rate up to 192KHz
  - Provides master and slave work mode, software configurable
  - Support 3 I2S formats (normal, left-justified, right-justified)
  - Support 4 PCM formats(early, late1, late2, late3)
  - 8-channel I2S and PCM mode cannot be used at the same time, but 2 channel I2S And PCM mode can used at the same time

- SPDIF

- Support two 16-bit audio data store together in one 32-bit wide location
- Support biphase format stereo audio data output
- Support 16 to 31 bit audio data left or right justified in 32-bit wide sample data buffer
- Support 16, 20, 24 bits audio data transfer in linear PCM mode
- Support non-linear PCM transfer

1.2.17 Connectivity

- SDIO interface
  - Compatible with SDIO 3.0 protocol
  - 4bits data bus widths

- High-speed ADC stream interface
  - Support single-channel 8bits/10bits interface
  - DMA-based and interrupt-based operation
  - Support 8bits TS stream interface

- TS interface
  - Supports one TS input channels.
  - Supports 4 TS Input Mode: sync/valid mode in the case of serial TS input; no-sync/valid mode, sync/valid, sync/burst mode in the case of parallel TS input.
  - Supports 2 TS sources: demodulators and local memory.
  - Supports 2 Built-in PTIs(Programmable Transport Interface) to process TS simultaneously, and Each PTI supports:
    - 64 PID filters.
    - TS descrambling with 16 sets of Control Word under CSA v2.0 standard, up to 104Mbps
    - 16 PES/ES filters with PTS/DTS extraction and ES start code detection.
    - 4/8 PCR extraction channels
    - 64 Section filters with CRC check, and three interrupt mode: stop per unit, full-stop, recycle mode with version number check
    - PID done and error interrupts for each channel
    - PCR/DTS/PTS extraction interrupt for each channel
  - Supports 1 PVR(Personal Video Recording) output channel.
  - 1 built-in multi-channel DMA Controller.

- Smart Card
  - support card activation and deactivation
  - support cold/warm reset
  - support Answer to Reset (ATR) response reception
  - support T0 for asynchronous half-duplex character transmission
  - support T1 for asynchronous half-duplex block transmission
  - support automatic operating voltage class selection
  - support adjustable clock rate and bit (baud) rate
  - support configurable automatic byte repetition

- GMAC 10/100/1000M Ethernet Controller
  - Supports 10/100/1000-Mbps data transfer rates with the RGMII interfaces
  - Supports 10/100-Mbps data transfer rates with the RMII interfaces
  - Supports both full-duplex and half-duplex operation
  - Preamble and start-of-frame data (SFD) insertion in Transmit, and deletion in Receive paths
  - Automatic CRC and pad generation controllable on a per-frame basis
  - Options for Automatic Pad/CRC Stripping on receive frames
  - Programmable Inter Frame Gap (40-96 bit times in steps of 8)
  - Supports a variety of flexible address filtering modes
  - Separate 32-bit status returned for transmission and reception packets
  - Supports IEEE 802.1Q VLAN tag detection for reception frames

- Support detection of LAN wake-up frames and AMD Magic Packet frames
- Support checksum off-load for received IPv4 and TCP packets encapsulated by the Ethernet frame
- Support checking IPv4 header checksum and TCP, UDP, or ICMP checksum encapsulated in IPv4 or IPv6 data grams
- Comprehensive status reporting for normal operation and transfers with errors
- Automatic generation of PAUSE frame control or backpressure signal to the GMAC core based on Receive FIFO-fill (threshold configurable) level
- Handles automatic retransmission of Collision frames for transmission
- Discards frames on late collision, excessive collisions, excessive deferral and under run conditions

- SPI Controller
  - 3 on-chip SPI controller inside PX5
  - Support serial-master and serial-slave mode, software-configurable
  - DMA-based or interrupt-based operation
  - Embedded two 32x16bits FIFO for TX and RX operation respectively
  - Support 2 chip-selects output in serial-master mode

- Uart Controller
  - 5 on-chip uart controller inside PX5
  - DMA-based or interrupt-based operation
  - For all UART, two 64Bytes FIFOs are embedded for TX/RX operation respectively
  - Support 5bit,6bit,7bit,8bit serial data transmit or receive
  - Standard asynchronous communication bits such as start, stop and parity
  - Support different input clock for uart operation to get up to 4Mbps or other special baud rate
  - Support non-integer clock divides for baud clock generation
  - Auto flow control mode is for all UART, except UART_DBG

- I2C controller
  - 6 on-chip I2C controller in PX5
  - Multi-master I2C operation
  - Support 7bits and 10bits address mode
  - Software programmable clock frequency and transfer rate up to 400Kbit/s in the fast mode
  - Serial 8bits oriented and bidirectional data transfers can be made at up to 100Kbit/s in the standard mode

- GPIO
  - Totally 128 GPIOs
  - All of GPIOs can be used to generate interrupt to Cortex-A53
  - GPIO0 can be used to wakeup system from low-power mode
  - The pull direction(pull-up or pull-down) for all of GPIOs are software-programmable
  - All of GPIOs are always in input direction in default after power-on-reset
  - The drive strength for all of GPIOs is software-programmable

- USB Host2.0
  - Embedded 2 USB Host2.0 interfaces
  - Compatible with USB Host2.0 specification
  - Supports high-speed(480Mbps), full-speed(12Mbps) and low-speed (1.5Mbps) mode
  - Provides 16 host mode channels
  - Support periodic out channel in host mode

- USB OTG2.0
  - Compatible with USB OTG2.0 specification
  - Supports high-speed(480Mbps), full-speed(12Mbps) and low-speed (1.5Mbps) mode

- Support up to 9 device mode endpoints in addition to control endpoint 0
- Support up to 6 device mode IN endpoints including control endpoint 0
- Endpoints 1/3/5/7 can be used only as data IN endpoint
- Endpoints 2/4/6 can be used only as data OUT endpoint
- Endpoints 8/9 can be used as data OUT and IN endpoint
- Provides 9 host mode channels

1.2.18 Others

- Temperature Sensor(TS-ADC)
  - 2 bipolar-based temperature-sensing cell embedded
  - 1-channel 8-bits SAR ADC
  - Temperature accuracy sensed is ±5 degree

- SAR-ADC(Successive Approximation Register)
  - 3-channel single-ended 10-bit SAR analog-to-digital converter
  - Conversion speed range is up to 1 MSPS
  - SAR-ADC clock must be less than 1MHz

- eFuse
  - Two high-density electrical Fuse is integrated: 256bits (32x8) / 1024bits (32x32)
  - Support standby mode

*Notes :*① *DDR3/LPDDR2/LPDDR3 are not used simultaneously as well as async and sync ddr nand flash*
② *In PX5, Video decoder and encoder are not used simultaneously because of shared internal buffer*
③ *Actual maximum frame rate will depend on the clock frequency and system bus performance*
④ *Actual maximum data rate will depend on the clock frequency and JPEG compression rate*

1.3 Block Diagram

The following diagram shows the basic block diagram for PX5.

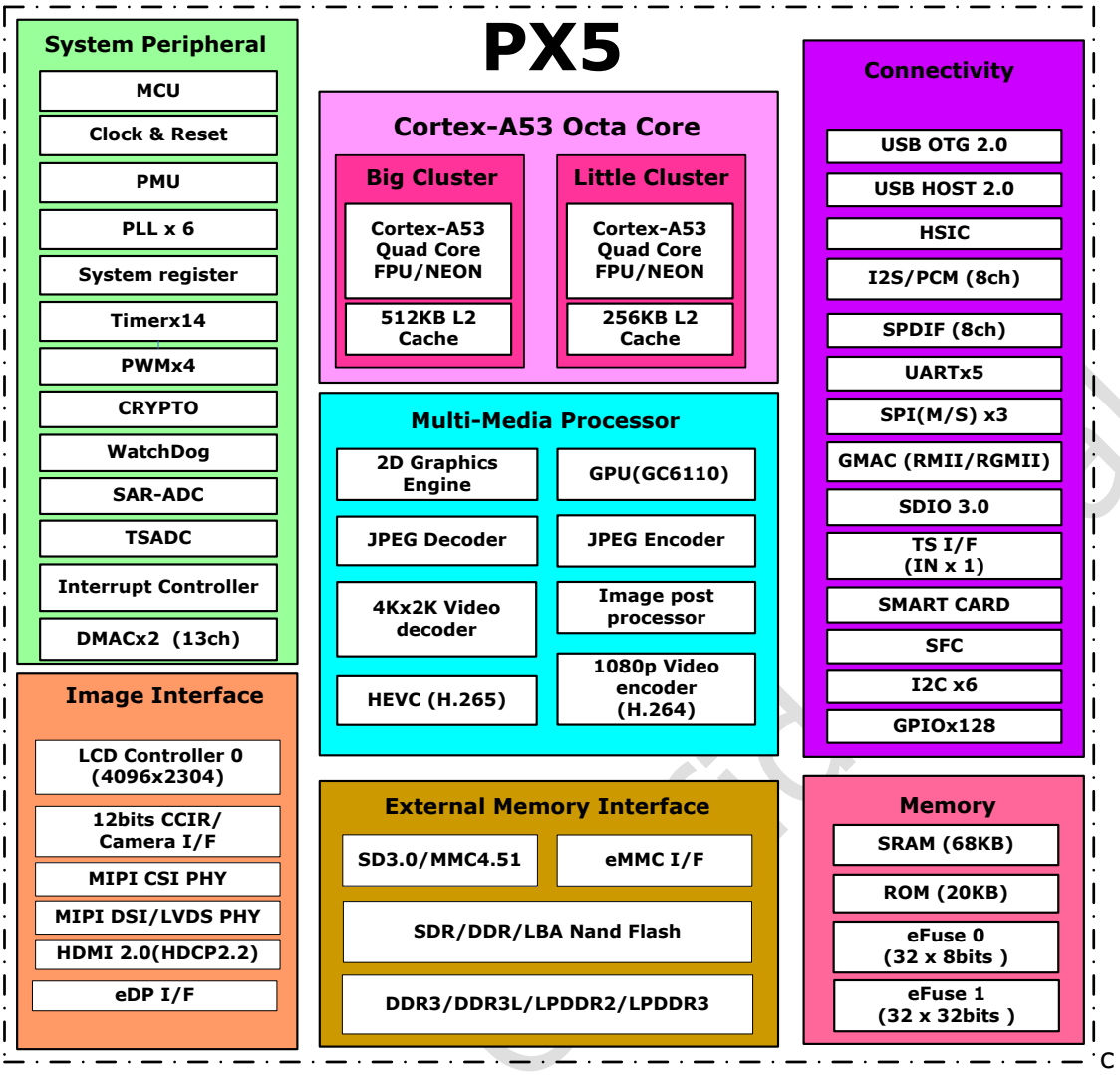


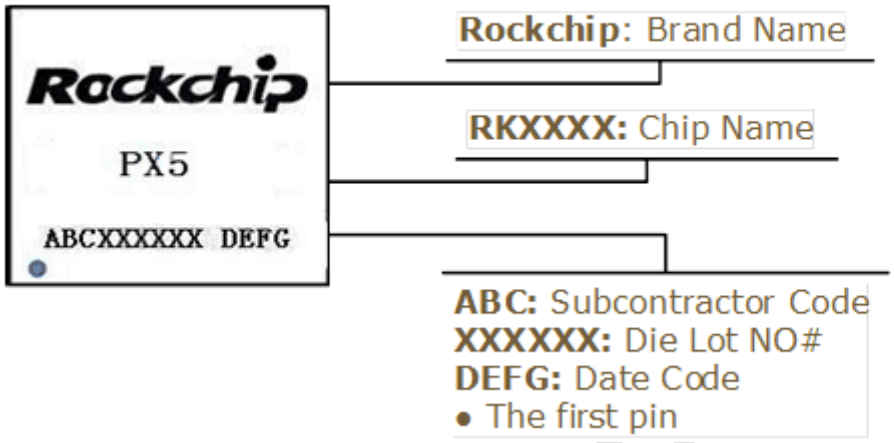
Fig. 1-1 PX5 Block Diagram

Chapter 2 Package information

2.1 Ordering information

Orderable Device	RoHS status	Package	Package Qty	Device special feature
PX5	Pb-Free	TFBGA453LD	700	Octa A53 Core AP

2.2 Top Marking



2.3 Dimension

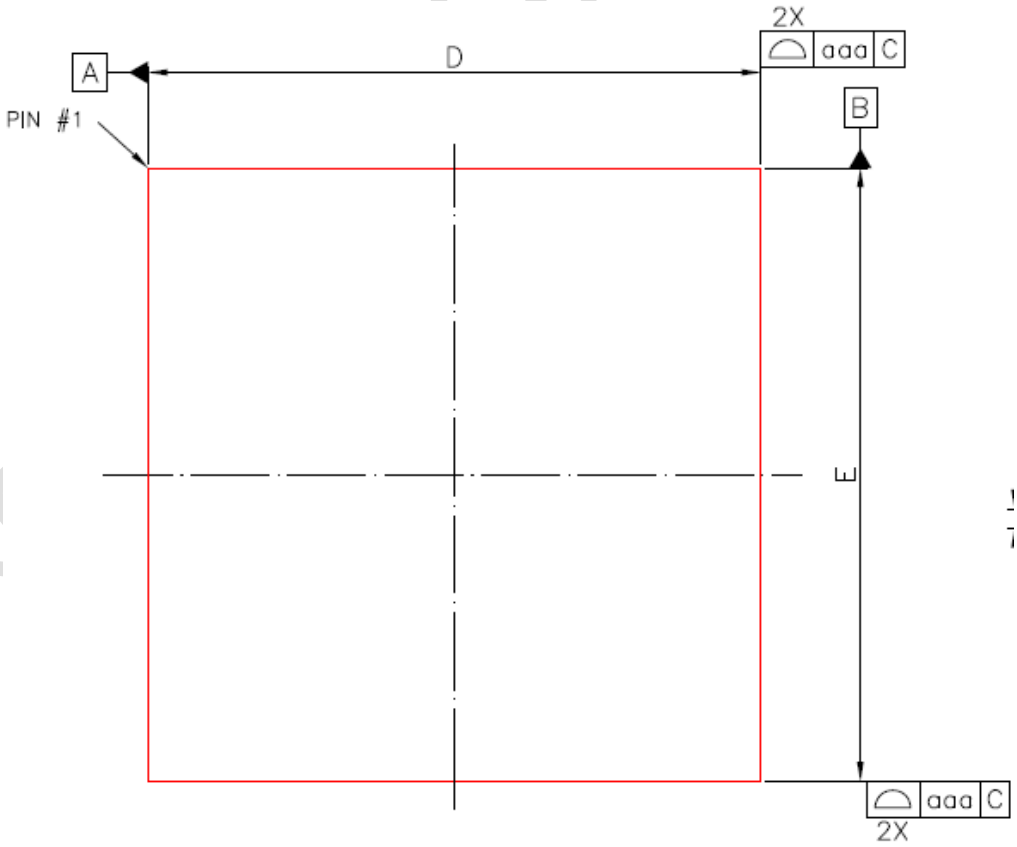


Fig. 2-1 PX5 TFBGA453 Package Top View

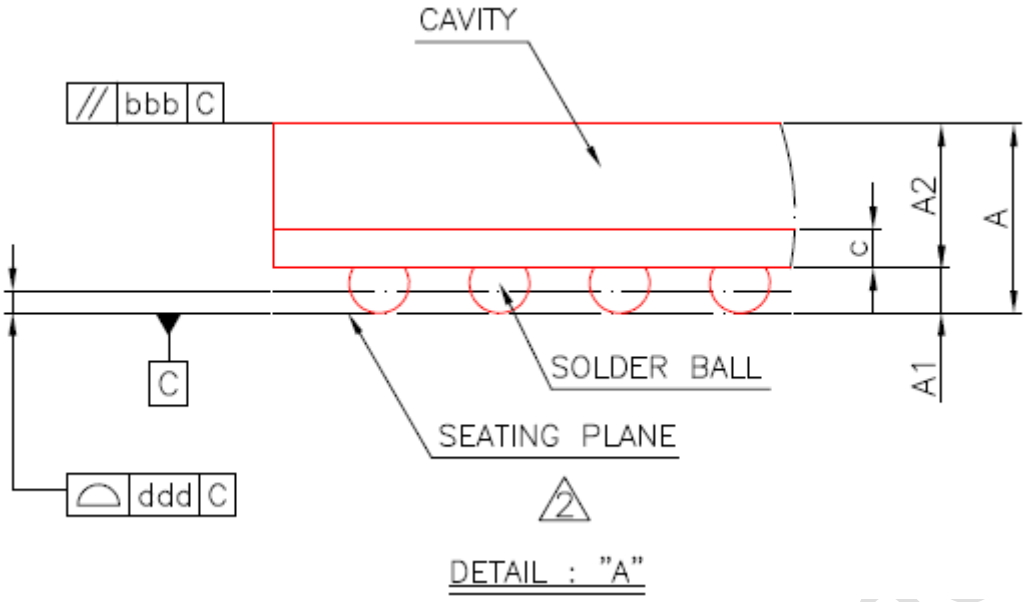


Fig. 2-2 PX5 TFBGA453 Package Side View

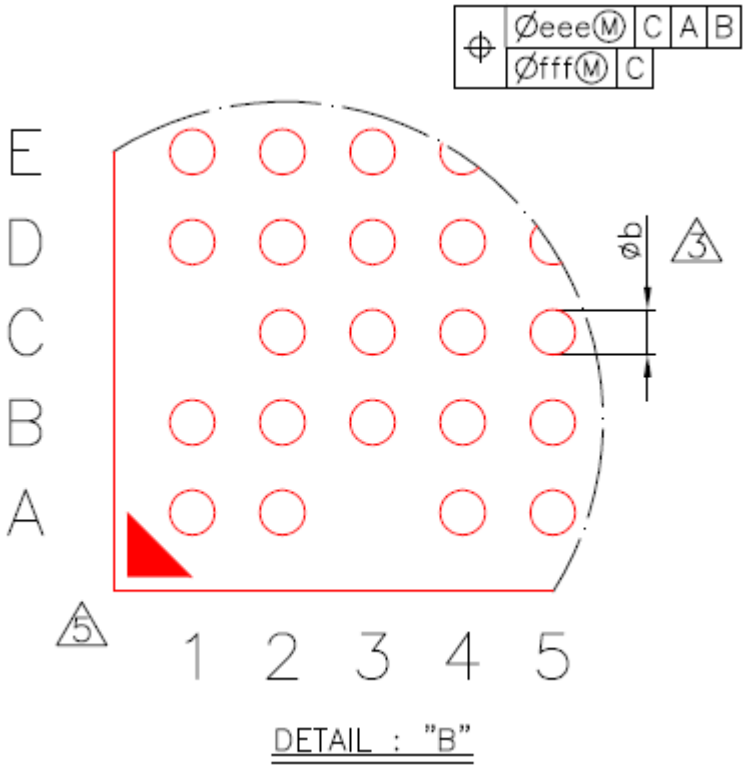


Fig. 2-3 PX5 TFBGA453 Package Bottom View

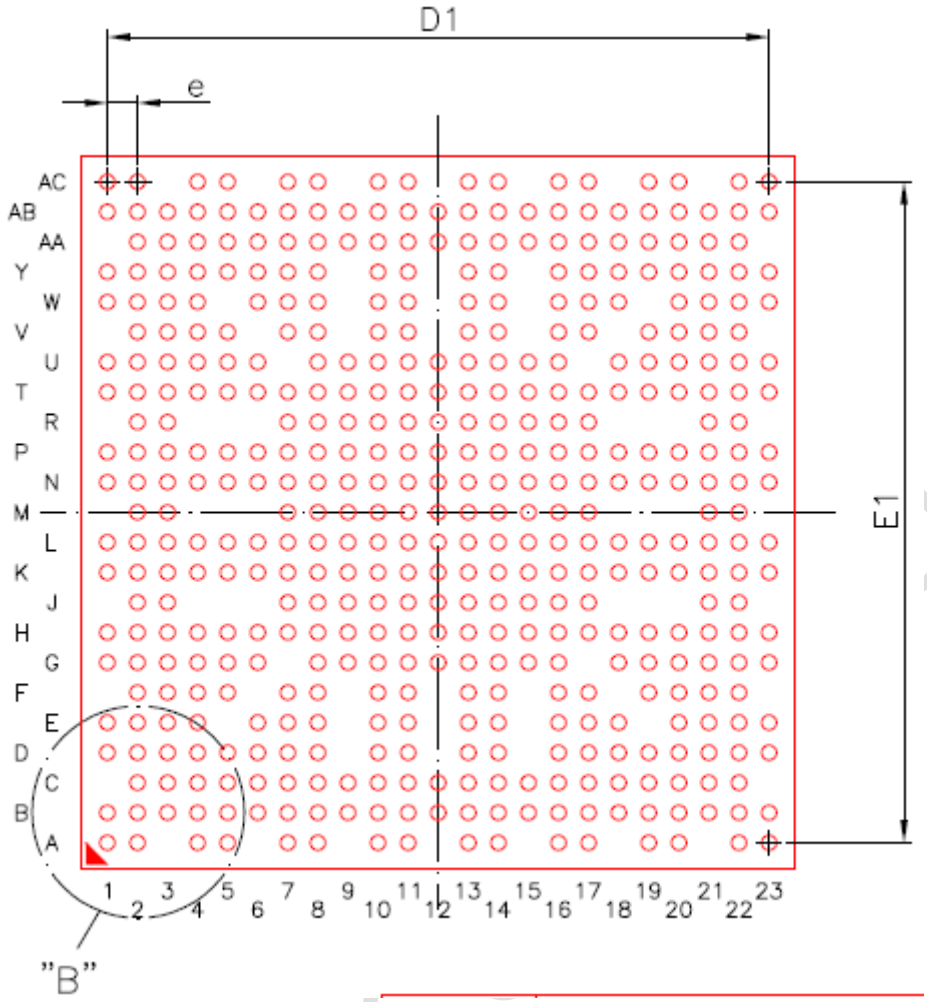


Fig. 2-4 PX5 TFBGA453 Package Bottom View

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.40	---	---	0.055
A1	0.25	0.30	0.35	0.010	0.012	0.014
A2	0.91	0.96	1.01	0.036	0.038	0.040
b	0.35	0.40	0.45	0.014	0.016	0.018
c	0.22	0.26	0.30	0.009	0.010	0.012
D	18.90	19.00	19.10	0.744	0.748	0.752
E	18.90	19.00	19.10	0.744	0.748	0.752
D1	---	17.60	---	---	0.693	---
E1	---	17.60	---	---	0.693	---
e	---	0.80	---	---	0.031	---
aaa	0.15			0.006		
bbb	0.20			0.008		
ddd	0.15			0.006		
eee	0.15			0.006		
fff	0.08			0.003		
MD/ME	23/23			23/23		

Fig. 2-5 PX5 TFBGA453 Package Dimension

2.4 Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12
A	GPIO0_C5/LCDC_D17/TRACE_D7/UART1_TX	GPIO0_C2/LCDC_D14/TRACE_D4/MCUJTAG_TDI	GPIO0_B7/LCDC_D11/TRACE_D1/JTAG_TDI	AVSS_1	HDMI_TX2N	HDMI_TX1N	HDMI_TX0N	HDMI_TCN	EDP_AUXP	EDP_TX3P	EDP_TX2P	EDP_TX1P
B	GPIO0_D1/LCDC_D21/TRACE_D11/UART4_RTSN	GPIO0_D2/LCDC_D22/TRACE_D12/UART4_TX	GPIO0_C6/LCDC_D18/TRACE_D8/UART1_CTSN	VSS_1	HDMI_TX2P	HDMI_TX1P	HDMI_TX0P	HDMI_TCP	EDP_AUXN	EDP_TX3N	EDP_TX2N	EDP_TX1N
C	GPIO0_D5/LCDC_VSYNC/TRACE_D15/PMU_DEBUG3	GPIO0_D4/LCDC_HSYNC/TRACE_D14/PMU_DEBUG2	NP	GPIO0_C7/LCDC_D19/TRACE_D9/UART1_RTSN	NP	AVSS_2	**LOGIC_VDD_9**	NP	AVSS_3	VSS_3	NP	AVSS_4
D	GPIO0_D6/LCDC_DEN/TRACE_CLK/PMU_DEBUG4	GPIO0_D7/LCDC_DCLK/TRACE_CTL/PMU_DEBUG5	GPIO0_D3/LCDC_D23/TRACE_D13/UART4_RX	NP	GPIO0_D0/LCDC_D20/TRACE_D10/UART4_CTSN	GPIO0_C4/LCDC_D16/TRACE_D6/UART1_RX	GPIO0_B6/LCDC_D10/TRACE_D0/JTAG_TRSTN	NP	LCDC_VDD_2	GPIO0_C3/LCDC_D15/TRACE_D5/MCUJTAG_TDO	NP	HDMI_HPD
E	NPOR	VSS_8	NP	EFUSE_VQPS	NP	PMU_VDD_1V0	PMUIO_VDD	NP	LCDC_VDD_1	GPIO0_C0/LCDC_D12/TRACE_D2/JTAG_TDO	NP	HDMI_RBIAS
F	OSC_24M_IN	OSC_24M_OUT	XVSS	C/DPLL_AVDD_1V0	G/NPLL_AVDD_1V0	G/NPLL_AVSS	ADC_AVDD_1V8	NP	HDMI_AVDD_1V0_1	HDMI_AVDD_1V0_2	NP	HDMI_AVDD_1V8
G	GPIO0_A4	CLK32K/PWM2	GPIO0_B0/TEST_CLKOUT/PWM_1/PMU_DEBUG1	APLL_AVDD_1V0	APLL_AVSS	C/DPLL_AVSS	**LOGIC_VDD_COM**	TEST	GPIO0_C1/LCDC_D13/TRACE_D3/MCUJTAG_TRSTN	AVSS_18	VSS_9	AVSS_10
H	GPIO0_A2	GPIO0_A7/I2C0_SCL	NP	NP	NP	NP	VSS_11	VSS_12	VSS_13	VSS_14	VSS_15	VSS_16
J	DDR_RETEN_OUT	GPIO0_A5	GPIO0_A6/I2C0_SDA	GPIO0_A3/OTP_OUT/PMU_DEBUG0	CPU_VDD_1	CPU_VDD_2	VSS_22	VSS_23	VSS_24	VSS_25	VSS_26	VSS_27
K	GPIO0_A1	GPIO0_A0/GLOBAL_PWROFF/PMIC_SLEEP	ADC_IN2	ADC_IN0	CPU_VDD_3	CPU_VDD_4	VSS_32	VSS_33	VSS_34	VSS_35	VSS_36	VSS_37
L	NC_1	ADC_IN1	NP	NP	NP	NP	VSS_43	VSS_44	VSS_45	VSS_46	VSS_47	VSS_48
M	NC_3	NC_2	CPU_VDD_15	CPU_VDD_16	CPU_VDD_5	CPU_VDD_6	VSS_53	VSS_54	VSS_55	VSS_56	VSS_57	VSS_58

13	14	15	16	17	18	19	20	21	22	23	24	
EDP_TX0P	MIPI_DSI_DN3/LCDC_D0/LVDS_DN3	MIPI_DSI_DN2/LCDC_D2/LVDS_DN2	MIPI_DSI_CLKN/LCDC_D5/LVDS_CLKN	MIPI_DSI_DN1/LCDC_D7/LVDS_DN1	MIPI_DSI_DN0/LCDC_D9/LVDS_DN0	AVSS_15	MIPI_CSI_DP3	MIPI_CSI_DP2	MIPI_CSI_CLKP	MIPI_CSI_DP1	MIPI_CSI_DP0	A
EDP_TX0N	MIPI_DSI_DP3/LCDC_D1/LVDS_DP3	MIPI_DSI_DP2/LCDC_D3/LVDS_DP2	MIPI_DSI_CLKP/LCDC_D4/LVDS_CLKP	MIPI_DSI_DP1/LCDC_D6/LVDS_DP1	MIPI_DSI_DP0/LCDC_D8/LVDS_DP0	AVSS_9	MIPI_CSI_DN3	MIPI_CSI_DN2	MIPI_CSI_CLKN	MIPI_CSI_DN1	MIPI_CSI_DN0	B
AVSS_5	NP	AVSS_6	AVSS_7	NP	AVSS_8	VSS_4	NP	AVSS_16	NP	AVSS_17	VSS_5	C
EDP_AVDD_1V0	NP	LVDS/MIPI_AVDD_1V8	MIPI_CSI_RBIAS	NP	GPIO1_A0/CIF_D2/TS_D0	GPIO1_A2/CIF_D4/TS_D2	GPIO1_A5/CIF_D7/TS_D5	NP	GPIO1_A4/CIF_D6/TS_D4	GPIO1_B0/CIF_VSYNC/TS_SYNC	GPIO1_A6/CIF_D8/TS_D6	D
EDP_RBIAS	NP	LVDS/MIPI_AVDD_1V0	MIPI_DSI_RBIAS	NP	GPIO1_A1/CIF_D3/TS_D1	GPIO1_A3/CIF_D5/TS_D3	NP	GPIO1_A7/CIF_D9/TS_D7	NP	GPIO1_B3/CIF_CLKOUT/TS_FAIL	DVPIO_VDD	E
EDP_AVDD_1V8	NP	EDP_CLKI_24M	LVDS/MIPI_AVDD_3V3	NP	MIPI_CSI_AVDD_1V0	NP	GPIO1_B1/CIF_HREF/TS_VALID	GPIO1_B4/CIF_D0	GPIO1_B5/CIF_D1	GPIO1_B6/CIF_D10/SPI1_CLK	GPIO1_C0/I2C3_SCL/SPI1_RXD	F
EDP_DC_TP	AVSS_11	AVSS_12	AVSS_13	AVSS_14	VSS_10	GPIO1_B2/CIF_CLKIN/TS_CLK	GPIO1_B7/CIF_D11/SPI1_CSN0	GPIO1_C1/I2C3_SDA/SPI1_TXD	DDR_DQ25	DDR_DM3	DDR_DQ24	G
VSS_17	VSS_18	VSS_19	VSS_20	VSS_21	DDR_VDD_1	NP	NP	NP	NP	DDR_DQS3N	DDR_DQS3	H
VSS_28	VSS_29	VSS_30	VSS_31	LOGIC_VDD_2	DDR_VDD_2	DDR_DQ26	DDR_DQ27	VSS_114	DDR_DQ28	DDR_DQ29	DDR_DQ30	J
VSS_38	VSS_39	VSS_40	VSS_41	VSS_42	DDR_VDD_3	DDR_DM1	DDR_DQ8	DDR_DQ9	DDR_DQ31	DDR_DQ10	DDR_DQ11	K
VSS_49	VSS_50	VSS_51	VSS_52	LOGIC_VDD_3	DDR_VDD_4	NP	NP	NP	NP	DDR_DQS1	DDR_DQS1N	L
VSS_59	VSS_60	VSS_61	VSS_62	VSS_7	DDRPLL_VDD_1V0	DDR_CKE1	DDR_RESETN	VSS_115	DDR_DQ15	DDR_DQ13	DDR_DQ12	M

N	GPIO2_A3/FLASH_CSN3/EMMC_RSTNOUT	NC_4	CPU_VDD_17	CPU_VDD_18	CPU_VDD_7	CPU_VDD_8	VSS_64	VSS_65	VSS_66	VSS_67	VSS_68
P	GPIO2_A2/FLASH_CSN2	GPIO2_A1/FLASH_CSN1	NP	NP	NP	NP	VSS_74	VSS_75	VSS_76	VSS_77	VSS_78
R	GPIO2_A4/FLASH_DQS/EMMC_CLKOUT	GPIO2_A0/FLASH_CSN0	CPU_VDD_19	CPU_VDD_20	CPU_VDD_9	CPU_VDD_10	CPU_VDD_COM	VSS_85	VSS_86	VSS_87	VSS_88
T	GPIO1_D2/FLASH_RDY/EMMC_CMD/SFC_CLK	GPIO1_D3/FLASH_WP/EMMC_PWREN	CPU_VDD_21	CPU_VDD_22	CPU_VDD_11	CPU_VDD_12	VSS_94	VSS_95	VSS_96	VSS_97	VSS_98
U	GPIO1_D5/FLASH_ALE/SPI0_CLK	GPIO1_D7/FLASH_WRN/SFC_CSN0	NP	NP	NP	NP	VSS_105	VSS_106	USB_AVSS_1	VSS_107	VSS_108
V	GPIO1_D6/FLASH_CLE	GPIO1_D4/FLASH_RDN/SFC_CSN1	GPIO1_C3/FLASH_D1/EMMC_D1/SFC_SIO1	GPIO1_C5/FLASH_D3/EMMC_D3/SFC_SIO3	CPU_VDD_13	CPU_VDD_14	FLASH_VDD	LOGIC_VDD_8	USB_AVDD_1V0	USB_AVDD_3V3	APIO1_VDD
W	GPIO1_C7/FLASH_D5/EMMC_D5/SPI0_TXD	GPIO1_C2/FLASH_D0/EMMC_D0/SFC_SIO0	GPIO1_C4/FLASH_D2/EMMC_D2/SFC_SIO2	GPIO1_C6/FLASH_D4/EMMC_D4/SPI0_RXD	USB0_ID	NP	GPIO3_D1/MAC_RXCLKIN/I2C4_SCL	NP	USB_AVDD_1V8	GPIO2_A5/SDMMC0_D0/UART2_TX	NP
Y	GPIO1_D1/FLASH_D7/EMMC_D7/SPI0_CSN1	GPIO1_D0/FLASH_D6/EMMC_D6/SPI0_CSN0	NP	USB_VBUS	NP	GPIO3_B5/MAC_TXEN	GPIO3_B1/MAC_TXD1	NP	GPIO3_B6/MAC_TXD3/GPS_MAG	GPIO3_D5/IR_RX/UART3_RX	NP
AA	VSS_63	USB_AVSS_3	GPIO3_B7/MAC_RXD0/GPS_SIG	NP	USIC_AVDD_1V2	GPIO3_B0/MAC_TXD0/PWM0/VOP_PWM	VSS_121	NP	GPIO3_B2/MAC_TXD2	VSS_120	NP
AB	USIC_STROBE	USIC_DATA	NP	VSS_2	NP	USB_RBIAS	GPIO3_C0/MAC_RXD1/UART3_CTSN/GPS_RFCLK	NP	GPIO3_C1/MAC_RXD2/UART3_RTSN/USB_DRVVBUS0	GPIO3_C5/MAC_RXER/ISP_PRELIGHTTRIG	NP
AC	USB0_DM	USB0_DP	USB_AVSS_2	GPIO3_D4/MAC_TX_CLKO/SPI1_CSN1	GPIO3_C6/MAC_CLK/ISP_SHUTTERTRIG	GPIO3_B3/MAC_CRS	GPIO3_C3/MAC_MDC/ISP_SHUTTEREN	GPIO3_D3/HDMI_I2C_SCL/I2C5_SCL	**GPIO3_D6/IR_TX/UART3_TX/PWM3/IR_REMOTE_IN**	GPIO2_A6/SDMMC0_D1/UART2_RX	GPIO2_B1/SDMMC0_CLKOUT/MCUJTAG_TCK
AD	USB1_DM	USB1_DP	VSS_6	GPIO3_C2/MAC_RXD3/USB_DRVVBUS1	GPIO3_C4/MAC_RXDV/ISP_FLASHTRIGOUT	GPIO3_B4/MAC_COL	GPIO3_C7/EDPHDMI_CEC/ISP_FLASHTRIGIN	GPIO3_D2/HDMI_I2C_SDA/I2C5_SDA	GPIO2_A7/SDMMC0_D2/JTAG_TCK	GPIO2_B0/SDMMC0_D3/JTAG_TMS	SDMMC_VDD
	1	2	3	4	5	6	7	8	9	10	11

VSS_69	VSS_70	VSS_71	VSS_72	VSS_73	LOGIC_VDD_1	DDR_VDD_5	DDR_A9	DDR_A7	DDR_WEN	DDR_CS0N	DDR_CKE0	DDR_DQ14	N
VSS_79	VSS_80	VSS_81	VSS_82	VSS_83	VSS_84	DDR_VDD_6	NP	NP	NP	NP	DDR_BA2	DDR_CS1N	P
VSS_89	VSS_90	VSS_91	VSS_92	VSS_93	LOGIC_VDD_4	DDR_VDD_7	DDR_A10	DDR_A12	VSS_116	DDR_A2	DDR_RASN	DDR_CASN	R
VSS_99	VSS_100	VSS_101	VSS_102	VSS_103	VSS_104	DDR_VDD_8	DDR_A15	DDR_ODT1	DDR_A4	DDR_A1	DDR_BA1	DDR_BA0	T
VSS_109	VSS_110	VSS_111	VSS_112	VSS_113	LOGIC_VDD_5	DDR_VDD_9	NP	NP	NP	NP	DDR_CLK	DDR_CLKN	U
LOGIC_VDD_7	GPIO3_A4/SDIO0_PWREN	APIO2_VDD	LOGIC_VDD_6	APIO3_VDD	APIO4_VDD	DDR_RETEN_IN	DDR_DQ4	DDR_DQ5	VSS_117	DDR_A6	DDR_A11	DDR_A0	V
GPIO2_D5/SDIO0_D1	GPIO3_A2/SDIO0_DETECTN	NP	GPIO2_B4/I2S_SCLK	GPIO2_D3/UART0_RTSN	NP	GPIO2_C1/I2S_SDO1/PCM_OUT	NP	DDR_DQ3	DDR_DM2	DDR_DQ19	DDR_A13	DDR_A3	W
GPIO2_B2/SDMMC0_CMD/MCUJTAG_TMS	GPIO3_A1/SDIO0_CLKOUT	NP	GPIO2_D2/UART0_CTSN	GPIO3_A7	NP	GPIO0_B1/SC_VCC33V/I2C2_SCL/GPUJTAG_TRSTN	GPIO0_B5/SC_DETECT/SPI2_CSN0/FLASH_VOL_SEL	NP	VSS_118	NP	DDR_A8	DDR_A5	Y
GPIO3_D0/MAC_MDIO/I2C4_SDA	GPIO2_D7/SDIO0_D3	NP	GPIO2_D0/UART0_RX	GPIO2_B7/I2S_SDI	NP	GPIO0_B2/SC_RST/SPI2_RXD/GPUJTAG_TMS	VSS_119	DDR_DQ2	NP	DDR_DQ23	DDR_ODT0	DDR_A14	AA
GPIO2_D6/SDIO0_D2	GPIO3_A0/SDIO0_CMD	NP	GPIO2_B5/I2S_LRCK_RX/PCM_SYNC	GPIO2_C3/I2S_SDO3/PCM_IN	NP	GPIO0_B3/SC_CLK/SPI2_TXD/GPUJTAG_TDI	GPIO3_D7/SC_VCC18V/I2C2_SDA/GPUJTAG_TCK	NP	DDR_DM0	NP	DDR_DQ17	DDR_DQ16	AB
GPIO2_B3/SDMMC0_DECTN	GPIO3_A3/SDIO0_WRPRT	GPIO3_A6/SDIO0_INTN	GPIO2_B6/I2S_LRCK_TX	GPIO2_C0/I2S_SDO0	GPIO2_C5/I2C1_SDA	GPIO0_B4/SC_IO/SPI2_CLK/GPUJTAG_TDO	DDR_DQ7	DDR_DQS0	DDR_DQ1	DDR_DQ22	DDR_DQS2	DDR_DQS2N	AC
GPIO2_D4/SDIO0_D0	GPIO3_A5/SDIO0_BKPWR	GPIO2_D1/UART0_TX	GPIO2_C2/I2S_SDO2/PCM_CLK	GPIO2_C4/I2S_CLK	GPIO2_C6/I2C1_SCL	GPIO2_C7/SPDIF_TX/EDP_HPD	DDR_DQ6	DDR_DQS0N	DDR_DQ0	DDR_DQ21	DDR_DQ20	DDR_DQ18	AD
12	13	14	15	16	17	18	19	20	21	22	23	24	

Fig. 2-6 PX5 Ball Mapping Diagram

2.5 Ball Pin Number Order

Table 2-1 PX5 Ball Pin Number Order Information

A1	GPIO1_C0/I2C3_SCL/SPI1_RXD	B1	GPIO1_B6/CIF_D10/SPI1_CLK
A2	DDR_DM3	B2	DDR_DQ24
A3	NP	B3	DDR_DQ25
A4	DDR_DQS3N	B4	DDR_DQS3
A5	DDR_DQ31	B5	DDR_DQ30
A6	NP	B6	DDR_DQ10
A7	DDR_DQS1N	B7	DDR_DQS1
A8	DDR_CS0N	B8	DDR_CKE1
A9	NP	B9	DDR_CS1N
A10	DDR_RASN	B10	DDR_CASN
A11	DDR_A0	B11	DDR_BA2
A12	NP	B12	DDR_A2
A13	DDR_CLKN	B13	DDR_CLK
A14	DDR_A5	B14	DDR_A6
A15	NP	B15	DDR_A11
A16	DDR_A15	B16	DDR_A14
A17	DDR_DQ18	B17	DDR_DQ17
A18	NP	B18	DDR_DQ21
A19	DDR_DQS2N	B19	DDR_DQS2
A20	DDR_DQ19	B20	DDR_DQ22
A21	NP	B21	DDR_DQ23
A22	DDR_DQS0N	B22	DDR_DQS0
A23	DDR_DQ4	B23	DDR_DQ5
C1	NP	D1	GPIO1_A6/CIF_D8/TS_D6
C2	VSS	D2	GPIO1_A7/CIF_D9/TS_D7
C3	DDR_DQ26	D3	GPIO1_B5/CIF_D1
C4	DDR_DQ27	D4	VSS
C5	DDR_DQ29	D5	DDR_DQ28
C6	DDR_DQ9	D6	DDR_DQ8
C7	DDR_DQ12	D7	VSS
C8	DDR_DQ15	D8	DDR_DQ14
C9	DDR_CKE0	D9	NP
C10	DDR_WEN	D10	VSS
C11	DDR_BA1	D11	DDR_BA0
C12	DDR_A1	D12	NP
C13	DDR_A4	D13	VSS
C14	DDR_A7	D14	DDR_A8
C15	DDR_A10	D15	NP
C16	DDR_A13	D16	VSS
C17	DDR_ODT1	D17	DDR_ODT0
C18	DDR_DQ16	D18	DDR_A12
C19	DDR_DQ20	D19	VSS
C20	DDR_DM2	D20	DDR_DM0

C21	VSS	D21	DDR_DQ1
C22	DDR_DQ2	D22	DDR_DQ3
C23	NP	D23	DDR_DQ6
E1	GPIO1_B0/CIF_VSYNC/TS_SYNC	F1	NP
E2	GPIO1_A4/CIF_D6/TS_D4	F2	VSS
E3	GPIO1_B4/CIF_D0	F3	GPIO1_A5/CIF_D7/TS_D5
E4	GPIO1_C1/I2C3_SDA/SPI1_TXD	F4	GPIO1_B1/CIF_HREF/TS_VALID
E5	NP	F5	GPIO1_B7/CIF_D11/SPI1_CSN0
E6	DDR_DM1	F6	NP
E7	DDR_DQ11	F7	DDR_VDD
E8	DDR_DQ13	F8	DDR_VDD
E9	NP	F9	NP
E10	DDR_RETEN_IN	F10	DDR_VDD
E11	DDR_RESETN	F11	DDR_VDD
E12	NP	F12	NP
E13	DDR_A3	F13	DDR_VDD
E14	DDR_A9	F14	DDR_VDD
E15	NP	F15	NP
E16	DDR_VDD	F16	DDR_VDD
E17	DDR_VDD	F17	DDR_VDD
E18	LOGIC_VDD	F18	NP
E19	NP	F19	GPIO2_C1/I2S_SDO1/PCM_OUT
E20	GPIO3_D7/SC_VCC18V/I2C2_SDA/GPUJTAG_TCK	F20	GPIO0_B1/SC_VCC33V/I2C2_SCL/GPUJTAG_TRSTN
E21	VSS	F21	GPIO0_B2/SC_RST/SPI2_RXD/GPUJTAG_TMS
E22	DDR_DQ0	F22	GPIO0_B5/SC_DETECT/SPI2_CSN0
E23	DDR_DQ7	F23	NP
G1	MIPI_CSI_DP0	H1	MIPI_CSI_DP1
G2	MIPI_CSI_DN0	H2	MIPI_CSI_DN1
G3	GPIO1_A2/CIF_D4/TS_D2	H3	AVSS
G4	GPIO1_A3/CIF_D5/TS_D3	H4	GPIO1_A0/CIF_D2/TS_D0
G5	GPIO1_B3/CIF_CLKOUT/TS_FAIL	H5	GPIO1_A1/CIF_D3/TS_D1
G6	GPIO1_B2/CIF_CLKIN/TS_CLK	H6	MIPI_CSI_RBIAS
G7	NP	H7	DVPIO_VDD
G8	LOGIC_VDD	H8	VSS
G9	VSS	H9	VSS
G10	LOGIC_VDD	H10	VSS
G11	VSS	H11	VSS
G12	LOGIC_VDD	H12	VSS
G13	DDRPLL_VDD_1V0	H13	VSS
G14	LOGIC_VDD	H14	VSS
G15	VSS	H15	VSS
G16	LOGIC_VDD	H16	VSS
G17	NP	H17	APIO3_VDD
G18	APIO4_VDD	H18	GPIO2_D3/UART0_RTSN

G19	GPIO2_C5/I2C1_SDA	H19	GPIO3_A7
G20	GPIO2_C6/I2C1_SCL	H20	GPIO2_B7/I2S_SDI
G21	GPIO0_B3/SC_CLK/SPI2_TXD/GPUJTAG_TDI	H21	GPIO2_C3/I2S_SDO3/PCM_IN
G22	GPIO0_B4/SC_IO/SPI2_CLK/GPUJTAG_TDO	H22	GPIO2_C0/I2S_SDO0
G23	GPIO2_C7/SPDIF_TX/EDP_HPD	H23	GPIO2_C4/I2S_CLK
J1	NP	K1	MIPI_CSI_DP2
J2	MIPI_CSI_CLKP	K2	MIPI_CSI_DN2
J3	MIPI_CSI_CLKN	K3	AVSS
J4	NP	K4	LVDS/MIPI_AVDD_1V8
J5	NP	K5	LVDS/MIPI_AVDD_1V0
J6	NP	K6	MIPI_DSI_RBIAS
J7	MIPI_CSI_AVDD_1V0	K7	LVDS/MIPI_AVDD_3V3
J8	VSS	K8	VSS
J9	VSS	K9	VSS
J10	VSS	K10	VSS
J11	VSS	K11	VSS
J12	VSS	K12	VSS
J13	VSS	K13	VSS
J14	VSS	K14	VSS
J15	VSS	K15	VSS
J16	VSS	K16	VSS
J17	LOGIC_VDD	K17	APIO2_VDD
J18	NP	K18	GPIO2_B4/I2S_SCLK
J19	NP	K19	GPIO2_D1/UART0_TX
J20	NP	K20	GPIO3_A6/SDIO0_INTN
J21	GPIO2_B6/I2S_LRCK_TX	K21	GPIO2_D2/UART0_CTSN
J22	GPIO2_C2/I2S_SDO2/PCM_CLK	K22	GPIO2_D0/UART0_RX
J23	NP	K23	GPIO2_B5/I2S_LRCK_RX/PCM_SYNC
L1	MIPI_CSI_DP3	M1	NP
L2	MIPI_CSI_DN3	M2	MIPI_DSI_DN0/LCDC_D9/LVDS_DN0
L3	AVSS	M3	MIPI_DSI_DP0/LCDC_D8/LVDS_DP0
L4	EDP_AVDD_1V0	M4	NP
L5	EDP_RBIAS	M5	NP
L6	EDP_AVDD_1V8	M6	NP
L7	EDP_CLKI_24M	M7	EDP_DC_TP
L8	VSS	M8	VSS
L9	VSS	M9	VSS
L10	VSS	M10	VSS
L11	VSS	M11	VSS
L12	VSS	M12	VSS
L13	VSS	M13	VSS
L14	VSS	M14	VSS
L15	VSS	M15	VSS
L16	VSS	M16	VSS
L17	GPIO3_A4/SDIO0_PWREN	M17	LOGIC_VDD

L18	GPIO3_A2/SDIO0_DETECTN	M18	NP
L19	GPIO3_A1/SDIO0_CLKOUT	M19	NP
L20	GPIO2_D7/SDIO0_D3	M20	NP
L21	GPIO3_A0/SDIO0_CMD	M21	GPIO2_B3/SDMMC0_DECTN
L22	GPIO3_A3/SDIO0_WRPRT	M22	GPIO2_D4/SDIO0_D0
L23	GPIO3_A5/SDIO0_BKPWR	M23	NP
N1	MIPI_DSI_DN1/LCDC_D7/LVDS_DN1	P1	MIPI_DSI_CLKN/LCDC_D5/LVDS_CLKN
N2	MIPI_DSI_DP1/LCDC_D6/LVDS_DP1	P2	MIPI_DSI_CLKP/LCDC_D4/LVDS_CLKP
N3	AVSS	P3	VSS
N4	HDMI_HPD	P4	GPIO0_C3/LCDC_D15/TRACE_D5/M3JTAG_TDO
N5	HDMI_RBIAS	P5	GPIO0_C0/LCDC_D12/TRACE_D2/JTAG_TDO
N6	HDMI_AVDD_1V8	P6	GPIO0_C1/LCDC_D13/TRACE_D3/M3JTAG_TRSTN
N7	HDMI_AVDD_1V0	P7	TEST
N8	VSS	P8	VSS
N9	VSS	P9	VSS
N10	VSS	P10	VSS
N11	VSS	P11	VSS
N12	VSS	P12	VSS
N13	VSS	P13	VSS
N14	VSS	P14	VSS
N15	VSS	P15	VSS
N16	VSS	P16	VSS
N17	APIO1_VDD	P17	USB_AVDD_3V3
N18	GPIO3_D0/MAC_MDIO/I2C4_SDA	P18	GPIO2_A5/SDMMC0_D0/UART2_TX
N19	GPIO2_B2/SDMMC0_CMD/M3JTAG_TMS	P19	GPIO3_D5/IR_RX/UART3_RX
N20	GPIO2_D5/SDIO0_D1	P20	VSS
N21	SDMMC_VDD	P21	GPIO3_C5/MAC_RXER/ISP_PRELIGHTTRIG
N22	GPIO2_B1/SDMMC0_CLKOUT/M3JTAG_TCK	P22	GPIO2_A6/SDMMC0_D1/UART2_RX
N23	GPIO2_D6/SDIO0_D2	P23	GPIO2_B0/SDMMC0_D3/JTAG_TMS
R1	NP	T1	MIPI_DSI_DN3/LCDC_D0/LVDS_DN3
R2	MIPI_DSI_DN2/LCDC_D2/LVDS_DN2	T2	MIPI_DSI_DP3/LCDC_D1/LVDS_DP3
R3	MIPI_DSI_DP2/LCDC_D3/LVDS_DP2	T3	AVSS
R4	NP	T4	LCDC_VDD
R5	NP	T5	LCDC_VDD
R6	NP	T6	PMUIO_VDD
R7	PMU_VDD_1V0	T7	ADC_AVDD_1V8
R8	VSS	T8	VSS
R9	VSS	T9	VSS
R10	VSS	T10	VSS
R11	VSS	T11	VSS
R12	VSS	T12	VSS
R13	VSS	T13	VSS
R14	VSS	T14	VSS
R15	VSS	T15	VSS

R16	VSS	T16	CPU_VDD
R17	USB_RBIAS	T17	LOGIC_VDD
R18	NP	T18	GPIO3_B0/MAC_TXD0/PWM0/VOP_PWM
R19	NP	T19	GPIO3_B6/MAC_TXD3/GPS_MAG
R20	NP	T20	GPIO3_B2/MAC_TXD2
R21	GPIO3_D6/IR_TX/UART3_TX/PWM_3	T21	GPIO3_C1/MAC_RXD2/UART3_RTSN/USB_DRVVBUS0
R22	GPIO2_A7/SDMMC0_D2/JTAG_TCK	T22	GPIO3_D2/HDMI_I2C_SDA/I2C5_SDA
R23	NP	T23	GPIO3_D3/HDMI_I2C_SCL/I2C5_SCL
U1	EDP_TX0P	V1	NP
U2	EDP_TX0N	V2	EDP_TX1P
U3	VSS	V3	EDP_TX1N
U4	GPIO0_B6/LCDC_D10/TRACE_D0/JTAG_TRSTN	V4	GPIO0_B7/LCDC_D11/TRACE_D1/JTAG_TDI
U5	GPIO0_C4/LCDC_D16/TRACE_D6/UART1_RX	V5	GPIO0_C6/LCDC_D18/TRACE_D8/UART1_CTSN
U6	GPIO0_D0/LCDC_D20/TRACE_D10/UART4_CTSN	V6	NP
U7	NP	V7	G/NPLL_AVSS
U8	APLL_AVSS	V8	C/DPLL_AVSS
U9	CPU_VDD	V9	NP
U10	CPU_VDD	V10	CPU_VDD
U11	CPU_VDD	V11	CPU_VDD
U12	CPU_VDD	V12	NP
U13	CPU_VDD	V13	CPU_VDD
U14	CPU_VDD	V14	CPU_VDD
U15	CPU_VDD	V15	NP
U16	CPU_VDD	V16	CPU_VDD
U17	NP	V17	FLASH_VDD
U18	GPIO3_D1/MAC_RXCLKIN/I2C4_SCL	V18	NP
U19	GPIO3_B1/MAC_TXD1	V19	GPIO3_B5/MAC_TXEN
U20	VSS	V20	USB_AVDD_1V8
U21	GPIO3_C0/MAC_RXD1/UART3_CTSN/GPS_RFCLK	V21	USB_AVDD_1V0
U22	GPIO3_C3/MAC_MDC/ISP_SHUTTEREN	V22	GPIO3_B3/MAC_CRS
U23	GPIO3_C7/EDPHDMI_CEC/ISP_FLASHTRIGIN	V23	NP
W1	EDP_TX2P	Y1	EDP_TX3P
W2	EDP_TX2N	Y2	EDP_TX3N
W3	AVSS	Y3	VSS
W4	GPIO0_C2/LCDC_D14/TRACE_D4/M3JTAG_TDI	Y4	GPIO0_C5/LCDC_D17/TRACE_D7/UART1_TX
W5	NP	Y5	GPIO0_D2/LCDC_D22/TRACE_D12/UART4_TX
W6	GPIO0_D4/LCDC_HSYNC/TRACE_D14/PMU_DEBUG2	Y6	GPIO0_C7/LCDC_D19/TRACE_D9/UART1_RTSN
W7	C/DPLL_AVDD_1V0	Y7	GPIO0_D3/LCDC_D23/TRACE_D13/UART4_RX
W8	G/NPLL_AVDD_1V0	Y8	APLL_AVDD_1V0
W9	NP	Y9	NP
W10	CPU_VDD	Y10	EFUSE_VQPS
W11	CPU_VDD	Y11	GPIO0_A7/I2C0_SCL

W12	NP	Y12	NP
W13	CPU_VDD	Y13	CPU_VDD
W14	CPU_VDD	Y14	CPU_VDD
W15	NP	Y15	NP
W16	CPU_VDD	Y16	GPIO2_A3/FLASH_CSN3/EMMC_RSTNOUT
W17	GPIO1_D5/FLASH_ALE/SPI0_CLK	Y17	GPIO1_D7/FLASH_WRN/SFC_CSN0
W18	GPIO1_C5/FLASH_D3/EMMC_D3/SFC_SIO3	Y18	GPIO1_C6/FLASH_D4/EMMC_D4/SPI0_RXD
W19	NP	Y19	GPIO1_D0/FLASH_D6/EMMC_D6/SPI0_CSN0
W20	GPIO3_D4/MAC_TX_CLKO/SPI1_CSN1	Y20	USB0_ID
W21	GPIO3_C6/MAC_CLK/ISP_SHUTTERTRIG	Y21	USIC_AVDD_1V2
W22	GPIO3_C4/MAC_RXDV/ISP_FLASHTRIGOUT	Y22	VSS
W23	GPIO3_B4/MAC_COL	Y23	GPIO3_C2/MAC_RXD3/USB_DRVVBUS1
AA1	NP	AB1	HDMI_TCP
AA2	EDP_AUXP	AB2	HDMI_TX0P
AA3	EDP_AUXN	AB3	AVSS
AA4	VSS	AB4	HDMI_TX1P
AA5	AVSS	AB5	HDMI_TX2P
AA6	GPIO0_D1/LCDC_D21/TRACE_D11/UART4_RTSN	AB6	VSS
AA7	GPIO0_D7/LCDC_DCLK/TRACE_CTL/PMU_DEBUG5	AB7	GPIO0_D6/LCDC_DEN/TRACE_CLK/PMU_DEBUG4
AA8	GPIO0_A4	AB8	GPIO0_A2
AA9	CLK32K/PWM2	AB9	VSS
AA10	VSS	AB10	OSC_24M_OUT
AA11	ADC_IN0	AB11	ADC_IN2
AA12	GPIO0_A1	AB12	DDR_RETEN_OUT
AA13	GPIO0_A6/I2C0_SDA	AB13	GPIO0_A5
AA14	GPIO2_A1/FLASH_CSN1	AB14	GPIO0_A3/OTP_OUT/PMU_DEBUG0
AA15	GPIO2_A4/FLASH_DQS/EMMC_CLKOUT	AB15	GPIO2_A2/FLASH_CSN2
AA16	GPIO2_A0/FLASH_CSN0	AB16	GPIO1_D3/FLASH_WP/EMMC_PWREN
AA17	GPIO1_C3/FLASH_D1/EMMC_D1/SFC_SIO1	AB17	GPIO1_D4/FLASH_RDN/SFC_CSN1
AA18	GPIO1_C4/FLASH_D2/EMMC_D2/SFC_SIO2	AB18	GPIO1_C2/FLASH_D0/EMMC_D0/SFC_SIO0
AA19	GPIO1_D1/FLASH_D7/EMMC_D7/SPI0_CSN1	AB19	GPIO3_B7/MAC_RXD0/GPS_SIG
AA20	USB_AVSS	AB20	USIC_DATA
AA21	USB_VBUS	AB21	USB_AVSS
AA22	USB_AVSS	AB22	USB0_DP
AA23	NP	AB23	USB1_DP
AC1	HDMI_TCN		
AC2	HDMI_TX0N		
AC3	NP		
AC4	NP		
AC5	HDMI_TX2N		
AC6	NP		
AC7	GPIO0_D5/LCDC_VSYNC/TRACE_D15/PMU_DEBUG3		
AC8	NPOR		

AC9	NP		
AC10	OSC_24M_IN		
AC11	ADC_IN1		
AC12	NP		
AC13	GPIO0_B0/TEST_CLKOUT/PWM_1/PMU_DEBUG 1		
AC14	GPIO0_A0/GLOBAL_PWROFF/PMIC_SLEEP		
AC15	NP		
AC16	GPIO1_D2/FLASH_RDY/EMMC_CMD/SFC_CLK		
AC17	GPIO1_D6/FLASH_CLE		
AC18	NP		
AC19	GPIO1_C7/FLASH_D5/EMMC_D5/SPI0_TXD		
AC20	USIC_STROBE		
AC21	NP		
AC22	USB0_DM		
AC23	USB1_DM		

2.6 Power/ground IO descriptions

Table 2-2 PX5 Power/Ground IO information

Group	Ball #	Descriptions
VSS	AA10 AA4 AB6 AB9 C2 C21 D10 D13 D16 D19 D4 D7 E21 F2 G11 G15 G9 H10 H11 H12 H13 H14 H15 H16 H8 H9 J10 J11 J12 J13 J14 J15 J16 J8 J9 K10 K11 K12 K13 K14 K15 K16 K8 K9 L10 L11 L12 L13 L14 L15 L16 L8 L9 M10 M11 M12 M13 M14 M15 M16 M8 M9 N10 N11 N12 N13 N14 N15 N16 N8 N9 P10 P11 P12 P13 P14 P15 P16 P20 P3 P8 P9 R10 R11 R12 R13 R14 R15 R16 R8 R9 T10 T11 T12 T13 T14 T15 T8 T9 U20 U3 Y22 Y3	Internal Logic Ground and Digital IO Ground
CPU_VDD	T16 U10 U11 U12 U13 U14 U15 U16 U9 V10 V11 V13 V14 V16 W10 W11 W13 W14 W16 Y13 Y14	Internal CPU Power (@ cpu frequency <= 900MHz)
		Internal CPU Power (@ cpu frequency <= 1.5GHz)
LOGIC_VDD	E18 G10 G12 G14 G16 G8 J17 M17 T17	Internal Logic Power
DDR_VDD	E16 E17 F10 F11 F13 F14 F16 F17 F7 F8	DDR3 Digital IO Power LPDDR2 Digital IO Power
DDRPLL_VDD_1V0	G13	DDR PHY PLL power
PMU_VDD_1V0	R7	Internal PMU Domain Logic Power
PMUIO_VDD	T6	PMU Domain Digital IO Power
APIO1_VDD	N17	GPIO30 Digital IO Power
APIO2_VDD	K17	GPIO1830 Digital IO Power
LCDC_VDD	T4 T5	LCDC Digital IO Power
DVPIO_VDD	H7	DVP Digital IO Power
FLASH_VDD	V17	Nand Flash0 Digital IO Power
SDMMC_VDD	N21	SDMMC0 Digital IO Power

Group	Ball #	Descriptions
APIO3_VDD	H17	WIFI Digital IO Power
APIO4_VDD	G18	AUDIO Digital IO Power
AVSS	AA5 AB3 H3 K3 L3 N3 T3 W3	Analog Ground
APLL_AVDD_1V0	Y8	PLL Analog Power
APLL_AVSS	U8	PLL Analog Ground
C/DPLL_AVDD_1V0	W7	PLL Analog Power
C/DPLL_AVSS	V8	PLL Analog Ground
G/NPLL_AVDD_1V0	W8	PLL Analog Power
G/NPLL_AVSS	V7	PLL Analog Ground
ADC_AVDD_1V8	T7	SAR-ADC/TSADC Analog Power
USB_AVDD_1V0	V21	USB OTG2.0/Host2.0 Digital Power
USB_AVDD_1V8	V20	USB OTG2.0/Host2.0 Analog Power
USB_AVDD_3V3	P17	USB OTG2.0/Host2.0 Analog Power
USB_AVSS	AA20 AA22 AB21	USB Analog Ground
EFUSE_VDDQ	Y10	eFuse IO Digital Power
USIC_VDD_1V2	Y21	USIC 1.2V Transmitter Power Supply
EDP_AVDD_1V0	L4	eDP 1.0V Power Supply
EDP_AVDD_1V8	L6	eDP 1.8V Power Supply
HDMI_AVDD_1V0	N7	HDMI 1.0V Power Supply
HDMI_AVDD_1V8	N6	HDMI 1.8V Power Supply
LVDS/MIPI_AVDD_1V0	K5	LVDS 1.0V Power Supply
LVDS/MIPI_AVDD_1V8	K4	LVDS 1.8V Power Supply
LVDS/MIPI_AVDD_3V3	K7	LVDS 3.3V Power Supply
MIPI_CSI_AVDD_1V0	J7	MIPI RX PHY 1.8V Power Supply

2.7 Function IO description

Pad#	Ball#	Func0	Func1	Func2	Func3	Pad type①	Current ②	Pull ⑤	Reset State③	Power Supply④
OSC_24M_IN	AC10	clk24m_xin				I	2mA	NA	I	
OSC_24M_OUT	AB10	clk24m_xout				O	2mA	NA	O	
NPOR	AC8	npor				I	2mA	up	I	
TEST	P7	test				I	2mA	down	I	
DDR_RETEN_OUT	AB12	ddr_reten				O	2mA	up	O	
CLK32_PWM2	AA9	pwm_2	clk_32K			I/O	2mA	up	I	
GLOBALpwroff_PMICsleep_PMUgpio0a0	AC14	pmu_gpio0a0	global_pwroff	pmic_sleep		I/O	2mA	down	I	
PMUgpio0a1	AA12	pmu_gpio0a1				I/O	2mA	up	I	PMU
PMUgpio0a2	AB8	pmu_gpio0a2				I/O	2mA	up	I	
TSADCint_PMUdebug0_PMUgpio0a3	AB14	pmu_gpio0a3	tsadc_int	pmu_debug0		I/O	2mA	down	I	
PMUgpio0a4	AA8	pmu_gpio0a4				I/O	2mA	down	I	
PMUgpio0a5	AB13	pmu_gpio0a5				I/O	2mA	down	I	
I2C0PMUsda_PMUgpio0a6	AA13	pmu_gpio0a6	i2c0pmu_sda			I/O	2mA	up	I	
I2C0PMUscl_PMUgpio0a7	Y11	pmu_gpio0a7	i2c0pmu_scl			I/O	2mA	up	I	
TESTclkout_PWM1_PMUdebug1_PMUgpio0b0	AC13	pmu_gpio0b0	test_clkout	pwm_1	pmu_debug1	I/O	2mA	down	I	
LCDCdata10_TRACEdata0_JTAGtrstn_LCDCgpio0b6	U4	lcdc_gpio0b6	lcdc_data10	trace_data0	jtag_trstn	I/O	8mA	down	I	
LCDCdata11_TRACEdata1_JTAGtdi_LCDCgpio0b7	V4	lcdc_gpio0b7	lcdc_data11	trace_data1	jtag_tdi	I/O	8mA	down	I	
LCDCdata12_TRACEdata2_JTAGtdo_LCDCgpio0c0	P5	lcdc_gpio0c0	lcdc_data12	trace_data2	jtag_tdo	I/O	8mA	down	I	
LCDCdata13_TRACEdata3_MCUJTAGtrstn_LCDCgpio0c1	P6	lcdc_gpio0c1	lcdc_data13	trace_data3	mcujtag_trstn	I/O	8mA	down	I	
LCDCdata14_TRACEdata4_MCUJTAGtdi_LCDCgpio0c2	W4	lcdc_gpio0c2	lcdc_data14	trace_data4	mcujtag_tdi	I/O	8mA	down	I	
LCDCdata15_TRACEdata5_MCUJTAGtdo_LCDCgpio0c3	P4	lcdc_gpio0c3	lcdc_data15	trace_data5	mcujtag_tdo	I/O	8mA	up	I	
LCDCdata16_TRACEdata6_UART1BBsin_LCDCgpio0c4	U5	lcdc_gpio0c4	lcdc_data16	trace_data6	uart1bb_sin	I/O	8mA	down	I	
LCDCdata17_TRACEdata7_UART1BBsout_LCDCgpio0c5	Y4	lcdc_gpio0c5	lcdc_data17	trace_data7	uart1bb_sout	I/O	8mA	down	I	
LCDCdata18_TRACEdata8_UART1BBctsn_LCDCgpio0c6	V5	lcdc_gpio0c6	lcdc_data18	trace_data8	uart1bb_ctsn	I/O	8mA	down	I	
LCDCdata19_TRACEdata9_UART1BBrtsn_LCDCgpio0c7	Y6	lcdc_gpio0c7	lcdc_data19	trace_data9	uart1bb_rtsn	I/O	8mA	down	I	LCDC
LCDCdata20_TRACEdata10_UART4EXPctsn_LCDCgpio0d0	U6	lcdc_gpio0d0	lcdc_data20	trace_data10	uart4exp_ctsn	I/O	8mA	down	I	
LCDCdata21_TRACEdata11_UART4EXPrtsn_LCDCgpio0d1	AA6	lcdc_gpio0d1	lcdc_data21	trace_data11	uart4exp_rtsn	I/O	8mA	down	I	
LCDCdata22_TRACEdata12_UART4EXPsout_LCDCgpio0d2	Y5	lcdc_gpio0d2	lcdc_data22	trace_data12	uart4exp_sout	I/O	8mA	down	I	
LCDCdata23_TRACEdata13_UART4EXPsin_LCDCgpio0d3	Y7	lcdc_gpio0d3	lcdc_data23	trace_data13	uart4exp_sin	I/O	8mA	down	I	
LCDChsync_TRACEdata14_PMUdebug2_LCDCgpio0d4	W6	lcdc_gpio0d4	lcdc_hsync	trace_data14	pmu_debug2	I/O	8mA	down	I	
LCDCvsync_TRACEdata15_PMUdebug3_LCDCgpio0d5	AC7	lcdc_gpio0d5	lcdc_vsync	trace_data15	pmu_debug3	I/O	8mA	down	I	
LCDCden_TRACEclk_PMUdebug4_LCDCgpio0d6	AB7	lcdc_gpio0d6	lcdc_den	trace_clk	pmu_debug4	I/O	8mA	down	I	
LCDCdclk_TRACEctl_PMUdebug5_LCDCgpio0d7	AA7	lcdc_gpio0d7	lcdc_dclk	trace_ctl	pmu_debug5	I/O	12mA	down	I	
CIFdata2_TSdata0_DVPgpio1a0	H4	dvp_gpio1a0	cif_data2	ts_data0		I/O	2mA	down	I	
CIFdata3_TSdata1_DVPgpio1a1	H5	dvp_gpio1a1	cif_data3	ts_data1		I/O	2mA	down	I	
CIFdata4_TSdata2_DVPgpio1a2	G3	dvp_gpio1a2	cif_data4	ts_data2		I/O	2mA	down	I	
CIFdata5_TSdata3_DVPgpio1a3	G4	dvp_gpio1a3	cif_data5	ts_data3		I/O	2mA	down	I	
CIFdata6_TSdata4_DVPgpio1a4	E2	dvp_gpio1a4	cif_data6	ts_data4		I/O	2mA	down	I	DVP
CIFdata7_TSdata5_DVPgpio1a5	F3	dvp_gpio1a5	cif_data7	ts_data5		I/O	2mA	down	I	
CIFdata8_TSdata6_DVPgpio1a6	D1	dvp_gpio1a6	cif_data8	ts_data6		I/O	2mA	down	I	
CIFdata9_TSdata7_DVPgpio1a7	D2	dvp_gpio1a7	cif_data9	ts_data7		I/O	2mA	down	I	
CIFvsync_TSsync_DVPgpio1b0	E1	dvp_gpio1b0	cif_vsync	ts_sync		I/O	2mA	down	I	

Pad#	Ball#	Func0	Func1	Func2	Func3	Pad type[1]	Current [2]	Pull [5]	Reset State[3]	Power Supply[4]
CIFhref_TSvalid_DVPgpio1b1	F4	dvp_gpio1b1	cif_href	ts_valid		I/O	2mA	down	I	
CIFclkin_TSclk_DVPgpio1b2	G6	dvp_gpio1b2	cif_clkin	ts_clk		I/O	2mA	down	I	
CIFclkout_TSfail_DVPgpio1b3	G5	dvp_gpio1b3	cif_clkout	ts_fail		I/O	8mA	down	I	
CIFdata0_DVPgpio1b4	E3	dvp_gpio1b4	cif_data0			I/O	2mA	down	I	
CIFdata1_DVPgpio1b5	D3	dvp_gpio1b5	cif_data1			I/O	2mA	down	I	
CIFdata10_SPI1clk_DVPgpio1b6	B1	dvp_gpio1b6	cif_data10	spi1_clk		I/O	2mA	down	I	
CIFdata11_SPI1csn0_DVPgpio1b7	F5	dvp_gpio1b7	cif_data11	spi1_csn0		I/O	2mA	down	I	
I2C3CAMscl_SPI1rxd_DVPgpio1c0	A1	dvp_gpio1c0	i2c3cam_scl	spi1_rxd		I/O	2mA	up	I	
I2C3CAMsda_SPI1txd_DVPgpio1c1	E4	dvp_gpio1c1	i2c3cam_sda	spi1_txd		I/O	2mA	up	I	
FLASHdata0_EMMCdata0_SFCsio0_FLASHgpio1c2	AB18	flash_gpio1c2	flash_data0	emmc_data0	sfc_sio0	I/O	8mA	up	I	
FLASHdata1_EMMCdata1_SFCsio1_FLASHgpio1c3	AA17	flash_gpio1c3	flash_data1	emmc_data1	sfc_sio1	I/O	8mA	up	I	
FLASHdata2_EMMCdata2_SFCsio2_FLASHgpio1c4	AA18	flash_gpio1c4	flash_data2	emmc_data2	sfc_sio2	I/O	8mA	up	I	
FLASHdata3_EMMCdata3_SFCsio3_FLASHgpio1c5	W18	flash_gpio1c5	flash_data3	emmc_data3	sfc_sio3	I/O	8mA	up	I	
FLASHdata4_EMMCdata4_SPI0rxd_FLASHgpio1c6	Y18	flash_gpio1c6	flash_data4	emmc_data4	spi0_rxd	I/O	8mA	up	I	
FLASHdata5_EMMCdata5_SPI0txd_FLASHgpio1c7	AC19	flash_gpio1c7	flash_data5	emmc_data5	spi0_txd	I/O	8mA	up	I	
FLASHdata6_EMMCdata6_SPI0csn0_FLASHgpio1d0	Y19	flash_gpio1d0	flash_data6	emmc_data6	spi0_csn0	I/O	8mA	up	I	
FLASHdata7_EMMCdata7_SPI0csn1_FLASHgpio1d1	AA19	flash_gpio1d1	flash_data7	emmc_data7	spi0_csn1	I/O	8mA	up	I	
FLASHrdy_EMMCcmd_SFCclk_FLASHgpio1d2	AC16	flash_gpio1d2	flash_rdy	emmc_cmd	sfc_clk	I/O	4mA	up	I	
FLASHwp_EMMCpwren_FLASHgpio1d3	AB16	flash_gpio1d3	flash_wp	emmc_pwren		I/O	4mA	down	I	FLASH
FLASHrdn_SFCcsn1_FLASHgpio1d4	AB17	flash_gpio1d4	flash_rdn	sfc_csn1		I/O	4mA	up	I	
FLASHale_SPI0clk_FLASHgpio1d5	W17	flash_gpio1d5	flash_ale	spi0_clk		I/O	4mA	down	I	
FLASHcle_FLASHgpio1d6	AC17	flash_gpio1d6	flash_cle			I/O	4mA	down	I	
FLASHwrn_SFCcsn0_FLASHgpio1d7	Y17	flash_gpio1d7	flash_wrn	sfc_csn0		I/O	8mA	up	I	
FLASHcsn0_FLASHgpio2a0	AA16	flash_gpio2a0	flash_csn0			I/O	4mA	up	I	
FLASHcsn1_FLASHgpio2a1	AA14	flash_gpio2a1	flash_csn1			I/O	4mA	up	I	
FLASHcsn2_FLASHgpio2a2	AB15	flash_gpio2a2	flash_csn2			I/O	4mA	up	I	
FLASHcsn3_EMMCrstnout_FLASHgpio2a3	Y16	flash_gpio2a3	flash_csn3	emmc_rstnout		I/O	4mA	up	I	
FLASHdqs_EMMCclkout_FLASHgpio2a4	AA15	flash_gpio2a4	flash_dqs	emmc_clkout		I/O	8mA	up	I	
SDMMC0data0_UART2DBGsout_SDCARDgpio2a5	P18	sdcard_gpio2a5	sdmmc0_data0	uart2dbg_sout		I/O	4mA	up	I	
SDMMC0data1_UART2DBGsin_SDCARDgpio2a6	P22	sdcard_gpio2a6	sdmmc0_data1	uart2dbg_sin		I/O	4mA	up	I	
SDMMC0data2_JTAGtck_SDCARDgpio2a7	R22	sdcard_gpio2a7	sdmmc0_data2	jtag_tck		I/O	4mA	up	I	
SDMMC0data3_JTAGtms_SDCARDgpio2b0	P23	sdcard_gpio2b0	sdmmc0_data3	jtag_tms		I/O	4mA	up	I	SDMMC
SDMMC0clkout_MCUJTAGtck_SDCARDgpio2b1	N22	sdcard_gpio2b1	sdmmc0_clkout	mcujtag_tck		I/O	8mA	down	I	
SDMMC0cmd_MCUJTAGtms_SDCARDgpio2b2	N19	sdcard_gpio2b2	sdmmc0_cmd	mcujtag_tms		I/O	4mA	up	I	
SDMMC0dectn_SDCARDgpio2b3	M21	sdcard_gpio2b3	sdmmc0_dectn			I/O	2mA	up	I	
I2Ssclk_AUDIOgpio2b4	K18	audio_gpio2b4	i2s_sclk			I/O	4mA	down	I	
I2Slrckrx_PCMsync_AUDIOgpio2b5	K23	audio_gpio2b5	i2s_lrckrx	pcm_sync		I/O	2mA	down	I	
I2Slrcktx_AUDIOgpio2b6	J21	audio_gpio2b6	i2s_lrcktx			I/O	2mA	down	I	
I2Ssdi_AUDIOgpio2b7	H20	audio_gpio2b7	i2s_sdi			I/O	2mA	down	I	
I2Ssdo0_AUDIOgpio2c0	H22	audio_gpio2c0	i2s_sdo0			I/O	2mA	down	I	
I2Ssdo1_PCMout_AUDIOgpio2c1	F19	audio_gpio2c1	i2s_sdo1	pcm_out		I/O	2mA	down	I	AUDIO (APIO3)
I2Ssdo2_PCMclk_AUDIOgpio2c2	J22	audio_gpio2c2	i2s_sdo2	pcm_clk		I/O	2mA	down	I	
I2Ssdo3_PCMin_AUDIOgpio2c3	H21	audio_gpio2c3	i2s_sdo3	pcm_in		I/O	2mA	down	I	
I2Sclk_AUDIOgpio2c4	H23	audio_gpio2c4	i2s_clk			I/O	2mA	down	I	
I2C1AUDIOsda_AUDIOgpio2c5	G19	audio_gpio2c5	i2c1audio_sda			I/O	2mA	up	I	
I2C1AUDIOscl_AUDIOgpio2c6	G20	audio_gpio2c6	i2c1audio_scl			I/O	2mA	up	I	
SPDIFtx_EDPhpd_AUDIOgpio2c7	G23	audio_gpio2c7	spdif_tx	edp_hpd		I/O	2mA	down	I	
UART0BTsin_WIFIgpio2d0	K22	wifi_gpio2d0	uart0bt_sin			I/O	2mA	up	I	
UART0BTsout_WIFIgpio2d1	K19	wifi_gpio2d1	uart0bt_sout			I/O	2mA	down	I	
UART0BTctsn_WIFIgpio2d2	K21	wifi_gpio2d2	uart0bt_ctsn			I/O	2mA	up	I	
UART0BTrtsn_WIFIgpio2d3	H18	wifi_gpio2d3	uart0bt_rtsn			I/O	2mA	up	I	WIFI_BT (APIO2)
SDIO0data0_WIFIgpio2d4	M22	wifi_gpio2d4	sdio0_data0			I/O	4mA	up	I	
SDIO0data1_WIFIgpio2d5	N20	wifi_gpio2d5	sdio0_data1			I/O	4mA	up	I	
SDIO0data2_WIFIgpio2d6	N23	wifi_gpio2d6	sdio0_data2			I/O	4mA	up	I	

Pad#	Ball#	Func0	Func1	Func2	Func3	Pad type[1]	Current [2]	Pull [5]	Reset State[3]	Power Supply[4]
SDIO0data3_WIFIgpio2d7	L20	wifi_gpio2d7	sdio0_data3			I/O	4mA	up	I	
SDIO0cmd_WIFIgpio3a0	L21	wifi_gpio3a0	sdio0_cmd			I/O	4mA	up	I	
SDIO0clkout_WIFIgpio3a1	L19	wifi_gpio3a1	sdio0_clkout			I/O	8mA	down	I	
SDIO0detectn_WIFIgpio3a2	L18	wifi_gpio3a2	sdio0_detectn			I/O	2mA	up	I	
SDIO0wrprt_WIFIgpio3a3	L22	wifi_gpio3a3	sdio0_wrprt			I/O	2mA	down	I	
SDIO0pwren_WIFIgpio3a4	L17	wifi_gpio3a4	sdio0_pwren			I/O	2mA	down	I	
SDIO0bkpwr_WIFIgpio3a5	L23	wifi_gpio3a5	sdio0_bkpwr			I/O	2mA	down	I	
SDIO0intn_WIFIgpio3a6	K20	wifi_gpio3a6	sdio0_intn			I/O	2mA	up	I	
WIFIgpio3a7	H19	wifi_gpio3a7				I/O	2mA	up	I	
MACtxd0_PWM0_VOPpwm_GPIO30gpio3b0	T18	gpio30_gpio3b0	mac_txd0	pwm_0	vop_pwm	I/O	8mA	down	I	
MACtxd1_GPIO30gpio3b1	U19	gpio30_gpio3b1	mac_txd1			I/O	8mA	down	I	
MACtxd2_GPIO30gpio3b2	T20	gpio30_gpio3b2	mac_txd2			I/O	8mA	down	I	
MACcrs_GPIO30gpio3b3	V22	gpio30_gpio3b3	mac_crs			I/O	2mA	down	I	
MACcol_GPIO30gpio3b4	W23	gpio30_gpio3b4	mac_col			I/O	2mA	up	I	
MACtxen_GPIO30gpio3b5	V19	gpio30_gpio3b5	mac_txen			I/O	8mA	down	I	
MACtxd3_GPSmag_GPIO30gpio3b6	T19	gpio30_gpio3b6	mac_txd3	gps_mag		I/O	8mA	up	I	
MACrxd0_GPSsig_GPIO30gpio3b7	AB19	gpio30_gpio3b7	mac_rxd0	gps_sig		I/O	4mA	down	I	
MACrxd1_UART3GPSctsn_GPSrfclk_GPIO30gpio3c0	U21	gpio30_gpio3c0	mac_rxd1	uart3gps_ctsn	gps_rfclk	I/O	4mA	up	I	
MACrxd2_UART3GPSrtsn_USBdrvvbus0_GPIO30gpio3c1	T21	gpio30_gpio3c1	mac_rxd2	uart3gps_rtsn	usb_drvvbus0	I/O	4mA	up	I	
MACrxd3_USBdrvvbus1_GPIO30gpio3c2	Y23	gpio30_gpio3c2	mac_rxd3	usb_drvvbus1		I/O	4mA	down	I	GPIO30 (APIO1)
MACmdc_ISPshutteren_GPIO30gpio3c3	U22	gpio30_gpio3c3	mac_mdc	isp_shutteren		I/O	2mA	down	I	
MACrxdv_ISPflashtrigout_GPIO30gpio3c4	W22	gpio30_gpio3c4	mac_rxdv	isp_flashtrigout		I/O	4mA	up	I	
MACrxer_ISPprelighttrig_GPIO30gpio3c5	P21	gpio30_gpio3c5	mac_rxer	isp_prelighttrig		I/O	2mA	down	I	
MACclk_ISPshuttertrig_GPIO30gpio3c6	W21	gpio30_gpio3c6	mac_clk	isp_shuttertrig		I/O	12mA	down	I	
EDPHDMIcecinout_ISPflashtrigin_GPIO30gpio3c7	U23	gpio30_gpio3c7	edphdmi_cecinout	isp_flashtrigin		I/O	2mA	up	I	
MACmdI2C4TPsda_GPIO30gpio3d0	N18	gpio30_gpio3d0	mac_mdio	i2c4tp_sda		I/O	2mA	up	I	
MACrxclkin_I2C4TPscl_GPIO30gpio3d1	U18	gpio30_gpio3d1	mac_rxclkin	i2c4tp_scl		I/O	4mA	up	I	
HDMII2Csda_I2C5HDMIsda_GPIO30gpio3d2	T22	gpio30_gpio3d2	hdmii2c_sda	i2c5hdmi_sda		I/O	2mA	up	I	
HDMII2Cscl_I2C5HDMIscl_GPIO30gpio3d3	T23	gpio30_gpio3d3	hdmii2c_scl	i2c5hdmi_scl		I/O	2mA	up	I	
MACtxclkout_SPI1csn1_GPIO30gpio3d4	W20	gpio30_gpio3d4	mac_txclkout	spi1_csn1		I/O	12mA	down	I	
IRrx_UART3GPSsin_GPIO30gpio3d5	P19	gpio30_gpio3d5	ir_rx	uart3gps_sin		I/O	2mA	up	I	
IRtx_UART3GPSsout_PWM3_GPIO30gpio3d6	R21	gpio30_gpio3d6	ir_tx	uart3gps_sout	pwm_3	I/O	2mA	up	I	
SCvcc18v_I2C2SENSORsda_GPUJTAGtck_GPIO1830gpio3d7	E20	gpio1830_gpio3d7	sc_vcc18v	i2c2sensor_sda	gpujtag_tck	I/O	2mA	up	I	
SCvcc33v_I2C2SENSORscl_GPUJTAGtrstn_GPIO1830gpio0b1	F20	gpio1830_gpio0b1	sc_vcc33v	i2c2sensor_scl	gpujtag_trstn	I/O	2mA	up	I	
SCrst_SPI2rxd_GPUJTAGtms_GPIO1830gpio0b2	F21	gpio1830_gpio0b2	sc_rst	spi2_rxd	gpujtag_tms	I/O	2mA	up	I	GPIO1830 (APIO4)
SCclk_SPI2txd_GPUJTAGtdi_GPIO1830gpio0b3	G21	gpio1830_gpio0b3	sc_clk	spi2_txd	gpujtag_tdi	I/O	2mA	up	I	
SCSPI2clk_GPUJTAGtdo_GPIO1830gpio0b4	G22	gpio1830_gpio0b4	sc_io	spi2_clk	gpujtag_tdo	I/O	2mA	up	I	
SCdetect_SPI2csn0_GPIO1830gpio0b5	F22	gpio1830_gpio0b5	sc_detect	spi2_csn0		I/O	2mA	up	I	
ADC_IN0	AA11	saradc_ain0				A	NA	NA	NA	
ADC_IN1	AC11	saradc_ain1				A	NA	NA	NA	SARADC
ADC_IN2	AB11	saradc_ain2				A	NA	NA	NA	
EDP_AUXN	AA3	edp_auxn				A	NA	NA	NA	
EDP_AUXP	AA2	edp_auxp				A	NA	NA	NA	
EDP_DC_TP	M7	edp_dctp				A	NA	NA	NA	
EDP_CLKI_24M	L7	edp_oscclk24m				A	NA	NA	NA	
EDP_RBIAS	L5	edp_rbias				A	NA	NA	NA	
EDP_TX0N	U2	edp_tx0n				A	NA	NA	NA	
EDP_TX0P	U1	edp_tx0p				A	NA	NA	NA	EDP
EDP_TX1N	V3	edp_tx1n				A	NA	NA	NA	
EDP_TX1P	V2	edp_tx1p				A	NA	NA	NA	
EDP_TX2N	W2	edp_tx2n				A	NA	NA	NA	
EDP_TX2P	W1	edp_tx2p				A	NA	NA	NA	
EDP_TX3N	Y2	edp_tx3n				A	NA	NA	NA	
EDP_TX3P	Y1	edp_tx3p				A	NA	NA	NA	

Pad#	Ball#	Func0	Func1	Func2	Func3	Pad type[1]	Current [2]	Pull [5]	Reset State[3]	Power Supply[4]
HDMI_HPD	N4	hdmiphy_hpd				A	NA	NA	NA	HDMI
HDMI_RBIAS	N5	hdmiphy_rext				A	NA	NA	NA	
HDMI_TCN	AC1	hdmiphy_tmdsclkn				A	NA	NA	NA	
HDMI_TCP	AB1	hdmiphy_tmdsclkp				A	NA	NA	NA	
HDMI_TX0N	AC2	hdmiphy_tmdsdatan0				A	NA	NA	NA	
HDMI_TX1N	AC4	hdmiphy_tmdsdatan1				A	NA	NA	NA	
HDMI_TX2N	AC5	hdmiphy_tmdsdatan2				A	NA	NA	NA	
HDMI_TX0P	AB2	hdmiphy_tmdsdatap0				A	NA	NA	NA	
HDMI_TX1P	AB4	hdmiphy_tmdsdatap1				A	NA	NA	NA	
HDMI_TX2P	AB5	hdmiphy_tmdsdatap2				A	NA	NA	NA	
USIC_DATA	AB20	USIC_data				A	NA	NA	NA	USIC
USIC_STROBE	AC20	USIC_strobe				A	NA	NA	NA	
MIPI_CSI_CLKN	J3	mipicsi_clkn				A	NA	NA	NA	MIPICSI
MIPI_CSI_CLKP	J2	mipicsi_clkp				A	NA	NA	NA	
MIPI_CSI_DN0	G2	mipicsi_datan0				A	NA	NA	NA	
MIPI_CSI_DN1	H2	mipicsi_datan1				A	NA	NA	NA	
MIPI_CSI_DN2	K2	mipicsi_datan2				A	NA	NA	NA	
MIPI_CSI_DN3	L2	mipicsi_datan3				A	NA	NA	NA	
MIPI_CSI_DP0	G1	mipicsi_datap0				A	NA	NA	NA	
MIPI_CSI_DP1	H1	mipicsi_datap1				A	NA	NA	NA	
MIPI_CSI_DP2	K1	mipicsi_datap2				A	NA	NA	NA	
MIPI_CSI_DP3	L1	mipicsi_datap3				A	NA	NA	NA	
MIPI_CSI_RBIAS	H6	mipicsi_extrbias				A	NA	NA	NA	
IO_LCDCdata5_LVDSclkn_MIPIDSIclkn	P1	mipidsi_clkn	lcdc_data5	lvds_clkn		A	NA	NA	NA	MIPIDSI
IO_LCDCdata4_LVDSclkp_MIPIDSIclkp	P2	mipidsi_clkp	lcdc_data4	lvds_clkp		A	NA	NA	NA	
IO_LCDCdata9_LVDSdatan0_MIPIDSIdatan0	M2	mipidsi_datan0	lcdc_data9	lvds_datan0		A	NA	NA	NA	
IO_LCDCdata7_LVDSdatan1_MIPIDSIdatan1	N1	mipidsi_datan1	lcdc_data7	lvds_datan1		A	NA	NA	NA	
IO_LCDCdata2_LVDSdatan2_MIPIDSIdatan2	R2	mipidsi_datan2	lcdc_data2	lvds_datan2		A	NA	NA	NA	
IO_LCDCdata0_LVDSdatan3_MIPIDSIdatan3	T1	mipidsi_datan3	lcdc_data0	lvds_datan3		A	NA	NA	NA	
IO_LCDCdata8_LVDSdatap0_MIPIDSIdatap0	M3	mipidsi_datap0	lcdc_data8	lvds_datap0		A	NA	NA	NA	
IO_LCDCdata6_LVDSdatap1_MIPIDSIdatap1	N2	mipidsi_datap1	lcdc_data6	lvds_datap1		A	NA	NA	NA	
IO_LCDCdata3_LVDSdatap2_MIPIDSIdatap2	R3	mipidsi_datap2	lcdc_data3	lvds_datap2		A	NA	NA	NA	
IO_LCDCdata1_LVDSdatap3_MIPIDSIdatap3	T2	mipidsi_datap3	lcdc_data1	lvds_datap3		A	NA	NA	NA	
MIPI_DSI_RBIAS	K6	mipidsi_rbias				A	NA	NA	NA	
USB0_ID	Y20	usbphy_usb0id				A	NA	NA	NA	USB
USB0_DM	AC22	usbphy_usb0pn				A	NA	NA	NA	
USB0_DP	AB22	usbphy_usb0pp				A	NA	NA	NA	
USB1_DM	AC23	usbphy_usb1pn				A	NA	NA	NA	
USB1_DP	AB23	usbphy_usb1pp				A	NA	NA	NA	
USB_RBIAS	R17	usbphy_usbrbias				A	NA	NA	NA	
USB_VBUS	AA21	usbphy_vbus				A	NA	NA	NA	
DDR_DM0	D20	ddrphya_dm0				A	NA	NA	NA	DDR
DDR_DM1	E6	ddrphya_dm1				A	NA	NA	NA	
DDR_DQ0	E22	ddrphya_dq0				A	NA	NA	NA	
DDR_DQ1	D21	ddrphya_dq1				A	NA	NA	NA	
DDR_DQ10	B6	ddrphya_dq10				A	NA	NA	NA	
DDR_DQ11	E7	ddrphya_dq11				A	NA	NA	NA	
DDR_DQ12	C7	ddrphya_dq12				A	NA	NA	NA	
DDR_DQ13	E8	ddrphya_dq13				A	NA	NA	NA	
DDR_DQ14	D8	ddrphya_dq14				A	NA	NA	NA	
DDR_DQ15	C8	ddrphya_dq15				A	NA	NA	NA	
DDR_DQ2	C22	ddrphya_dq2				A	NA	NA	NA	
DDR_DQ3	D22	ddrphya_dq3				A	NA	NA	NA	
DDR_DQ4	A23	ddrphya_dq4				A	NA	NA	NA	

Pad#	Ball#	Func0	Func1	Func2	Func3	Pad type[1]	Current [2]	Pull [5]	Reset State[3]	Power Supply[4]
DDR_DQ5	B23	ddrphya_dq5				A	NA	NA	NA	
DDR_DQ6	D23	ddrphya_dq6				A	NA	NA	NA	
DDR_DQ7	E23	ddrphya_dq7				A	NA	NA	NA	
DDR_DQ8	D6	ddrphya_dq8				A	NA	NA	NA	
DDR_DQ9	C6	ddrphya_dq9				A	NA	NA	NA	
DDR_DQS0	B22	ddrphya_dqs0				A	NA	NA	NA	
DDR_DQS1	B7	ddrphya_dqs1				A	NA	NA	NA	
DDR_DQS0N	A22	ddrphya_dqsb0				A	NA	NA	NA	
DDR_DQS1N	A7	ddrphya_dqsb1				A	NA	NA	NA	
DDR_A0	A11	ddrphy_a0				A	NA	NA	NA	
DDR_A1	C12	ddrphy_a1				A	NA	NA	NA	
DDR_A10	C15	ddrphy_a10				A	NA	NA	NA	
DDR_A11	B15	ddrphy_a11				A	NA	NA	NA	
DDR_A12	D18	ddrphy_a12				A	NA	NA	NA	
DDR_A13	C16	ddrphy_a13				A	NA	NA	NA	
DDR_A14	B16	ddrphy_a14				A	NA	NA	NA	
DDR_A15	A16	ddrphy_a15				A	NA	NA	NA	
DDR_A2	B12	ddrphy_a2				A	NA	NA	NA	
DDR_A3	E13	ddrphy_a3				A	NA	NA	NA	
DDR_A4	C13	ddrphy_a4				A	NA	NA	NA	
DDR_A5	A14	ddrphy_a5				A	NA	NA	NA	
DDR_A6	B14	ddrphy_a6				A	NA	NA	NA	
DDR_A7	C14	ddrphy_a7				A	NA	NA	NA	
DDR_A8	D14	ddrphy_a8				A	NA	NA	NA	
DDR_A9	E14	ddrphy_a9				A	NA	NA	NA	
DDR_DM2	C20	ddrphyb_dm0				A	NA	NA	NA	
DDR_DM3	A2	ddrphyb_dm1				A	NA	NA	NA	
DDR_DQ16	C18	ddrphyb_dq0				A	NA	NA	NA	
DDR_DQ17	B17	ddrphyb_dq1				A	NA	NA	NA	
DDR_DQ26	C3	ddrphyb_dq10				A	NA	NA	NA	
DDR_DQ27	C4	ddrphyb_dq11				A	NA	NA	NA	
DDR_DQ28	D5	ddrphyb_dq12				A	NA	NA	NA	
DDR_DQ29	C5	ddrphyb_dq13				A	NA	NA	NA	
DDR_DQ30	B5	ddrphyb_dq14				A	NA	NA	NA	
DDR_DQ31	A5	ddrphyb_dq15				A	NA	NA	NA	
DDR_DQ18	A17	ddrphyb_dq2				A	NA	NA	NA	
DDR_DQ19	A20	ddrphyb_dq3				A	NA	NA	NA	
DDR_DQ20	C19	ddrphyb_dq4				A	NA	NA	NA	
DDR_DQ21	B18	ddrphyb_dq5				A	NA	NA	NA	
DDR_DQ22	B20	ddrphyb_dq6				A	NA	NA	NA	
DDR_DQ23	B21	ddrphyb_dq7				A	NA	NA	NA	
DDR_DQ24	B2	ddrphyb_dq8				A	NA	NA	NA	
DDR_DQ25	B3	ddrphyb_dq9				A	NA	NA	NA	
DDR_DQS2	B19	ddrphyb_dqs0				A	NA	NA	NA	
DDR_DQS3	B4	ddrphyb_dqs1				A	NA	NA	NA	
DDR_DQS2N	A19	ddrphyb_dqsb0				A	NA	NA	NA	
DDR_DQS3N	A4	ddrphyb_dqsb1				A	NA	NA	NA	
DDR_BA0	D11	ddrphy_b0				A	NA	NA	NA	
DDR_BA1	C11	ddrphy_b1				A	NA	NA	NA	
DDR_BA2	B11	ddrphy_b2				A	NA	NA	NA	
DDR_CASN	B10	ddrphy_casb				A	NA	NA	NA	
DDR_CLK	B13	ddrphy_ck				A	NA	NA	NA	
DDR_CLKN	A13	ddrphy_ckb				A	NA	NA	NA	
DDR_CKE0	C9	ddrphy_cke0				A	NA	NA	NA	

Pad#	Ball#	Func0	Func1	Func2	Func3	Pad type①	Current ②	Pull ⑤	Reset State③	Power Supply④
DDR_CKE1	B8	ddrphy_cke1				A	NA	NA	NA	
DDR_CS0N	A8	ddrphy_csb0				A	NA	NA	NA	
DDR_CS1N	B9	ddrphy_csb1				A	NA	NA	NA	
DDR_RETEN_IN	E10	ddrphy_bufferen				A	NA	NA	NA	
DDR_ODT0	D17	ddrphy_odt0				A	NA	NA	NA	
DDR_ODT1	C17	ddrphy_odt1				A	NA	NA	NA	
DDR_RASN	A10	ddrphy_rasb				A	NA	NA	NA	
DDR_RESETN	E11	ddrphy_resetn				A	NA	NA	NA	
DDR_WEN	C10	ddrphy_web				A	NA	NA	NA	

Notes :

①:Pad types : I = input , O = output , I/O = input/output (bidirectional) ,
AP = Analog Power , AG = Analog Ground
DP = Digital Power , DG = Digital Ground
A = Analog

②: Output Drive strength is configurable, it's the suggested value in this table. Unit is mA , only Digital IO have drive value

③:Reset state: I = input without any pull resistor O = output

④:It is die location. For examples, "Left side" means that all the related IOs are always in left side of die

⑤:Power supply means that all the related IOs are in this IO power domain. If multiple powers are included, they are connected together in one IO power ring

⑥:The pull up/pull down is configurable.

2.8 IO pin name descriptions

This sub-chapter will focus on the detailed function description of every pins based on different interface.

Table 2-3 PX5 IO function description list

Interface	Pin Name	Direction	Description
Misc	XIN24M	I	Clock input of 24MHz crystal
	XOUT24M	O	Clock output of 24MHz crystal
	CLK32K	I	Clock input of 32.768KHz
	NPOR	I	Chip hardware reset
	ddr_reten	O	DDR IO retention control
	tsadc_int	O	TSADC trigger to shut down chip
	global_pwroff	O	System power off control port
	pmic_sleep	O	Sleep control to external PMIC chip

Interface	Pin Name	Direction	Description
	jtag_trstn	I	Cortex-A53 JTAG interface reset input
	jtag_tck	I	Cortex-A53 JTAG interface clock input/SWD interface clock input
	jtag_tdi	I	Cortex-A53 JTAG interface TDI input
	jtag_tms	I/O	Cortex-A53 JTAG interface TMS input/SWD interface data out
	jtag_tdo	O	Cortex-A53 JTAG interface TDO output

Interface	Pin Name	Direction	Description
	mcujtag_trstn	I	mcu JTAG interface reset input
	mcujtag_tck	I	mcu JTAG interface clock input/SWD interface clock input
	mcujtag_tdi	I	mcu JTAG interface TDI input
	mcujtag_tms	I/O	mcu JTAG interface TMS input/SWD interface data out
	mcujtag_tdo	O	mcu JTAG interface TDO output

Interface	Pin Name	Direction	Description
	gpujtag_trstn	I	gpu JTAG interface reset input
	gpujtag_tck	I	gpu JTAG interface clock input/SWD interface clock input
	gpujtag_tdi	I	gpu JTAG interface TDI input
	gpujtag_tms	I/O	gpu JTAG interface TMS input/SWD interface data out
	gpujtag_tdo	O	gpu JTAG interface TDO output

Interface	Pin Name	Direction	Description
ETM Trace	trace_clk	O	Cortex-A53 ETM trace port clk
	trace_ctl	O	Cortex-A53 ETM trace port control
	trace_data*i*(*i*=0~15)	O	Cortex-A53 ETM trace port data

Interface	Pin Name	Direction	Description

Interface	Pin Name	Direction	Description
SD/MMC Host Controller	sdmmc_clkout	O	sdmmc card clock.
	sdmmc_cmd	I/O	sdmmc card command output and reponse input.
	sdmmc_data*i* (*i*=0~3)	I/O	sdmmc card data input and output.
	sdmmc_detect_n	I	sdmmc card detect signal, a 0 represents presence of card.

Interface	Pin Name	Direction	Description
SDIO Host Controller	sdio*x*_clkout*(x=0,1)*	O	sdio card clock.
	sdio*x*_cmd*(x=0,1)*	I/O	sdio card command output and reponse input.
	sdio*x*_data*i* (*i*=0~3) *(x=0,1)*	I/O	sdio card data input and output.
	sdio*x*_detectn*(x=0,1)*	I	sdio card detect signal, a 0 represents presence of card.
	sdio*x*_wrprt*(x=0,1)*	I	sdio card write protect signal, a 1 represents write is protected.
	sdio*x*_pwren*(x=0,1)*	O	sdio card power-enable control signal
	sdio*x*_intn*(x=0,1)*	O	sdio card interrupt indication
	sdio*x*_bkpwr*(x=0,1)*	O	the back-end power supply for embedded device

Interface	Pin Name	Direction	Description
eMMC Interface	emmc_clkout	O	emmc card clock.
	emmc_cmd	I/O	emmc card command output and reponse input.
	emmc_data*i* (*i*=0~7)	I/O	emmc card data input and output.
	emmc_pwren	O	emmc card power-enable control signal
	emmc_rstnout	O	emmc card reset signal

Interface	Pin Name	Direction	Description
DMC	DDR*x*_CK*(x=0,1)*	O	Active-high clock signal to the memory device.
	DDR*x*_CK_N*(x=0,1)*	O	Active-low clock signal to the memory device.
	DDR*x*_CKE*i* (*i*=0,1) *(x=0,1)*	O	Active-high clock enable signal to the memory device for two chip select.
	DDR*x*_CSN*i* (*i*=0,1) *(x=0,1)*	O	Active-low chip select signal to the memory device. A There are two chip select.
	DDR*x*_RASN*(x=0,1)*	O	Active-low row address strobe to the memory device.
	DDR*x*_CASN*(x=0,1)*	O	Active-low column address strobe to the memory device.
	DDR*x*_WEN*(x=0,1)*	O	Active-low write enable strobe to the memory device.
	DDR*x*_BA[2:0] *(x=0,1)*	O	Bank address signal to the memory device.
	DDR*x*_ADDR[15:0] *(x=0,1)*	O	Address signal to the memory device.
	DDR*x*_DQ[31:0] *(x=0,1)*	I/O	Bidirectional data line to the memory device.
	DDR*x*_DQS[3:0] *(x=0,1)*	I/O	Active-high bidirectional data strobes to the memory device.
	DDR*x*_DQS_B[3:0] *(x=0,1)*	I/O	Active-low bidirectional data strobes to the memory device.
	DDR*x*_DM[3:0] *(x=0,1)*	O	Active-low data mask signal to the memory device.

Interface	Pin Name	Direction	Description
	DDR*x*_ODT*i* (*i*=0,1) *(x=0,1)*	O	On-Die Termination output signal for two chip select.
	DDR*x*_RETEN*(x=0,1)*	I	Active-low retention latch enable input
	DDR*x*_RESET*(x=0,1)*	O	DDR3 reset signal to the memory device
	DDR*x*_VREF*i* (*i*=0,1,2,3) *(x=0,1)*	I/O	Reference Voltage input for three regions of DDR IO
	DDR*x*_PZQ*(x=0,1)*	I/O	ZQ calibration pad which connects 240ohm±1% resistor

Interface	Pin Name	Direction	Description
NandC	flash_wp	O	Flash write-protected signal
	flash_ale	O	Flash address latch enable signal
	flash_cle	O	Flash command latch enable signal
	flash_wrn	O	Flash write enable and clock signal
	flash_rdn	O	Flash read enable and write/read signal
	flash_data*i*(*i*=0~7)	I/O	Flash data inputs/outputs signal
	flash*x*_dqs	I/O	Flash data strobe signal
	flash*x*_rdy	I	Flash ready/busy signal
	flash*x*_csn*i*=0~4)	O	Flash chip enable signal for chip i, i=0~7

Interface	Pin Name	Direction	Description
HSADC	hsadc_data*i* (*i*=0~1)	I	gps data(i=0,1)
	gps_clk	I	hsadc/tsi/gps reference clock

Interface	Pin Name	Direction	Description
TSP Interface	ts_clk	I/O	TSI reference clock
	ts_data*i* (*i*=0~7)	I	TSI data(i=0~7)
	ts_sync	I	TSI synchronizer signal
	ts_valid	I	TSI valid signal
	ts_err	I	TSI fail signal

Interface	Pin Name	Direction	Description
I2S_8ch/PCM Controller	i2s_clk	O	I2S/PCM clock source
	i2s_sclk	I/O	I2S/PCM serial clock
	i2s_lrckrx	I/O	I2S/PCM left & right channel signal for receiving serial data, synchronous left & right channel in I2S mode and the beginning of a group of left & right channels in PCM mode
	i2s_sdi	I	I2S/PCM serial data input
	i2s_sdo*i* (*i*=0~3)	O	I2S/PCM serial data ouput
	i2s_lrcktx	I/O	I2S/PCM left & right channel signal for transmitting serial data, synchronous left & right channel in I2S mode and the beginning of a group of left & right channels in PCM mode

Interface	Pin Name	Direction	Description
I2S_2CH/PCM	pcm_clk	I/O	I2S/PCM serial clock

Interface	Pin Name	Direction	Description
Controller	pcm_sync	I/O	I2S/PCM left & right channel signal for receiving serial data, synchronous left & right channel in I2S mode and the beginning of a group of left & right channels in PCM mode
	i2s_sdi	I	I2S/PCM serial data input
	i2s_sdo	O	I2S/PCM serial data ouput

Interface	Pin Name	Direction	Description
SPDIF transmitter	spdif_tx	O	spdif biphase data ouput

Interface	Pin Name	Direction	Description
SPI Controller	spi*x*_clk*(x=0,2)*	I/O	spi serial clock
	spi*x*_csn*y* *(x=0,2)(y=0,1)*	I/O	spi chip select signal,low active
	spi*x*_txd*(x=0,2)*	O	spi serial data output
	spi*x*_rxd*(x=0,2)*	I	spi serial data input

Interface	Pin Name	Direction	Description
SFC Controller	sfc_clk	I/O	sfc serial clock
	sfc_csnx*(x=0,1)*	I/O	sfc chip select signal,low active
	sfc_siox*(x=0,3)*	O	sfc serial data output

Interface	Pin Name	Direction	Description
LCDC	lcdc_dclk	O	LCDC RGB interface display clock out, MCU i80 interface RS signal
	lcdc_vsync	O	LCDC RGB interface vertical sync pulse, MCU i80 interface CSN signal
	lcdc_hsync	O	LCDC RGB interface horizontal sync pulse, MCU i80 interface WEN signal
	lcdc_den	O	LCDC RGB interface data enable, MCU i80 interface REN signal
	lcdc_data*i*(*i*=0~23)	O	LCDC data output/input
	vop_pwm	O	VOP_BIG CABAC PWM control signal

Interface	Pin Name	Direction	Description
Camera IF	cif_clkin	I	Camera0 interface input pixel clock
	cif_clkout	O	Camera0 interface output work clock
	cif_vsync	I	Camera0 interface vertical sync signal
	cif_href	I	Camera0 interface horizontial sync signal
	cif_data *i*(*i*=0~11)	I	Camera0 interface input pixel data

Interface	Pin Name	Direction	Description
PWM	pwm3	I/O	Pulse Width Modulation output

Interface	Pin Name	Direction	Description
	pwm2	I/O	Pulse Width Modulation output
	pwm1	I/O	Pulse Width Modulation output
	pwm0	I/O	Pulse Width Modulation output

Interface	Pin Name	Direction	Description
I2C	i2c0pmu_sda	I/O	I2C_PMU data
	i2c0pmu_scl	I/O	I2C_PMU clock
	i2c1sensor_sda	I/O	I2C1_SENSOR data
	i2c1sensor_scl	I/O	I2C1_SENSOR clock
	i2c2audio_sda	I/O	I2C2_AUDIO data
	i2c2audio_scl	I/O	I2C2_AUDIO clock
	i2c3cam_sda	I/O	I2C3_CAM data
	i2c3cam_scl	I/O	I2C3_CAM clock
	i2c4tp_sda	I/O	I2C4_TP data
	i2c4tp_scl	I/O	I2C4_TP clock
	i2c5hdmi_sda	I/O	I2C5_HDMI data
	i2c5hdmi_scl	I/O	I2C5_HDMI clock

Interface	Pin Name	Direction	Description
UART	uart0bt_sin	I	UART_BT searial data input
	uart0bt_sout	O	UART_BT searial data output
	uart0bt_ctsn	I	UART_BT clear to send
	uart0bt_rtsn	O	UART_BT request to send
	uart1bb_sin	I	UART_BB searial data input
	uart1bb_sout	O	UART_BB searial data output
	uart1bb_ctsn	O	UART_BB clear to send
	uart1bb_rtsn	I	UART_BB request to send
	uart2dbg_sin	I	UART_DBG searial data input
	uart2dbg_sout	O	UART_DBG searial data output
	uart3gps_sin	I	UART_GPS searial data input
	uart3gps_sout	O	UART_GPS searial data output
	uart3gps_ctsn	I	UART_GPS clear to send
	uart3gps_rtsn	O	UART_GPS request to send
	uart4exp_sin	I	UART_EXP searial data input
	uart4exp_sout	O	UART_EXP searial data output
	uart4exp_ctsn	I	UART_EXP clear to send
	uart4exp_rtsn	O	UART_EXP request to send

Interface	Pin Name	Direction	Description
GMAC	mac_clk	I/O	RMII REC_CLK output or GMAC external clock input
	mac_txclk	O	RGMII TX clock output
	mac_rxclk	I	RGMII RX clock input
	mac_mdc	O	GMAC management interface clock
	mac_mdio	I/O	GMAC management interface data
	mac_txd*i*(*i*=0~3)	O	GMAC TX data
	max_rxd*i*(*i*=0~3)	I	GMAC RX data

Interface	Pin Name	Direction	Description
	mac_txen	O	GMAC TX data enable
	mac_rxdv	I	GMAC RX data valid signal
	mac_rxer	I	GMAC RX error signal
	mac_col	I	PHY Collision signal
	mac_crs	I	PHY CRS signal

Interface	Pin Name	Direction	Description
USB 2.0 PHY	USB0_ID	I/O	USB 2.0 ID input
	USB0_DM	I/O	USB 2.0 channel0 data DM
	USB0_DP	I/O	USB 2.0 channel0 data DP
	USB1_DM	I/O	USB 2.0 channel0 data DM
	USB1_DP	I/O	USB 2.0 channel0 data DP
Interface	USB_RBIAS	I	Connect 135ohm resister to ground
USB Host 2.0 (2 channel)	USB_VBUS	I	USB 2.0 VBUS input

Interface	Pin Name	Direction	Description
USIC	USIC_DATA	N/A	USIC DATA signal
	USIC_STROBE	N/A	USIC STROBE signal

Interface	Pin Name	Direction	Description
SAR-ADC	SARADC_AIN[i] (i=0~2)	N/A	SAR-ADC input signal for 3 channel

Interface	Pin Name	Direction	Description
eFuse	EFUSE_VDDQ	N/A	eFuse program and sense power

Interface	Pin Name	Direction	Description
SIM Card	sc_clk	O	Smart card clock output
	sc_rst	O	Smart card reset output
	sc_io	I/O	Smart card data
	sc_detect	O	Smart card detect input
	sc_vcc18v	O	Smart card 1.8V voltage select
	sv_vcc33v	O	Smart card 3.3V voltage select

Interface	Pin Name	Direction	Description
ISP	isp_shutteren	O	Hold signal for shutter open
	isp_flashtrigout	O	Hold signal for flash light
	isp_prelighttrig	O	Hold signal for prelight
	isp_shuttertrig	I	External shutter trigger pulse
	isp_flashtrigin	I	External flash trigger pulse

Interface	Pin Name	Direction	Description

Interface	Pin Name	Direction	Description
eDP	EDP_TX*i*P(*i*=0~3)	O	eDP data lane positive output
	EDP_TX*i*N(*i*=0~3)	O	eDP data lane negative output
	EDP_DC_TP	O	eDP PHY DC test point
	EDP_AUXP	I/O	eDP CH-AUX positive differential output
	EDP_AUXN	I/O	eDP CH-AUX negative differential output
	EDP_R_BIAS	I	Let it floating
	EDP_OSC_CLK_24M	I	24MHz input reference clock
	edp_hotplug	I	eDP external hot plug signal
	edphdmi_cecinout	I/O	eDP HDMI CEC bus
	edphdmii2c_sda	I/O	eDP HDMI I2C data
	edphdmii2c_scl	I/O	eDP HDMI I2C clock

Interface	Pin Name	Direction	Description
HDMI	HDMI_TMDSDATAN*i*(*i*=0~2)	O	HDMI negative TMDS differential line driver data output
	HDMI_TMDSDATAP*i*(*i*=0~2)	O	HDMI positive TMDS differential line driver data output
	HDMI_TMDSCLKN	O	HDMI negative TMDS differential line driver clock output
	HDMI_TMDSCLKP	O	HDMI positive TMDS differential line driver clock output
	HDMI_RESREF	I/O	HDMI reference resistor connection
	HDMI_HPD	I/O	HDMI hot plug detect signal
	HDMI_DDCCEC	I/O	HDMI ground reference for the hot plug detect signal

Interface	Pin Name	Direction	Description
MIPI_DSI	MIPI_DSI_DN*i*(*i*=0~3)	I/O	MIPI DSI negative differential data line transceiver output
	MIPI_DSI_DP*i*(*i*=0~3)	I/O	MIPI DSI positive differential data line transceiver output
	MIPI_DSI_CLKP	I/O	MIPI DSI positive differential clock line transceiver output
	MIPI_DSI_CLKN	I/O	MIPI DSI negative differential clock line transceiver output
	MIPI_DSI_RBIAS	I/O	MIPI DSI external resistor connection

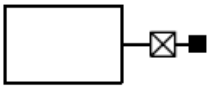
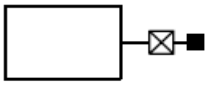
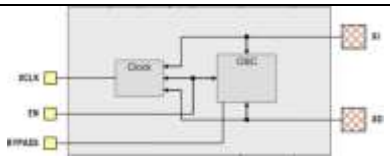
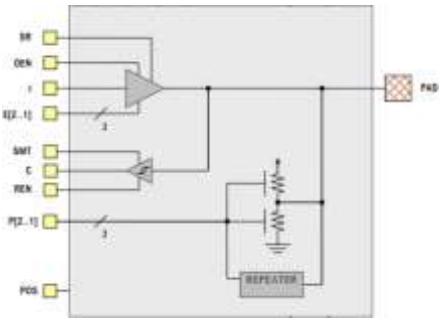
Interface	Pin Name	Direction	Description
MIPI_CSI	MIPI_CSI_DN*i*(*i*=0~3)	I/O	MIPI CSI negative differential data line transceiver output
	MIPI_CSI_DP*i*(*i*=0~3)	I/O	MIPI CSI positive differential data line transceiver output
	MIPI_CSI_CLKP	I/O	MIPI CSI positive differential clock line transceiver output
	MIPI_CSI_CLKN	I/O	MIPI CSI negative differential clock line transceiver output
	MIPI_CSI_RBIAS	I/O	MIPI CSI external resistor connection

2.9 IO Type

The following list shows IO type except DDR IO and all of Power/Ground IO.

Table 2-4 PX5 IO Type List

Type	Diagram	Description	Pin Name

Type	Diagram	Description	Pin Name
A		Analog IO Cell with IO voltage	EFUSE_VQPS
B		Dedicated Power supply to Internal Macro with IO voltage	SARADC_AIN[2:0]
C		Crystal Oscillator with high enable	XIN24M/XOUT24M
D		Tri-state output pad with input, which pullup/pulldown, slew rate and drive strength is configurable	Part of digital GPIO

Chapter 3 Electrical Specification

3.1 Absolute Maximum Ratings

Table 3-1 PX5 absolute maximum ratings

Paramerters	Related Power Group	Max	Unit
DC supply voltage for Internal digital logic	CPU_VDD, LOGIC_VDD, PMU_VDD_1V0, USB_AVDD_1V0 DDRPLL_VDD_1V0	1.4	V
DC supply voltage for Digital GPIO (except for SAR-ADC, PLL, USB, DDR, MIPI PHY,LVDS, eDP, HDMI IO)	PMUIO_VDD APIO1_VDD APIO2_VDD APIO3_VDD APIO4_VDD LCDC_VDD SDMMC_VDD FLASH_VDD DVPIO_VDD	3.6	V
DC supply voltage for DDR IO	DDR_VDD	1.65	V
DC supply voltage for Analog part of PLL	APLL_AVDD_1V0 C/DPLL_AVDD_1V0 G/NPLL_AVDD_1V0	1.1	V
DC supply voltage for Analog part of USB OTG/Host2.0	USB_AVDD_1V8 USB_AVDD_3V3	1.98 3.63	V
DC supply voltage for Analog part of USIC	USIC_AVDD_1V2	1.32	V
Analog Input voltage for SAR-ADC/TS-ADC	ADC_AVDD_1V8	1.98	V
DC supply voltage for Analog part of MIPI_DSI/LVDS/TTL combo PHY	LVDS/MIPI_AVDD_1V0 LVDS/MIPI_AVDD_1V8 LVDS/MIPI_AVDD_3V3	1.1 1.98 3.6	V
DC supply voltage for Analog part of MIPI_CSI PHY	MIPI_CSI_AVDD_1V0	1.1	V
DC supply voltage for Analog part of eDP	EDP_AVDD_1V0 EDP_AVDD_1V8	1.1 1.98	V
DC supply voltage for Analog part of HDMI	HDMI_AVDD_1V0 HDMI_AVDD_1V8	1.1 1.98	V
Analog Input voltage for DP/DM/VBUS of USB OTG/Host2.0		5	V
Digital input voltage for input buffer of GPIO		3.6	V
Digital output voltage for output buffer of GPIO		3.6	V
Storage Temperature	Tstg	125	℃
Max Conjunction Temperature	Tj	125	℃

Absolute maximum ratings specify the values beyond which the device may be damaged permanently. Long-term exposure to absolute maximum ratings conditions may affect device reliability.

3.2 Recommended Operating Conditions

Table 1-6 describes the recommended operating condition for every clock domain.

Table 3-2 PX5 recommended operating conditions

Parameters	Symbol	Min	Typ	Max	Units
Internal digital logic Power	CPU_VDD, LOGIC_VDD, PMU_VDD_1V0, USB_AVDD_1V0 DDRPLL_VDD_1V0	0.9	1.0	TBD	V
Digital GPIO Power(3.3V/2.5V/1.8V)	PMUIO_VDD APIO1_VDD APIO2_VDD APIO3_VDD APIO4_VDD LCDC_VDD SDMMC_VDD FLASH_VDD DVPIO_VDD FLASH_VDD	3 2.25 1.62	3.3 2.5 1.8	3.6 2.75 1.98	V
DDR IO (DDR3 mode) Power	DDR_VDD	1.425	1.5	1.575	V
DDR IO (DDR3L mode) Power	DDR_VDD	1.283	1.35	1.417	V
DDR IO (LPDDR2/LPDDR3 mode) Power	DDR_VDD	1.14	1.2	1.3	V
PLL Analog Power	APLL_AVDD_1V0 C/DPLL_AVDD_1V0 G/NPLL_AVDD_1V0	0.9	1.0	1.1	V
SAR-ADC/TSADC Analog Power	ADC_AVDD_1V8	1.62	1.8	1.98	V
USB OTG/Host2.0 Digital Power	USB_AVDD_1V0	0.9	1.0	1.1	V
USB OTG/Host2.0 Analog Power(1.8V)	USB_AVDD_1V8	1.62	1.8	1.98	V
USB OTG/Host2.0 Analog Power(3.3V)	USB_AVDD_3V3	3.069	3.3	3.63	V
USIC Analog Power	USIC_AVDD_1V2	1.08	1.2	1.32	V
DSI combo PHY Analog Power(1.0V)	LVDS/MIPI_AVDD_1V0	0.9	1.0	1.1	V
DSI combo PHY Analog Power(1.8V)	LVDS/MIPI_AVDD_1V8	1.62	1.8	1.98	V
DSI combo PHY Analog Power(3.3V)	LVDS/MIPI_AVDD_3V3	3.0	3.3	3.6	V
eDP Analog Power(1.0V)	EDP_AVDD_1V0	0.9	1.0	1.1	V
eDP Analog Power(1.8V)	EDP_AVDD_1V8	1.62	1.8	1.98	V
HDMI Analog Power(1.0V)	HDMI_AVDD_1V0	0.9	1.0	1.1	V
HDMI Analog Power(1.8V)	HDMI_AVDD_1V8	1.62	1.8	1.98	V
PLL input clock frequency		N/A	24	N/A	MHz
Ambient Operating Temperature ②	Ta	-40	25	80	℃

Notes : ①' Symbol name is same as the pin name in the io descriptions

② Theoretically, PX5 could work in -40° C environment, but Rockchip didn't do fully test and verification to make sure this condition.

3.3 DC Characteristics

Table 3-3 PX5 DC Characteristics

Parameters		Symbol	Min	Typ	Max	Units
Digital GPIO @3.3V	Input Low Voltage	Vil	-0.3	0	3.3x0.3	V
	Input High Voltage	Vih	3.3x0.7	3.3	3.3+0.3	V
	Output Low Voltage	Vol	-0.3	NA	NA	V

Parameters		Symbol	Min	Typ	Max	Units
	Output High Voltage	Voh	NA	NA	3.6	V
	Threshold Point	Vtr+	1.53	1.46	1.43	V
		Vtr-	1.19	1.12	1.05	V
	Pullup Resistor	Rpu	33.7	58	101.5	Kohm
	Pulldown Resistor	Rpd	34.2	60.1	109.3	Kohm
Digital GPIO @1.8V	Input Low Voltage	Vil	-0.3	0	1.8x0.3	V
	Input High Voltage	Vih	1.8x0.7	1.8	1.8 + 0.3	V
	Output Low Voltage	Vol	-0.3	NA	NA	V
	Output High Voltage	Voh	NA	NA	1.8+0.3	V
	Threshold Point	Vtr+	1.23	1.12	1.03	V
		Vtr-	0.91	0.82	0.73	V
	Pullup Resistor	Rpu	35	62.9	120	Kohm
	Pulldown Resistor	Rpd	35.1	61	113.9	Kohm
DDR IO @DDR3 mode	Input High Voltage	Vih_ddr	VREF + 0.10	NA	DDR_VDD+0.4	V
	Input Low Voltage	Vil_ddr	-0.4	NA	VREF - 0.10	V
	Output High Voltage	Voh_ddr	0.9xDDR_VDD	NA	N/A	V
	Output Low Voltage	Vol_ddr	N/A	NA	0.1*DDR_VDD	V
	Input termination resistance(ODT) to VDDIO_DDRi/2 (i=0~6)	Rtt	100 54 36	120 60 40	140 66 44	Ohm
DDR IO @LPDDR2/ LPDDR3 mode	Input High Voltage	Vih_ddr	VREF + 0.13	NA	DDR_VDD	V
	Input Low Voltage	Vil_ddr	0	NA	VREF - 0.13	V
	Output High Voltage	Voh_ddr	NA	NA	0.9*DDR_VDD	V
	Output Low Voltage	Vol_ddr	0.1*DDR_VDD	NA	NA	V
MIPI_DSI IO @LVDS mode	Output High Voltage	Voh	NA	NA	1100	mV
	Output Low Voltage	Vol	700	NA	NA	mV
	Output differential voltage	|Vod|	250	NA	400	mV
	Output offset voltage	Vos	825	NA	975	mV
	Output impedance, single ended	Ro	40	NA	140	Ω
	Ro mismatch between A & B	ΔRo	NA	NA	10	%
	Change in |Vod| between 0 and 1	|ΔVod|	NA	NA	25	mV
	Change in Vod between 0 and 1	ΔVos	NA	NA	25	mV
MIPI_DSI IO @TTL mode	Output High Voltage	Voh	3	3.3	NA	V
	Output Low Voltage	Vol	NA	0	0.2	V
	Short-Circuit Output Current	Ios	NA	35	60	mA
	Output impedance	Zolp	40	NA	460	Ω
MIPI_DSI IO @MIPI mode	HS TX static Common-mode voltage	VCMTX	150	200	250	mV
	VCMTX mismatch when output is Differential-1 or Differential-0	|ΔVCMTX(1,0)|	NA	NA	5	mV
	HS transmit differential voltage	|VOD|	140	200	270	mV
	VOD mismatch when output is Differential-1 or Differential-0	|ΔVOD|	NA	NA	10	mV
	HS output high voltage	VOHHS	NA	NA	360	mV
	Single ended output impedance	ZOS	40	50	62.5	Ω
	Single ended output impedance mismatch	ΔZOS	NA	NA	10	%
HDMI	Single-ended standby voltage	Voff	avddtmds±10			mV
	Single-ended output swing	Vswing	400	NA	600	mV

Parameters		Symbol	Min	Typ	Max	Units
	voltage RT=50Ω	Vswing_data	400	NA	600	mV
		Vswing_clock	200	NA	600	mV
	Single-ended output high voltage	Vh	avddtmds±10			mV
			avddtmds-200	NA	avddtmds+10	mV
		Vh_data	avddtmds-400	NA	avddtmds+10	mV
		Vh_clock	avddtmds-400	NA	avddtmds+10	mV
	Single-ended output low voltage	Vl	avddtmds-600	NA	avddtmds-400	mV
			avddtmds-700	NA	avddtmds-400	mV
		Vl_data	avddtmds-1000	NA	avddtmds-400	mV
		Vl_clock	avddtmds-1000	NA	avddtmds-200	mV
	Differential source termination load	Rterm	50	NA	200	Ω

3.4 Electrical Characteristics for General IO

Table 3-4 PX5 Electrical Characteristics for Digital General IO

Parameters		Symbol	Test condition	Min	Typ	Max	Units
Digital GPIO @3.3V	Input leakage current	Ii	Vin = 3.3V or 0V	NA	NA	10	uA
	Tri-state output leakage current	Ioz	Vout = 3.3V or 0V	NA	NA	10	uA
	High level input current	Iih	Vin = 3.3V, pulldown disabled	NA	NA	10	uA
			Vin = 3.3V, pulldown enabled	NA	NA	106.4	uA
	Low level input current	Iil	Vin = 0V, pullup disabled	NA	NA	10	uA
			Vin = 0V, pullup enabled	NA	NA	107.8	uA
Digital GPIO @1.8V	Input leakage current	Ii	Vin = 1.8V or 0V	NA	NA	10	uA
	Tri-state output leakage current	Ioz	Vout = 1.8V or 0V	NA	NA	10	uA
	High level input current	Iih	Vin = 1.8V, pulldown disabled	NA	NA	10	uA
			Vin = 1.8V, pulldown enabled	NA	NA	61.3	uA
	Low level input current	Iil	Vin = 0V, pullup disabled	NA	NA	10	uA
			Vin = 0V, pullup enabled	NA	NA	61.4	uA

3.5 Electrical Characteristics for PLL

Table 3-5 PX5 Electrical Characteristics for PLL

Parameters		Symbol	Test condition	Min	Typ	Max	Units
PLL	Divided reference frequency range	Fin		0.269	NA	2200	MHz
	output frequency range	Fout		0.440	N/A	2200	MHz
	Lock time	Tlt		N/A	NA	500	Cycles of divided reference clock
	Power consumption (normal mode)	N/A		N/A	3	N/A	mW
	Period jitter (P-P)	N/A		N/A	NA	+/-2.5	%

Parameters		Symbol	Test condition	Min	Typ	Max	Units
	Junction temperature	N/A			70	125	℃

3.6 Electrical Characteristics for SAR-ADC

Table 3-6 PX5 Electrical Characteristics for SAR-ADC

Parameters	Symbol	Test condition	Min	Typ	Max	Units
ADC resolution			N/A	10	N/A	bits
Conversion speed	Fs	The duty cycle should be between 40%~60%	NA	N/A	1	MSPS
Differential Non Linearity	DNL		N/A	±1	N/A	LSB
Integral Nn Linearity	INL		N/A	±2	N/A	LSB
Gain Error	Egain		-8	N/A	8	LSB
Offset Error	Eoffset		-8	N/A	8	mV
Analog Supply Current(VDDA_SARADC)			N/A	200	N/A	uA
Digital Supply Current			N/A	50	N/A	uA
Power Down Current from AVDD			NA	0.5	NA	uA
Power Down Current from DVDD			N/A	1	N/A	uA
Power up time			N/A	7	N/A	1/Fs

3.7 Electrical Characteristics for TSADC

Table 3-7 PX5 Electrical Characteristics for TSADC

Parameters	Symbol	Test condition	Min	Typ	Max	Units
ADC resolution			N/A	8	N/A	bits
TSADC Accuracy	Fs		NA	N/A	+/-5	℃
Active power			N/A	0.1	N/A	mW
Clock Frequency	Fclk		NA	NA	550	KHz
Power Down Current from DVDD			N/A	1	N/A	uA

3.8 Electrical Characteristics for USB Interface

Table 3-8 PX5 Electrical Characteristics for USB Interface

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Transmitter						
High input level	VIH		NA	1.0	NA	V
Low input level	VIL		NA	0	NA	V
Output resistance	ROUT	Classic mode (Vout = 0 or 3.3V)	40.5	45	49.5	ohms
		HS mode (Vout = 0 to 800mV)	40.5	45	49.5	ohms
Output Capacitance	COUT	seen from D+ or D-			3	pF
Output Common Mode Voltage	VM	Classic (LS/FS) mode	1.45	1.65	1.85	V
		HS mode	0.175	0.2	0.225	V
Differential output signal high	VOH	Classic (LS/FS); Io=0mA	2.97	3.3	3.63	V
		Classic (LS/FS); Io=6mA	2.2	0.3	NA	V
		HS mode; Io=0mA	360	400	440	mV

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Differential output signal low	VOL	Classic (LS/FS); Io=0mA	-0.33	0	0.33	V
		Classic (LS/FS); Io=6mA	NA	0.3	0.8	V
		HS mode; Io=0mA	-40	0	40	mV
Receiver						
Receiver sensitivity	RSENS	Classic mode		+-250		mV
		HS mode		+-25		mV
Receiver common mode	RCM	Classic mode	0.8	1.65	2.5	V
		HS mode (differential and squelch comparator)	0.1	0.2	0.3	V
		HS mode (disconnect comparator)	0.5	0.6	0.7	V
Input capacitance (seen at D+ or D-)			NA	NA	3	pF
Squelch threshold			100	112	150	mV
Disconnect threshold			570	590	625	mV
High output level	VOH		NA	3.3	NA	V
Low output level	VOL		NA	0	NA	V

3.9 Electrical Characteristics for DDR IO

Table 3-9 PX5 Electrical Characteristics for DDR IO

Parameters		Symbol	Test condition	Min	Typ	Max	Units
DDR IO @DDR3 mode	Input leakage current, SSTL mode, unterminated		@ 1.5V , 125℃	NA	0		uA
DDR IO @DDR3L mode	Input leakage current		@ 1.35V , 125℃	NA	0	NA	nA
DDR IO @LPDDR2/LPDDR3 mode	Input leakage current		@ 1.2V , 125℃	NA	0	0.49	nA

3.10 Electrical Characteristics for eFuse

Table 3-10 PX5 Electrical Characteristics for eFuse

	Parameters	Symbol	Test condition	Min	Typ	Max	Units
Active mode	VDD current in Read mode	Iread_vdd	nomal read	15	20	30	mA
	VDD current in PGM mode	Ipgm_vdd	STROBE high	0.5	1	2.5	mA
	VQPS current in PGM mode	Ipgm_vqps	STROBE high	5	10	15	mA
standby mode	VDD current in standby mode	Istandby_vdd	Standby	0.2	0.5	2	A

3.11 Electrical Characteristics for HDMI

Table 3-11 PX5 Electrical Characteristics for HDMI

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Differential output signal rise time	tR	20~80% RL=50Ω	75	NA	0.4UI	ps
	tR_DATA	20~80% RL=50Ω	42.5	NA	NA	ps
	tR_CLOCK	20~80% RL=50Ω	75	NA	NA	ps
Differential output signal fall time	tF	20~80% RL=50Ω	75	NA	NA	ps
	tF_DATA	20~80%	42.5	NA	NA	ps

Parameters	Symbol	Test condition	Min	Typ	Max	Units
		RL=50Ω				
	tF_CLOCK	20~80% RL=50Ω	75	NA	NA	ps

3.12 Electrical Characteristics for MIPI PHY

Table 3-12 PX5 Electrical Characteristics for MIPI PHY

Parameters	Symbol	Test condition	Min	Typ	Max	Units
HS Transmitter AC specifications (MIPI mode)						
Common-mode variations above 450 MHz	ΔVCMTX(HF)		NA	NA	15	mVRMS
Common-mode variations between 50MHz – 450MHz	ΔVCMTX(LF)		NA	NA	25	mVPEAK
20%-80% rise time and fall time	TR and TF		150	NA	NA	ps
HS Receiver AC specifications (MIPI mode)						
Common-mode interference beyond 450 MHz	ΔVCMRX(HF)		NA	NA	100	mV
Common-mode interference	ΔVCMRX(LF)		-50	NA	50	mV
Common-mode termination	CCM		NA	NA	60	pF
HS transmitter AC specification(LVDS)						
Vod fall time 20-80%	Tfall	Rload=100 ohms+1%	100		250	ps
Vod rise time 20-80	Rrise	Rload=100 ohms+1%	100		250	ps
Differential skew	Tskew	Tskew			30	ps
LP receiver AC specifications(only for MIPI mode)						
Input pulse rejection	eSPIKE		NA	NA	300	V.ps
Minimum pulse width response	TMIN-RX		20	NA	NA	ns
Peak interference amplitude	VINT		NA	NA	200	mV
Interference frequency	fINT		450	NA	NA	MHz
LP Transmitter AC Specifications(only for MIPI mode)						
15%-85% rise time and fall time	TRLP/TFLP		NA	NA	25	ns
30%-85% rise time and fall time	TREOT		NA	NA	35	ns
Pulse width of exclusiveOR clock the LP	TLP-PULSE-TX	First LP exclusive-OR clock pulse after Stop state or last pulse before Stop state	40	NA	NA	ns
		All other pulse	20	NA	NA	
Period of the LP exclusive OR clock	TLP-PER-TX		90	NA	NA	ns
Slew rate @ CLOAD=0pF	δV/δtSR		NA	NA	500	mV/ns
Slew rate @ CLOAD=5pF			NA	NA	300	mV/ns
Slew rate @ CLOAD=20pF			NA	NA	250	mV/ns
Slew rate @ CLOAD=70pF			NA	NA	150	mV/ns
Slew rate @ CLOAD= 0 to 70pF(Falling Edge			30	NA	NA	mV/ns

Parameters	Symbol	Test condition	Min	Typ	Max	Units
HS Transmitter AC specifications (MIPI mode)						
Only)						
Slew rate @ CLOAD= 0 to 70pF(Rising Edge Only)			30	NA	NA	mV/ns
Slew rate @ CLOAD= 0 to 70pF(Rising Edge Only)			30-0.075 * (VO,INST – 700)	NA	NA	mV/ns
Load capacitance	CLOAD		0	NA	70	pF
CMOS Transmitter DC Specifications(CMOS mode)						
Maximum data rate	DMAX		NA	200	NA	Mbit/s
15%-85% rise time and fall time	TRLP/TFLP		1	1.5	2	Ns
Slew rate, transition region	SR		20	27	30	V/ns

Chapter 4 Thermal Management

4.1 Overview

For reliability and operability concerns, the absolute maximum junction temperature of PX5 has to be below 125℃.

4.2 Package Thermal Characteristics

Table 4-1 provides the thermal resistance characteristics for the package used on PX5. The resulting simulation data for reference only, please prevail in kind test.

Table 4-1 PX5 Thermal Resistance Characteristics

Package (TFBGA)	Power(W)	$\theta_{JA}(℃/W)$	$\theta_{JB}(℃/W)$	$\theta_{JC}(℃/W)$
PX5	4.5	14.595	6.70	3.683

Note: The testing PCB is based on 6 layers, 107x105 mm, 1 mm Thickness, ambient temperature is 25℃,