

Version : <u>1.6</u>

TECHNICAL SPECIFICATION

MODEL NO.: PW065XS1

Customer's Confirmation			
Customer	-		
Date			
Ву			
		☐PVI's Confirmat	
		Confirmed By	PRE
			黄山谷

Date: Apr. 12, 2005

This technical specification is subject to change without notice. Please return 1 copy with your signature on this page for approval.



TECHNICAL SPECIFICATION <u>CONTENTS</u>

NO.	ITEM	PAGE
ı	Cover	1
-	Contents	2
1	Application	3
2	Features	3
3	Mechanical Specifications	3
4	Mechanical Drawing of TFT-LCD module	4
5	Input / Output Terminals	5
6	Pixel Arrangement and input connector pin NO.	6
7	Absolute Maximum Ratings	7
8	Electrical Characteristics	7
9	Power Sequence	17
10	Optical Characteristics	17
11	Handling Cautions	21
12	Reliability Test	22
13	Block Diagram	23
14	Packing	24
-	Revision History	25



1. Application

This technical specification applies to 6.5" color TFT-LCD module, PW065XS1. The applications of the panel are car TV, portable DVD, GPS, multimedia applications and others AV system.

2. Features

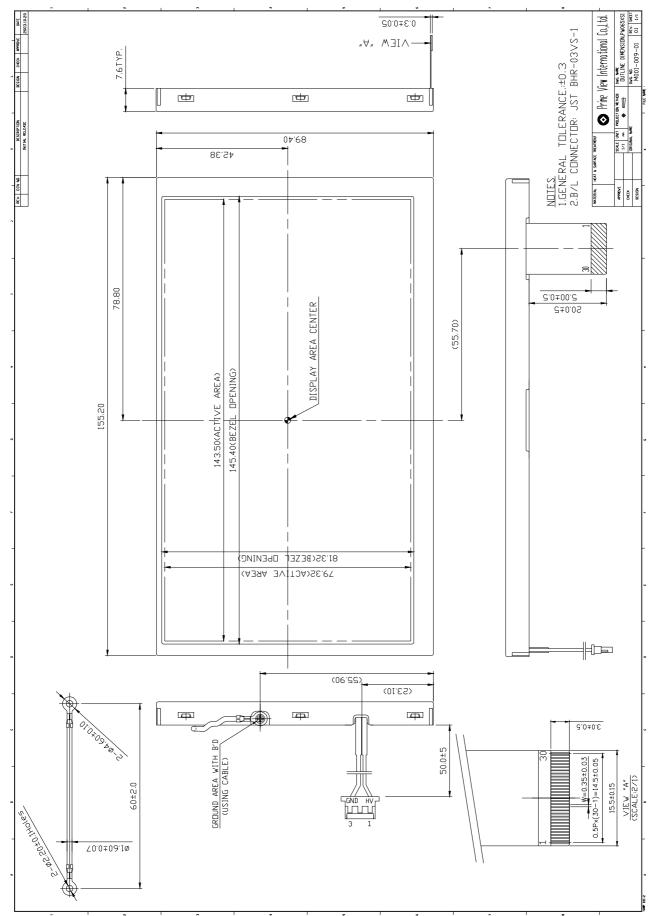
- . Pixel in stripe configuration
- . Compatible with NTSC and PAL system
- . Slim and compact
- . High Brightness
- . Up / Down and Left / Right Image Reversion
- . Wide Viewing Angle
- . Support Multi Video Display Mode (With PVI timing controller : PVI-1004D)

3. Mechanical Specifications

Parameter	Specifications	Unit
Screen Size	6.5 (16:9 diagonal)	Inch
Display Format	1200 (H) ×234(V)	Dot
Active Area	143.40 (H)×79.32 (V)	Mm
Dot Pitch	0.119 (H)×0.345 (V)	Mm
Pixel Configuration	Stripe	
Outline Dimension	155.0 (W)×89.2 (H)×7.6 (D) (typ.)	mm
Surface Treatment	Anti-Glare+WV film	
Weight	164±3	g



4. Mechanical Drawing of TFT-LCD Module





5. Input / Output Terminals

LCD Module Connector

FPCDown Connect, 30 Pins, Pitch: 0.5 mm

Pin No	Symbol	I/O	Description	Remark
1	GND	-	Ground for logic circuit	
2	V_{CC}	I	Supply voltage of logic control circuit for gate driver	Note 5-3
3	NC	1	No connection	
4	V_{EE}	I	Negative power for gate driver	Note 5-4
5	NC	-	No connection	
6	V_{GH}	I	Positive power for gate driver	Note 5-5
7	NC	1	No connection	
8	STVD	I/O	Vertical start pulse	Note 5-1
9	STVU	I/O	Vertical start pulse	14010 5-1
10	CKV	ı	Shift clock for gate driver	
11	U/D	I	Up / Down Control for gate driver	Note 5-1
12	OE3	I	Output enable for gate driver	
13	OE2	I	Output enable for gate driver	
14	OE1	I	Output enable for gate driver	
15	V_{COM}	I	Common electrode voltage	
16	STHL	I/O	Start pulse for source driver	Note 5-2
17	V_{SS2}	-	Ground for analog circuit	
18	V_R	I	Video Input R	
19	V_{G}	I	Video Input G	
20	V_{B}	I	Video Input B	
21	V_{SS1}	1	Ground for digital circuit	
22	V_{DD2}	Ι	Supply power for analog circuit	Note 5-6
23	CPH1	Ι	Sampling and shift clock for source driver	
24	CPH2	Ι	Sampling and shift clock for source driver	
25	CPH3	Ι	Sampling and shift clock for source driver	
26	V_{DD1}	ı	Supply power for digital circuit	Note 5-7
27	R/L	ı	Left / Right Control for source driver	Note 5-2
28	NC	ı	No Connection	
29	OEH	ı	Output enable for source driver	
30	STHR	I/O	Start pulse for source driver	Note 5-2

Note 5-1

U/D	STVD	STVU	scanning direction
Vcc	Input	output	down to up
GND	Output	input	up to down

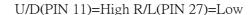
Note 5-2

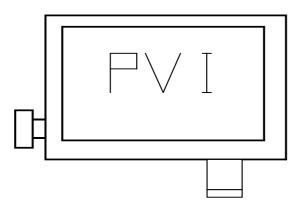
R/L	STHL	STHR	scanning direction
Vcc	output	input	left to right
GND	input	output	right to left

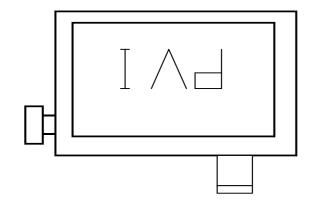


The definitions of Note 5-1,5-2

U/D(PIN 11)=Low R/L(PIN 27)=High







Note 5-3: V_{CC} TYP. = +3.3V

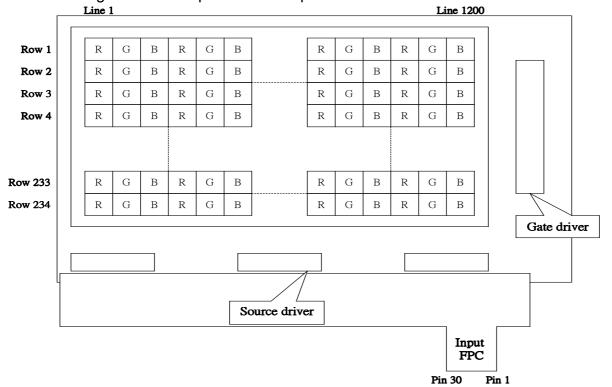
Note 5-4 : V_{EE} TYP. = -12V

Note 5-5: V_{GH} TYP.=+17V

Note 5-6 : V_{DD2} TYP.=+5V

Note 5-7: V_{DD1} TYP.=+3.3V

6. Pixel Arrangement and input connector pin NO.





7. Absolute Maximum Ratings

The followings are maximum values , which if exceeded, may cause faulty operation or damage to the unit.

Parameter		Symbol	MIN.	MAX.	Unit	Remark
Supply Voltage For Source Driver		V_{DD2}	-0.3	+5.8	V	
Supply vollage For Source Drive	1	V_{DD1}	-0.3	+7.0	V	
		V_{CC}	-0.3	+6.0	V	
Supply Voltage For Gate Driver		V_{GH} - V_{EE}	-0.3	+40.0	V	
	H Level	V_{GH}	-0.3	+25.0	V	
	L Level	V_{EE}	-16	+0.3	V	
Analog Signal Input Level		V_R, V_G, V_B	-0.2	V _{DD1} +0.2	V	Note 7-1
Storage Temperature			-40	+95	$^{\circ}\!\mathbb{C}$	
Operation Temperature			-30	+85	$^{\circ}\!\mathbb{C}$	Note 7-2

Notes 7-1: Analog Input Voltage means V_R,V_G,V_B.

Notes 7-2 : Optical characteristics shown in Table 10-1 are measured under Ta=+25℃.

8. Electrical Characteristics

8-1) Recommended Driving condition for TFT-LCD panel

Parameter		Symbol	MIN.	Тур.	MAX.	Unit	Remark
Supply Voltage For Source	Analog	V_{DD2}	+4.5	+5.0	+5.5	V	
Driver	Logic	V_{DD1}	+3.0	+3.3	+3.6	V	
	H level	V_{GH}	+15	+17	+19	V	
Supply Voltage For Cate Driver	L level	V _{EE DC}	-13.0	-12	-10.5	V	DC Component of V _{EE}
Supply Voltage For Gate Driver		V _{EE AC}		+6.0		V_{P-P}	AC Component of V_{EE}
	Logic	V_{CC}	+3.0	+3.3	+3.6	>	
Analog Signal input Level	Amplitud		+0.3		Vcc-0.3	V	
Digital input voltage	H level	V_{IH}	0.7 V _{DD1}	-	V _{DD1}	V	
Digital input voltage	L level	V_{IL}	-0.3	-	0.3 V _{DD1}	V	
Digital output voltage	H level	V_{OH}	0.7 V _{DD1}	-	V _{DD1}	V	
Digital output voltage	L level	V_{OL}	-0.3	-	0.3 V _{DD1}	٧	
V	V _{COM AC}	-	+6.0	-	V_{P-P}	AC Component of V _{COM}	
V _{COM}	V _{COM DC}	1.3	1.5	1.7	V	DC Component of V _{COM} Note 8-1	

Note 8-1 : PVI strongly suggests that the $V_{\text{COM DC}}$ level shall be adjustable , and the adjustable level range is $1.5V\pm1V$, every module's $V_{\text{COM DC}}$ level shall be carefully adjusted to show a best image performance.



8-2) Recommended driving condition for back light

Ta= 25 ℃

Parameter	Symbol	Min.	Тур.	Max.	Unit	Remark
Lamp voltage	V_L	500	550	600	Vrms	I∟=6mA
Lamp current	Iι	3	6	8	mA	Note 8-2
Lamp frequency	PL	30	43	80	KHz	Note 8-3
Kick-off voltage(25 [°] C) (Reference Value)	Vs	-	720	830	Vrms	Note 8-4
Kick-off voltage(0°) (Reference Value)	VS	-	910	1100	Vrms	11016 0-4

Note 8-2: In order to satisfy the quality of B/L, no matter use what kind of inverter, the output lamp current must between Min. and Max. to avoid the abnormal display image caused by B/L.

Note 8-3: The waveform of lamp driving voltage should be as closed to a perfect sine wave as possible.

Note 8-4 : The Kick-off times ≥ 1sec.

Back Light driving

Back Light Connector: JST BHR-03VS-1, Pin No.: 3, Pitch: 4 mm

Pin No	Symbol	Description	Remark
1	VL1	Input terminal (Hi voltage side)	
2	NC	No Connection	
3	VL2	Input terminal (Low voltage side)	Note 8-5

Note 8-5: Low voltage side of back light inverter connects with Ground of inverter circuits.

8-3) Power Consumption

Ta= 25 °C

Parameter	Symbol	Conditions	TYP.	MAX	Unit	Remark
Supply current for Gate Driver (Hi level)	I_{GH}	$V_{GH} = +17V$	0.76	1.35	mA	
Supply current for Gate Driver (Low level)	I _{EE}	$V_{EE} = -12V$	1.02	1.53	mA	V _{EE} center voltage
Supply current for Source Driver(Digital)	I _{DD1}	$V_{DD1} = +3.3V$	1.5	5.0	mA	
Supply current for Source Driver(Analog)	I_{DD2}	$V_{DD2} = +5V$	19.9	22.5	mA	
Supply current for Gate Driver (Digital)	I _{CC}	$V_{CC} = +3.3V$	0.036	0.075	mA	
LCD Panel Power Consumption			129.73	170.56	mW	Note 8-6
Back Light Lamp Power Consumption			3.30		W	Note 8-7

Note 8-6: The power consumption for back light is not included.

Note 8-7: Back light lamp power consumption is calculated by I₁×V₁.



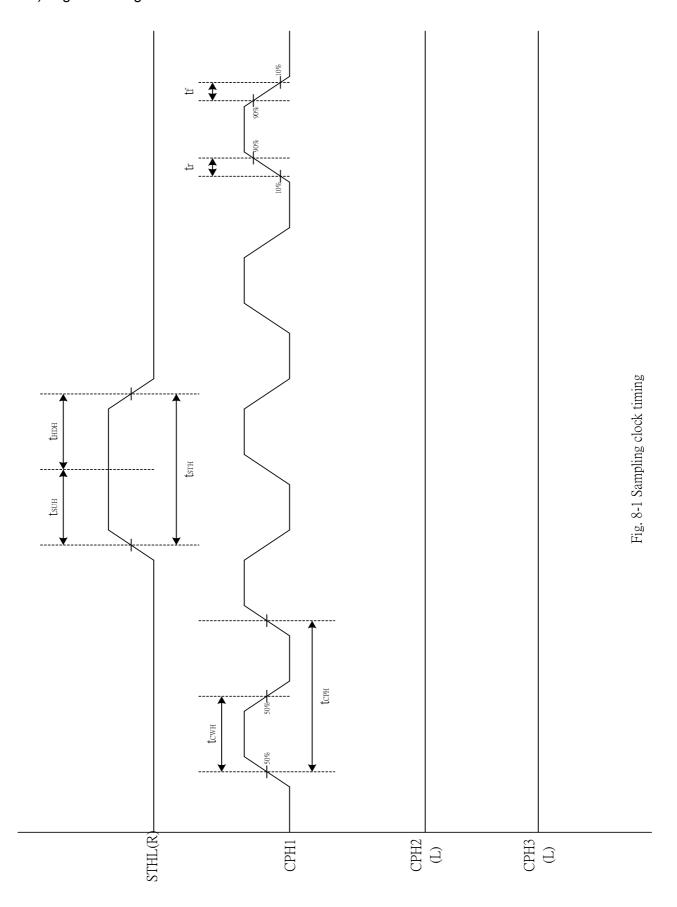


8-4) Timing Characteristics Of Input Signals

Characteristics	Symbol	Min.	Тур.	Max.	Unit	Remark
Rising time	$t_{\rm r}$	-	-	10	ns	
Falling time	$t_{\rm f}$	-	-	10	ns	
High and low level pulse width	t_{CPH}	120	125	130	ns	СРН1~СРН3
CPH pulse duty	t_{CWH}	40	50	60	%	СРН1~СРН3
STH setup time	$t_{ m SUH}$	20	-	-	ns	STHR,STHL
STH hold time	$t_{ m HDH}$	20	-	-	ns	STHR,STHL
STH pulse width	$t_{ m STH}$	-	1	-	t_{CPH}	STHR,STHL
STH period	$t_{\rm H}$	61.5	63.5	65.5	μ s	STHR,STHL
OEH pulse width	$t_{ m OEH}$	-	1.22	-	μs	OEH
Sample and hold disable time	$t_{ m DIS1}$		8.28	-	μ s	
OEV pulse width	t_{OEV}	-	10.8	-	μ s	OEV
CKV pulse width	t_{CKV}	-	32	-	μ s	CKV
Clean enable time	$t_{ m DIS2}$	-	5.4	-	μ s	
Horizontal display start	$t_{ m SH}$	-	0	-	$t_{CPH}/3$	
Horizontal display timing range	$t_{ m DH}$	-	1200	-	$t_{CPH}/3$	
STV setup time	$t_{ m SUV}$	400	-	-	ns	STVU,STVD
STV hold time	$t_{ m HDV}$	400	-	-	ns	STVU,STVD
STV pulse width	t_{STV}	-	-	1	t_{H}	STVU,STVD
Horizontal lines per field	$t_{\rm V}$	256	262	268	t_{H}	
Vertical display start	$t_{ m SV}$		3	-	t_{H}	
Vertical display timing range	$t_{ m DV}$		234	-	t_{H}	
VCOM rising time	t_{rCOM}		-	5	μ s	
VCOM falling time	$t_{ m fCOM}$		-	5	μ s	
VCOM delay time	t_{DCOM}		-	3	μ s	
RGB delay time	t_{DRGB}		-	1	μ s	



8-5) Signal Timing Waveforms



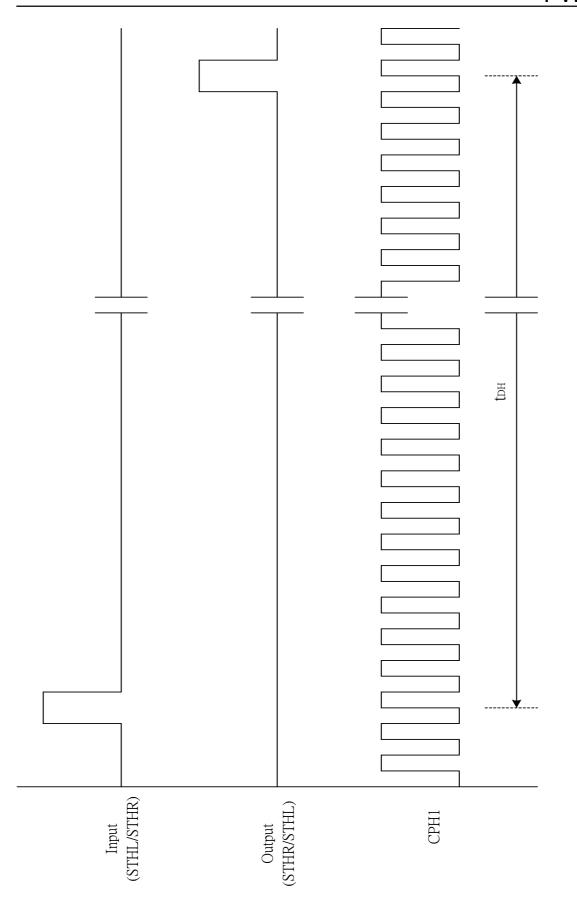
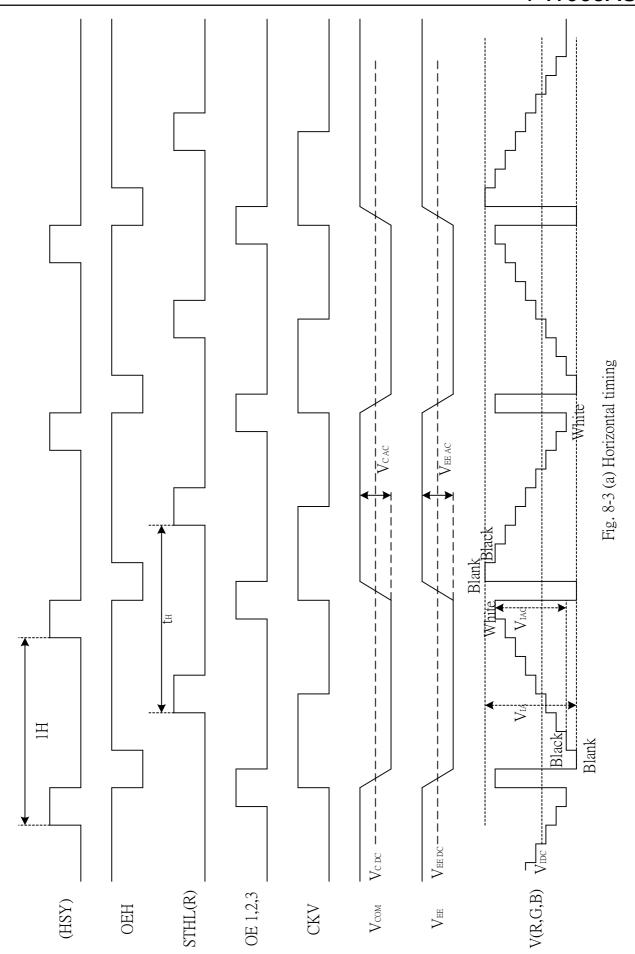
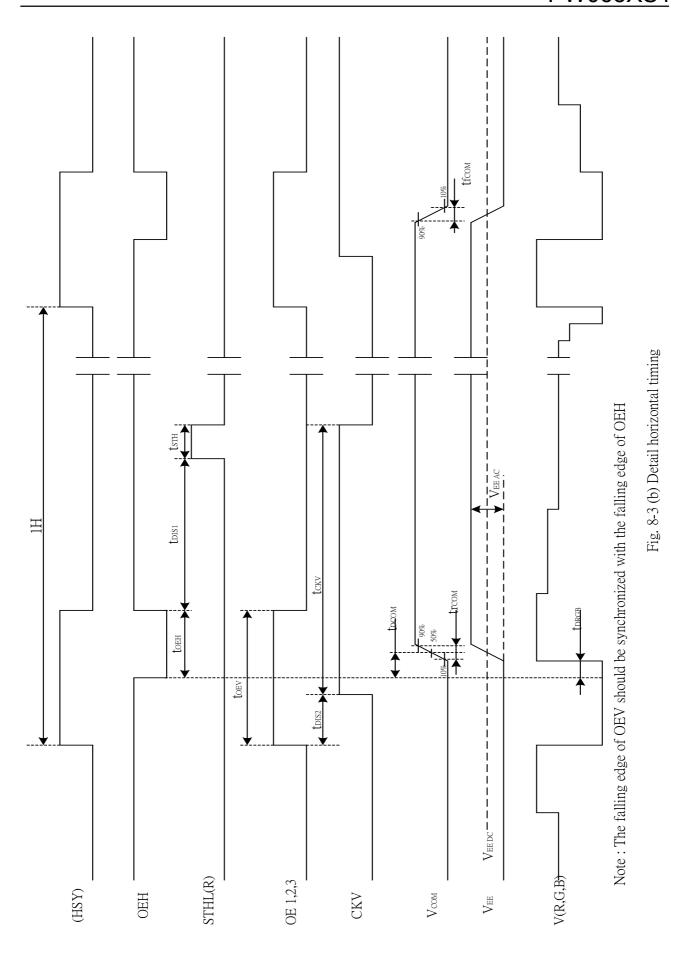


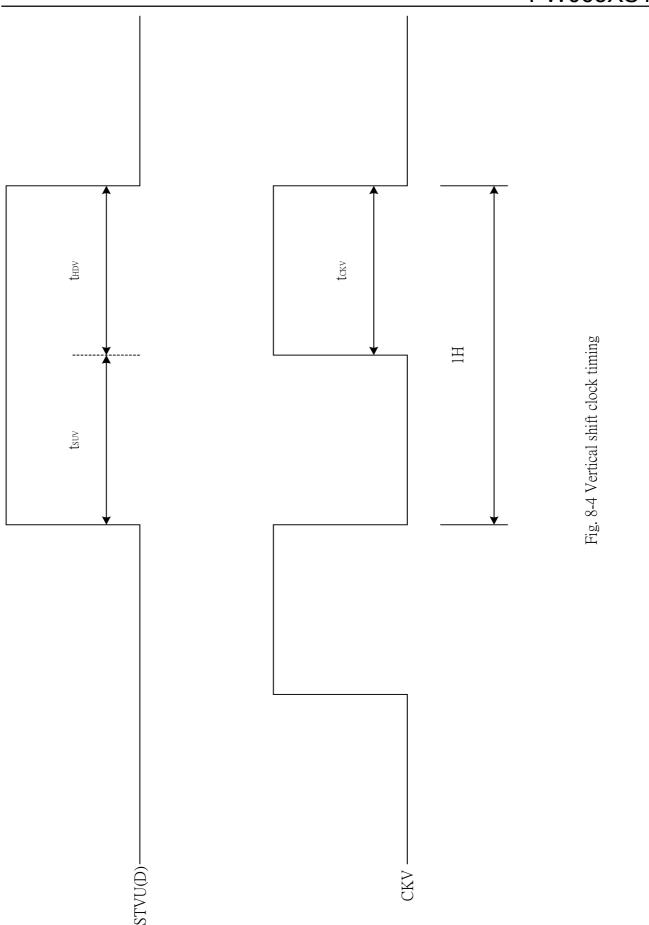
Fig. 8-2 Horizontal display timing range





The information contained herein is the exclusive property of Prime View International Co., Ltd. and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of Prime View International Co., Ltd.

PAGE:13

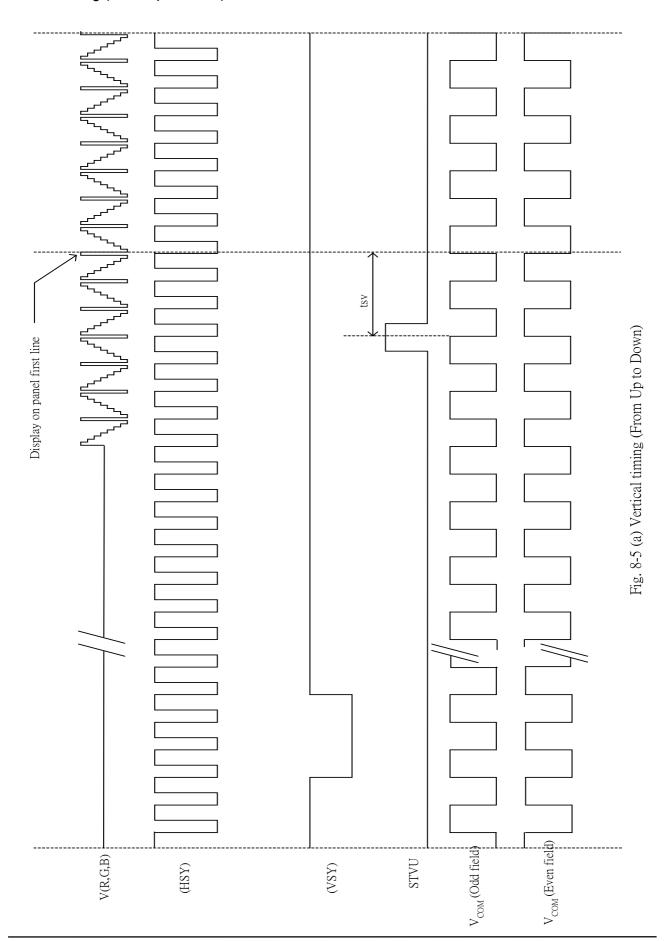


The information contained herein is the exclusive property of Prime View International Co., Ltd. and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of Prime View International Co., Ltd.

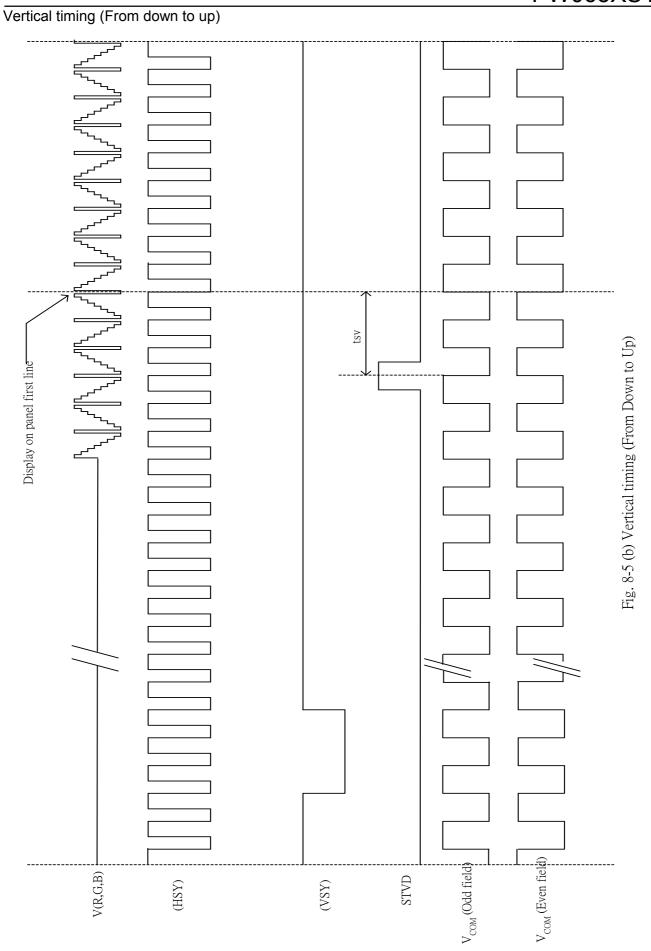
PAGE:14



Vertical timing (From up to down)



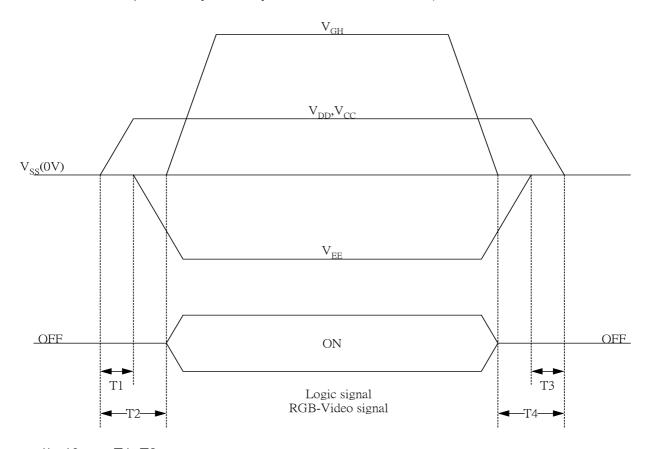






9. Power on Sequence

The Power on Sequence only effect by $V_{\text{CC}}, V_{\text{SS}}, V_{\text{DD}}, V_{\text{EE}}$ and $V_{\text{GH},}$ the others do not care.



- 1) 10ms≦T1<T2
- 2) 0ms<T3≦T4≦10ms

10. Optical Characteristics

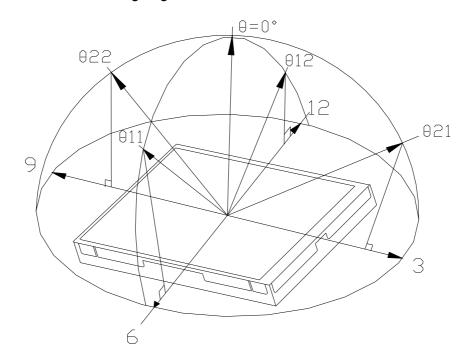
10-1) Specification

Ta = 25[°]C

Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit	Remarks
Viewing	Horizontal	θ 21, θ 22		55	60		deg	
Angle	Vertical	θ 12	CR≧10	35	40		deg	Note 10-1
		θ 11		50	55		deg	
Contrast Ratio		CR	At optimized Viewing angle	200	350			Note 10-2
Response time	Rise	Tr	$\theta = 0^{\circ}$		15	30	ms	Note 10-4
	Fall	Tf	0 -0		25	50	ms	
Brightness				350	400		cd/m²	Note 103
Uniformity		U		70	75		%	Note 10-5
White		Х	$\theta = 0^{\circ}$	0.283	0.313	0.343		Note 10-3
Chromaticity		у	0 -0	0.299	0.329	0.359		
Lamp Life Time +25℃				20000	30000		hr	



Note 10-1: The definitions of viewing angles

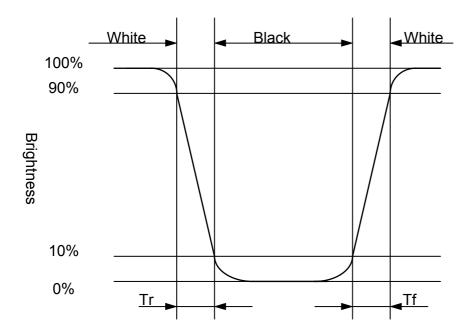


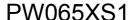
Note 10-2 : CR = Luminance when Testing point is White Luminance when Testing point is Black (Testing configuration see 10-2)
Contrast Ratio is measured in optimum common electrode voltage.

Note 10-3 : 1.Topcon BM-7(fast) luminance meter 1° field of view is used in the testing (after 20~30 minutes operation).

2.Lamp current : 6 mA 3.Inverter model : TDK-347.

Note 10-4: The definition of response time:







Note 10-5: The uniformity of LCD is defined as

U = The Minimum Brightness of the 9 testing Points
The Maximum Brightness of the 9 testing Points

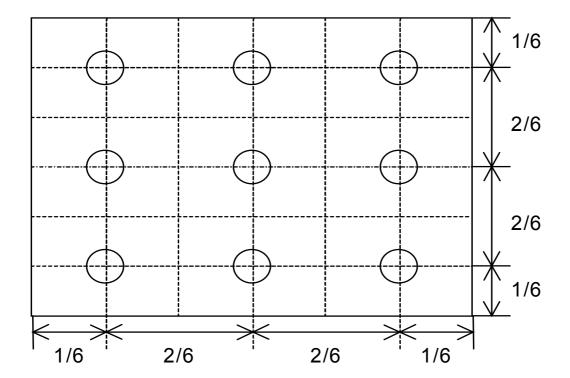
Luminance meter : BM-5A or BM-7 fast (TOPCON)

Measurement distance: 500 mm +/- 50 mm

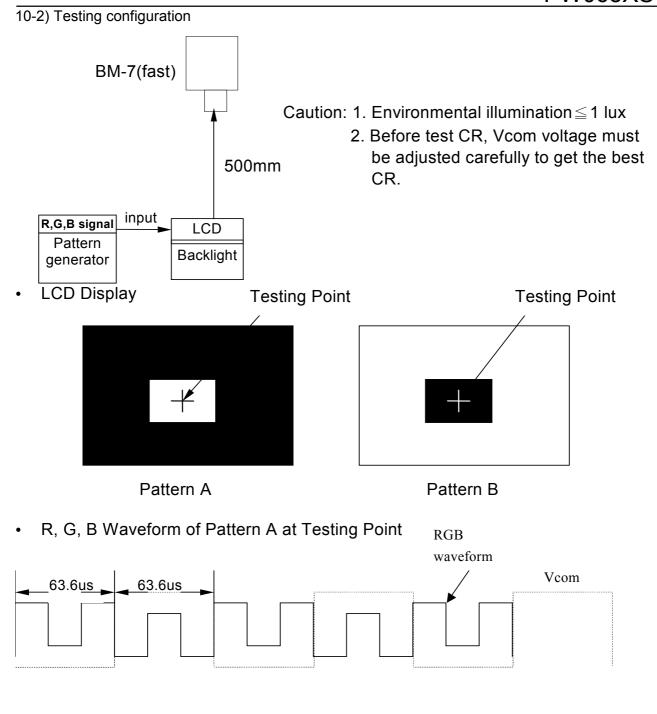
Ambient illumination : < 1 Lux

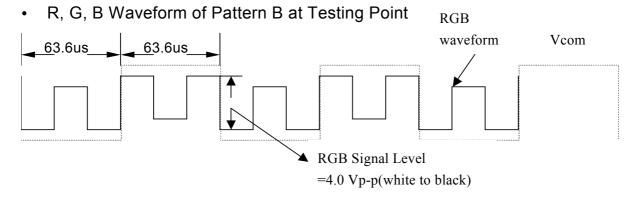
Measuring direction: Perpendicular to the surface of module

The test pattern is white (Gray Level 63).











11. Handling Cautions

11-1) Mounting of module

- 1. Please power off the module when you connect the input/output connector.
- b) Please connect the ground pattern of the inverter circuit surely. If the connection is not perfect, some following problems may happen possibly.
- 1. The noise from the backlight unit will increase.
- 2. The output from inverter circuit will be unstable.
- 1. In some cases a part of module will heat.
- c) Polarizer which is made of soft material and susceptible to flaw must be handled carefully.
- d) Protective film (Laminator) is applied on surface to protect it against scratches and dirt. It is recommended to peel off the laminator before use and taking care of static electricity.

11-2) Precautions in mounting

- 1. When metal part of the TFT-LCD module (shielding lid and rear case) is soiled, wipe it with soft dry cloth.
- b) Wipe off water drops or finger grease immediately. Long contact with water may cause discoloration or spots.
- c) TFT-LCD module uses glass which breaks or cracks easily if dropped or bumped on hard surface. Please handle with care.
- d) Since CMOS LSI is used in the module. So take care of static electricity and earth yourself when handling.

11-3) Others

- 1. Do not expose the module to direct sunlight or intensive ultraviolet rays for many hours.
- b) Store the module at a room temperature place.
- c) The voltage of beginning electric discharge may over the normal voltage because of leakage current from approach conductor by to draw lump read lead line around.
- d) If LCD panel breaks, it is possibly that the liquid crystal escapes from the panel. Avoid putting it into eyes or mouth. When liquid crystal sticks on hands, clothes or feet. Wash it out immediately with soap.
- e) Observe all other precautionary requirements in handling general electronic components.

11-4) Polarizer mark

The polarizer mark is to describe the direction of wide view angle film how to mach up with the rubbing direction.



12. Reliability Test

No.	Test Item	Test Condition		
1	High Temperature Storage Test	Ta = +95°ℂ, 240 hrs		
2	Low Temperature Storage Test	Ta = -40℃, 240 hrs		
3	High Temperature Operation Test	Ta = +85°ℂ, 240 hrs		
4	Low Temperature Operation Test	Ta = -30℃, 240 hrs (Note 12-1)		
5	High Temperature & High Humidity Operation Test	Ta = +60℃, 90%RH , 240 hrs		
6	Thermal Cycling Test	-30°C → +80°C , 200 Cycles		
0	(non-operating)	30 min 30 min		
7	\ -	Frequency : 10 ~ 55 H _z		
	Vibration Test	Amplitude : 1 mm		
	(non-operating)	Sweep time : 11 mins		
		Test Period: 6 Cycles for each direction of X, Y, Z		
8	Shock Test	100G , 6ms		
	(non-operating)	Direction: ±X, ±Y, ±Z		
	(non-operating)	Cycle: 3 times		
9	E	200pF, 0Ω		
	Electrostatic Discharge Test	±200V		
	(non-operating)	1 time / each terminal		

Ta: ambient temperature

Note : PVI guarantee the module can power on under −30°C

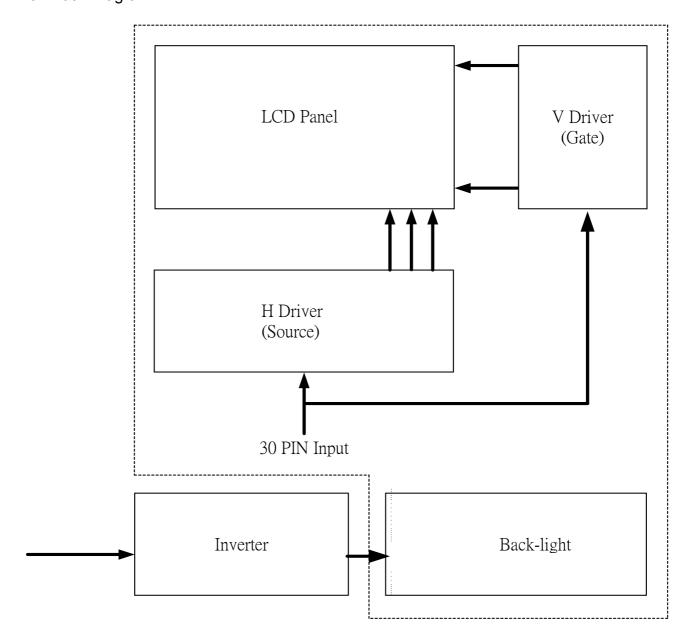
Note: The protective film must be removed before temperature test.

[Criteria]

Under the display quality test conditions with normal operation state, there should be no change which may affect practical display function.

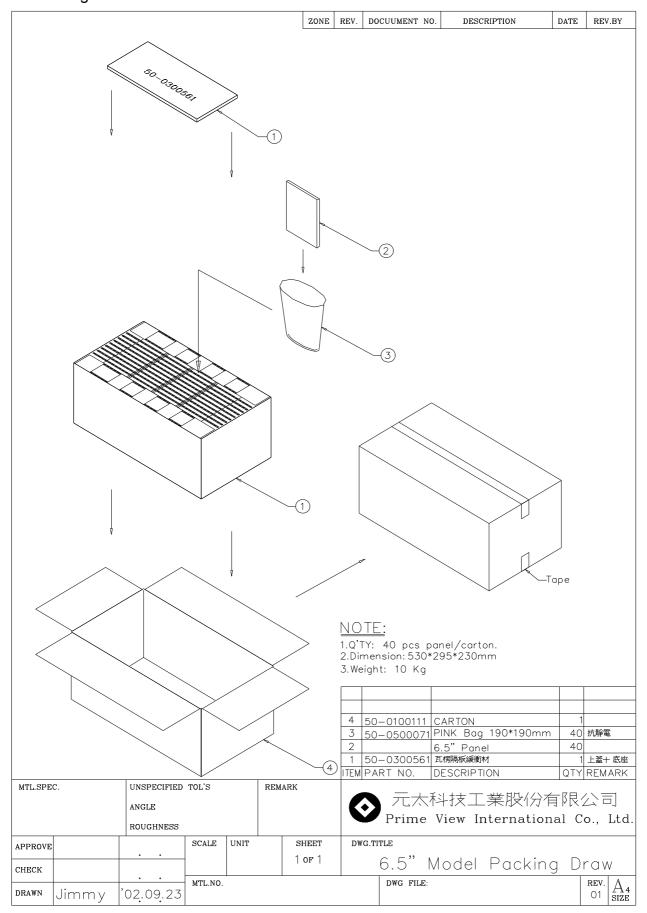


13. Block Diagram





14. Packing





Revision History

Rev.	Rev. Issued Date Revised Contents					
0.1	Oct. 30, 2001	NEW Contents				
0.1						
0.2	Mar. 05, 2002	Modify Page 17: Power on seguence				
		Page 17: Power on sequence Page 19: Note 10-5: The uniformity of LCD testing points defined				
		Page 22 : Reliability test condition				
0.3	Mar. 14, 2002	Modify				
0.5	Wai. 14, 2002	Page 8 : Power Consumption				
0.4	Apr. 12, 2002	Modify				
	- F ,,	Page 4 : Mechanical Drawing of TFT-LCD Module				
0.5	Jul. 12, 2002	Modify				
		Page 6: Pixel Arrangement and input connector pin NO.				
		Page 8 : Power Consumption				
		Page 10 : Signal Timing Waveforms				
		Pge 17: Optical Characteristics				
0.6	Aug. 21, 2002	Modify				
		Page 22 : Reliability Test (About High Temperature test)				
0.7	Sep. 16, 2002	Modify				
		Page 5: Note description				
0.0	G 26 2002	Page 7: Recommended Driving condition for TFT-LCD panel				
8.0	Sep. 26, 2002	Modify Page 23 : Packing				
1.0	Nov. 04, 2002	Modify				
1.0	1107.04,2002	Page 3 : Mechanical Specifications				
		Page 4 : Mechanical Drawing of TFT-LCD Module (FPC length)				
		Page 8: Power Consumption				
1.1	Mar. 27, 2003	Modify				
		Page 8: Power Consumption (From 79.83mW to 109.76mW Typ.)				
		(From 98.54mW to 134.14mW Max.)				
1.2	Aug. 29, 2003	Modify				
		Page 4: Mechanical Drawing of TFT-LCD Module				
1.3	Sep. 19, 2003	Modify				
		Page 8: Power Consumption (From 109.76mW to 132.34mW Typ.)				
1.4	Nov. 25, 2003	(From 134.14mW to 179.19mW Max.) Modify				
1.4	100. 23, 2003	Page 17 : Optical Characteristics (contrast ratio from 110 to 200 Min.)				
		(contrast ratio from 150 to 350 Typ.)				
1.5	Jan. 11, 2005					
	,	Removed				
		Page 22 : Indication of Lot Number Label				
		Add				
		Page 22 : Reliability				
		(Note: The protective film must be removed before temperature test.)				
		(· · · · · · · · · · · · · · · · · · ·				
1.6	Apr. 12, 2005	Modify:				
		Page 04: Mechanical Drawing of TFT-LCD Module(GND line).				
		, ,				
		Page 06: Note 5-3 : V _{CC} TYP.=+3.3V				
		Note 5-7: V _{DD1} TYP.=+3.3V				
		Page 07: 8-1) Recommended Driving condition for TFT-LCD panel				
		1 VDD1 , VCC Typ. 5V to 3.3V ; Max. 5.5V to 3.6V ; Min 4.5V to 3.0V.				
		1, VDD1, VOO 1 yp. OV to 0.0 V, Wan. 0.0 V to 0.0 V, Will 7.0 V to 0.0 V.				



PW065XS1

	2 Power Consumption Typ. 132.34mW to 129.73mW; Max 179.19mW to 170.56mW
	Page 22: Reliability Test condition change to Car application SPEC.