Version : 0.1

Preliminary

TECHNICAL SPECIFICATION

MODEL NO : PW035XS4

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Please contact PVI or its agent for further information.

☐ Customer's Confirmation

Customer ____________________

Date ____________________

By ____________________

☐ PVI's Confirmation

Dep	FAE	Panel Design	Electronic Design	Mechanical Design	Product Verification	Prepared by
SIGN						

TECHNICAL SPECIFICATION

CONTENTS

1. Application

This technical specification applies to 3.5" color TFT-LCD module , PW035XS4.

The applications of the panel are car TV, portable DVD, DV,GPS, multimedia applications and other AV systems..

2. Features

. Amorphous silicon TFT-LCD panel with LED Backlight unit.

. Compatible with NTSC & PAL system

. Pixel in stripe configuration

. Slim and compact

. Image Reversion : Up/Down and Left/Right

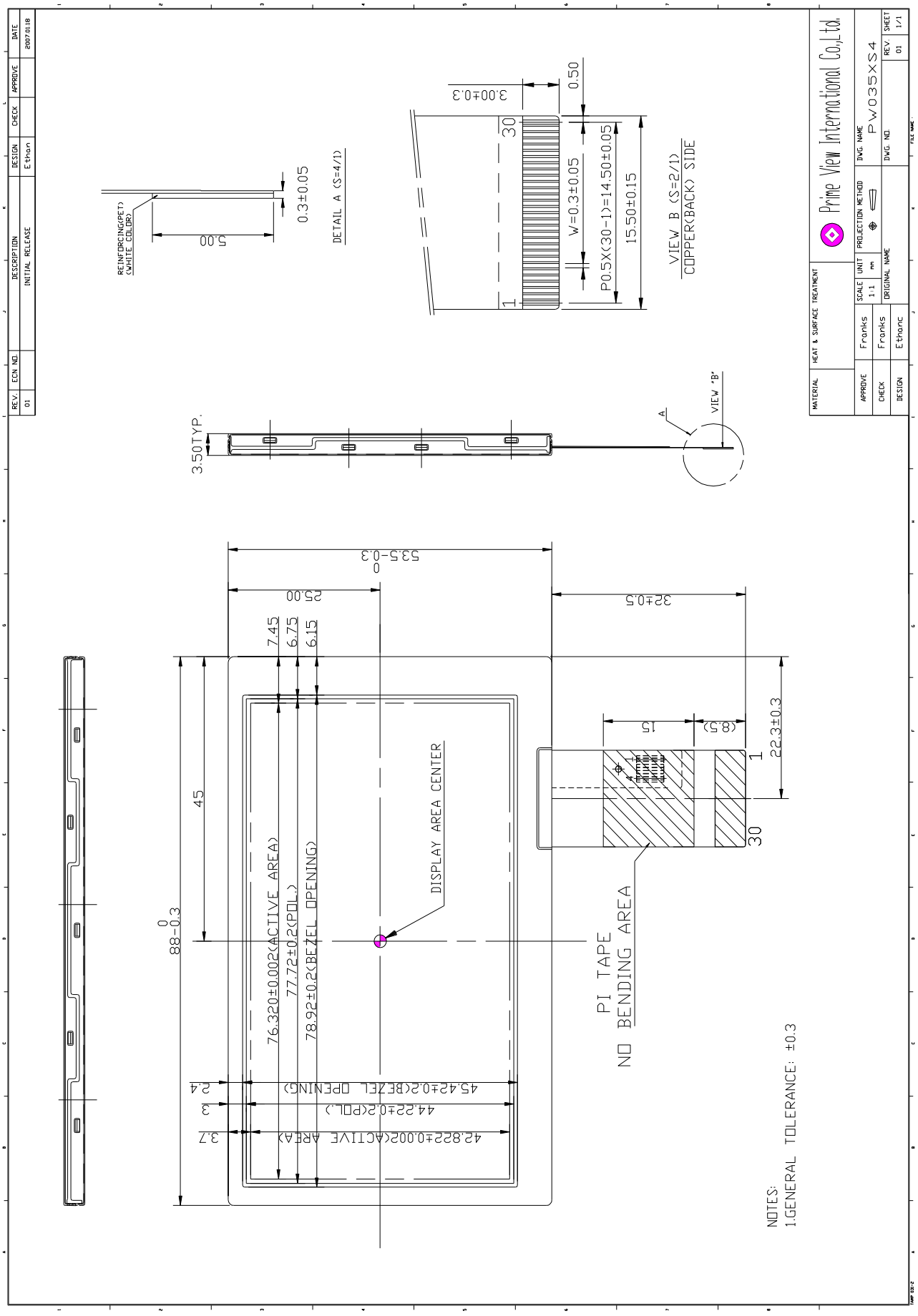
. Support multi display mode
(If you use this mode ,you must use PVI-1004D's timing controller (made by PVI))

.Wide viewing angle

3. Mechanical Specifications

Parameter	**Specifications**	**Unit**
Screen Size	3.5 (16:9 diagonal)	inch
Display Format	320×(RGB)×234	dot
Active Area	76.32(H)×42.822(V)	mm
Pixel Pitch	0.2385(H)×0.183 (V)	mm
Pixel Configuration	Stripe	
Outline Dimension	88(W) × 53.5(H) × 3.5(D)(typ.)	mm
Weight	34±5	g
Back-light	6-LED	
Surface Treatment	Anti – Glare	
Display model	Normally white	
Gray scale inversion direction	6 o'clock [ref to Page 20 viewing angle]	

4. Mechanical Drawing of TFT-LCD Module



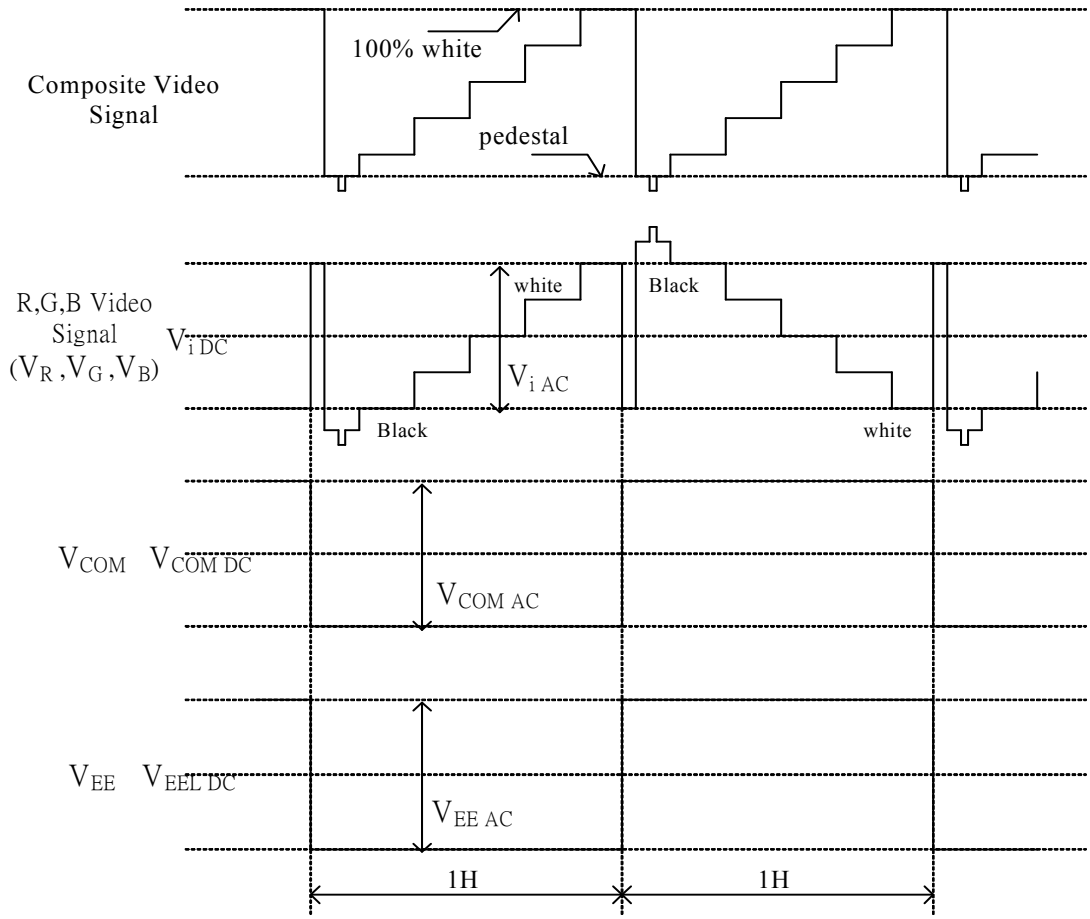
5. Input / Output Terminals

TFT-LCD Module Connector
FPC Down Connect , 30Pins , Pitch : 0.5 mm

Pin No	Symbol	I/O	Description	Remark
1	GLED1	I	Ground for LED backlight	
2	VLED1	I	Supply voltage of LED backlight	Note 5-7
3	GLED2	I	Ground for LED backlight	
4	VLED2	I	Supply voltage of LED backlight	Note 5-7
5	GND	-	Ground for logic circuit	
6	V_{CC}	I	Supply voltage of logic control circuit for gate driver	Note 5-2
7	V_{EE}	I	Negative power for gate driver	Note 5-3
8	V_{GH}	I	Positive power for gate driver	Note 5-4
9	STVD	I/O	Vertical start pulse	Note 5-8
10	STVU	I/O	Vertical start pulse	
11	CKV	I	Shift clock for gate driver	
12	U/D	I	Up / Down control for gate driver	Note 5-8
13	OE3	I	Output enable for gate driver	
14	OE2	I	Output enable for gate driver	
15	OE1	I	Output enable for gate driver	
16	V_{COM}	I	Common electrode voltage	Note 5-1
17	STHL	I/O	Start pulse for source driver	Note 5-8
18	V_{SS2}	-	Ground for analog circuit	
19	V_R	I	Video Input R	
20	V_G	I	Video Input G	
21	V_B	I	Video Input B	
22	V_{SS1}	-	Ground for digital circuit	
23	V_{DD2}	I	Supply power of analog circuit	Note 5-5
24	CPH1	I	Sampling and shift clock for source driver	
25	CPH2	I	Sampling and shift clock for source driver	
26	CPH3	I	Sampling and shift clock for source driver	
27	V_{DD1}	I	Supply power for digital circuit	Note 5-6
28	R/L	I	Left / Right control for source driver	Note 5-8
29	OEH	I	Output enable for source driver	
30	STHR	I/O	Start pulse for source driver	Note 5-8

Note5-1: V_{COM} (Typ.)= 6.0 V_{PP}.

Phase of the video signal input and V_{COM}
The relation between these values could refer to 8-1 Operating condition



Liquid crystal transmission of the video signal input , V_{COM} and timing

	V_{COM}	
	H Level	L Level
Video Signal Input Maximum	Black	White
Video Signal Input Minimum	White	Black

White : maximum transmission / Black : minimum transmission

Note 5-2 : V_{CC} TYP.＝+3.3V

Note 5-3 : V_{EE} TYP.＝-12V

Note 5-4 : V_{GH} TYP.＝+17V

Note 5-5 : V_{DD2} TYP.＝+5V

Note 5-6 : V_{DD1} TYP.＝+3.3V

Note 5-7 : I_{LED1} , I_{LED2} TYP.=20 mA

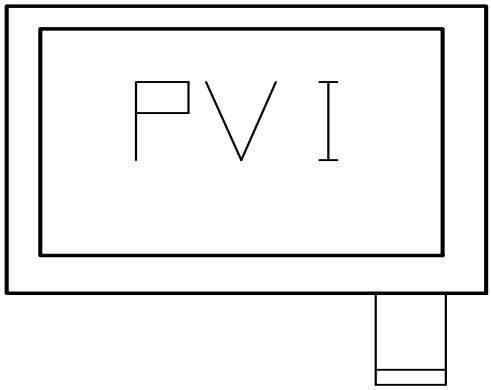
Note 5-8: STHL,STHR and R/L mode

R/L	STHL	STHR	Remark
High(V_{DD1})	Output	Iinput	Left to Right
Low(0 Volt.)	Iinput	Output	Right to Left

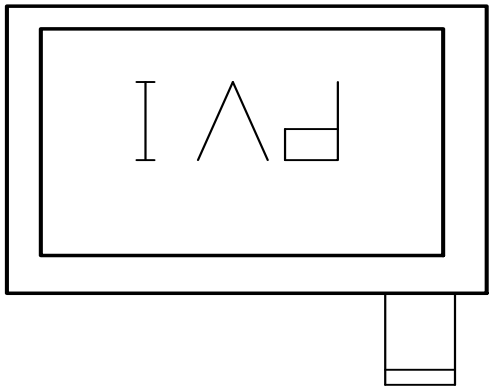
STVD,STVU and U/D mode

U/D	STVD	STVU	Remark
High(V_{CC})	Input	Output	Down to Up
Low(0 Volt.)	Output	Input	Up to Down

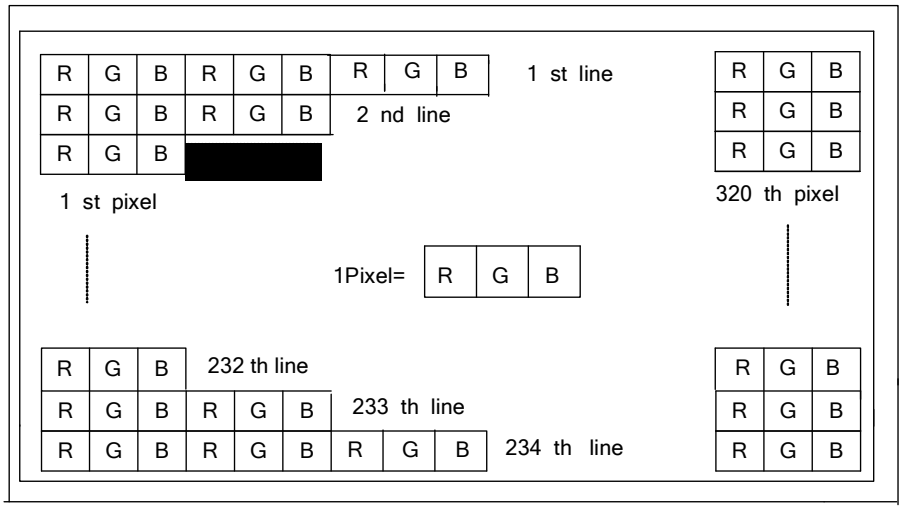
U/D(PIN 12)=Low R/L(PIN 28)=High



U/D(PIN 12)=High R/L(PIN 28)=Low



6. Pixel Arrangement



7. Absolute Maximum Ratings :

The followings are maximum values , which if exceeded, may cause faulty operation or damage to the unit.

GND = 0 V , Ta = 25 ℃

Parameter		Symbol	MIN.	MAX.	Unit	Remark
Supply Voltage For Source Driver		V_{DD2}	-0.3	+5.8	V	
		V_{DD1}	-0.3	+7.0	V	
Supply Voltage For Gate Driver		V_{CC}	-0.3	+6.0	V	
		V_{GH}-V_{EE}	-0.3	+40.0	V	
	H Level	V_{GH}	-0.3	+25.0	V	
	L Level	V_{EE}	-16	+0.3	V	

8. Electrical Characteristics

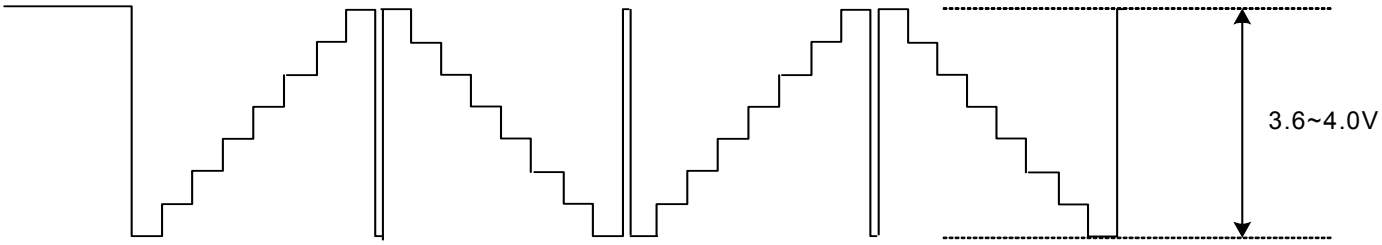
8-1) Operating Condition for TFT-LCD panel

Ta=25℃

Parameter		Symbol	MIN.	Typ.	MAX.	Unit	Remark
Supply Voltage For Source Driver	Analog	V_{DD2}	+4.5	+5.0	+5.5	V	
	Logic	V_{DD1}	+3.0	+3.3	+3.6	V	Depend on T/C Signal voltage
			+4.5	+5.0	+5.5		
Supply Voltage For Gate Driver	V_{GH}		+15	+17	+19	V	
	$V_{EE\ DC}$		-13	-12	-10.5	V	DC Component of V_{EE}
	$V_{EE\ AC}$		-	+6.0	-	V_{P-P}	AC Component of V_{EE}
	Logic	V_{CC}	+3.0	+3.3	+3.6	V	Depend on T/C Signal voltage
			+4.5	+5.0	+5.5		
Analog Signal input Level (V_R , V_G , V_B)	V_{iAC}		-	+3.6	+4.0	V	Note 8-2
	V_{iDC}		-	2.5	-	V	
Digital input voltage	H level	V_{IH}	0.7 V_{DD1}	-	V_{DD1}	V	
	L level	V_{IL}	-0.3	-	0.3 V_{DD1}	V	
Digital output voltage	H level	V_{OH}	0.7 V_{DD1}	-	V_{DD1}	V	
	L level	V_{OL}	-0.3	-	0.3 V_{DD1}	V	
V_{COM}		$V_{COM\ AC}$	-	+6.0	-	V_{P-P}	AC Component of V_{COM}
		$V_{COM\ DC}$	-	1.5	-	V	DC Component of V_{COM} Note 8-1

Note 8-1 : PVI strongly suggests that the $V_{COM\ DC}$ level shall be adjustable , and the adjustable level range is 1.5V±1V , every module's $V_{COM\ DC}$ level shall be carefully adjusted to show a best image performance.

Note 8-2: Both NTSC and PAL system Video Signal input waveform is based on 8 steps gray scale.



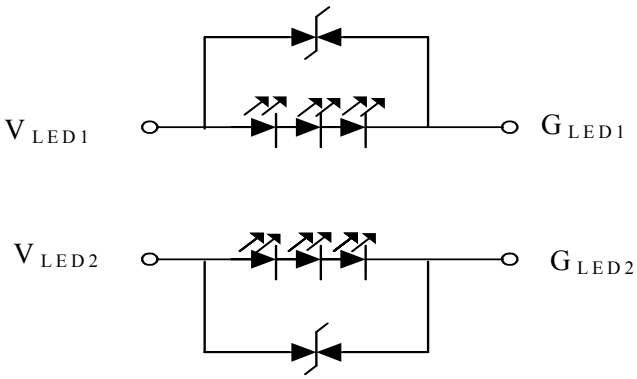
8-2) Recommended driving condition for LED backlight

GND = 0 V， Ta = 25 ℃

Parameter	Symbol	Min	TYP	MAX	Unit	Remark
Supply voltage of LED backlight	VLED1 VLED2	---	9.9	10.8	V	I_L = 15 mA
Supply current of LED backlight	ILED1 ILED2	-	20	-	mA	Note 8-4
Backlight Power Consumption	PLED	---	TBD	TBD	mW	Note 8-5

Note 8-4 : LED B/L applied information , please refer to the appendix at the end .

Note 8-5 : $P_{LED} = V_{LED1} * I_{LED1} + V_{LED2} * I_{LED2}$.



8-3) Power Consumption

Ta = 25 ℃

Parameter	Symbol	Conditions	TYP.	MAX	Unit	Remark
Supply current for Gate Driver (Hi level)	I_{GH}	V_{GH} =+17V	0.08	0.1	mA	
Supply current for Gate Driver (Low level)	I_{EE}	V_{EE} =-12V	0.1	0.12	mA	V_{EE} center voltage
Supply current for Source Driver(Digital)	I_{DD1}	V_{DD1}=+3.3V	0.8	2.0	mA	
Supply current for Source Driver(Analog)	I_{DD2}	V_{DD2}=+5V	3.5	5.0	mA	
Supply current for Gate Driver (Digital)	I_{CC}	V_{CC} =+3.3V	0.017	0.021	mA	
LCD Panel Power Consumption		-	22.742	34.792	mW	
Backlight Power Consumption	PLED	-	TBD	TBD	mW	
Total Power Consumption		-	TBD	TBD	mW	

8-4) Timing Characteristics Of Input Signals

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Remark
Rising time	t_r	-	-	10	ns	
Falling time	t_f	-	-	10	ns	
High and low level pulse width	t_{CPH}	147	156	166	ns	CPH1~CPH3
CPH pulse duty	t_{CWH}	30	50	70	%	CPH1~CPH3
STH setup time	t_{SUH}	20	-	-	ns	STHR,STHL
STH hold time	t_{HDH}	20	-	-	ns	STHR,STHL
STH pulse width	t_{STH}	-	1	-	t_{CPH}	STHR,STHL
STH period	t_H	61.5	63.5	65.5	μs	STHR,STHL
OEH pulse width	t_{OEH}	-	1.6	-	μs	OEH
Sample and hold disable time	t_{DIS1}	-	4.4	-	μs	
OEV pulse width	t_{OEV}	-	12	-	μs	OEV
CKV pulse width	t_{CKV}	-	32	-	μs	CKV
Clean enable time	t_{DIS2}	-	6	-	μs	
Horizontal display timing range	t_{DH}	-	320	-	t_{CPH}	
STV setup time	t_{SUV}	400	-	-	ns	
STV hold time	t_{HDV}	400	-	-	ns	STVU,STVD
STV pulse width	t_{STV}	-	-	1	t_H	STVU,STVD
Horizontal lines per field	t_V	256	262	268	t_H	
Vertical display start	t_{SV}		3	-	t_H	
Vertical display timing range	t_{DV}		234	-	t_H	
VCOM rising time	t_{rCOM}		-	5	μs	
VCOM falling time	t_{fCOM}		-	5	μs	
VCOM delay time	t_{DCOM}		-	3	μs	
RGB delay time	t_{DRGB}		-	1	μs	

8-5) Signal Timing Waveforms

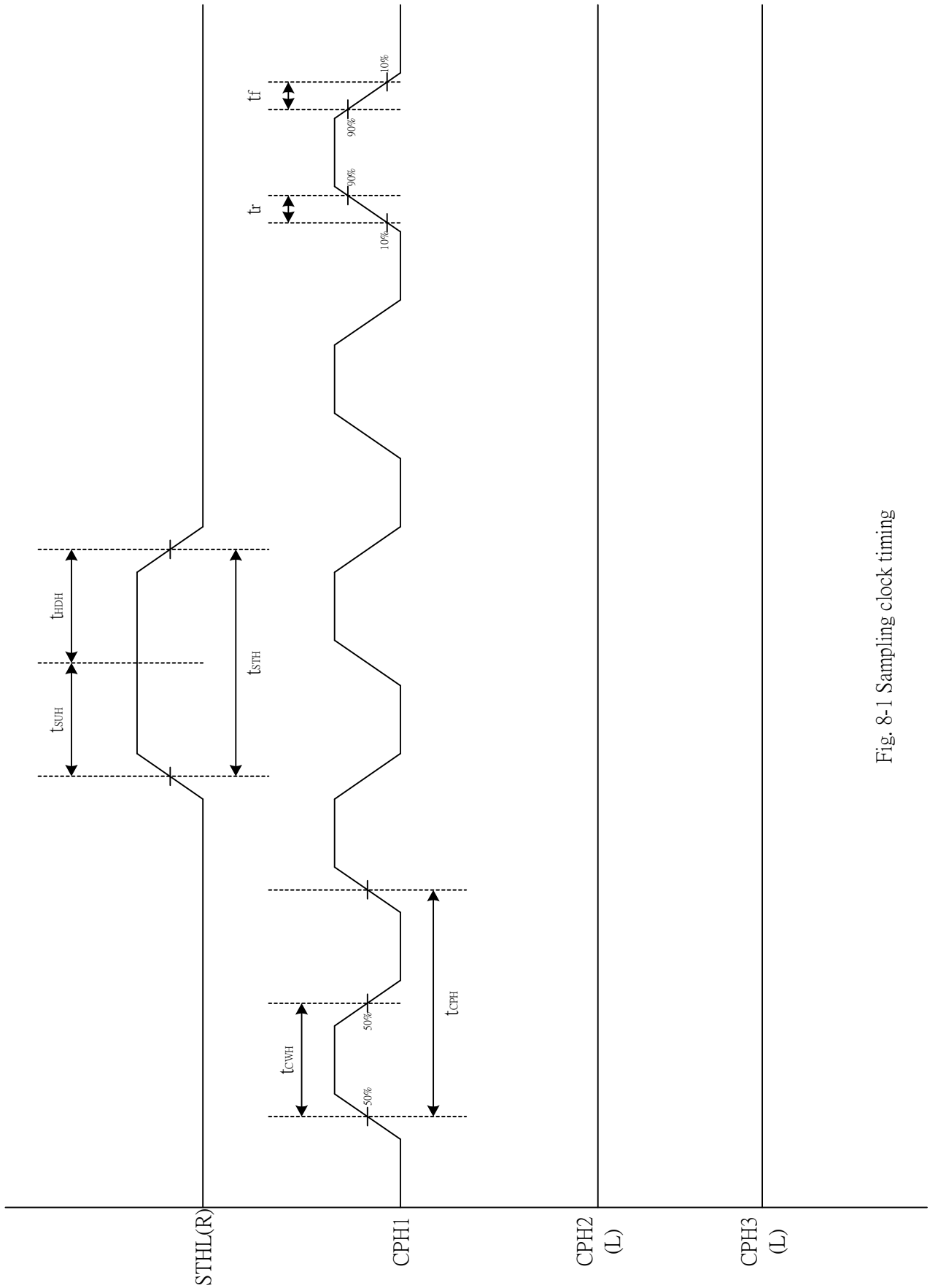


Fig. 8-1 Sampling clock timing

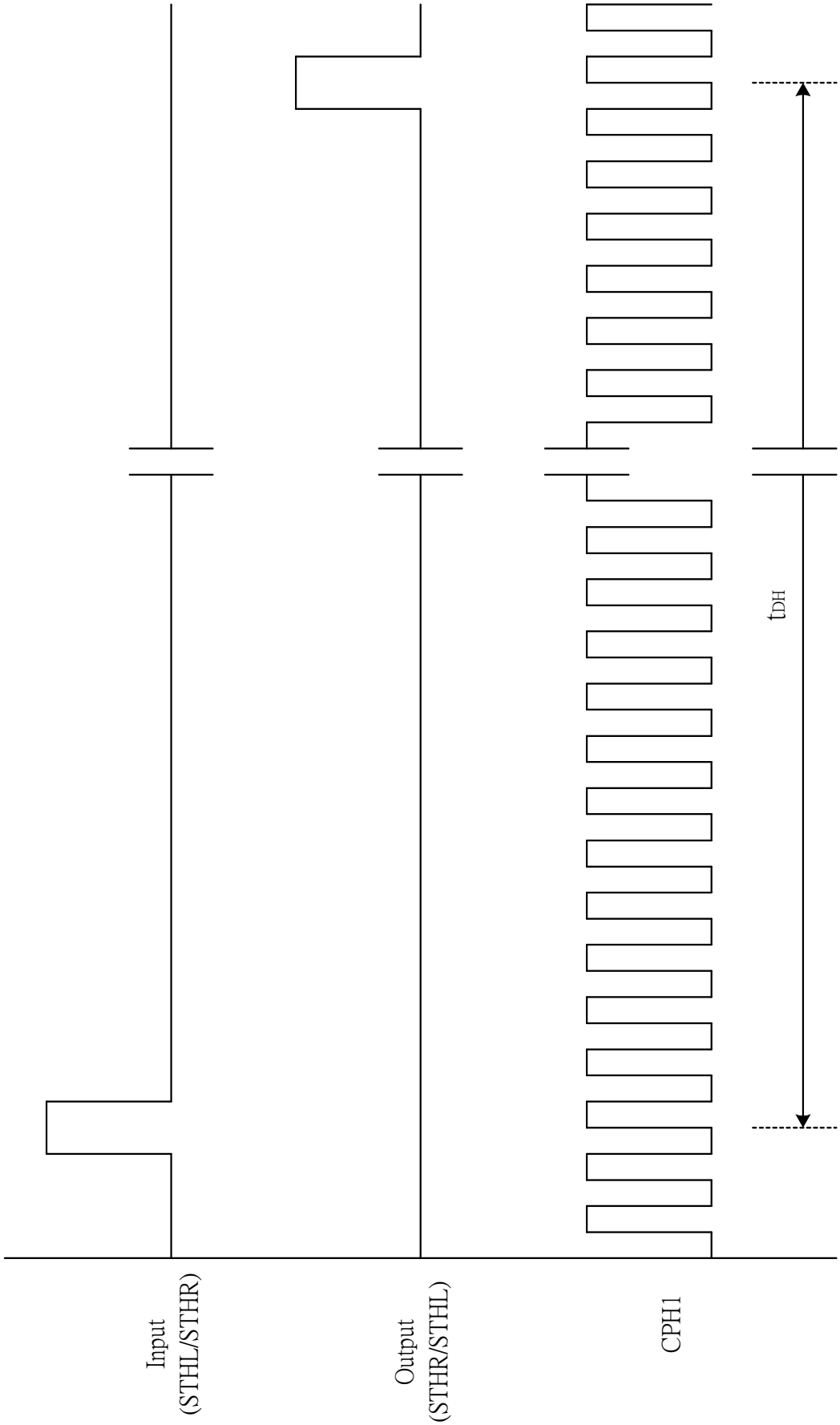


Fig. 8-2 Horizontal display timing range

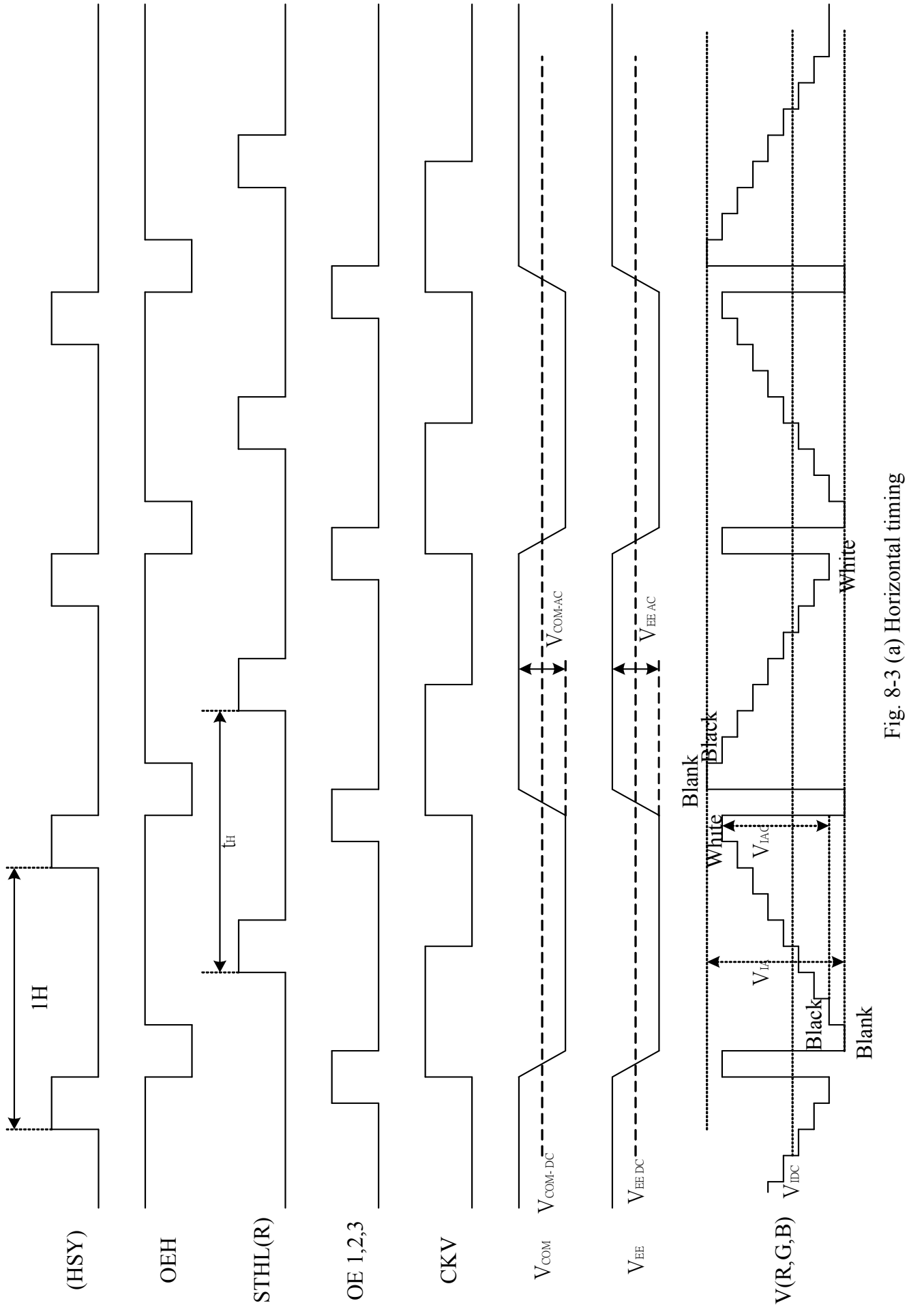
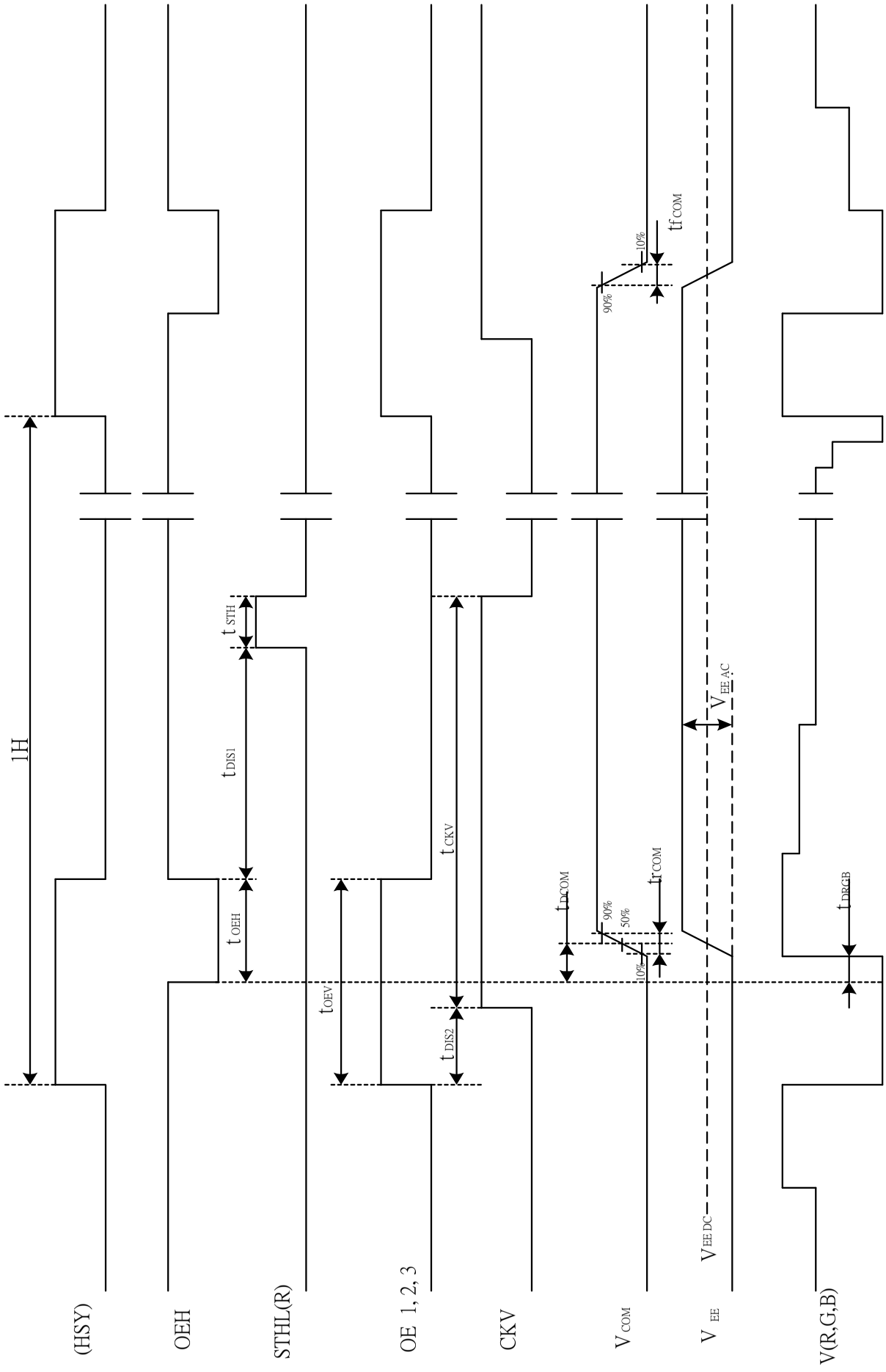


Fig. 8-3 (a) Horizontal timing



Note : The falling edge of OEV should be synchronized with the falling edge of OEH

Fig. 8-3 (b) Detail horizontal timing

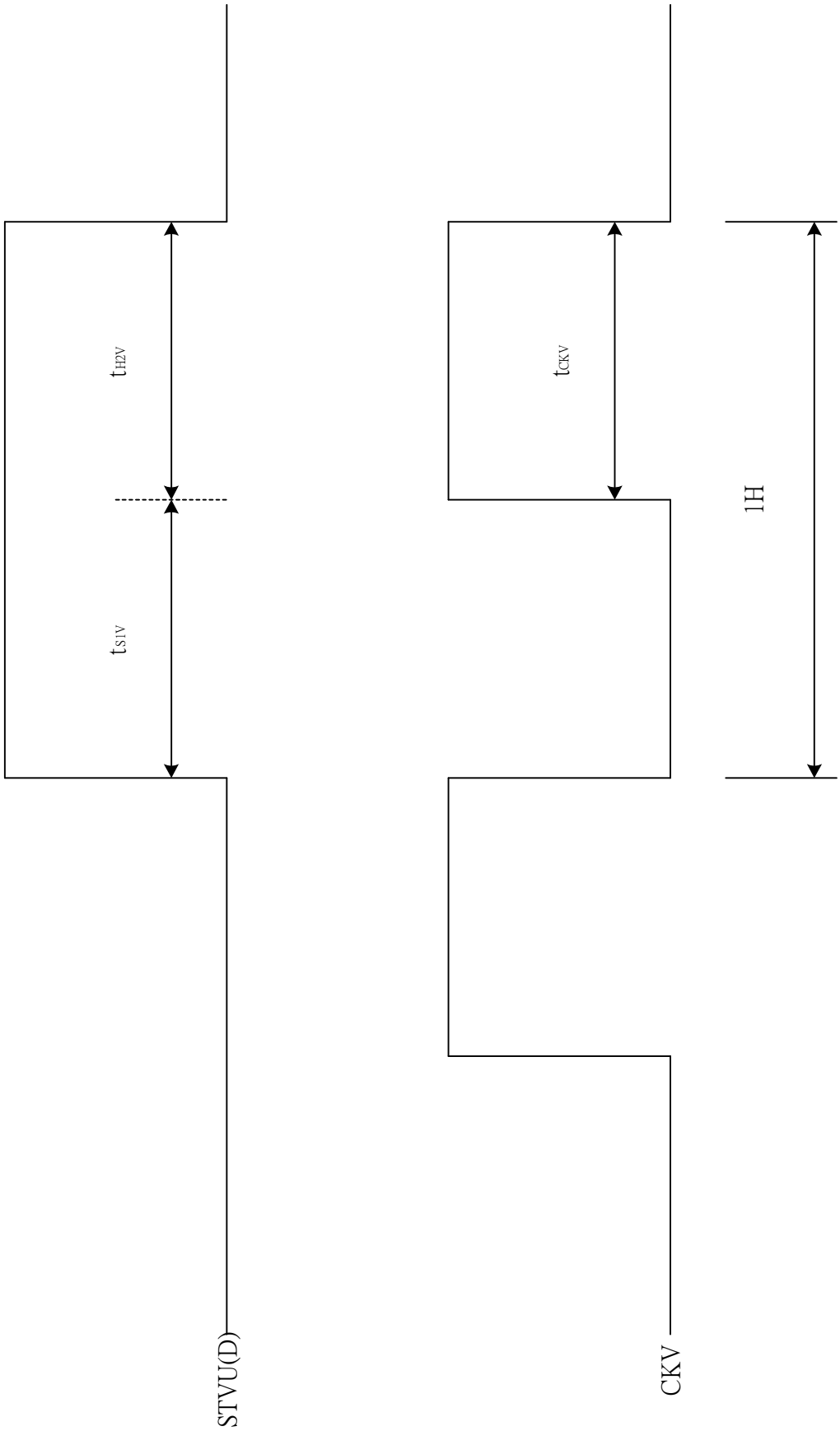


Fig. 8-4 Vertical shift clock timing

Vertical timing (From up to down)

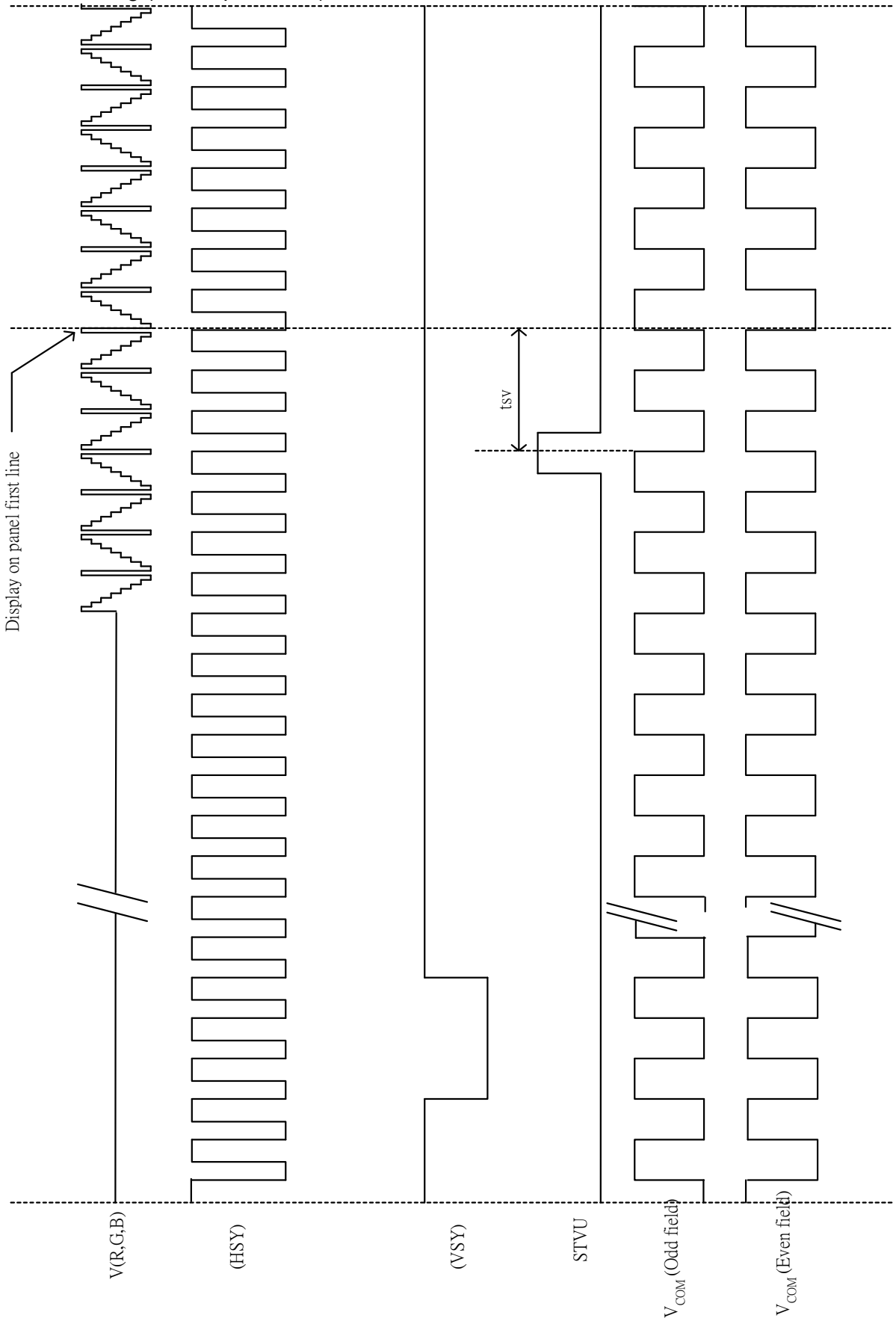


Fig. 8-5 (a) Vertical timing (From Up to Down)

Vertical timing (From down to up)

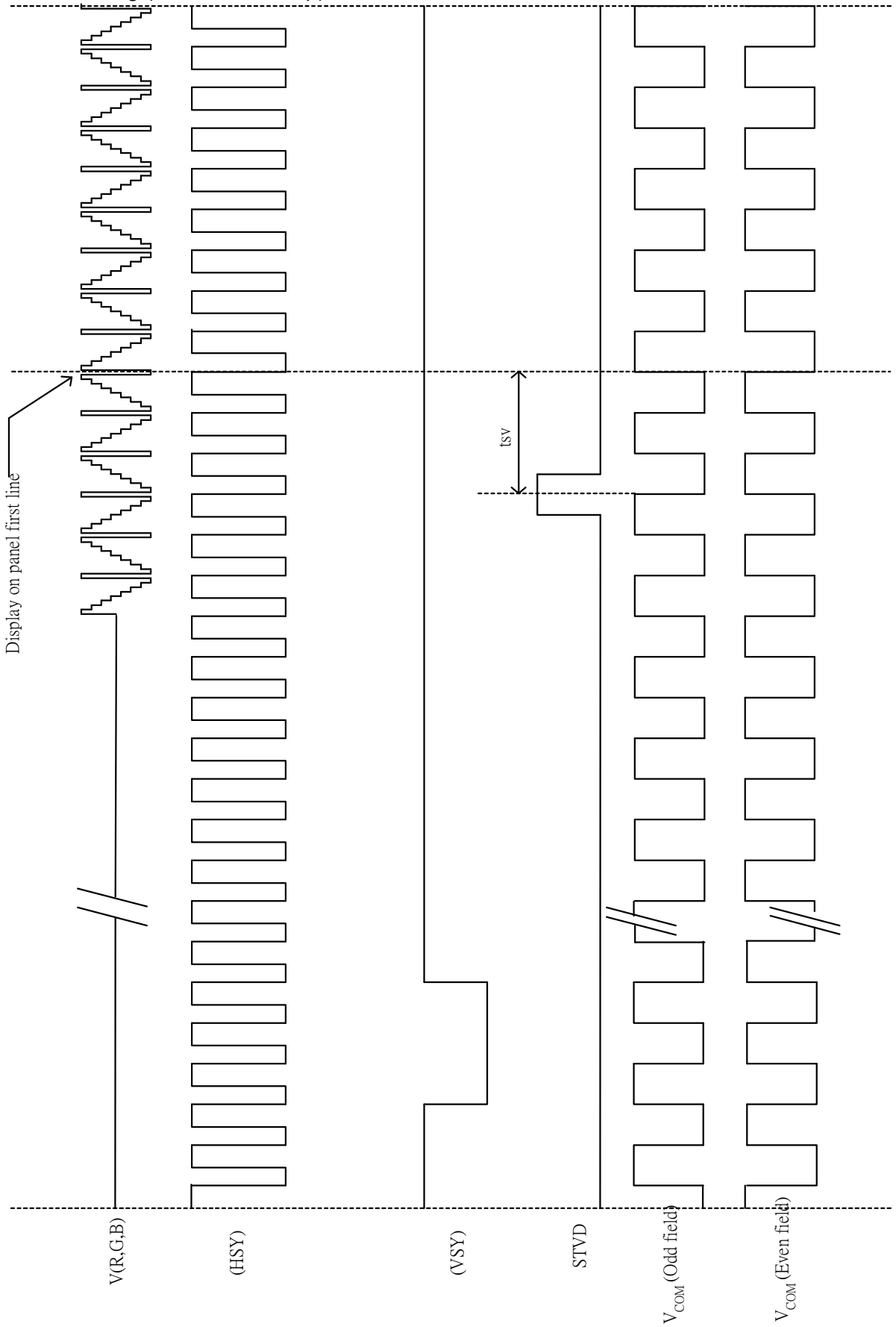
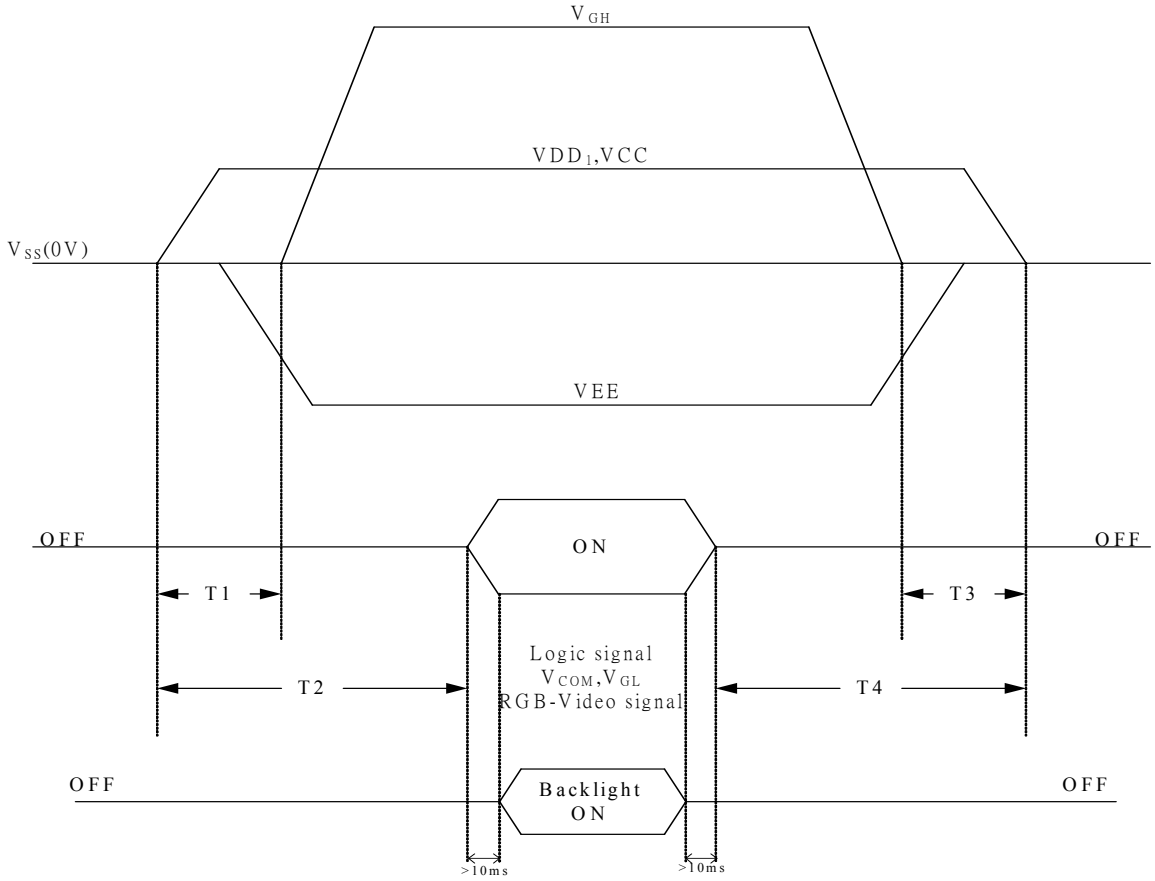


Fig. 8-5 (b) Vertical timing (From Down to Up)

9. Power On Sequence

The Power on Sequence only effect by V_{CC},V_{SS},V_{DD},V_{EE} and $V_{GH,}$ the others do not care.



1) 10ms≦T1<T2
2) 0ms<T3≦T4≦10ms

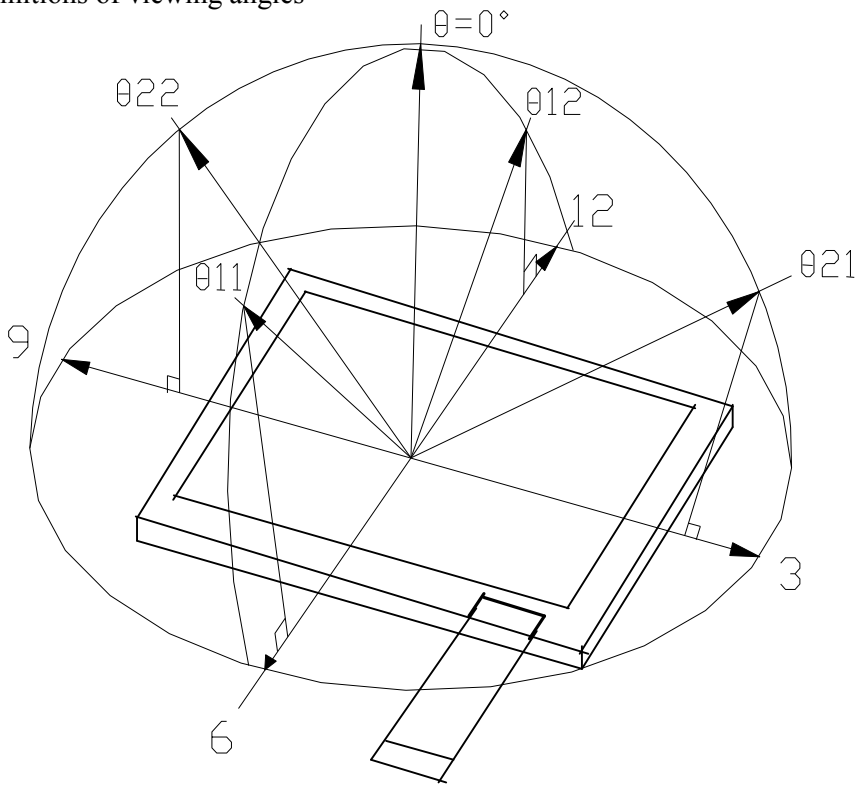
10. Optical Characteristics

10-1) Specification:

Ta = 25℃

Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit	Remarks
Viewing Angle	Horizontal	θ 21, θ 22	CR≧10	±55	±60	---	deg	Note 10-1
	Vertical	θ 11		35	40	---	deg	
		θ 12		45	50	---	deg	
Contrast Ratio		CR	At optimized Viewing angle	200	350	---		Note 10-2
Response time	Rise	Tr	θ =0°	---	15	20	ms	Note 10-4
	Fall	Tf		---	25	30	ms	
Uniformity		U	9 point	75	80	---		Note 10-3
Brightness		L	θ =0°	350	400	---	cd/㎡	
White Chromaticity		x	θ =0°	TBD	TBD	TBD		
		y	θ =0°	TBD	TBD	TBD		
LED Life time		-	+25℃	20000	30000	---	hrs	Note 10-5

Note 10-1 : The definitions of viewing angles



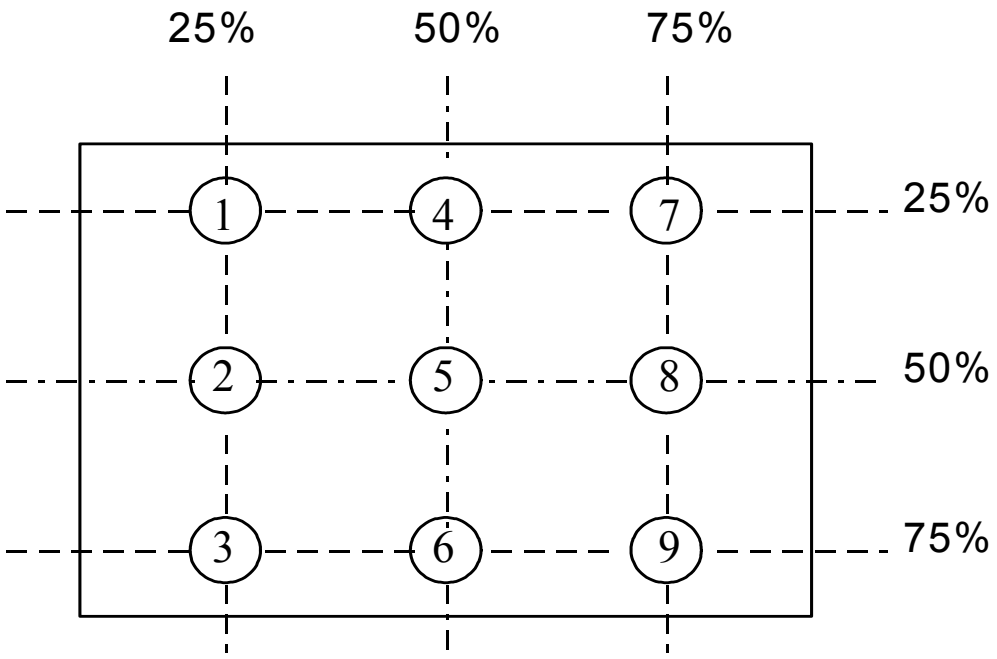
Note 10-2 : CR = $\frac{\text{Luminance when Testing point is White}}{\text{Luminance when Testing point is Black}}$

(Testing configuration see 10-2)

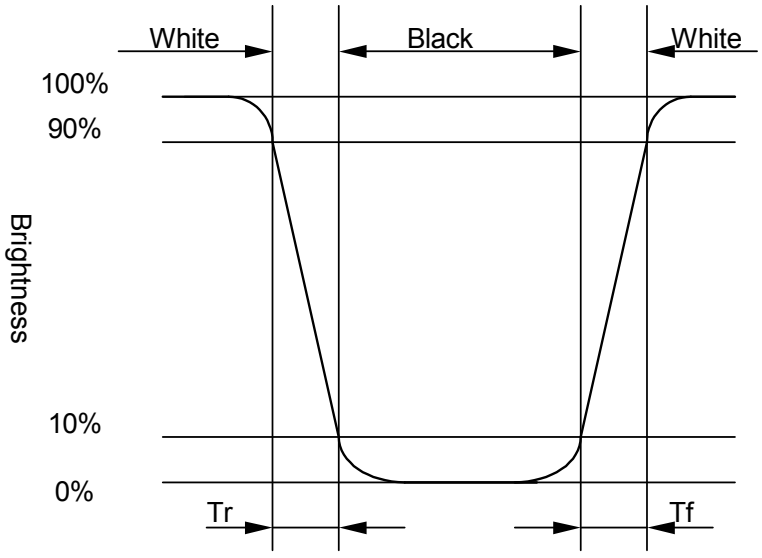
Contrast Ratio is measured in optimum common electrode voltage.

Note 10-3 : Topcon BM-7(fast) luminance meter 1.0˚field of view is used in the testing (after 10 minutes operation).

$$U = \frac{\text{The Minimum Brightness of the 9 testing Points}}{\text{The Maximum Brightness of the 9 testing Points}}$$

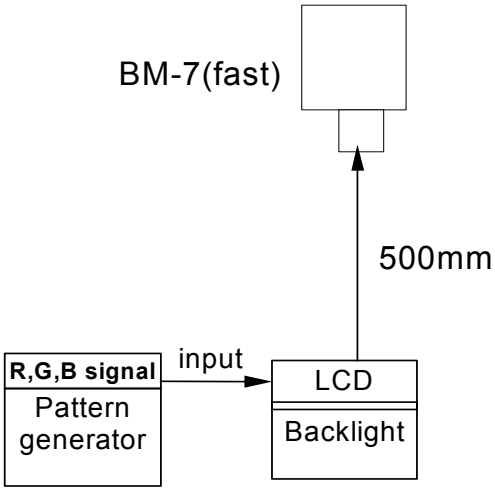


Note 10-4 : The definition of response time :



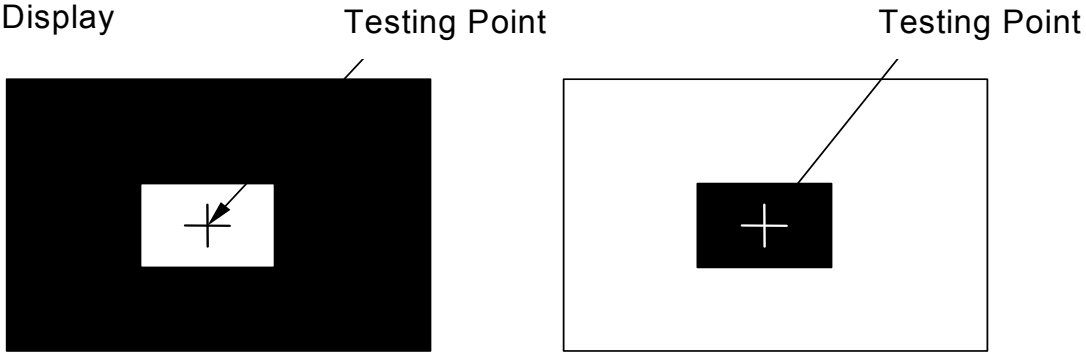
Note 10-5: The “LED Life time “ is defined as the module brightness decrease to 50% original Brightness that the ambient temperature is 25℃ and I_{LED} =20mA.

10-2) Testing configuration



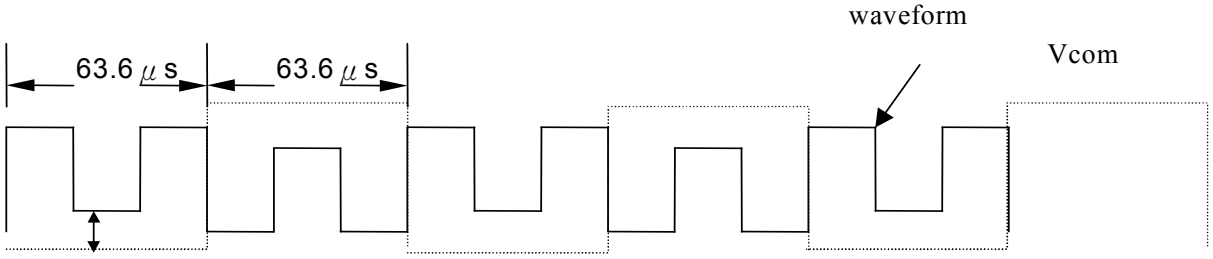
Caution: 1. Environmental illumination ≦ 1 lux
2. Before test CR, Vcom voltage must be adjusted carefully to get the best CR.

- LCD Display



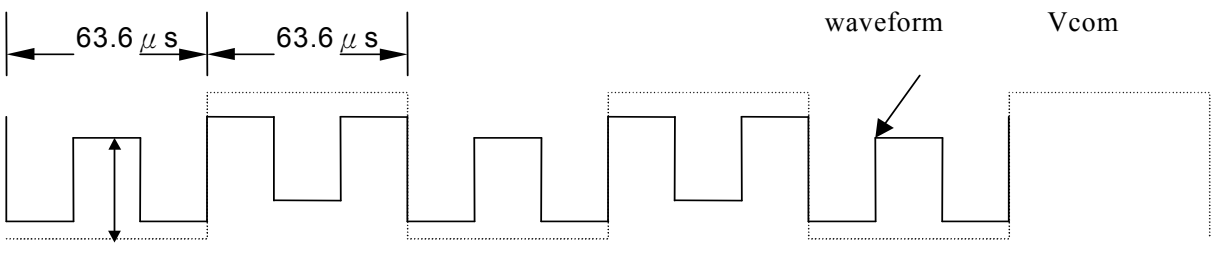
Pattern A Pattern B

- R, G, B Waveform of Pattern A at Testing Point



Vw=1.3V +/- 0.2V

- R, G, B Waveform of Pattern B at Testing Point



Vb=5.0V +/- 0.2V

11. Handling Cautions

11-1) Mounting of module

a) Please power off the module when you connect the input/output connector.

b) Please connect the ground pattern of the inverter circuit surely. If the connection is not perfect, some following problems may happen possibly.

1.The noise from the backlight unit will increase.

2.The output from inverter circuit will be unstable.

3.In some cases a part of module will heat.

c) Polarizer which is made of soft material and susceptible to flaw must be handled carefully.

d) Protective film (Laminator) is applied on surface to protect it against scratches and dirt. It is recommended to peel off the laminator before use and taking care of static electricity.

11-2) Precautions in mounting

a) Wipe off water drops or finger grease immediately. Long contact with water may cause discoloration or spots.

b) TFT-LCD module uses glass which breaks or cracks easily if dropped or bumped on hard surface. Please handle with care.

c) Since CMOS LSI is used in the module. So take care of static electricity and earth yourself when handling.

11-3) Others

a) Do not expose the module to direct sunlight or intensive ultraviolet rays for many hours.

b) The voltage of beginning electric discharge may over the normal voltage because of leakage current from approach conductor by to draw lump read lead line around.

c) If LCD panel breaks, it is possibly that the liquid crystal escapes from the panel. Avoid putting it into eyes or mouth. When liquid crystal sticks on hands, clothes or feet. Wash it out immediately with soap.

d) Observe all other precautionary requirements in handling general electronic components.

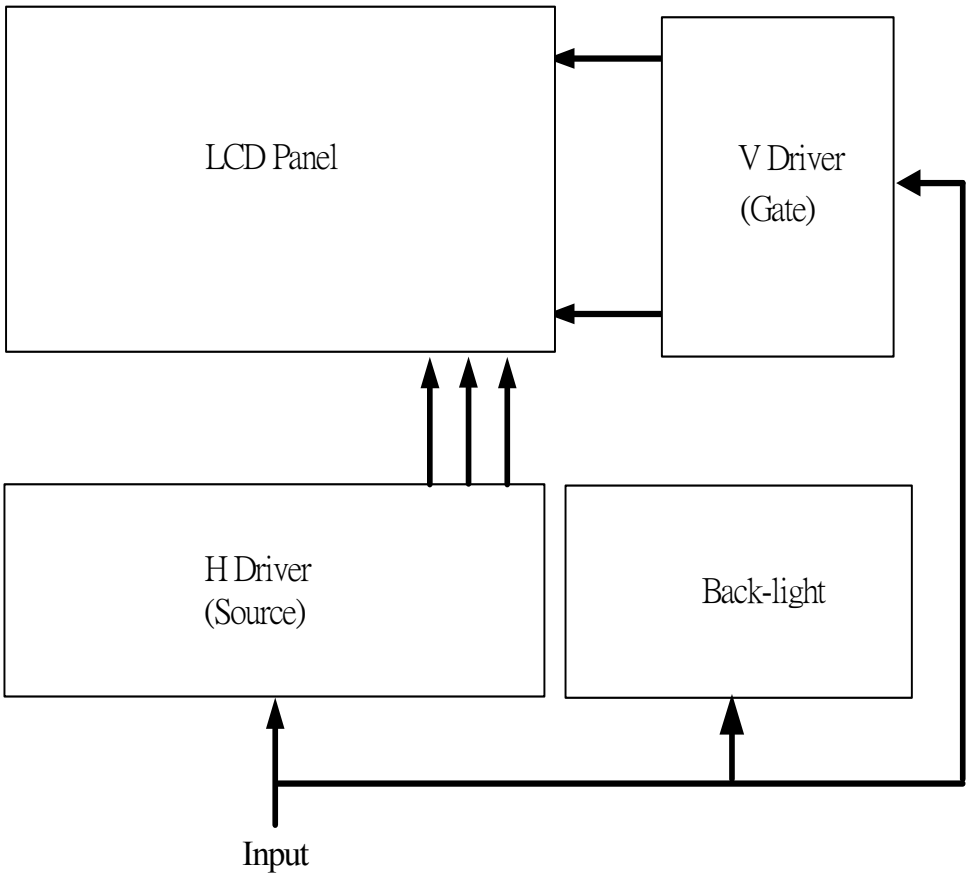
12. Reliability Test

No	Test Item	Test Condition	Note
1	High Temperature Storage Test	Ta = +85℃, 240 hrs	
2	Low Temperature Storage Test	Ta = -30℃, 240 hrs	
3	High Temperature Operation Test	Ta = +75℃, 240 hrs	
4	Low Temperature Operation Test	Ta = -20℃, 240 hrs	
5	High Temperature & High Humidity Operation Test	Ta = +60℃, 95%RH, 240 hrs	
6	Thermal Cycling Test (non-operating)	-30℃ ← → +80℃ , 100 Cycles 60 min 60 min	
7	Vibration test (non-operating)	Frequency : 10 ~ 55Hz Amplitude : 1mm , sweep time : 11 mins Test period : 6 cycles for each direction of X,Y, Z	
8	Shock Test(non-operating)	100G , 6ms , 3cycles for each direction of X,Y,Z	
9	Electrostatic Discharge Test (non-operating)	200pF, 0Ω Machine mode = ±200V 1 time / each terminal	

Ta: ambient temperature

[Criteria]
In the standard conditions, there is not display function NG issue occurred. (including : line defect ,no image). All the cosmetic specification is judged before the reliability stress.

13. Block Diagram



14. Packing

TBD

Revision History

Rev.	Issued Date	Revised Contents
0.1	Jan. 18, 2007	NEW