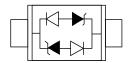


Low Capacitance TVS

Description

The PTVSUC3D3V3B is a ultra-low capacitance transient voltage suppressor for high speed data interface that designed to protect sensitive electronics from damage or latch-up due to ESD lightning, and other voltage induced transient events.

All pins are rated to withstand 15kV ESD pulses using the IEC61000-4-2 air discharge method, which can meet the requirement of level 4.



Feature

- \rightarrow 350W peak pulse power per line ($t_P = 8/20\mu s$)
- SOD-323 package
- Replacement for MLV(0805)
- Bidirectional configurations
- Protects one power or I/O port
- ESD protection > 15kV
- Low clamping voltage
- RoHS compliant
- > Transient protection for data lines to IEC61000-4-2(ESD)
 - ±15kV (air), ±8kV (contact); IEC61000-4-4 (EFT) 40A (5/50ns)

Applications

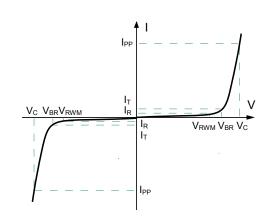
- ➤ Ethernet 10/100/1000 Base T
- Cellular phones
- Handheld-wireless systems
- PDAs
- USB interface

Mechanical Characteristics

- Lead finish:100% matte Sn(Tin)
- Mounting position: Any
- ➤ Qualified max reflow temperature:260 °C
- Device meets MSL 1 requirements
- ➤ Pure tin plating: 7 ~ 17 um
- Pin flatness:≤3mil

Electronics Parameter

Symbol	Parameter
V_{RWM}	Peak Reverse Working Voltage
I _R	Reverse Leakage Current @ V _{RWM}
V_{BR}	Breakdown Voltage @ I⊤
I _T	Test Current
I _{PP}	Maximum Reverse Peak Pulse Current
Vc	Clamping Voltage @ IPP
P _{PK}	Peak Power Dissipation
CJ	Junction Capacitance
I _F	Forward Current
V _F	Forward Voltage @ I _F



Electrical characteristics per line@25℃(unless otherwise specified)

Device	V _{RWM}	I _R @ V _{RWM}	V _{BR} @ 1mA	V _C @I _P =1A	V _C @I _{PP}	C _j (Max.) @0V,1MHz
	(V)	(µA)	(V)	(V)	(V)	(pF)
PTVSUC3D3V3B	3.3	1	4.0	8.0	25@15A	0.8

Absolute maximum rating@25℃

Rating	Symbol	Value	Units
Peak Pulse Power (t _p =8/20μs)	P _{pp}	350	W
Operating Temperature	TJ	-55 to +150	$^{\circ}\! \mathbb{C}$
Storage Temperature	T _{STG}	-55 to +150	°C

Typical Characteristics

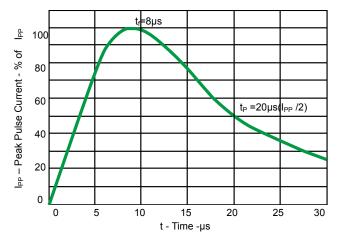


Fig 1.Pulse Waveform

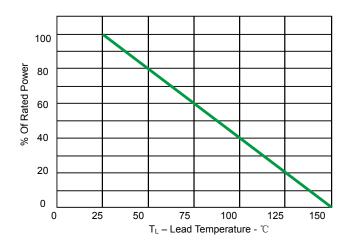


Fig 2.Power Derating Curve

Low Capacitance TVS

PTVSUC3D3V3B

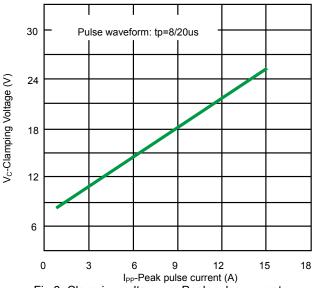


Fig 3. Clamping voltage vs. Peak pulse current

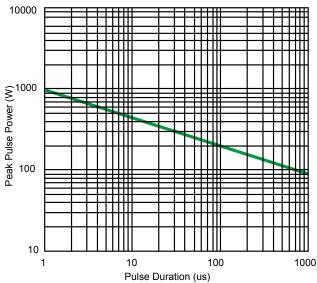
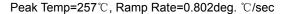
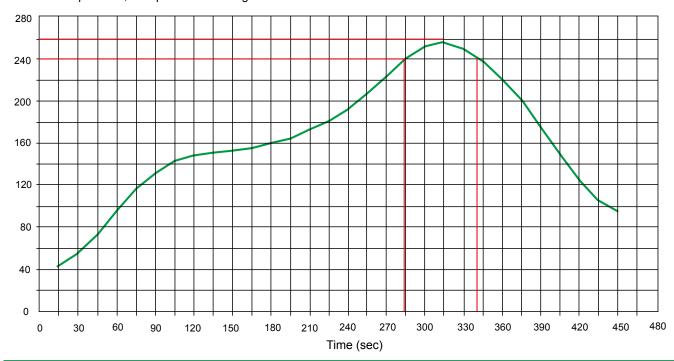


Fig 4. Non Repetitive Peak Pulse Power vs. Pulse time

Solder Reflow Recommendation



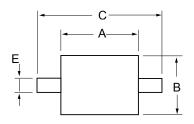


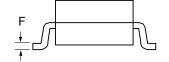
PCB Design

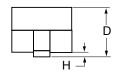
For TVS diodes a low-ohmic and low-inductive path to chassis earth is absolutely mandatory in order to achieve good ESD protection. Novices in the area of ESD protection should take following suggestions to heart:

- > Do not use stubs, but place the cathode of the TVS diode directly on the signal trace.
- Do not make false economies and save copper for the ground connection.
- Place via holes to ground as close as possible to the anode of the TVS diode.
- Use as many via holes as possible for the ground connection.
- > Keep the length of via holes in mind! The longer the more inductance they will have.

Product dimension (SOD-323)

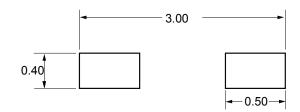






Dim	Incl	nes	Millimeters		
DIM	MIN	MAX	MIN	MAX	
Α	0.063	0.075	1.60	1.90	
В	0.045	0.057	1.15	1.45	
С	0.090	0.106	2.30	2.70	
D	0.031	0.043	0.80	1.10	
E	0.010	0.01	0.25	0.40	
F	0.004	0.007	0.09	0.18	
Н	0.000	0.004	0.00	0.10	

Unit:mm



Ordering information

Device	Package	Shipping
PTVSUC3D3V3B	SOD-323 (Pb-Free)	3000 / Tape & Reel

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